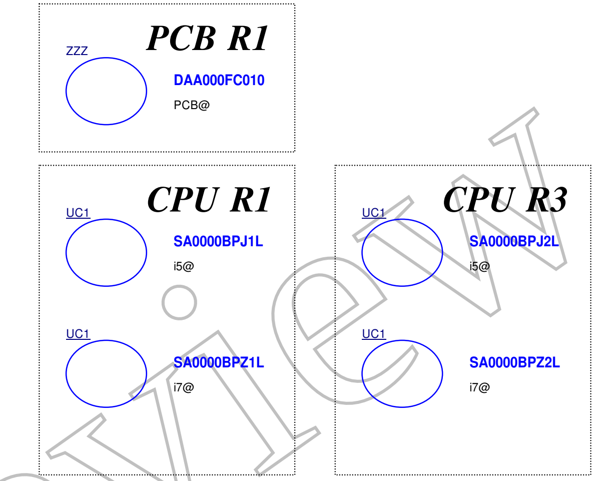
COMPAL CONFIDENTIAL

MODEL NAME : Loki-G 15/17
MB PCB PN : DAA000FC010
PWR/B PCB PN : DA4002L3010
IO/B PCB PN : DA6001XF010


PCB R1
ZZZ
DAA000FC010
PCB@
CPU R1
UC1
SA0000BPJ1L
i5@
UC1
SA0000BPZ1L
i7@
CPU R3
UC1
SA0000BPJ2L
i5@
UC1
SA0000BPZ2L
i7@

Dell/Compal Confidential

Schematic Document

COFFEE LAKE H
N17P-G0/G1

Loki-G 15/17

2018-03-22

REV : 1.0 (A00)

Layout Dell logo

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REV: X00
PWB: 9HTP8

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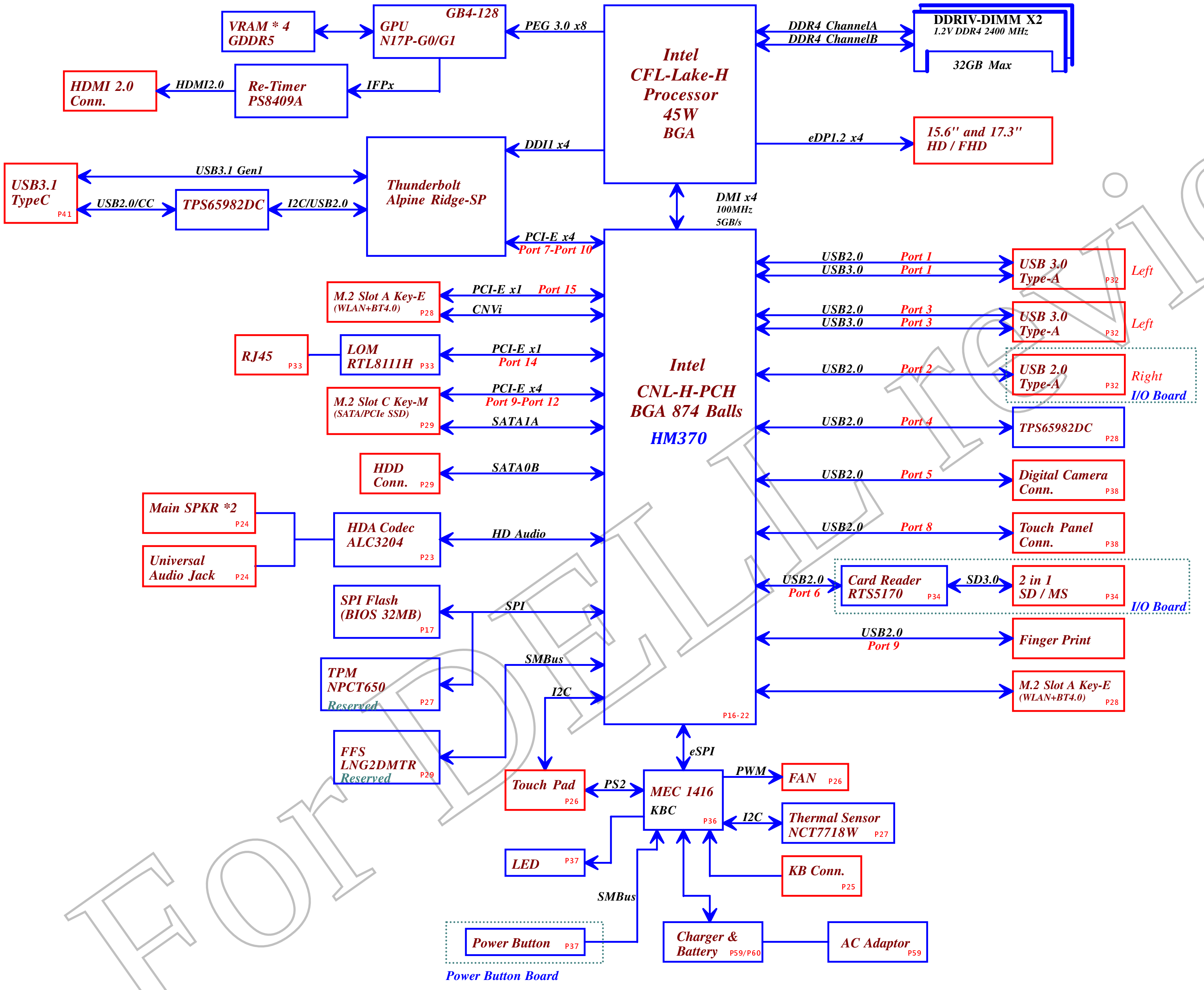
Date: Thursday, March 22, 2018


VRAM * 4
GDDR5
GPU
N17P-G0/G1
GB4-128
PEG 3.0 x8
Intel
CFL-Lake-H
Processor
45W
BGA
DDR4 ChannelA
DDR4 ChannelB
DDRIV-DIMM X2
1.2V DDR4 2400 MHz
32GB Max
HDMI 2.0
Conn.
HDMI2.0
Re-Timer
PS8409A
IFPx
eDP1.2 x4
15.6'' and 17.3''
HD / FHD
DDI1 x4
USB3.1
TypeC
P41
USB3.1 Gen1
USB2.0/CC
TPS65982DC
I2C/USB2.0
Thunderbolt
Alpine Ridge-SP
DMI x4
100MHz
5GB/s
PCI-E x4
Port 7-Port 10
M.2 Slot A Key-E
(WLAN+BT4.0)
P28
PCI-E x1
Port 15
CNVi
RJ45
P33
LOM
RTL8111H
P33
PCI-E x1
Port 14
M.2 Slot C Key-M
(SATA/PCIe SSD)
P29
PCI-E x4
Port 9-Port 12
SATA1A
HDD
Conn.
P29
SATA0B
Main SPKR *2
P24
Universal
Audio Jack
P24
HDA Codec
ALC3204
P23
HD Audio
SPI Flash
(BIOS 32MB)
P17
SPI
TPM
NPCT650
Reserved
P27
SMBus
I2C
FFS
LNG2DMTR
Reserved
P29
Intel
CNL-H-PCH
BGA 874 Balls
HM370
P16-22
USB2.0
Port 1
USB3.0
Port 1
USB 3.0
Type-A
P32
Left
USB2.0
Port 3
USB3.0
Port 3
USB 3.0
Type-A
P32
Left
USB2.0
Port 2
USB 2.0
Type-A
P32
Right
I/O Board
USB2.0
Port 4
TPS65982DC
P28
USB2.0
Port 5
Digital Camera
Conn.
P38
USB2.0
Port 8
Touch Panel
Conn.
P38
USB2.0
Port 6
Card Reader
RTS5170
P34
SD3.0
2 in 1
SD / MS
P34
I/O Board
USB2.0
Port 9
Finger Print
M.2 Slot A Key-E
(WLAN+BT4.0)
P28
eSPI
Touch Pad
P26
PS2
MEC 1416
KBC
P36
PWM
FAN
P26
I2C
Thermal Sensor
NCT7718W
P27
LED
P37
KB Conn.
P25
SMBus
Power Button
P37
Power Button Board
Charger &
Battery
P59/P60
AC Adaptor
P59

128M*32 x4 =2G
256M*32 x4 =4G

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Refer Page 26

Board ID	Resistor
X00	15K
X01	17.8K
X02	27K
X03	37.4K
A00	49.9K

HSIO port Alloction

USB3	DESTINATION
1	USB JUSB1 (Left Side)
2	None
3	USB JUSB3 (Left Side)
4	None
5	None
6	None

USB2	DESTINATION
1	USB JUSB1 (Left Side)
2	USB JUSB2 (I/O)
3	USB JUSB3 (Left Side)
4	TYPEC PD
5	CAMERA
6	Card Reader (I/O)
7	BT & CNVi BRI
8	Touch Screen
9	Finger Print
10	None
11	None
12	None
13	None
14	None

PCI EXPRESS	DESTINATION
Lane 1	None
Lane 2	None
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None
Lane 9	NGFF - NVMe SSD
Lane 10	
Lane 11	
Lane 12	
Lane 13	None (HDD)
Lane 14	LAN
Lane 15	NGFF - WLAN
Lane 16	None
Lane 17	None
Lane 18	None
Lane 19	None
Lane 20	None
Lane 21	Alpine Ridge - SP
Lane 22	
Lane 23	
Lane 24	

USB3	DESTINATION
7	None
8	None
9	None
10	None

SATA	DESTINATION
0a	None (NVMe)
1a	NGFF - SSD
0b	HDD
1b	None (LAM)
2	None (WLAN)
3	None
4	None
5	None
6	None
7	None

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	HDMI2.0 LSPCON PS175

CLK_PCIE	DESTINATION	CLK_REQ	DESTINATION
0	TBT-AR	0	TBT-AR
1	None	1	None
2	None	2	None
3	None	3	None
4	None	4	None
5	None	5	None
6	None	6	None
7	GPU	7	GPU
8	None	8	None
9	NGFF - SSD	9	NVMe
10	None	10	None
11	None	11	None
12	None	12	None
13	None	13	None
14	LAN	14	LAN
15	WLAN	15	WLAN

eSPI Virtual Wires (VW) (Sheet 1 of 2)

Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SUS_STAT#	Output	ESPI_RESET#	No
SUS_PWRDN_ACK	Output	ESPI_RESET#	No
PLTRST#	Output	ESPI_RESET#	Yes
PME#	Input	ESPI_RESET#	No
WAKE#	Input	ESPI_RESET#	No
SMI#	Input	PLTRST#	N/A
SCI#	Input	PLTRST#	N/A
RCIN#	Input	PLTRST#	No
SLP_A#	Output	ESPI_RESET#	Yes

eSPI Virtual Wires (VW) (Sheet 2 of 2)

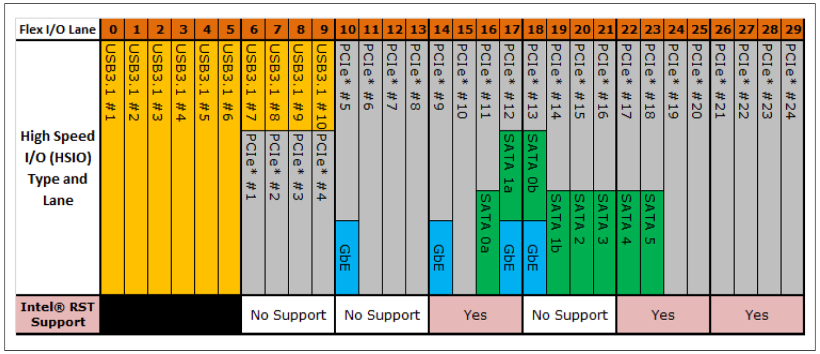
Virtual Wire	PCH Pin Direction	Reset Control	Pin Retained in PCH (For Use by Other Components)
SLP_S3#/SLP_S4#/ SLP_S5#/SLP_LAN#/ SLP_WLAN#	Output	DSW_PWROK	Yes

Table 1-7. PCH HSIO Detail (SKU 9-11of 11)

Flex I/O Lane	SKU		
	HM370	QM370	CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

13.2.1 Coffee Lake PCH-H

Figure 13-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H



Flex I/O Lane	High Speed I/O (HSIO) Type and Lane	Intel® RST Support
0	USB3.1 #1	
1	USB3.1 #2	
2	USB3.1 #3	
3	USB3.1 #4	
4	USB3.1 #5	
5	USB3.1 #6	
6	USB3.1 #7 PCIe* #1	No Support
7	USB3.1 #8 PCIe* #2	
8	USB3.1 #9 PCIe* #3	
9	USB3.1 #10 PCIe* #4	
10	PCIe* #5 GbE	No Support
11	PCIe* #6	
12	PCIe* #7	
13	PCIe* #8	
14	PCIe* #9 GbE	Yes
15	PCIe* #10	
16	PCIe* #11 SATA 0a	
17	PCIe* #12 SATA 1a GbE	
18	PCIe* #13 SATA 0b GbE	No Support
19	PCIe* #14 SATA 1b	
20	PCIe* #15 SATA 2	
21	PCIe* #16 SATA 3	
22	PCIe* #17 SATA 4	Yes
23	PCIe* #18 SATA 5	
24	PCIe* #19	
25	PCIe* #20	
26	PCIe* #21	Yes
27	PCIe* #22	
28	PCIe* #23	
29	PCIe* #24	

Symbol Note :

: means Digital Ground

: means Analog Ground

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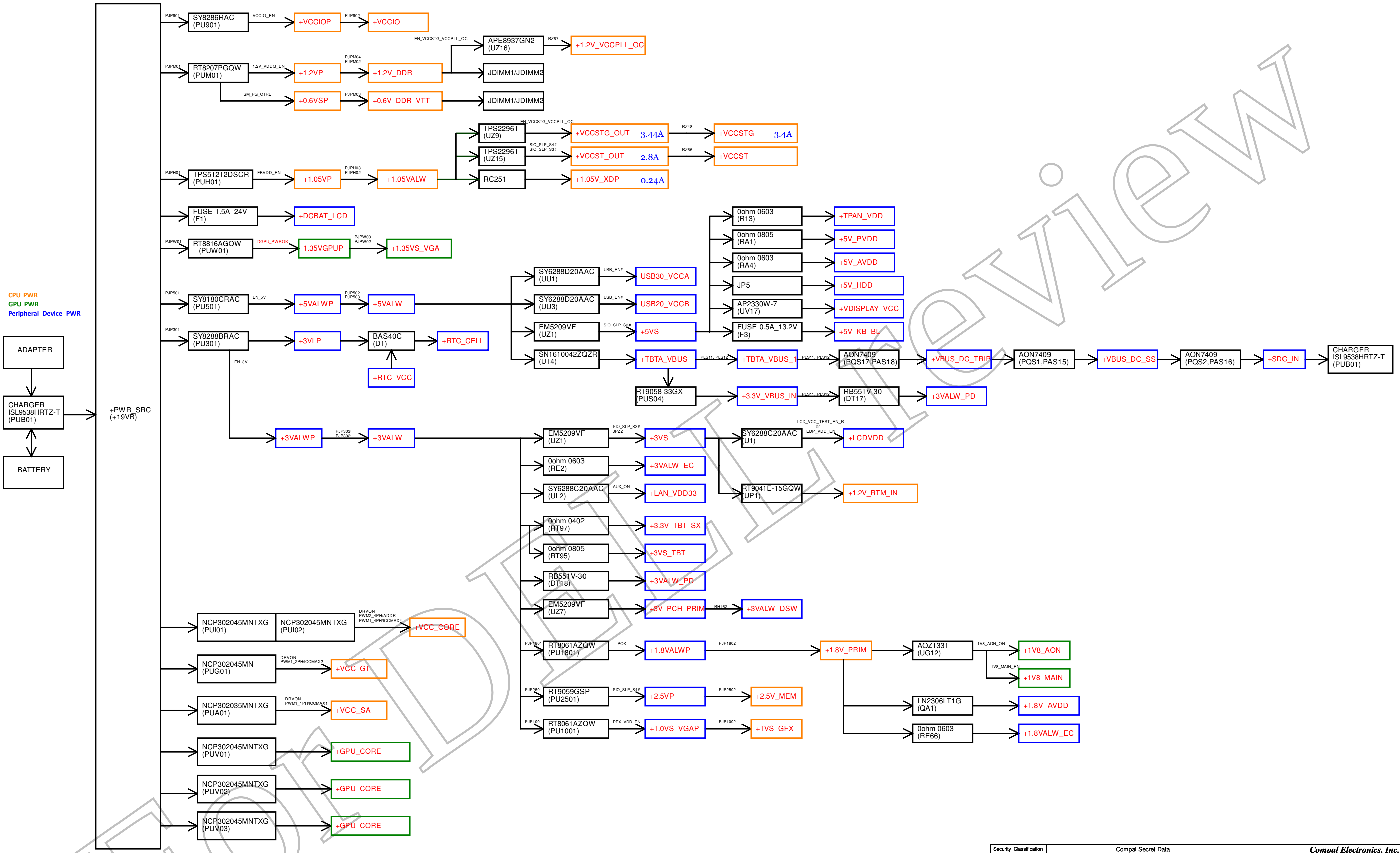
CPU PWR
GPU PWR
Peripheral Device PWR
ADAPTER
CHARGER ISL9538HRTZ-T (PUB01)
BATTERY
+PWR_SRC (+19VB)
PJP901
SY8286RAC (PU901)
VCCIO_EN
+VCCIOP
PJP902
+VCCIO
EN_VCCSTG_VCCPLL_OC
APE8937GN2 (UZ16)
RZ67
+1.2V_VCCPLL_OC
PJPM01
RT8207PGQW (PUM01)
1.2V_VDDQ_EN
+1.2VP
PJPM04
PJPM02
+1.2V_DDR
JDIMM1/JDIMM2
SM_PG_CTRL
+0.6VSP
PJPM03
+0.6V_DDR_VTT
JDIMM1/JDIMM2
EN_VCCSTG_VCCPLL_OC
TPS22961 (UZ9)
+VCCSTG_OUT 3.44A
RZ48
+VCCSTG 3.4A
SIO_SLP_S4#
SIO_SLP_S3#
TPS22961 (UZ15)
+VCCST_OUT 2.8A
RZ66
+VCCST
PJPH01
TPS51212DSCR (PUH01)
FBVDD_EN
+1.05VP
PJPH03
PJPH02
+1.05VALW
RC251
+1.05V_XDP 0.24A
FUSE 1.5A_24V (F1)
+DCBAT_LCD
PJPW01
RT8816AGQW (PUW01)
DGPU_PWROK
1.35VGPUP
PJPW03
PJPW02
+1.35VS_VGA
PJP501
SY8180CRAC (PU501)
EN_5V
+5VALWP
PJP502
PJP503
+5VALW
SY6288D20AAC (UU1)
USB_EN#
USB30_VCCA
SY6288D20AAC (UU3)
USB_EN#
USB20_VCCB
EM5209VF (UZ1)
SIO_SLP_S3#
+5VS
0ohm 0603 (R13)
+TPAN_VDD
0ohm 0805 (RA1)
+5V_PVDD
0ohm 0603 (RA4)
+5V_AVDD
JP5
+5V_HDD
AP2330W-7 (UV17)
+VDISPLAY_VCC
FUSE 0.5A_13.2V (F3)
+5V_KB_BL
SN1610042ZQZR (UT4)
+TBTA_VBUS
PLS11, PLS12
+TBTA_VBUS_1
PLS11, PLS12
AON7409 (PQS17,PAS18)
+VBUS_DC_TRIP
AON7409 (PQS1,PAS15)
+VBUS_DC_SS
AON7409 (PQS2,PAS16)
+SDC_IN
CHARGER ISL9538HRTZ-T (PUB01)
RT9058-33GX (PUS04)
+3.3V_VBUS_IN
PLS11, PLS12
RB551V-30 (DT17)
+3VALW_PD
PJP301
SY8288BRAC (PU301)
+3VLP
BAS40C (D1)
+RTC_CELL
+RTC_VCC
EN_3V
+3VALWP
PJP303
PJP302
+3VALW
EM5209VF (UZ1)
SIO_SLP_S3#
JPZ2
+3VS
SY6288C20AAC (U1)
LCD_VCC_TEST_EN_R
or
EDP_VDD_EN
+LCDVDD
RT9041E-15GQW (UP1)
+1.2V_RTM_IN
0ohm 0603 (RE2)
+3VALW_EC
SY6288C20AAC (UL2)
AUX_ON
+LAN_VDD33
0ohm 0402 (RT97)
+3.3V_TBT_SX
0ohm 0805 (RT95)
+3VS_TBT
RB551V-30 (DT18)
+3VALW_PD
EM5209VF (UZ7)
+3V_PCH_PRIM
RH162
+3VALW_DSW
PJP1801
RT8061AZQW (PU1801)
POK
+1.8VALWP
PJP1802
+1.8V_PRIM
AOZ1331 (UG12)
1V8_AON_ON
+1V8_AON
1V8_MAIN_EN
+1V8_MAIN
LN2306LT1G (QA1)
+1.8V_AVDD
0ohm 0603 (RE66)
+1.8VALW_EC
PJP2501
RT9059GSP (PU2501)
SIO_SLP_S4#
+2.5VP
PJP2502
+2.5V_MEM
PJP1001
RT8061AZQW (PU1001)
PEX_VDD_EN
+1.0VS_VGAP
PJP1002
+1VS_GFX
NCP302045MNTXG (PUI01)
NCP302045MNTXG (PUI02)
DRVON
PWM2_4PH/ADDR
PWM1_4PH/ICCMAX4
+VCC_CORE
NCP302045MN (PUG01)
DRVON
PWM1_2PH/ICCMAX2
+VCC_GT
NCP302035MNTXG (PUA01)
DRVON
PWM1_1PH/ICCMAX1
+VCC_SA
NCP302045MNTXG (PUV01)
+GPU_CORE
NCP302045MNTXG (PUV02)
+GPU_CORE
NCP302045MNTXG (PUV03)
+GPU_CORE

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Power Rail

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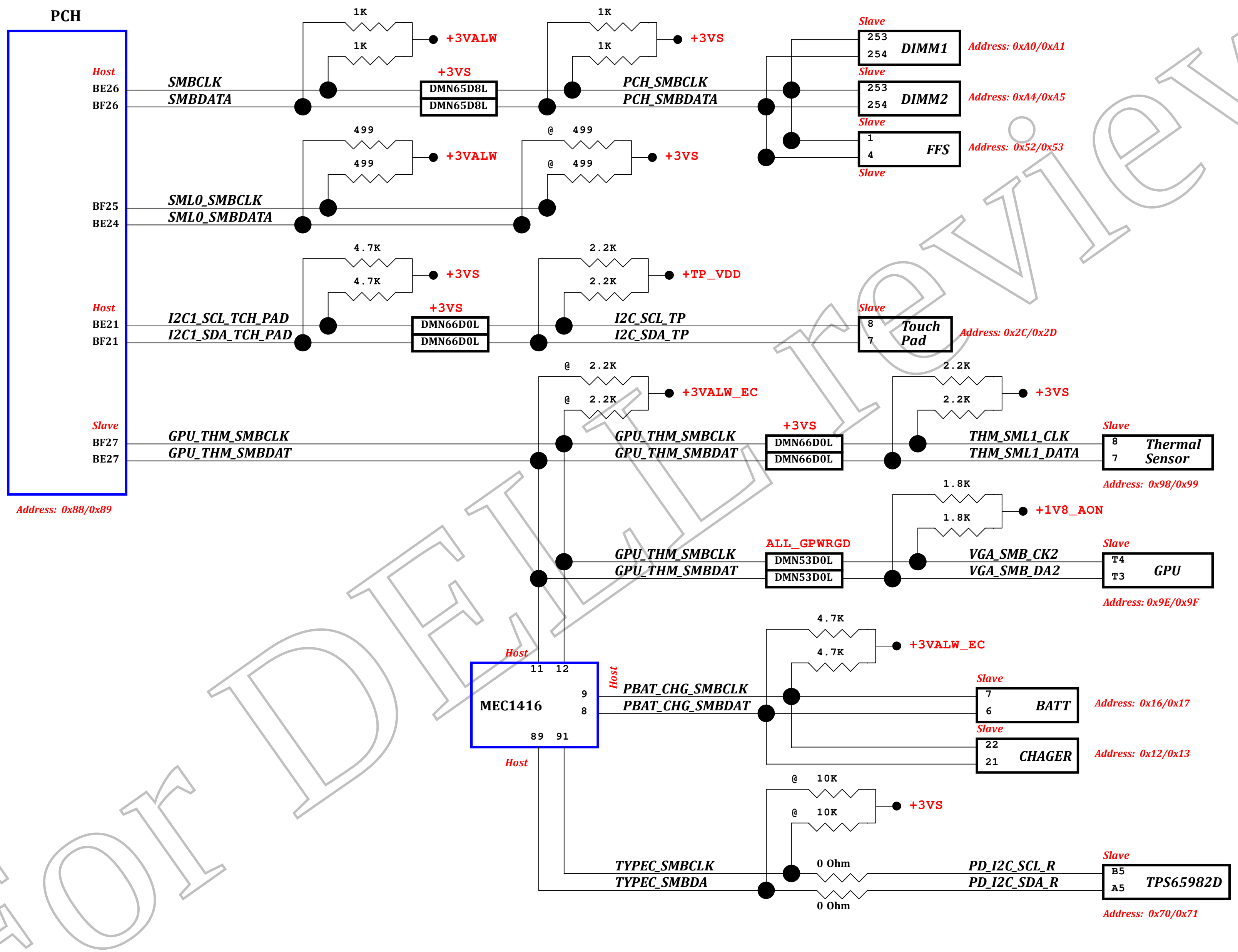
PCH
Host
BE26
BF26
SMBCLK
SMBDATA
1K
1K
+3VALW
+3VS
DMN65D8L
DMN65D8L
1K
1K
+3VS
PCH_SMBCLK
PCH_SMBDATA
Slave
253
254
DIMM1
Address: 0xA0/0xA1
Slave
253
254
DIMM2
Address: 0xA4/0xA5
Slave
1
4
FFS
Address: 0x52/0x53
Slave
499
499
+3VALW
@ 499
@ 499
+3VS
BF25
BE24
SML0_SMBCLK
SML0_SMBDATA
4.7K
4.7K
+3VS
2.2K
2.2K
+TP_VDD
Host
BE21
BF21
I2C1_SCL_TCH_PAD
I2C1_SDA_TCH_PAD
+3VS
DMN66D0L
DMN66D0L
I2C_SCL_TP
I2C_SDA_TP
Slave
8
7
Touch Pad
Address: 0x2C/0x2D
@ 2.2K
@ 2.2K
+3VALW_EC
2.2K
2.2K
+3VS
Slave
BF27
BE27
GPU_THM_SMBCLK
GPU_THM_SMBDAT
GPU_THM_SMBCLK
GPU_THM_SMBDAT
+3VS
DMN66D0L
DMN66D0L
THM_SML1_CLK
THM_SML1_DATA
Slave
8
7
Thermal Sensor
Address: 0x98/0x99
Address: 0x88/0x89
1.8K
1.8K
+1V8_AON
GPU_THM_SMBCLK
GPU_THM_SMBDAT
ALL_GPWRGD
DMN53D0L
DMN53D0L
VGA_SMB_CK2
VGA_SMB_DA2
Slave
T4
T3
GPU
Address: 0x9E/0x9F
4.7K
4.7K
+3VALW_EC
Host
11 12
MEC1416
9
8
89 91
Host
Host
PBAT_CHG_SMBCLK
PBAT_CHG_SMBDAT
Slave
7
6
BATT
Address: 0x16/0x17
Slave
22
21
CHAGER
Address: 0x12/0x13
@ 10K
@ 10K
+3VS
TYPEC_SMBCLK
TYPEC_SMBDA
0 Ohm
0 Ohm
PD_I2C_SCL_R
PD_I2C_SDA_R
Slave
B5
A5
TPS65982D
Address: 0x70/0x71

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Title
SMBus Block Diagram

Size Custom
Document Number **LA-F611P**
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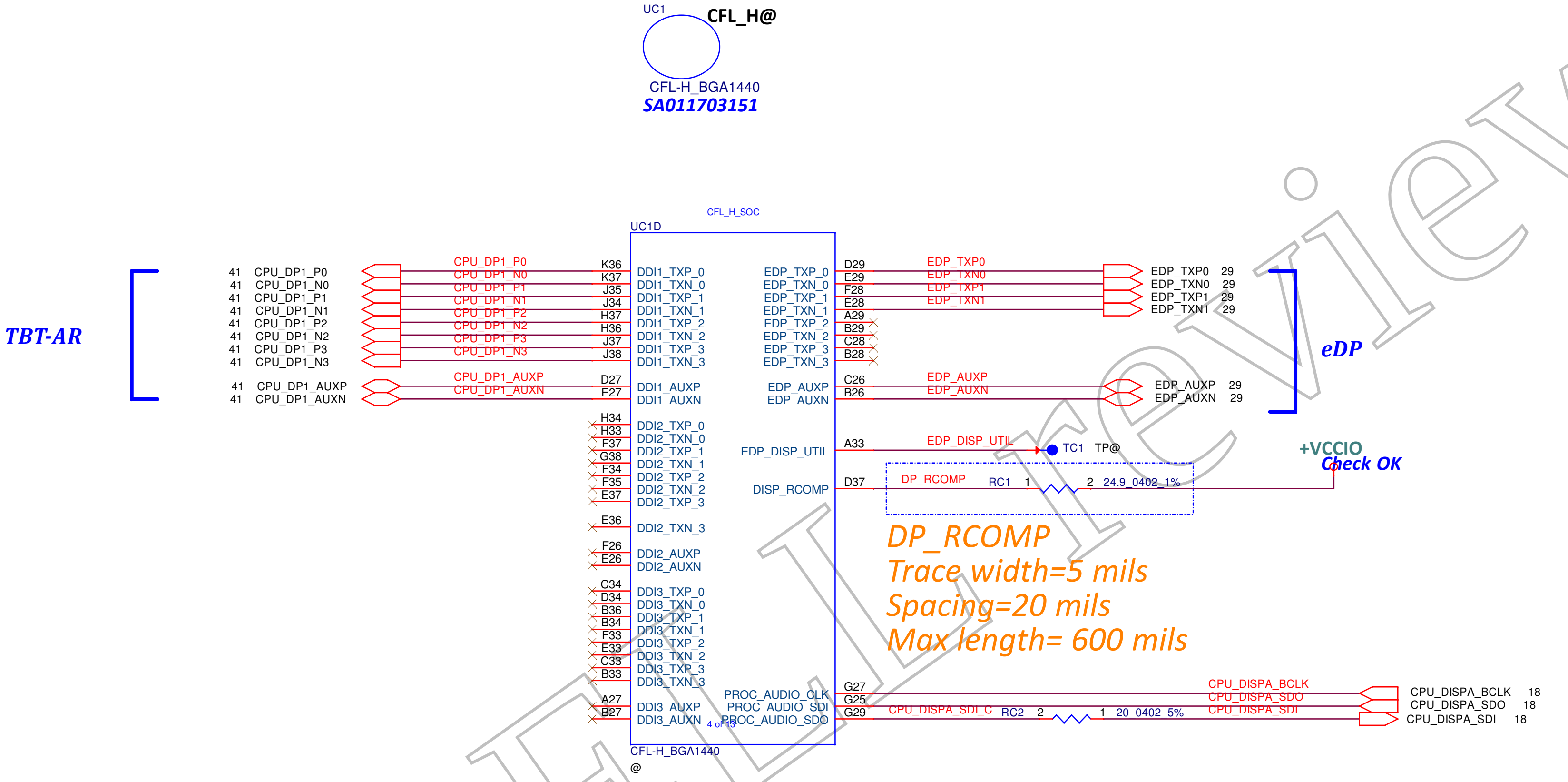
Main Func = CPU


UC1
CFL_H@
CFL-H_BGA1440
SA011703151
CFL_H_SOC
UC1D
TBT-AR
41 CPU_DP1_P0
41 CPU_DP1_N0
41 CPU_DP1_P1
41 CPU_DP1_N1
41 CPU_DP1_P2
41 CPU_DP1_N2
41 CPU_DP1_P3
41 CPU_DP1_N3
41 CPU_DP1_AUXP
41 CPU_DP1_AUXN
K36 DDI1_TXP_0
K37 DDI1_TXN_0
J35 DDI1_TXP_1
J34 DDI1_TXN_1
H37 DDI1_TXP_2
H36 DDI1_TXN_2
J37 DDI1_TXP_3
J38 DDI1_TXN_3
D27 DDI1_AUXP
E27 DDI1_AUXN
H34 DDI2_TXP_0
H33 DDI2_TXN_0
F37 DDI2_TXP_1
G38 DDI2_TXN_1
F34 DDI2_TXP_2
F35 DDI2_TXN_2
E37 DDI2_TXP_3
E36 DDI2_TXN_3
F26 DDI2_AUXP
E26 DDI2_AUXN
C34 DDI3_TXP_0
D34 DDI3_TXN_0
B36 DDI3_TXP_1
B34 DDI3_TXN_1
F33 DDI3_TXP_2
E33 DDI3_TXN_2
C33 DDI3_TXP_3
B33 DDI3_TXN_3
A27 DDI3_AUXP
B27 DDI3_AUXN
EDP_TXP_0 D29
EDP_TXN_0 E29
EDP_TXP_1 F28
EDP_TXN_1 E28
EDP_TXP_2 A29
EDP_TXN_2 B29
EDP_TXP_3 C28
EDP_TXN_3 B28
EDP_AUXP C26
EDP_AUXN B26
EDP_DISP_UTIL A33
DISP_RCOMP D37
PROC_AUDIO_CLK G27
PROC_AUDIO_SDI G25
PROC_AUDIO_SDO G29
4 of 13
CFL-H_BGA1440
@
EDP_TXP0
EDP_TXN0
EDP_TXP1
EDP_TXN1
EDP_TXP0 29
EDP_TXN0 29
EDP_TXP1 29
EDP_TXN1 29
EDP_AUXP
EDP_AUXN
EDP_AUXP 29
EDP_AUXN 29
eDP
EDP_DISP_UTIL
TC1 TP@
DP_RCOMP
RC1 1 2 24.9_0402_1%
+VCCIO
Check OK
CPU_DISPA_BCLK
CPU_DISPA_SDO
CPU_DISPA_SDI_C
RC2 2 1 20_0402_5%
CPU_DISPA_SDI
CPU_DISPA_BCLK 18
CPU_DISPA_SDO 18
CPU_DISPA_SDI 18

DP_RCOMP
Trace width=5 mils
Spacing=20 mils
Max length= 600 mils

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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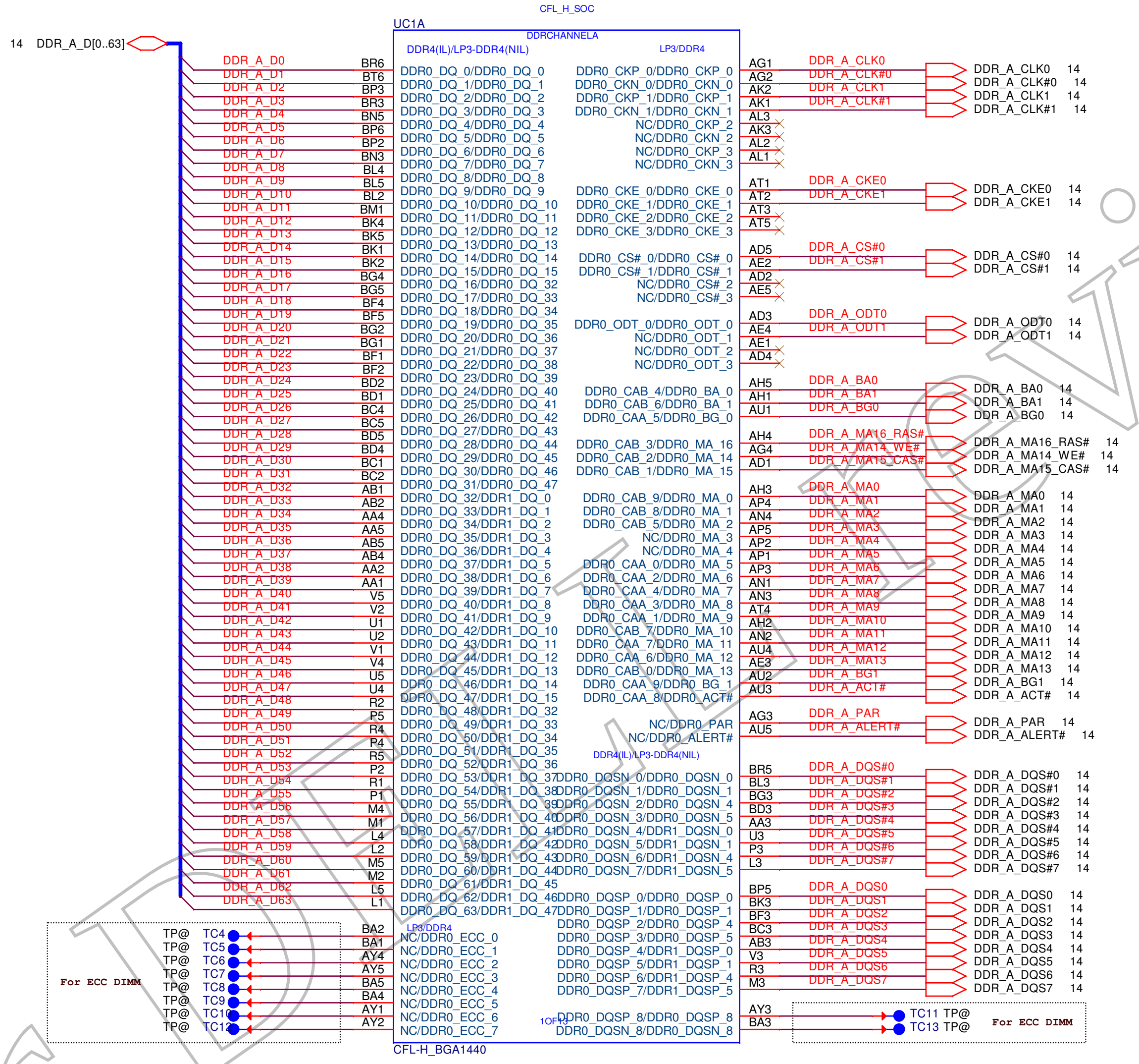
Compal Electronics, Inc.

Title
CFL-H(1/8)DDI/eDP

Size Document Number Rev
LA-F611P 0.3

Date: Thursday, March 22, 2018 Sheet 6 of 78

Main Func = CPU


CFL_H_SOC
UC1A
DDRCHANNELA
DDR4(IL)/LP3-DDR4(NIL)
LP3/DDR4
14 DDR_A_D[0..63]
DDR_A_D0 BR6 DDR0_DQ_0/DDR0_DQ_0
DDR_A_D1 BT6 DDR0_DQ_1/DDR0_DQ_1
DDR_A_D2 BP3 DDR0_DQ_2/DDR0_DQ_2
DDR_A_D3 BR3 DDR0_DQ_3/DDR0_DQ_3
DDR_A_D4 BN5 DDR0_DQ_4/DDR0_DQ_4
DDR_A_D5 BP6 DDR0_DQ_5/DDR0_DQ_5
DDR_A_D6 BP2 DDR0_DQ_6/DDR0_DQ_6
DDR_A_D7 BN3 DDR0_DQ_7/DDR0_DQ_7
DDR_A_D8 BL4 DDR0_DQ_8/DDR0_DQ_8
DDR_A_D9 BL5 DDR0_DQ_9/DDR0_DQ_9
DDR_A_D10 BL2 DDR0_DQ_10/DDR0_DQ_10
DDR_A_D11 BM1 DDR0_DQ_11/DDR0_DQ_11
DDR_A_D12 BK4 DDR0_DQ_12/DDR0_DQ_12
DDR_A_D13 BK5 DDR0_DQ_13/DDR0_DQ_13
DDR_A_D14 BK1 DDR0_DQ_14/DDR0_DQ_14
DDR_A_D15 BK2 DDR0_DQ_15/DDR0_DQ_15
DDR_A_D16 BG4 DDR0_DQ_16/DDR0_DQ_32
DDR_A_D17 BG5 DDR0_DQ_17/DDR0_DQ_33
DDR_A_D18 BF4 DDR0_DQ_18/DDR0_DQ_34
DDR_A_D19 BF5 DDR0_DQ_19/DDR0_DQ_35
DDR_A_D20 BG2 DDR0_DQ_20/DDR0_DQ_36
DDR_A_D21 BG1 DDR0_DQ_21/DDR0_DQ_37
DDR_A_D22 BF1 DDR0_DQ_22/DDR0_DQ_38
DDR_A_D23 BF2 DDR0_DQ_23/DDR0_DQ_39
DDR_A_D24 BD2 DDR0_DQ_24/DDR0_DQ_40
DDR_A_D25 BD1 DDR0_DQ_25/DDR0_DQ_41
DDR_A_D26 BC4 DDR0_DQ_26/DDR0_DQ_42
DDR_A_D27 BC5 DDR0_DQ_27/DDR0_DQ_43
DDR_A_D28 BD5 DDR0_DQ_28/DDR0_DQ_44
DDR_A_D29 BD4 DDR0_DQ_29/DDR0_DQ_45
DDR_A_D30 BC1 DDR0_DQ_30/DDR0_DQ_46
DDR_A_D31 BC2 DDR0_DQ_31/DDR0_DQ_47
DDR_A_D32 AB1 DDR0_DQ_32/DDR1_DQ_0
DDR_A_D33 AB2 DDR0_DQ_33/DDR1_DQ_1
DDR_A_D34 AA4 DDR0_DQ_34/DDR1_DQ_2
DDR_A_D35 AA5 DDR0_DQ_35/DDR1_DQ_3
DDR_A_D36 AB5 DDR0_DQ_36/DDR1_DQ_4
DDR_A_D37 AB4 DDR0_DQ_37/DDR1_DQ_5
DDR_A_D38 AA2 DDR0_DQ_38/DDR1_DQ_6
DDR_A_D39 AA1 DDR0_DQ_39/DDR1_DQ_7
DDR_A_D40 V5 DDR0_DQ_40/DDR1_DQ_8
DDR_A_D41 V2 DDR0_DQ_41/DDR1_DQ_9
DDR_A_D42 U1 DDR0_DQ_42/DDR1_DQ_10
DDR_A_D43 U2 DDR0_DQ_43/DDR1_DQ_11
DDR_A_D44 V1 DDR0_DQ_44/DDR1_DQ_12
DDR_A_D45 V4 DDR0_DQ_45/DDR1_DQ_13
DDR_A_D46 U5 DDR0_DQ_46/DDR1_DQ_14
DDR_A_D47 U4 DDR0_DQ_47/DDR1_DQ_15
DDR_A_D48 R2 DDR0_DQ_48/DDR1_DQ_32
DDR_A_D49 P5 DDR0_DQ_49/DDR1_DQ_33
DDR_A_D50 R4 DDR0_DQ_50/DDR1_DQ_34
DDR_A_D51 P4 DDR0_DQ_51/DDR1_DQ_35
DDR_A_D52 R5 DDR0_DQ_52/DDR1_DQ_36
DDR_A_D53 P2 DDR0_DQ_53/DDR1_DQ_37
DDR_A_D54 R1 DDR0_DQ_54/DDR1_DQ_38
DDR_A_D55 P1 DDR0_DQ_55/DDR1_DQ_39
DDR_A_D56 M4 DDR0_DQ_56/DDR1_DQ_40
DDR_A_D57 M1 DDR0_DQ_57/DDR1_DQ_41
DDR_A_D58 L4 DDR0_DQ_58/DDR1_DQ_42
DDR_A_D59 L2 DDR0_DQ_59/DDR1_DQ_43
DDR_A_D60 M5 DDR0_DQ_60/DDR1_DQ_44
DDR_A_D61 M2 DDR0_DQ_61/DDR1_DQ_45
DDR_A_D62 L5 DDR0_DQ_62/DDR1_DQ_46
DDR_A_D63 L1 DDR0_DQ_63/DDR1_DQ_47
LP3/DDR4
For ECC DIMM
TP@ TC4 BA2 NC/DDR0_ECC_0
TP@ TC5 BA1 NC/DDR0_ECC_1
TP@ TC6 AY4 NC/DDR0_ECC_2
TP@ TC7 AY5 NC/DDR0_ECC_3
TP@ TC8 BA5 NC/DDR0_ECC_4
TP@ TC9 BA4 NC/DDR0_ECC_5
TP@ TC10 AY1 NC/DDR0_ECC_6
TP@ TC12 AY2 NC/DDR0_ECC_7
DDR0_CKP_0/DDR0_CKP_0 AG1 DDR_A_CLK0 DDR_A_CLK0 14
DDR0_CKN_0/DDR0_CKN_0 AG2 DDR_A_CLK#0 DDR_A_CLK#0 14
DDR0_CKP_1/DDR0_CKP_1 AK2 DDR_A_CLK1 DDR_A_CLK1 14
DDR0_CKN_1/DDR0_CKN_1 AK1 DDR_A_CLK#1 DDR_A_CLK#1 14
NC/DDR0_CKP_2 AL3
NC/DDR0_CKN_2 AK3
NC/DDR0_CKP_3 AL2
NC/DDR0_CKN_3 AL1
DDR0_CKE_0/DDR0_CKE_0 AT1 DDR_A_CKE0 DDR_A_CKE0 14
DDR0_CKE_1/DDR0_CKE_1 AT2 DDR_A_CKE1 DDR_A_CKE1 14
DDR0_CKE_2/DDR0_CKE_2 AT3
DDR0_CKE_3/DDR0_CKE_3 AT5
DDR0_CS#_0/DDR0_CS#_0 AD5 DDR_A_CS#0 DDR_A_CS#0 14
DDR0_CS#_1/DDR0_CS#_1 AE2 DDR_A_CS#1 DDR_A_CS#1 14
NC/DDR0_CS#_2 AD2
NC/DDR0_CS#_3 AE5
DDR0_ODT_0/DDR0_ODT_0 AD3 DDR_A_ODT0 DDR_A_ODT0 14
NC/DDR0_ODT_1 AE4 DDR_A_ODT1 DDR_A_ODT1 14
NC/DDR0_ODT_2 AE1
NC/DDR0_ODT_3 AD4
DDR0_CAB_4/DDR0_BA_0 AH5 DDR_A_BA0 DDR_A_BA0 14
DDR0_CAB_6/DDR0_BA_1 AH1 DDR_A_BA1 DDR_A_BA1 14
DDR0_CAA_5/DDR0_BG_0 AU1 DDR_A_BG0 DDR_A_BG0 14
DDR0_CAB_3/DDR0_MA_16 AH4 DDR_A_MA16_RAS# DDR_A_MA16_RAS# 14
DDR0_CAB_2/DDR0_MA_14 AG4 DDR_A_MA14_WE# DDR_A_MA14_WE# 14
DDR0_CAB_1/DDR0_MA_15 AD1 DDR_A_MA15_CAS# DDR_A_MA15_CAS# 14
DDR0_CAB_9/DDR0_MA_0 AH3 DDR_A_MA0 DDR_A_MA0 14
DDR0_CAB_8/DDR0_MA_1 AP4 DDR_A_MA1 DDR_A_MA1 14
DDR0_CAB_5/DDR0_MA_2 AN4 DDR_A_MA2 DDR_A_MA2 14
NC/DDR0_MA_3 AP5 DDR_A_MA3 DDR_A_MA3 14
NC/DDR0_MA_4 AP2 DDR_A_MA4 DDR_A_MA4 14
DDR0_CAA_0/DDR0_MA_5 AP1 DDR_A_MA5 DDR_A_MA5 14
DDR0_CAA_2/DDR0_MA_6 AP3 DDR_A_MA6 DDR_A_MA6 14
DDR0_CAA_4/DDR0_MA_7 AN1 DDR_A_MA7 DDR_A_MA7 14
DDR0_CAA_3/DDR0_MA_8 AN3 DDR_A_MA8 DDR_A_MA8 14
DDR0_CAA_1/DDR0_MA_9 AT4 DDR_A_MA9 DDR_A_MA9 14
DDR0_CAB_7/DDR0_MA_10 AH2 DDR_A_MA10 DDR_A_MA10 14
DDR0_CAA_7/DDR0_MA_11 AN2 DDR_A_MA11 DDR_A_MA11 14
DDR0_CAA_6/DDR0_MA_12 AU4 DDR_A_MA12 DDR_A_MA12 14
DDR0_CAB_0/DDR0_MA_13 AE3 DDR_A_MA13 DDR_A_MA13 14
DDR0_CAA_9/DDR0_BG_1 AU2 DDR_A_BG1 DDR_A_BG1 14
DDR0_CAA_8/DDR0_ACT# AU3 DDR_A_ACT# DDR_A_ACT# 14
NC/DDR0_PAR AG3 DDR_A_PAR DDR_A_PAR 14
NC/DDR0_ALERT# AU5 DDR_A_ALERT# DDR_A_ALERT# 14
DDR4(IL)/LP3-DDR4(NIL)
DDR0_DQSN_0/DDR0_DQSN_0 BR5 DDR_A_DQS#0 DDR_A_DQS#0 14
DDR0_DQSN_1/DDR0_DQSN_1 BL3 DDR_A_DQS#1 DDR_A_DQS#1 14
DDR0_DQSN_2/DDR0_DQSN_4 BG3 DDR_A_DQS#2 DDR_A_DQS#2 14
DDR0_DQSN_3/DDR0_DQSN_5 BD3 DDR_A_DQS#3 DDR_A_DQS#3 14
DDR0_DQSN_4/DDR1_DQSN_0 AA3 DDR_A_DQS#4 DDR_A_DQS#4 14
DDR0_DQSN_5/DDR1_DQSN_1 U3 DDR_A_DQS#5 DDR_A_DQS#5 14
DDR0_DQSN_6/DDR1_DQSN_4 P3 DDR_A_DQS#6 DDR_A_DQS#6 14
DDR0_DQSN_7/DDR1_DQSN_5 L3 DDR_A_DQS#7 DDR_A_DQS#7 14
DDR0_DQSP_0/DDR0_DQSP_0 BP5 DDR_A_DQS0 DDR_A_DQS0 14
DDR0_DQSP_1/DDR0_DQSP_1 BK3 DDR_A_DQS1 DDR_A_DQS1 14
DDR0_DQSP_2/DDR0_DQSP_4 BF3 DDR_A_DQS2 DDR_A_DQS2 14
DDR0_DQSP_3/DDR0_DQSP_5 BC3 DDR_A_DQS3 DDR_A_DQS3 14
DDR0_DQSP_4/DDR1_DQSP_0 AB3 DDR_A_DQS4 DDR_A_DQS4 14
DDR0_DQSP_5/DDR1_DQSP_1 V3 DDR_A_DQS5 DDR_A_DQS5 14
DDR0_DQSP_6/DDR1_DQSP_4 R3 DDR_A_DQS6 DDR_A_DQS6 14
DDR0_DQSP_7/DDR1_DQSP_5 M3 DDR_A_DQS7 DDR_A_DQS7 14
1OF13
DDR0_DQSP_8/DDR0_DQSP_8 AY3 TC11 TP@
DDR0_DQSN_8/DDR0_DQSN_8 BA3 TC13 TP@
For ECC DIMM
CFL-H_BGA1440

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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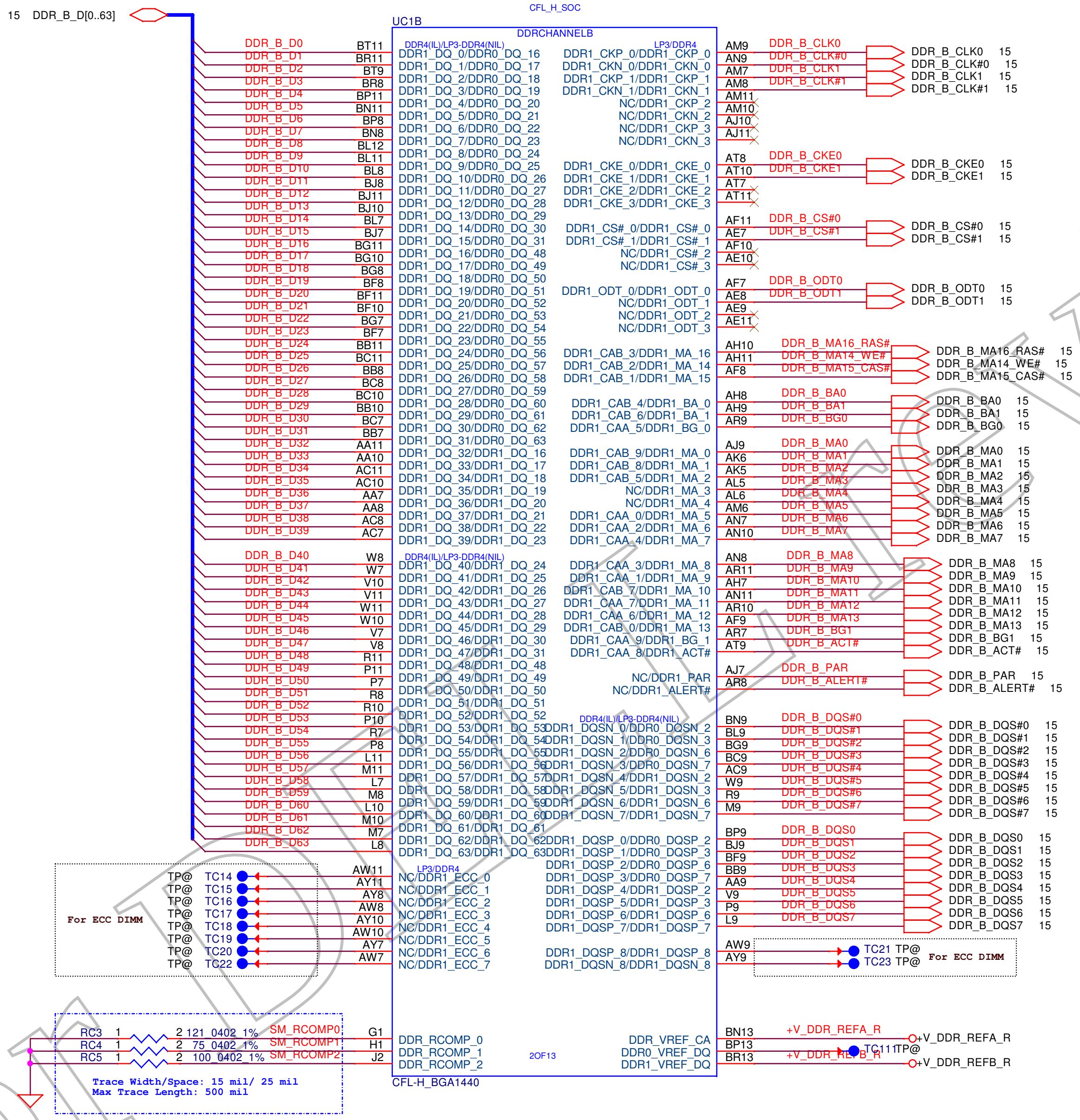
Compal Electronics, Inc.

Title
CFL-H(2/8)DIMMA

Size Document Number
LA-F611P
Rev
0.3

Date: Thursday, March 22, 2018

Main Func = CPU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CFL_H_SOC
UC1B
DDRCHANNELB
DDR4(IL)/LP3-DDR4(NIL)
LP3/DDR4
DDR1_DQ_0/DDR0_DQ_16
DDR1_CKP_0/DDR1_CKP_0
DDR1_CKN_0/DDR1_CKN_0
DDR1_CKP_1/DDR1_CKP_1
DDR1_CKN_1/DDR1_CKN_1
DDR1_CKE_0/DDR1_CKE_0
DDR1_CKE_1/DDR1_CKE_1
DDR1_CS#_0/DDR1_CS#_0
DDR1_CS#_1/DDR1_CS#_1
DDR1_ODT_0/DDR1_ODT_0
DDR1_CAB_3/DDR1_MA_16
DDR1_CAB_2/DDR1_MA_14
DDR1_CAB_1/DDR1_MA_15
DDR1_CAB_4/DDR1_BA_0
DDR1_CAB_6/DDR1_BA_1
DDR1_CAA_5/DDR1_BG_0
DDR1_CAA_9/DDR1_BG_1
DDR1_CAA_8/DDR1_ACT#
NC/DDR1_PAR
NC/DDR1_ALERT#
DDR1_DQSN_0/DDR0_DQSN_2
DDR1_DQSP_0/DDR0_DQSP_2
DDR1_DQSP_8/DDR1_DQSP_8
DDR1_DQSN_8/DDR1_DQSN_8
NC/DDR1_ECC_0
NC/DDR1_ECC_7
DDR_B_CLK0 15
DDR_B_CLK#0 15
DDR_B_CLK1 15
DDR_B_CLK#1 15
DDR_B_CKE0 15
DDR_B_CKE1 15
DDR_B_CS#0 15
DDR_B_CS#1 15
DDR_B_ODT0 15
DDR_B_ODT1 15
DDR_B_MA16_RAS# 15
DDR_B_MA14_WE# 15
DDR_B_MA15_CAS# 15
DDR_B_BA0 15
DDR_B_BA1 15
DDR_B_BG0 15
DDR_B_BG1 15
DDR_B_ACT# 15
DDR_B_PAR 15
DDR_B_ALERT# 15
For ECC DIMM
TP@ TC14 … TC22
TC21 TP@
TC23 TP@
DDR_RCOMP_0
DDR_RCOMP_1
DDR_RCOMP_2
RC3 1 2 121_0402_1% SM_RCOMP0
RC4 1 2 75_0402_1% SM_RCOMP1
RC5 1 2 100_0402_1% SM_RCOMP2
Trace Width/Space: 15 mil/ 25 mil
Max Trace Length: 500 mil
DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ
+V_DDR_REFA_R
+V_DDR_REFB_R
TC111TP@
2OF13
CFL-H_BGA1440

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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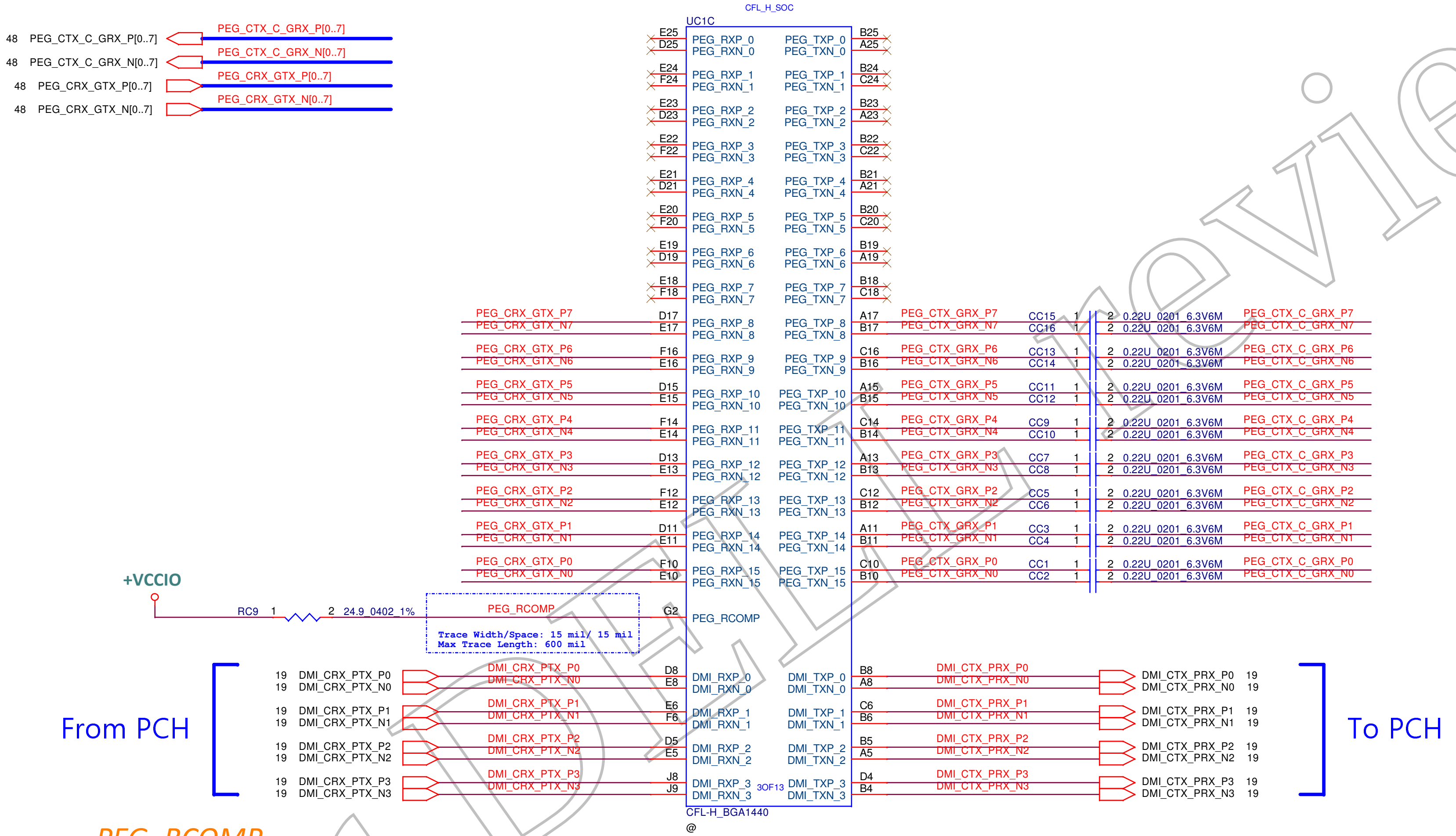
Compal Electronics, Inc.

Title
CFL-H(3/8)DIMMB

Size Document Number **LA-F611P** Rev 0.3

Date: Thursday, March 22, 2018 Sheet 8 of 78

Main Func = CPU



CFL_H_SOC
UC1C
48 PEG_CTX_C_GRX_P[0..7]
48 PEG_CTX_C_GRX_N[0..7]
48 PEG_CRX_GTX_P[0..7]
48 PEG_CRX_GTX_N[0..7]
PEG_CTX_C_GRX_P[0..7]
PEG_CTX_C_GRX_N[0..7]
PEG_CRX_GTX_P[0..7]
PEG_CRX_GTX_N[0..7]
E25 D25 PEG_RXP_0 PEG_RXN_0
E24 F24 PEG_RXP_1 PEG_RXN_1
E23 D23 PEG_RXP_2 PEG_RXN_2
E22 F22 PEG_RXP_3 PEG_RXN_3
E21 D21 PEG_RXP_4 PEG_RXN_4
E20 F20 PEG_RXP_5 PEG_RXN_5
E19 D19 PEG_RXP_6 PEG_RXN_6
E18 F18 PEG_RXP_7 PEG_RXN_7
PEG_CRX_GTX_P7 PEG_CRX_GTX_N7 D17 E17 PEG_RXP_8 PEG_RXN_8
PEG_CRX_GTX_P6 PEG_CRX_GTX_N6 F16 E16 PEG_RXP_9 PEG_RXN_9
PEG_CRX_GTX_P5 PEG_CRX_GTX_N5 D15 E15 PEG_RXP_10 PEG_RXN_10
PEG_CRX_GTX_P4 PEG_CRX_GTX_N4 F14 E14 PEG_RXP_11 PEG_RXN_11
PEG_CRX_GTX_P3 PEG_CRX_GTX_N3 D13 E13 PEG_RXP_12 PEG_RXN_12
PEG_CRX_GTX_P2 PEG_CRX_GTX_N2 F12 E12 PEG_RXP_13 PEG_RXN_13
PEG_CRX_GTX_P1 PEG_CRX_GTX_N1 D11 E11 PEG_RXP_14 PEG_RXN_14
PEG_CRX_GTX_P0 PEG_CRX_GTX_N0 F10 E10 PEG_RXP_15 PEG_RXN_15
PEG_TXP_0 PEG_TXN_0 B25 A25
PEG_TXP_1 PEG_TXN_1 B24 C24
PEG_TXP_2 PEG_TXN_2 B23 A23
PEG_TXP_3 PEG_TXN_3 B22 C22
PEG_TXP_4 PEG_TXN_4 B21 A21
PEG_TXP_5 PEG_TXN_5 B20 C20
PEG_TXP_6 PEG_TXN_6 B19 A19
PEG_TXP_7 PEG_TXN_7 B18 C18
PEG_TXP_8 PEG_TXN_8 A17 B17 PEG_CTX_GRX_P7 PEG_CTX_GRX_N7 CC15 CC16 0.22U_0201_6.3V6M PEG_CTX_C_GRX_P7 PEG_CTX_C_GRX_N7
PEG_TXP_9 PEG_TXN_9 C16 B16 PEG_CTX_GRX_P6 PEG_CTX_GRX_N6 CC13 CC14 0.22U_0201_6.3V6M PEG_CTX_C_GRX_P6 PEG_CTX_C_GRX_N6
PEG_TXP_10 PEG_TXN_10 A15 B15 PEG_CTX_GRX_P5 PEG_CTX_GRX_N5 CC11 CC12 0.22U_0201_6.3V6M PEG_CTX_C_GRX_P5 PEG_CTX_C_GRX_N5
PEG_TXP_11 PEG_TXN_11 C14 B14 PEG_CTX_GRX_P4 PEG_CTX_GRX_N4 CC9 CC10 0.22U_0201_6.3V6M PEG_CTX_C_GRX_P4 PEG_CTX_C_GRX_N4
PEG_TXP_12 PEG_TXN_12 A13 B13 PEG_CTX_GRX_P3 PEG_CTX_GRX_N3 CC7 CC8 0.22U_0201_6.3V6M PEG_CTX_C_GRX_P3 PEG_CTX_C_GRX_N3
PEG_TXP_13 PEG_TXN_13 C12 B12 PEG_CTX_GRX_P2 PEG_CTX_GRX_N2 CC5 CC6 0.22U_0201_6.3V6M PEG_CTX_C_GRX_P2 PEG_CTX_C_GRX_N2
PEG_TXP_14 PEG_TXN_14 A11 B11 PEG_CTX_GRX_P1 PEG_CTX_GRX_N1 CC3 CC4 0.22U_0201_6.3V6M PEG_CTX_C_GRX_P1 PEG_CTX_C_GRX_N1
PEG_TXP_15 PEG_TXN_15 C10 B10 PEG_CTX_GRX_P0 PEG_CTX_GRX_N0 CC1 CC2 0.22U_0201_6.3V6M PEG_CTX_C_GRX_P0 PEG_CTX_C_GRX_N0
+VCCIO
RC9 1 2 24.9_0402_1%
PEG_RCOMP G2 PEG_RCOMP
Trace Width/Space: 15 mil/ 15 mil
Max Trace Length: 600 mil
From PCH
19 DMI_CRX_PTX_P0 19 DMI_CRX_PTX_N0 D8 E8 DMI_RXP_0 DMI_RXN_0
19 DMI_CRX_PTX_P1 19 DMI_CRX_PTX_N1 E6 F6 DMI_RXP_1 DMI_RXN_1
19 DMI_CRX_PTX_P2 19 DMI_CRX_PTX_N2 D5 E5 DMI_RXP_2 DMI_RXN_2
19 DMI_CRX_PTX_P3 19 DMI_CRX_PTX_N3 J8 J9 DMI_RXP_3 DMI_RXN_3
DMI_TXP_0 DMI_TXN_0 B8 A8 DMI_CTX_PRX_P0 DMI_CTX_PRX_N0 19
DMI_TXP_1 DMI_TXN_1 C6 B6 DMI_CTX_PRX_P1 DMI_CTX_PRX_N1 19
DMI_TXP_2 DMI_TXN_2 B5 A5 DMI_CTX_PRX_P2 DMI_CTX_PRX_N2 19
DMI_TXP_3 DMI_TXN_3 D4 B4 DMI_CTX_PRX_P3 DMI_CTX_PRX_N3 19
3OF13
CFL-H_BGA1440
@
To PCH

PEG_RCOMP
Trace width=15 mils
Spacing=15 mils
Max length= 600 mils

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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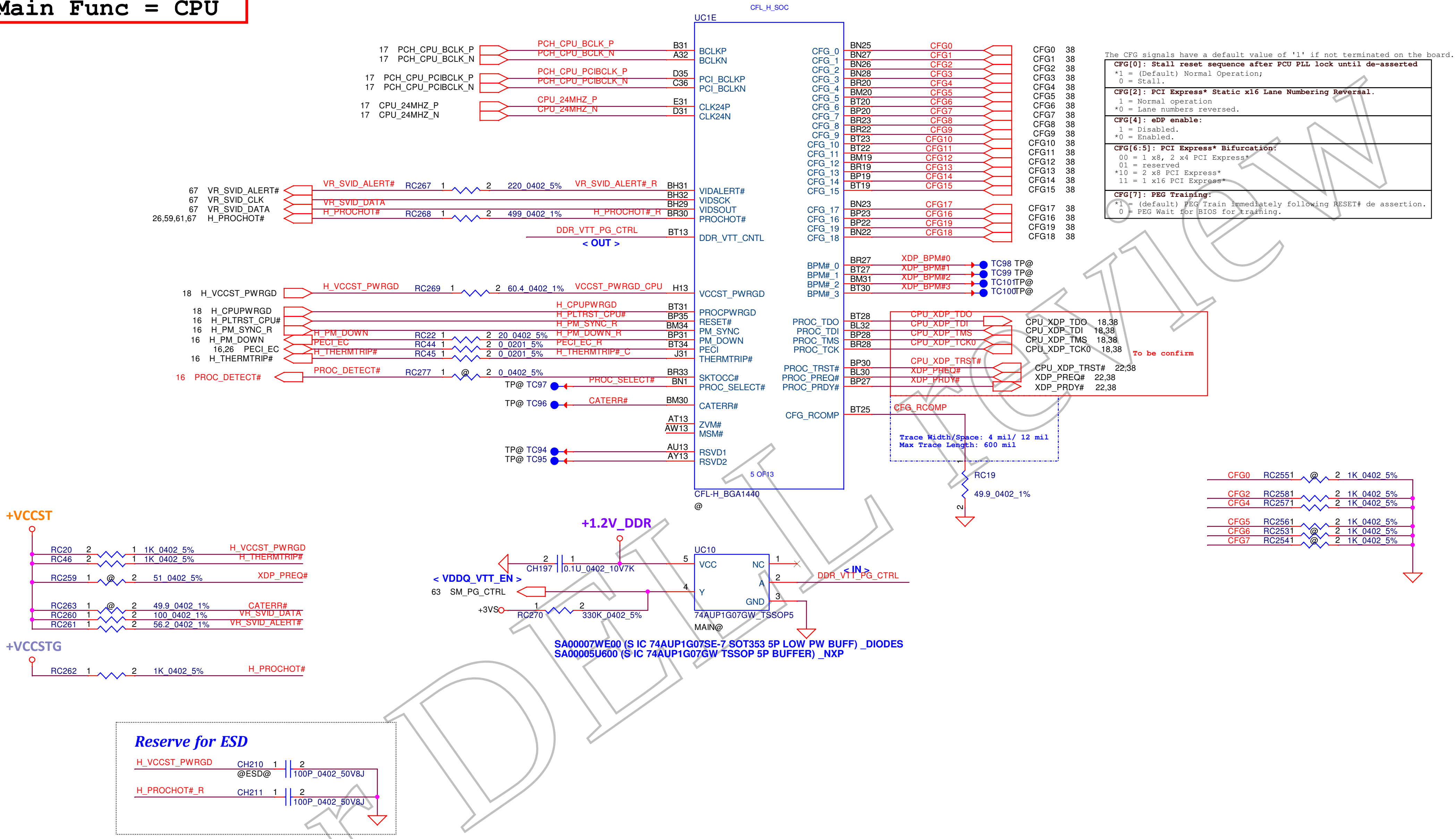
Compal Electronics, Inc.

Title
CFL-H(4/8)PEG

Size Document Number
LA-F611P
Rev 0.3

Date: Thursday, March 22, 2018 Sheet 9 of 78

Main Func = CPU


CFL_H_SOC
UC1E
17 PCH_CPU_BCLK_P
17 PCH_CPU_BCLK_N
17 PCH_CPU_PCIBCLK_P
17 PCH_CPU_PCIBCLK_N
17 CPU_24MHZ_P
17 CPU_24MHZ_N
B31 A32 BCLKP BCLKN
D35 C36 PCI_BCLKP PCI_BCLKN
E31 D31 CLK24P CLK24N
67 VR_SVID_ALERT#
67 VR_SVID_CLK
67 VR_SVID_DATA
26,59,61,67 H_PROCHOT#
RC267 1 2 220_0402_5% VR_SVID_ALERT#_R
RC268 1 2 499_0402_1% H_PROCHOT#_R
BH31 VIDALERT#
BH32 VIDSCK
BH29 VIDSOUT
BR30 PROCHOT#
DDR_VTT_PG_CTRL < OUT >
BT13 DDR_VTT_CNTL
18 H_VCCST_PWRGD
RC269 1 2 60.4_0402_1% VCCST_PWRGD_CPU
H13 VCCST_PWRGD
18 H_CPUPWRGD
16 H_PLTRST_CPU#
16 H_PM_SYNC_R
16 H_PM_DOWN
16,26 PECI_EC
16 H_THERMTRIP#
RC22 1 2 20_0402_5% H_PM_DOWN_R
RC44 1 2 0_0201_5% PECI_EC_R
RC45 1 2 0_0201_5% H_THERMTRIP#_C
BT31 PROCPWRGD
BP35 RESET#
BM34 PM_SYNC
BP31 PM_DOWN
BT34 PECI
J31 THERMTRIP#
16 PROC_DETECT#
RC277 1 @ 2 0_0402_5%
BR33 SKTOCC#
BN1 PROC_SELECT#
TP@ TC97
TP@ TC96 CATERR# BM30 CATERR#
AT13 ZVM#
AW13 MSM#
TP@ TC94 AU13 RSVD1
TP@ TC95 AY13 RSVD2
5 OF 13
CFL-H_BGA1440
@
CFG_0 … CFG_15: BN25 BN27 BN26 BN28 BR20 BM20 BT20 BP20 BR23 BR22 BT23 BT22 BM19 BR19 BP19 BT19
CFG0 38
CFG1 38
CFG2 38
CFG3 38
CFG4 38
CFG5 38
CFG6 38
CFG7 38
CFG8 38
CFG9 38
CFG10 38
CFG11 38
CFG12 38
CFG13 38
CFG14 38
CFG15 38
CFG_17 BN23 CFG17 38
CFG_16 BP23 CFG16 38
CFG_19 BP22 CFG19 38
CFG_18 BN22 CFG18 38
BPM#_0 BR27 XDP_BPM#0 TC98 TP@
BPM#_1 BT27 XDP_BPM#1 TC99 TP@
BPM#_2 BM31 XDP_BPM#2 TC101TP@
BPM#_3 BT30 XDP_BPM#3 TC100TP@
PROC_TDO BT28 CPU_XDP_TDO 18,38
PROC_TDI BL32 CPU_XDP_TDI 18,38
PROC_TMS BP28 CPU_XDP_TMS 18,38
PROC_TCK BR28 CPU_XDP_TCK0 18,38
To be confirm
PROC_TRST# BP30 CPU_XDP_TRST# 22,38
PROC_PREQ# BL30 XDP_PREQ# 22,38
PROC_PRDY# BP27 XDP_PRDY# 22,38
CFG_RCOMP BT25 CFG_RCOMP
Trace Width/Space: 4 mil/ 12 mil
Max Trace Length: 600 mil
RC19 49.9_0402_1%
CFG0 RC2551 @ 2 1K_0402_5%
CFG2 RC2581 2 1K_0402_5%
CFG4 RC2571 2 1K_0402_5%
CFG5 RC2561 2 1K_0402_5%
CFG6 RC2531 @ 2 1K_0402_5%
CFG7 RC2541 @ 2 1K_0402_5%
+VCCST
RC20 2 1 1K_0402_5% H_VCCST_PWRGD
RC46 2 1 1K_0402_5% H_THERMTRIP#
RC259 1 @ 2 51_0402_5% XDP_PREQ#
RC263 1 @ 2 49.9_0402_1% CATERR#
RC260 1 2 100_0402_1% VR_SVID_DATA
RC261 1 2 56.2_0402_1% VR_SVID_ALERT#
+VCCSTG
RC262 1 2 1K_0402_5% H_PROCHOT#
+1.2V_DDR
CH197 0.1U_0402_10V7K
UC10 VCC NC Y A GND
< VDDQ_VTT_EN >
63 SM_PG_CTRL
+3VS RC270 330K_0402_5%
< IN > DDR_VTT_PG_CTRL
74AUP1G07GW_TSSOP5
MAIN@
SA00007WE00 (S IC 74AUP1G07SE-7 SOT353 5P LOW PW BUFF) _DIODES
SA00005U600 (S IC 74AUP1G07GW TSSOP 5P BUFFER) _NXP
Reserve for ESD
H_VCCST_PWRGD CH210 1 2 @ESD@ 100P_0402_50V8J
H_PROCHOT#_R CH211 1 2 100P_0402_50V8J

The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
*1 = (Default) Normal Operation;
0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
*0 = Lane numbers reversed.

CFG[4]: eDP enable:
1 = Disabled.
*0 = Enabled.

CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express
11 = 1 x16 PCI Express*

CFG[7]: PEG Training:
*1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.

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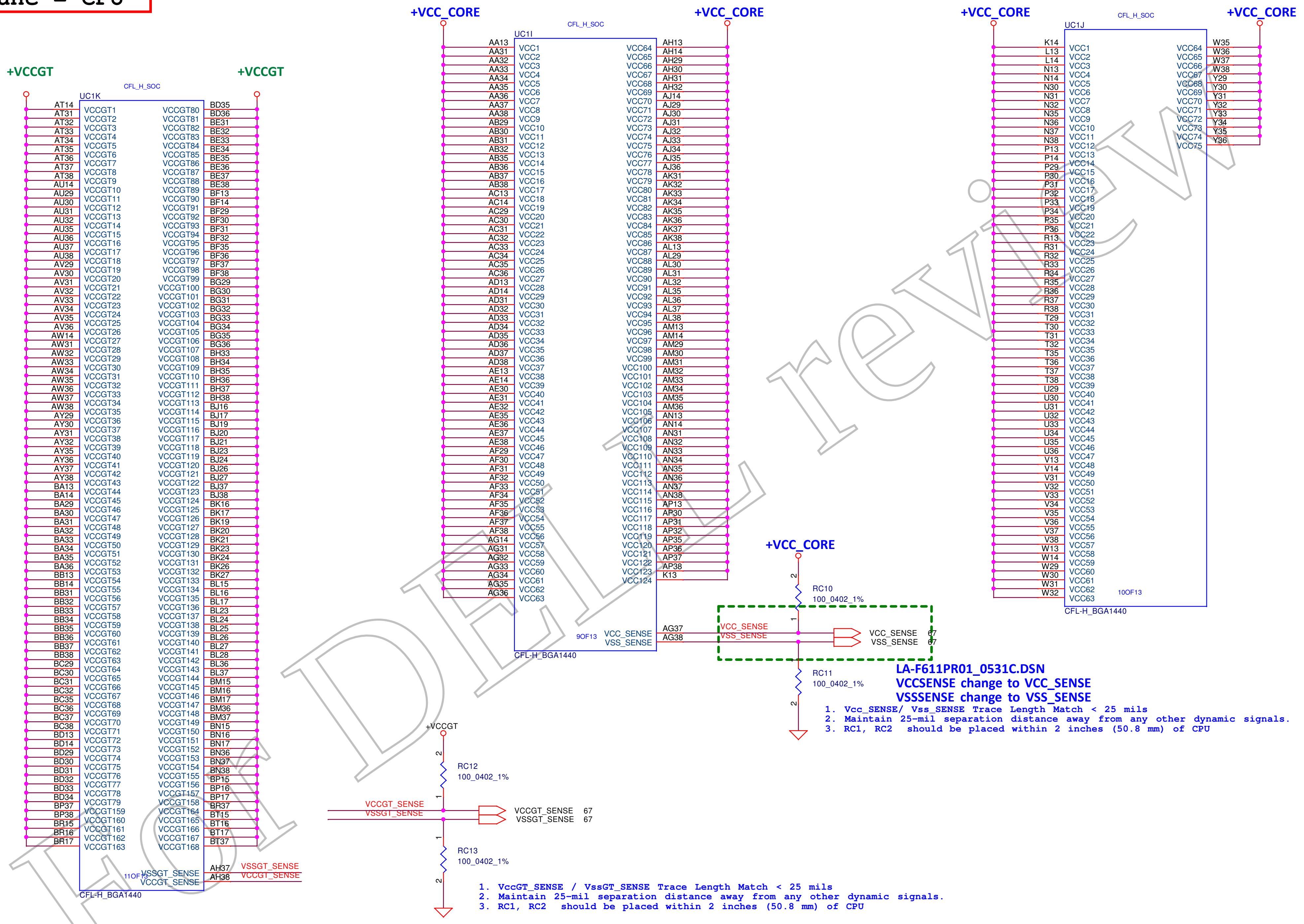
Compal Electronics, Inc.

Title
CFL-H(5/8)CFG

Size Document Number
LA-F611P
Rev 0.3

Date: Thursday, March 22, 2018 Sheet 10 of 78


+VCCGT
+VCCGT
CFL_H_SOC
UC1K
VCCGT1 … VCCGT163
VCCGT80 … VCCGT168
11OF13
VSSGT_SENSE
VCCGT_SENSE
AH37
AH38
VSSGT_SENSE
VCCGT_SENSE
CFL-H_BGA1440
+VCC_CORE
+VCC_CORE
CFL_H_SOC
UC1I
VCC1 … VCC63
VCC64 … VCC124
9OF13
VCC_SENSE
VSS_SENSE
AG37
AG38
CFL-H_BGA1440
+VCC_CORE
+VCC_CORE
CFL_H_SOC
UC1J
VCC1 … VCC63
VCC64 … VCC75
10OF13
CFL-H_BGA1440
+VCC_CORE
RC10
100_0402_1%
VCC_SENSE
VSS_SENSE
VCC_SENSE 67
VSS_SENSE 67
RC11
100_0402_1%
+VCCGT
RC12
100_0402_1%
VCCGT_SENSE
VSSGT_SENSE
VCCGT_SENSE 67
VSSGT_SENSE 67
RC13
100_0402_1%

LA-F611PR01_0531C.DSN

VCCSENSE change to VCC_SENSE

VSSSENSE change to VSS_SENSE

1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

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Compal Electronics, Inc.

Title

CFL-H(6/8)VCC_CORE/GT

Size	Document Number	Rev
	LA-F611P	0.3

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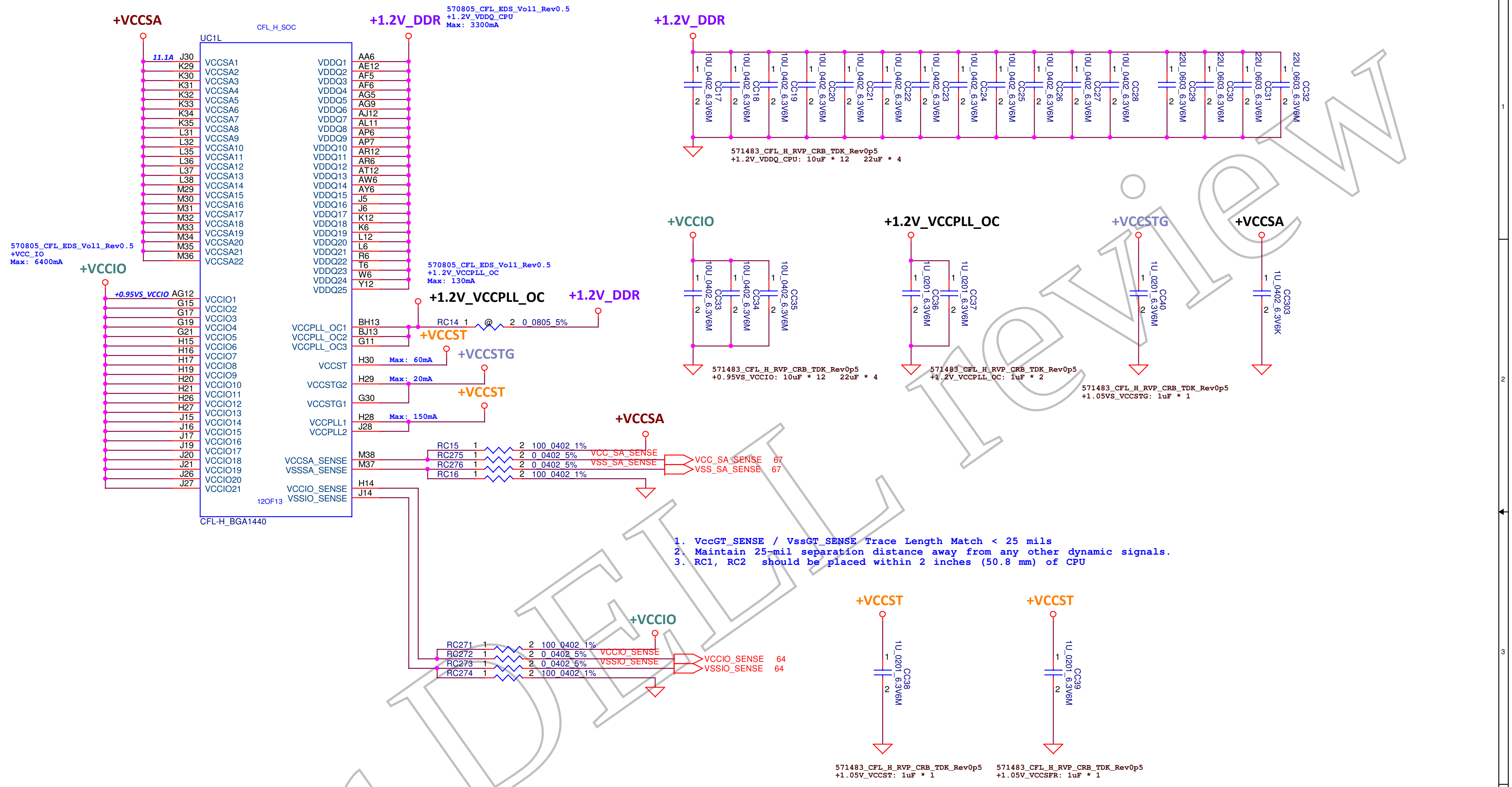
Main Func = CPU



+VCCSA
CFL_H_SOC
UC1L
11.1A
J30 VCCSA1
K29 VCCSA2
K30 VCCSA3
K31 VCCSA4
K32 VCCSA5
K33 VCCSA6
K34 VCCSA7
K35 VCCSA8
L31 VCCSA9
L32 VCCSA10
L35 VCCSA11
L36 VCCSA12
L37 VCCSA13
L38 VCCSA14
M29 VCCSA15
M30 VCCSA16
M31 VCCSA17
M32 VCCSA18
M33 VCCSA19
M34 VCCSA20
M35 VCCSA21
M36 VCCSA22
+1.2V_DDR
570805_CFL_EDS_Vol1_Rev0.5
+1.2V_VDDQ_CPU
Max: 3300mA
VDDQ1 AA6
VDDQ2 AE12
VDDQ3 AF5
VDDQ4 AF6
VDDQ5 AG5
VDDQ6 AG9
VDDQ7 AJ12
VDDQ8 AL11
VDDQ9 AP6
VDDQ10 AP7
VDDQ11 AR12
VDDQ12 AR6
VDDQ13 AT12
VDDQ14 AW6
VDDQ15 AY6
VDDQ16 J5
VDDQ17 J6
VDDQ18 K12
VDDQ19 K6
VDDQ20 L12
VDDQ21 L6
VDDQ22 R6
VDDQ23 T6
VDDQ24 W6
VDDQ25 Y12
570805_CFL_EDS_Vol1_Rev0.5
+VCC_IO
Max: 6400mA
+VCCIO
+0.95VS_VCCIO
AG12 VCCIO1
G15 VCCIO2
G17 VCCIO3
G19 VCCIO4
G21 VCCIO5
H15 VCCIO6
H16 VCCIO7
H17 VCCIO8
H19 VCCIO9
H20 VCCIO10
H21 VCCIO11
H26 VCCIO12
H27 VCCIO13
J15 VCCIO14
J16 VCCIO15
J17 VCCIO16
J19 VCCIO17
J20 VCCIO18
J21 VCCIO19
J26 VCCIO20
J27 VCCIO21
570805_CFL_EDS_Vol1_Rev0.5
+1.2V_VCCPLL_OC
Max: 130mA
+1.2V_VCCPLL_OC
+1.2V_DDR
VCCPLL_OC1 BH13
VCCPLL_OC2 BJ13
VCCPLL_OC3 G11
RC14 1 @ 2 0_0805_5%
+VCCST
VCCST H30 Max: 60mA
+VCCSTG
VCCSTG2 H29 Max: 20mA
VCCSTG1 G30
+VCCST
VCCPLL1 H28 Max: 150mA
VCCPLL2 J28
+VCCSA
VCCSA_SENSE M38
VSSSA_SENSE M37
RC15 1 2 100_0402_1%
RC275 1 2 0_0402_5%
RC276 1 2 0_0402_5%
RC16 1 2 100_0402_1%
VCC_SA_SENSE
VSS_SA_SENSE
VCC_SA_SENSE 67
VSS_SA_SENSE 67
VCCIO_SENSE H14
VSSIO_SENSE J14
12OF13
CFL-H_BGA1440
+VCCIO
RC271 1 2 100_0402_1%
RC272 1 2 0_0402_5%
RC273 1 2 0_0402_5%
RC274 1 2 100_0402_1%
VCCIO_SENSE
VSSIO_SENSE
VCCIO_SENSE 64
VSSIO_SENSE 64
+1.2V_DDR
CC17 10U_0402_6.3V6M
CC18 10U_0402_6.3V6M
CC19 10U_0402_6.3V6M
CC20 10U_0402_6.3V6M
CC21 10U_0402_6.3V6M
CC22 10U_0402_6.3V6M
CC23 10U_0402_6.3V6M
CC24 10U_0402_6.3V6M
CC25 10U_0402_6.3V6M
CC26 10U_0402_6.3V6M
CC27 10U_0402_6.3V6M
CC28 10U_0402_6.3V6M
CC29 22U_0603_6.3V6M
CC30 22U_0603_6.3V6M
CC31 22U_0603_6.3V6M
CC32 22U_0603_6.3V6M
571483_CFL_H_RVP_CRB_TDK_Rev0p5
+1.2V_VDDQ_CPU: 10uF * 12 22uF * 4
+VCCIO
CC33 10U_0402_6.3V6M
CC34 10U_0402_6.3V6M
CC35 10U_0402_6.3V6M
571483_CFL_H_RVP_CRB_TDK_Rev0p5
+0.95VS_VCCIO: 10uF * 12 22uF * 4
+1.2V_VCCPLL_OC
CC36 1U_0201_6.3V6M
CC37 1U_0201_6.3V6M
571483_CFL_H_RVP_CRB_TDK_Rev0p5
+1.2V_VCCPLL_OC: 1uF * 2
+VCCSTG
CC40 1U_0201_6.3V6M
571483_CFL_H_RVP_CRB_TDK_Rev0p5
+1.05VS_VCCSTG: 1uF * 1
+VCCSA
CC303 1U_0402_6.3V6K
+VCCST
CC38 1U_0201_6.3V6M
571483_CFL_H_RVP_CRB_TDK_Rev0p5
+1.05V_VCCST: 1uF * 1
+VCCST
CC39 1U_0201_6.3V6M
571483_CFL_H_RVP_CRB_TDK_Rev0p5
+1.05V_VCCSFR: 1uF * 1

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

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Compal Electronics, Inc.

Title
CFL-H(7/8)VCCSA/VCCIO/VDDQ

Size Document Number Rev
LA-F611P 0.3

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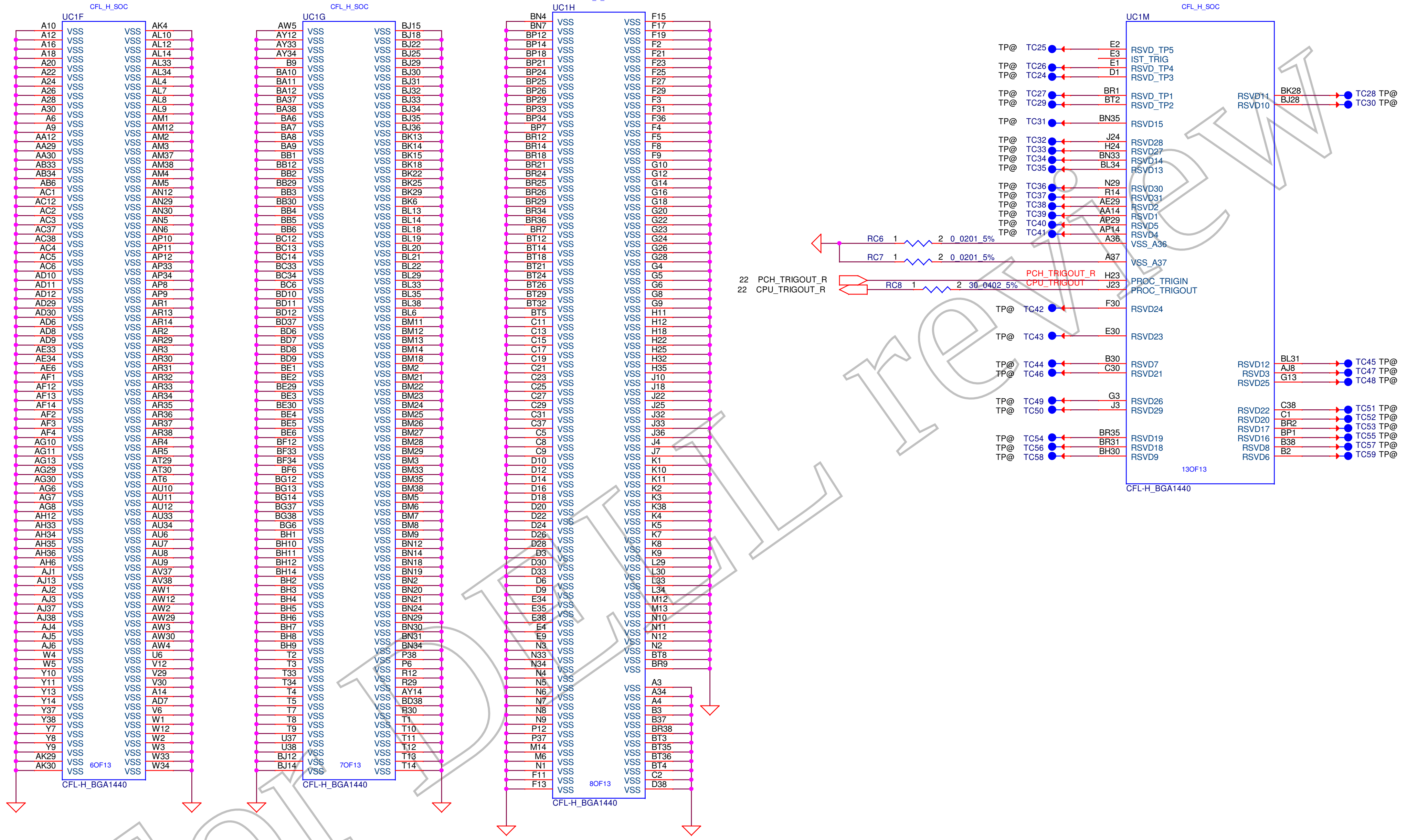
Main Func = CPU


CFL_H_SOC
UC1F
A10 A12 A16 A18 A20 A22 A24 A26 A28 A30 A6 A9 AA12 AA29 AA30 AB33 AB34 AB6 AC1 AC12 AC2 AC3 AC37 AC38 AC4 AC5 AC6 AD10 AD11 AD12 AD29 AD30 AD6 AD8 AD9 AE33 AE34 AE6 AF1 AF12 AF13 AF14 AF2 AF3 AF4 AG10 AG11 AG13 AG29 AG30 AG6 AG7 AG8 AH12 AH33 AH34 AH35 AH36 AH6 AJ1 AJ13 AJ2 AJ3 AJ37 AJ38 AJ4 AJ5 AJ6 W4 W5 Y10 Y11 Y13 Y14 Y37 Y38 Y7 Y8 Y9 AK29 AK30
AK4 AL10 AL12 AL14 AL33 AL34 AL4 AL7 AL8 AL9 AM1 AM12 AM2 AM3 AM37 AM38 AM4 AM5 AN12 AN29 AN30 AN5 AN6 AP10 AP11 AP12 AP33 AP34 AP8 AP9 AR1 AR13 AR14 AR2 AR29 AR3 AR30 AR31 AR33 AR34 AR35 AR36 AR37 AR38 AR4 AR5 AT29 AT30 AT6 AU10 AU11 AU12 AU33 AU6 AU7 AU8 AU9 AV37 AV38 AW1 AW12 AW2 AW29 AW3 AW30 AW4 U6 V12 V29 V30 A14 AD7 V6 W1 W12 W2 W3 W33 W34
VSS
6OF13
CFL-H_BGA1440
CFL_H_SOC
UC1G
AW5 AY12 AY33 AY34 B9 BA10 BA11 BA12 BA37 BA38 BA6 BA7 BA8 BA9 BB1 BB12 BB2 BB29 BB3 BB30 BB4 BB5 BB6 BC12 BC13 BC14 BC33 BC34 BC6 BD10 BD11 BD12 BD37 BD6 BD7 BD8 BD9 BE1 BE2 BE29 BE3 BE30 BE4 BE5 BE6 BF12 BF33 BF34 BF6 BG12 BG13 BG14 BG37 BG38 BG6 BH1 BH10 BH11 BH12 BH14 BH2 BH3 BH4 BH5 BH6 BH7 BH8 BH9 T2 T3 T33 T34 T4 T5 T7 T8 T9 U37 U38 BJ12 BJ14
BJ15 BJ18 BJ22 BJ25 BJ29 BJ30 BJ31 BJ32 BJ33 BJ34 BJ35 BJ36 BK13 BK14 BK15 BK18 BK22 BK25 BK29 BK6 BL13 BL14 BL18 BL19 BL20 BL21 BL29 BL33 BL35 BL38 BL6 BM11 BM12 BM13 BM14 BM18 BM2 BM21 BM22 BM23 BM24 BM25 BM26 BM27 BM28 BM29 BM3 BM33 BM35 BM38 BM5 BM6 BM7 BM8 BM9 BN12 BN14 BN18 BN19 BN2 BN20 BN21 BN24 BN29 BN30 BN31 BN34 P38 P6 R12 R29 AY14 BD38 R30 T1 T10 T11 T12 T13 T14
VSS
7OF13
CFL-H_BGA1440
CFL_H_SOC
UC1H
BN4 BN7 BP12 BP14 BP18 BP21 BP24 BP25 BP26 BP29 BP33 BP34 BP7 BR12 BR14 BR18 BR21 BR24 BR25 BR26 BR29 BR34 BR36 BR7 BT12 BT14 BT18 BT21 BT24 BT26 BT29 BT32 BT5 C11 C13 C15 C17 C19 C21 C23 C25 C27 C29 C31 C37 C5 C8 C9 D10 D12 D14 D16 D18 D20 D22 D24 D26 D28 D3 D30 D33 D6 D9 E34 E35 E38 E4 E9 N3 N33 N34 N4 N5 N6 N7 N8 N9 P12 P37 M14 M6 N1 F11 F13
F15 F17 F19 F2 F21 F23 F25 F27 F29 F3 F31 F36 F4 F5 F8 F9 G10 G12 G14 G16 G18 G20 G22 G23 G24 G26 G28 G4 G5 G6 G8 G9 H11 H12 H18 H22 H25 H32 H35 J10 J18 J22 J25 J32 J33 J36 J4 J7 K1 K10 K11 K2 K3 K38 K4 K5 K7 K8 K9 L29 L30 L33 L34 M12 M13 N10 N11 N12 N2 BT8 BR9
A3 A34 A4 B3 B37 BR38 BT3 BT35 BT36 BT4 C2 D38
VSS
8OF13
CFL-H_BGA1440
CFL_H_SOC
UC1M
TP@ TC25 E2 RSVD_TP5
E3 IST_TRIG
TP@ TC26 E1 RSVD_TP4
TP@ TC24 D1 RSVD_TP3
TP@ TC27 BR1 RSVD_TP1
TP@ TC29 BT2 RSVD_TP2
TP@ TC31 BN35 RSVD15
TP@ TC32 J24 RSVD28
TP@ TC33 H24 RSVD27
TP@ TC34 BN33 RSVD14
TP@ TC35 BL34 RSVD13
TP@ TC36 N29 RSVD30
TP@ TC37 R14 RSVD31
TP@ TC38 AE29 RSVD2
TP@ TC39 AA14 RSVD1
TP@ TC40 AP29 RSVD5
TP@ TC41 AP14 RSVD4
RC6 1 2 0_0201_5% A36 VSS_A36
RC7 1 2 0_0201_5% A37 VSS_A37
22 PCH_TRIGOUT_R
22 CPU_TRIGOUT_R
PCH_TRIGOUT_R H23 PROC_TRIGIN
RC8 1 2 30_0402_5% CPU_TRIGOUT J23 PROC_TRIGOUT
TP@ TC42 F30 RSVD24
TP@ TC43 E30 RSVD23
TP@ TC44 B30 RSVD7
TP@ TC46 C30 RSVD21
TP@ TC49 G3 RSVD26
TP@ TC50 J3 RSVD29
TP@ TC54 BR35 RSVD19
TP@ TC56 BR31 RSVD18
TP@ TC58 BH30 RSVD9
RSVD11 BK28 TC28 TP@
RSVD10 BJ28 TC30 TP@
RSVD12 BL31 TC45 TP@
RSVD3 AJ8 TC47 TP@
RSVD25 G13 TC48 TP@
RSVD22 C38 TC51 TP@
RSVD20 C1 TC52 TP@
RSVD17 BR2 TC53 TP@
RSVD16 BP1 TC55 TP@
RSVD8 B38 TC57 TP@
RSVD6 B2 TC59 TP@
13OF13
CFL-H_BGA1440

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Compal Electronics, Inc.

Title
CFL-H(8/8)GND/RSVD

Size Document Number **LA-F611P** Rev 0.3

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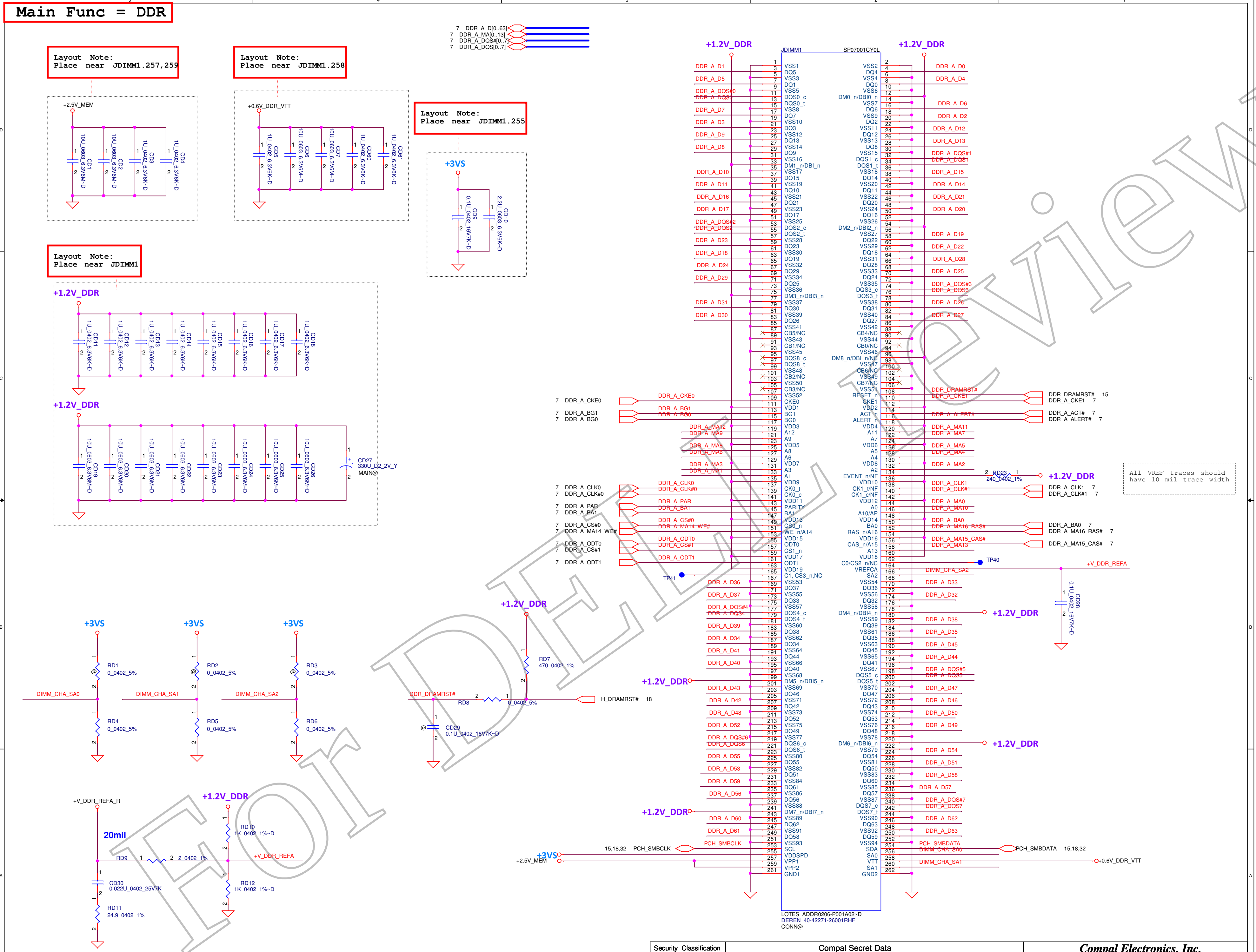
Main Func = DDR
Layout Note: Place near JDIMM1.257,259
Layout Note: Place near JDIMM1.258
Layout Note: Place near JDIMM1.255
Layout Note: Place near JDIMM1
+2.5V_MEM
CD1 10U_0603_6.3V6M-D
CD2 10U_0603_6.3V6M-D
CD3 1U_0402_6.3V6K-D
CD4 1U_0402_6.3V6K-D
+0.6V_DDR_VTT
CD5 1U_0402_6.3V6K-D
CD6 10U_0603_6.3V6M-D
CD7 10U_0603_6.3V6M-D
CD60 1U_0402_6.3V6K-D
CD61 1U_0402_6.3V6K-D
+3VS
CD9 0.1U_0402_16V7K-D
CD10 2.2U_0603_6.3V6K-D
+1.2V_DDR
CD11 CD12 CD13 CD14 CD15 CD16 CD17 CD18 1U_0402_6.3V6K-D
CD19 CD20 CD21 CD22 CD23 CD24 CD25 CD26 10U_0603_6.3V6M-D
CD27 330U_D2_2V_Y MAIN@
7 DDR_A_D[0..63]
7 DDR_A_MA[0..13]
7 DDR_A_DQS#[0..7]
7 DDR_A_DQS[0..7]
JDIMM1
SP07001CY0L
7 DDR_A_CKE0
7 DDR_A_BG1
7 DDR_A_BG0
7 DDR_A_CLK0
7 DDR_A_CLK#0
7 DDR_A_PAR
7 DDR_A_BA1
7 DDR_A_CS#0
7 DDR_A_MA14_WE#
7 DDR_A_ODT0
7 DDR_A_CS#1
7 DDR_A_ODT1
DDR_DRAMRST# 15
DDR_A_CKE1 7
DDR_A_ACT# 7
DDR_A_ALERT# 7
DDR_A_CLK1 7
DDR_A_CLK#1 7
DDR_A_BA0 7
DDR_A_MA16_RAS# 7
DDR_A_MA15_CAS# 7
RD23 240_0402_1%
All VREF traces should have 10 mil trace width
TP40
TP41
+V_DDR_REFA
CD28 0.1U_0402_16V7K-D
DIMM_CHA_SA2
RD1 0_0402_5%
RD2 0_0402_5%
RD3 0_0402_5%
RD4 0_0402_5%
RD5 0_0402_5%
RD6 0_0402_5%
DIMM_CHA_SA0
DIMM_CHA_SA1
RD7 470_0402_1%
RD8 0_0402_5%
DDR_DRAMRST#
H_DRAMRST# 18
CD29 0.1U_0402_16V7K-D
+V_DDR_REFA_R
20mil
RD9 2_0402_1%
RD10 1K_0402_1%~D
RD12 1K_0402_1%~D
CD30 0.022U_0402_25V7K
RD11 24.9_0402_1%
15,18,32 PCH_SMBCLK
PCH_SMBDATA 15,18,32
+0.6V_DDR_VTT
LOTES_ADDR0206-P001A02~D
DEREN_40-42271-26001RHF
CONN@

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

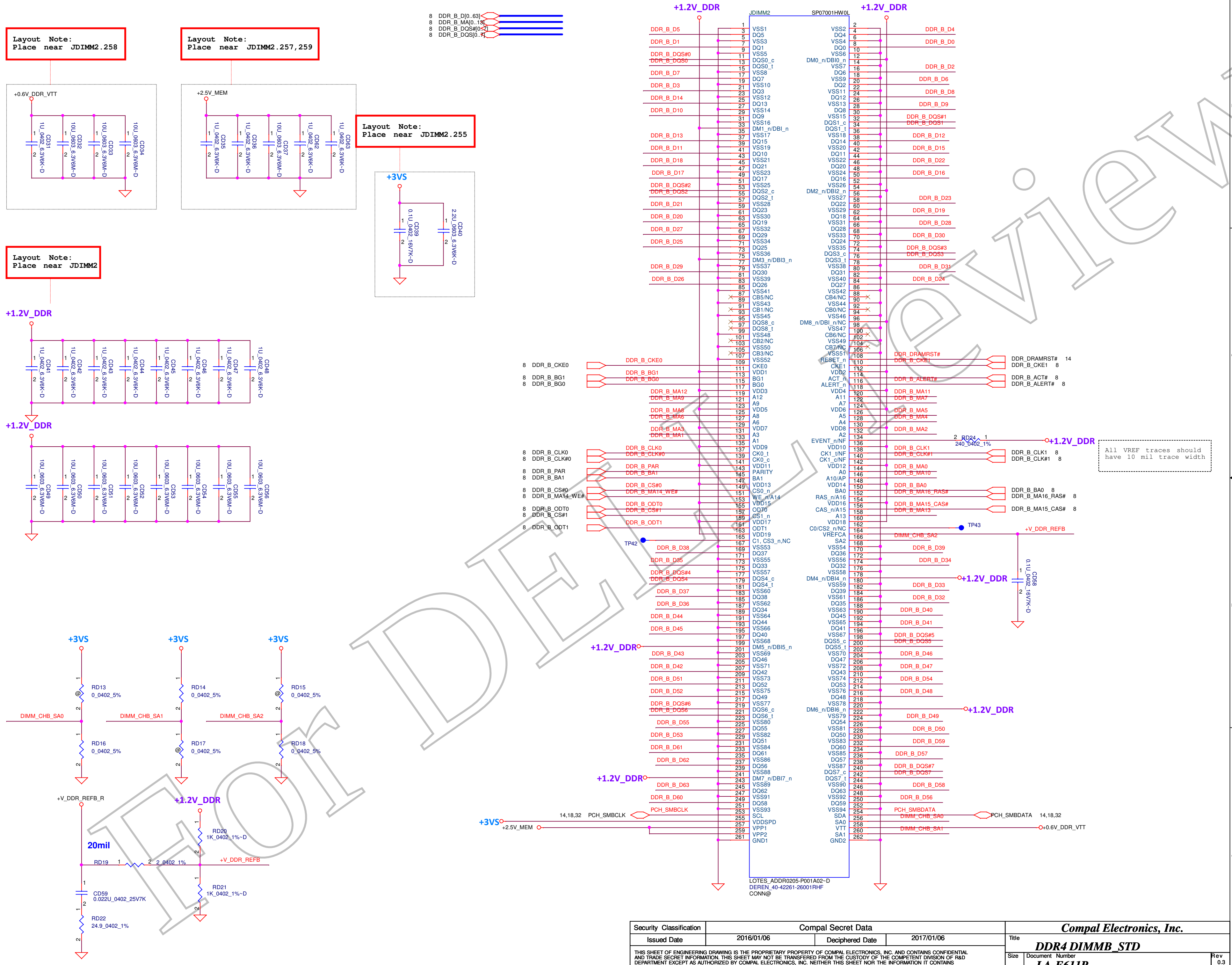
Title

DDR4 DIMMA_RVS

Size Document Number **LA-F611P** Rev 0.3

Date: Thursday, March 22, 2018 Sheet 14 of 78

Main Func = DDR


Layout Note:
Place near JDIMM2.258
Layout Note:
Place near JDIMM2.257,259
Layout Note:
Place near JDIMM2.255
Layout Note:
Place near JDIMM2
+0.6V_DDR_VTT
CD31 1U_0402_6.3V6K~D
CD32 10U_0603_6.3V6M~D
CD33 10U_0603_6.3V6M~D
CD34 10U_0603_6.3V6M~D
+2.5V_MEM
CD35 1U_0402_6.3V6K~D
CD36 1U_0402_6.3V6K~D
CD37 10U_0603_6.3V6M~D
CD62 1U_0402_6.3V6K~D
CD63 1U_0402_6.3V6K~D
+3VS
CD39 0.1U_0402_16V7K~D
CD40 2.2U_0603_6.3V6K~D
+1.2V_DDR
CD41 1U_0402_6.3V6K~D
CD42 1U_0402_6.3V6K~D
CD43 1U_0402_6.3V6K~D
CD44 1U_0402_6.3V6K~D
CD45 1U_0402_6.3V6K~D
CD46 1U_0402_6.3V6K~D
CD47 1U_0402_6.3V6K~D
CD48 1U_0402_6.3V6K~D
CD49 10U_0603_6.3V6M~D
CD50 10U_0603_6.3V6M~D
CD51 10U_0603_6.3V6M~D
CD52 10U_0603_6.3V6M~D
CD53 10U_0603_6.3V6M~D
CD54 10U_0603_6.3V6M~D
CD55 10U_0603_6.3V6M~D
CD56 10U_0603_6.3V6M~D
8 DDR_B_D[0..63]
8 DDR_B_MA[0..13]
8 DDR_B_DQS#[0..7]
8 DDR_B_DQS[0..7]
JDIMM2
SP07001HW0L
8 DDR_B_CKE0
8 DDR_B_BG1
8 DDR_B_BG0
8 DDR_B_CLK0
8 DDR_B_CLK#0
8 DDR_B_PAR
8 DDR_B_BA1
8 DDR_B_CS#0
8 DDR_B_MA14_WE#
8 DDR_B_ODT0
8 DDR_B_CS#1
8 DDR_B_ODT1
TP42
TP43
DDR_DRAMRST# 14
DDR_B_CKE1 8
DDR_B_ACT# 8
DDR_B_ALERT# 8
RD24 240_0402_1%
All VREF traces should have 10 mil trace width
DDR_B_CLK1 8
DDR_B_CLK#1 8
DDR_B_BA0 8
DDR_B_MA16_RAS# 8
DDR_B_MA15_CAS# 8
+V_DDR_REFB
DIMM_CHB_SA2
CD58 0.1U_0402_16V7K~D
14,18,32 PCH_SMBCLK
PCH_SMBDATA 14,18,32
DIMM_CHB_SA0
DIMM_CHB_SA1
+0.6V_DDR_VTT
+2.5V_MEM
LOTES_ADDR0205-P001A02~D
DEREN_40-42261-26001RHF
CONN@
RD13 0_0402_5%
RD14 0_0402_5%
RD15 0_0402_5%
RD16 0_0402_5%
RD17 0_0402_5%
RD18 0_0402_5%
DIMM_CHB_SA0
DIMM_CHB_SA1
DIMM_CHB_SA2
+V_DDR_REFB_R
20mil
RD19 2_0402_1%
+V_DDR_REFB
RD20 1K_0402_1%~D
RD21 1K_0402_1%~D
CD59 0.022U_0402_25V7K
RD22 24.9_0402_1%

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title **DDR4 DIMMB_STD**

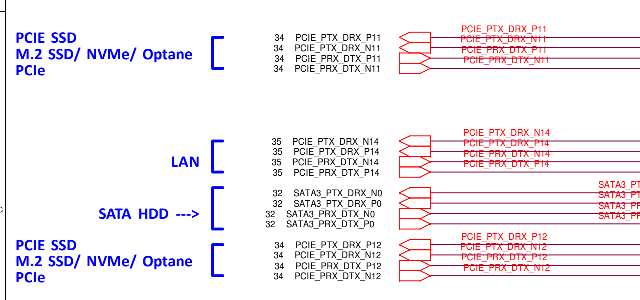
Size Document Number **LA-F611P** Rev 0.3

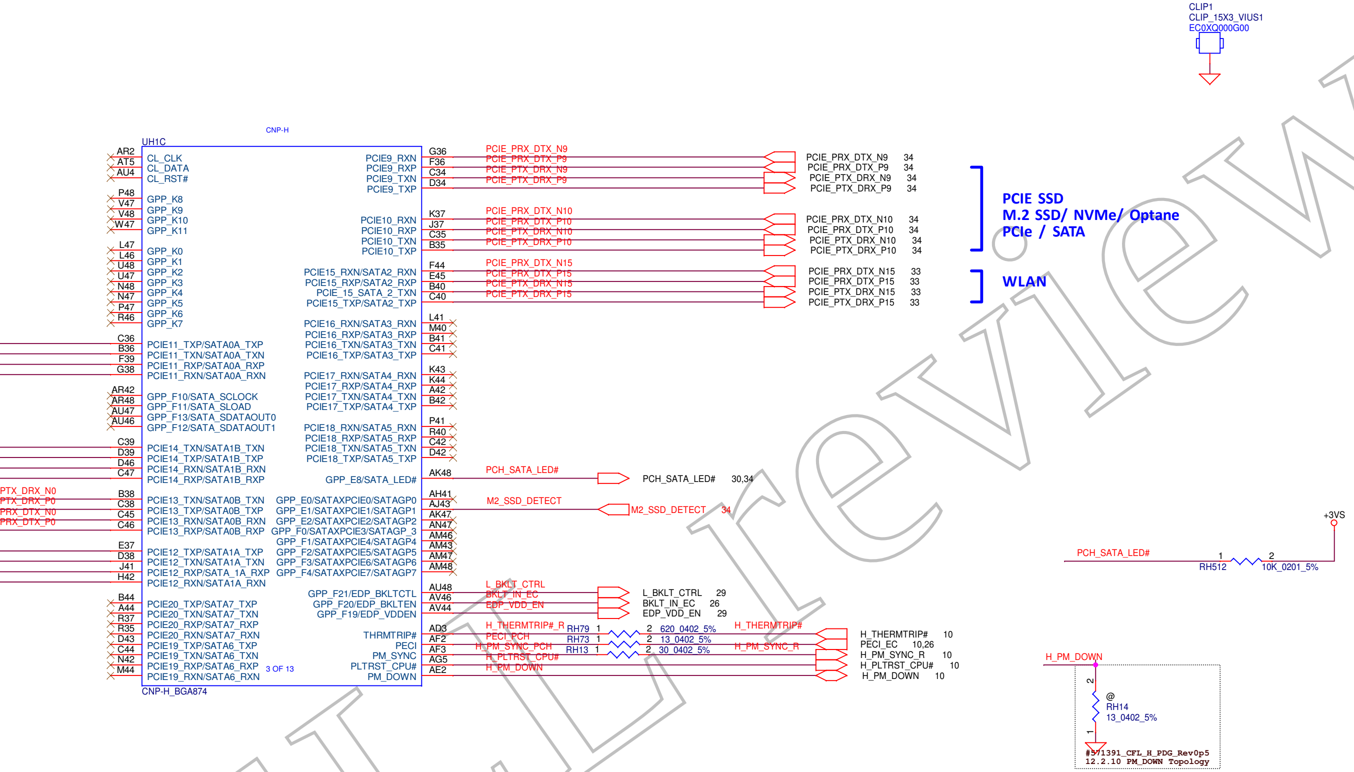
Date: Thursday, March 22, 2018 Sheet 15 of 78

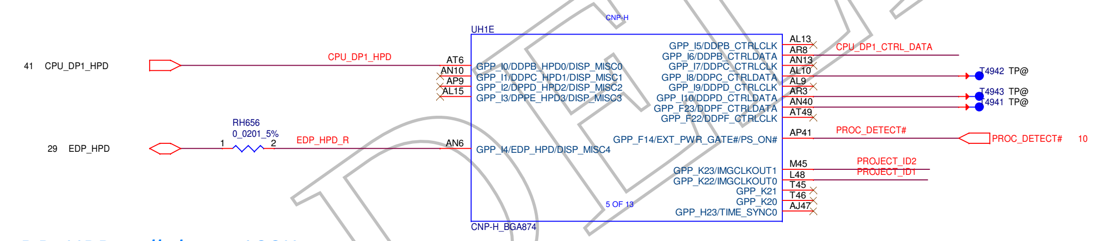
Main Func = PCH

SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

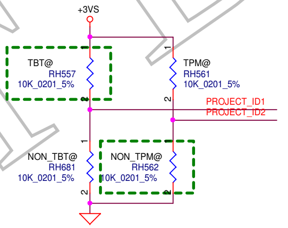
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[1]	None[2]	None[3]


PCIE SSD
M.2 SSD/ NVMe/ Optane
PCIe
34 PCIE_PTX_DRX_P11
34 PCIE_PTX_DRX_N11
34 PCIE_PRX_DTX_P11
34 PCIE_PRX_DTX_N11
LAN
35 PCIE_PTX_DRX_N14
35 PCIE_PTX_DRX_P14
35 PCIE_PRX_DTX_N14
35 PCIE_PRX_DTX_P14
SATA HDD --->
32 SATA3_PTX_DRX_N0
32 SATA3_PTX_DRX_P0
32 SATA3_PRX_DTX_N0
32 SATA3_PRX_DTX_P0
PCIE SSD
M.2 SSD/ NVMe/ Optane
PCIe
34 PCIE_PTX_DRX_P12
34 PCIE_PTX_DRX_N12
34 PCIE_PRX_DTX_P12
34 PCIE_PRX_DTX_N12


CLIP1
CLIP_15X3_VIUS1
EC0XQ000G00
CNP-H
UH1C
CL_CLK
CL_DATA
CL_RST#
GPP_K8
GPP_K9
GPP_K10
GPP_K11
GPP_K0
GPP_K1
GPP_K2
GPP_K3
GPP_K4
GPP_K5
GPP_K6
GPP_K7
PCIE11_TXP/SATA0A_TXP
PCIE11_TXN/SATA0A_TXN
PCIE11_RXP/SATA0A_RXP
PCIE11_RXN/SATA0A_RXN
GPP_F10/SATA_SCLOCK
GPP_F11/SATA_SLOAD
GPP_F13/SATA_SDATAOUT0
GPP_F12/SATA_SDATAOUT1
PCIE14_TXN/SATA1B_TXN
PCIE14_TXP/SATA1B_TXP
PCIE14_RXN/SATA1B_RXN
PCIE14_RXP/SATA1B_RXP
PCIE13_TXN/SATA0B_TXN
PCIE13_TXP/SATA0B_TXP
PCIE13_RXN/SATA0B_RXN
PCIE13_RXP/SATA0B_RXP
PCIE12_TXP/SATA1A_TXP
PCIE12_TXN/SATA1A_TXN
PCIE12_RXP/SATA1A_RXP
PCIE12_RXN/SATA1A_RXN
PCIE20_TXP/SATA7_TXP
PCIE20_TXN/SATA7_TXN
PCIE20_RXP/SATA7_RXP
PCIE20_RXN/SATA7_RXN
PCIE19_TXP/SATA6_TXP
PCIE19_TXN/SATA6_TXN
PCIE19_RXP/SATA6_RXP
PCIE19_RXN/SATA6_RXN
3 OF 13
CNP-H_BGA874
PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP
PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP
PCIE15_RXN/SATA2_RXN
PCIE15_RXP/SATA2_RXP
PCIE_15_SATA_2_TXN
PCIE15_TXP/SATA2_TXP
PCIE16_RXN/SATA3_RXN
PCIE16_RXP/SATA3_RXP
PCIE16_TXN/SATA3_TXN
PCIE16_TXP/SATA3_TXP
PCIE17_RXN/SATA4_RXN
PCIE17_RXP/SATA4_RXP
PCIE17_TXN/SATA4_TXN
PCIE17_TXP/SATA4_TXP
PCIE18_RXN/SATA5_RXN
PCIE18_RXP/SATA5_RXP
PCIE18_TXN/SATA5_TXN
PCIE18_TXP/SATA5_TXP
GPP_E8/SATA_LED#
GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
GPP_F0/SATAXPCIE3/SATAGP_3
GPP_F1/SATAXPCIE4/SATAGP4
GPP_F2/SATAXPCIE5/SATAGP5
GPP_F3/SATAXPCIE6/SATAGP6
GPP_F4/SATAXPCIE7/SATAGP7
GPP_F21/EDP_BKLTCTL
GPP_F20/EDP_BKLTEN
GPP_F19/EDP_VDDEN
THRMTRIP#
PECI
PM_SYNC
PLTRST_CPU#
PM_DOWN
PCIE_PRX_DTX_N9 34
PCIE_PRX_DTX_P9 34
PCIE_PTX_DRX_N9 34
PCIE_PTX_DRX_P9 34
PCIE_PRX_DTX_N10 34
PCIE_PRX_DTX_P10 34
PCIE_PTX_DRX_N10 34
PCIE_PTX_DRX_P10 34
PCIE SSD
M.2 SSD/ NVMe/ Optane
PCIe / SATA
PCIE_PRX_DTX_N15 33
PCIE_PRX_DTX_P15 33
PCIE_PTX_DRX_N15 33
PCIE_PTX_DRX_P15 33
WLAN
PCH_SATA_LED# 30,34
M2_SSD_DETECT 34
+3VS
PCH_SATA_LED#
RH512
10K_0201_5%
L_BKLT_CTRL 29
BKLT_IN_EC 26
EDP_VDD_EN 29
H_THERMTRIP#_R
RH79 2 620_0402_5%
RH73 2 13_0402_5%
RH13 2 30_0402_5%
PECI_PCH
H_PM_SYNC_PCH
H_PLTRST_CPU#
H_PM_DOWN
H_THERMTRIP# 10
PECI_EC 10,26
H_PM_SYNC_R 10
H_PLTRST_CPU# 10
H_PM_DOWN 10
H_PM_DOWN
@
RH14
13_0402_5%
#571391_CFL_H_PDG_Rev0p5
12.2.10 PM_DOWN Topology

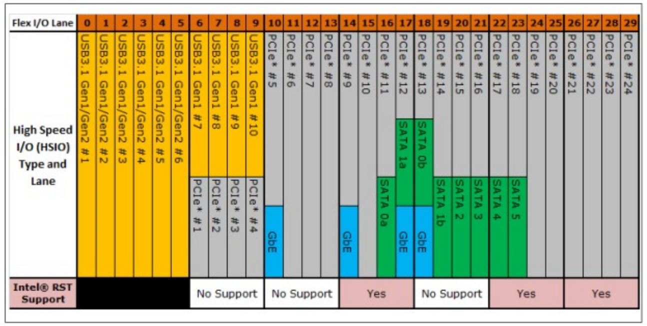

CNP-H
UH1E
41 CPU_DP1_HPD
CPU_DP1_HPD
GPP_I0/DDPB_HPD0/DISP_MISC0
GPP_I1/DDPC_HPD1/DISP_MISC1
GPP_I2/DDPD_HPD2/DISP_MISC2
GPP_I3/DPPE_HPD3/DISP_MISC3
RH656
0_0201_5%
29 EDP_HPD
EDP_HPD_R
GPP_I4/EDP_HPD/DISP_MISC4
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_F23/DDPF_CTRLDATA
GPP_F22/DDPF_CTRLCLK
CPU_DP1_CTRL_DATA
T4942 TP@
T4943 TP@
T4941 TP@
GPP_F14/EXT_PWR_GATE#/PS_ON#
PROC_DETECT#
PROC_DETECT# 10
GPP_K23/IMGCLKOUT1
GPP_K22/IMGCLKOUT0
GPP_K21
GPP_K20
GPP_H23/TIME_SYNC0
PROJECT_ID2
PROJECT_ID1
5 OF 13
CNP-H_BGA874

eDP_HPD pull down 100K


+3VS
TBT@
RH557
10K_0201_5%
TPM@
RH561
10K_0201_5%
PROJECT_ID1
PROJECT_ID2
NON_TBT@
RH681
10K_0201_5%
NON_TPM@
RH562
10K_0201_5%

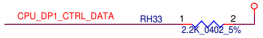
PROJECT ID	PROJECT ID1 (GPP_K22)
Non-TBT	0
TBT	1

TPM ID	PROJECT ID2 (GPP_K23)
SW TPM	0
HW TPM	1



Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7 PCIe* #1	USB3.1 Gen1 #8 PCIe* #2	USB3.1 Gen1 #9 PCIe* #3	USB3.1 Gen1 #10 PCIe* #4	PCIe* #5 GbE	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9 GbE	PCIe* #10	PCIe* #11 SATA 0a	PCIe* #12 SATA 1a GbE	PCIe* #13 SATA 0b GbE	PCIe* #14 SATA 1b	PCIe* #15 SATA 2	PCIe* #16 SATA 3	PCIe* #17 SATA 4	PCIe* #18 SATA 5	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

PCH Strap PIN


+3VS
CPU_DP1_CTRL_DATA
RH33
2.2K_0402_5%

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

```
DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.
Notes:
1. The internal Pull-down is disabled after
PCH_PWROK de-asserts.
2. This signal is in the primary well.
```

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

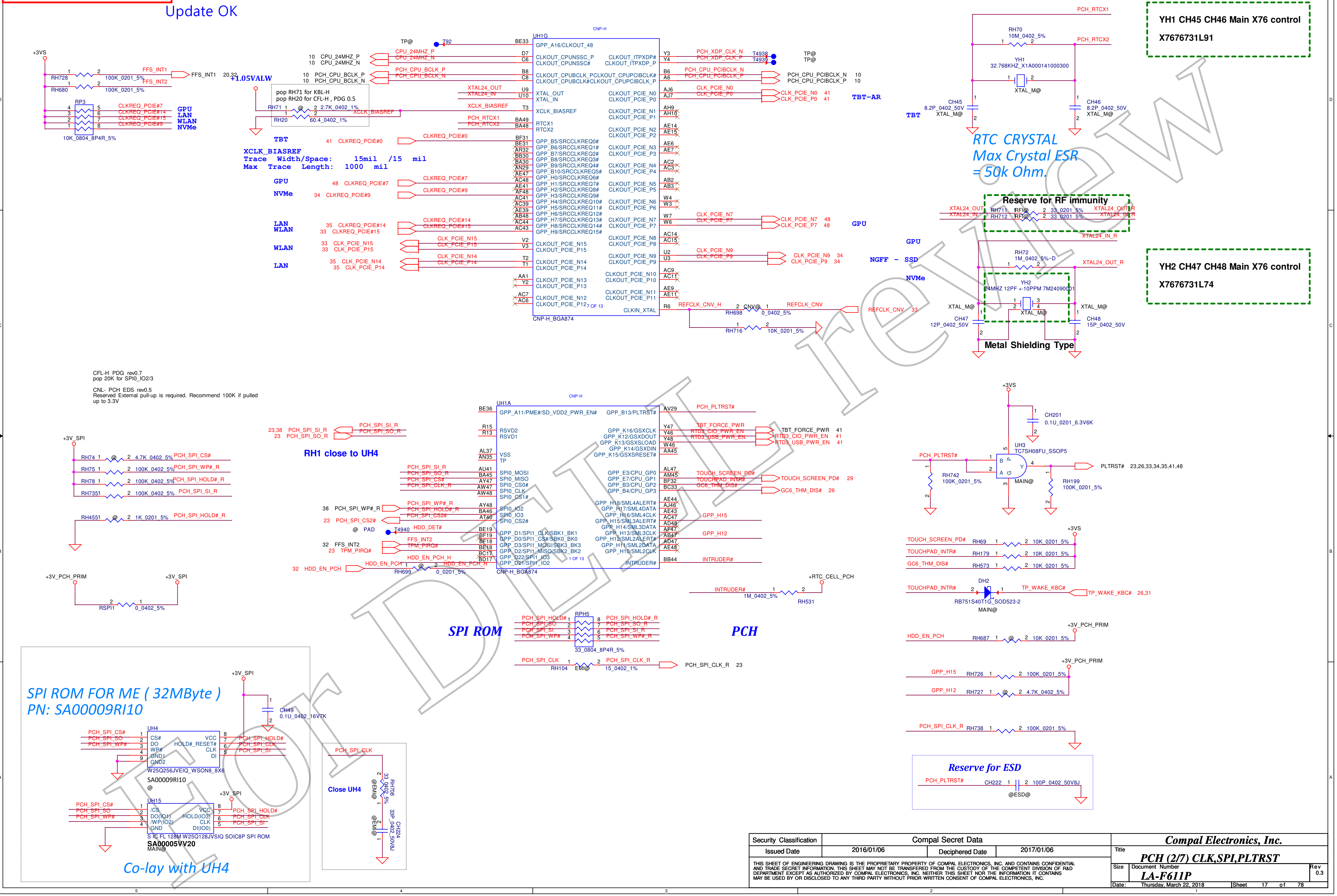
Title
PCH (1/7) SATA,DDC,PCIE

Size
Document Number
LA-F611P
Rev
0.3

Date: Thursday, March 22, 2018

Main Func = PCH

Update OK



UH1G
CNP-H
GPP_A16/CLKOUT_48
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC#
CLKOUT_ITPXDP#
CLKOUT_ITPXDP_P
CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK#
CLKOUT_CPUPCIBCLK#
CLKOUT_CPUPCIBCLK_P
XTAL_OUT
XTAL_IN
XCLK_BIASREF
RTCX1
RTCX2
CLKOUT_PCIE_N0 ... CLKOUT_PCIE_P15
GPP_B5/SRCCLKREQ0# ... GPP_H9/SRCCLKREQ15#
CLKIN_XTAL
CNP-H_BGA874
7 OF 13
TP@
T92
CPU_24MHZ_P
CPU_24MHZ_N
PCH_CPU_BCLK_P
PCH_CPU_BCLK_N
PCH_XDP_CLK_N
PCH_XDP_CLK_P
T4938
T4939
PCH_CPU_PCIBCLK_N
PCH_CPU_PCIBCLK_P
XTAL24_OUT
XTAL24_IN
XCLK_BIASREF
PCH_RTCX1
PCH_RTCX2
CLK_PCIE_N0
CLK_PCIE_P0
TBT-AR
pop RH71 for KBL-H
pop RH20 for CFL-H , PDG 0.5
RH71 2.7K_0402_1%
RH20 60.4_0402_1%
+1.05VALW
TBT
XCLK_BIASREF
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil
CLKREQ_PCIE#0
CLKREQ_PCIE#7
CLKREQ_PCIE#9
CLKREQ_PCIE#14
CLKREQ_PCIE#15
CLK_PCIE_N15
CLK_PCIE_P15
CLK_PCIE_N14
CLK_PCIE_P14
CLK_PCIE_N7
CLK_PCIE_P7
CLK_PCIE_N9
CLK_PCIE_P9
GPU
NVMe
LAN
WLAN
NGFF - SSD
REFCLK_CNV_H
RH698 0_0402_5%
CNV@
REFCLK_CNV
RH716 10K_0201_5%
+3VS
RH728 100K_0201_5%
RH680 100K_0201_5%
FFS_INT1
FFS_INT2
RP3 10K_0804_8P4R_5%
CLKREQ_PCIE#7
CLKREQ_PCIE#14
CLKREQ_PCIE#15
CLKREQ_PCIE#9
GPU
LAN
WLAN
NVMe
PCH_RTCX1
PCH_RTCX2
RH70 10M_0402_5%
YH1 32.768KHZ_X1A000141000300
XTAL_M@
CH45 8.2P_0402_50V
CH46 8.2P_0402_50V
RTC CRYSTAL
Max Crystal ESR
= 50k Ohm.
Reserve for RF immunity
RH711 RF@ 33_0201_5%
RH712 RF@ 33_0201_5%
XTAL24_OUT_R
XTAL24_IN_R
RH72 1M_0402_5%~D
YH2 24MHZ 12PF +-10PPM 7M24090001
CH47 12P_0402_50V
CH48 15P_0402_50V
Metal Shielding Type
YH1 CH45 CH46 Main X76 control
X7676731L91
YH2 CH47 CH48 Main X76 control
X7676731L74
CFL-H PDG rev0.7
pop 20K for SPI0_IO2/3
CNL- PCH EDS rev0.5
Reserved External pull-up is required. Recommend 100K if pulled up to 3.3V
+3V_SPI
RH74 4.7K_0402_5% PCH_SPI_CS#
RH75 100K_0402_5% PCH_SPI_WP#_R
RH78 100K_0402_5% PCH_SPI_HOLD#_R
RH7351 100K_0402_5% PCH_SPI_SI_R
RH4551 1K_0201_5% PCH_SPI_HOLD#_R
+3V_PCH_PRIM
RSPI1 0_0402_5%
UH1A
GPP_A11/PME#/SD_VDD2_PWR_EN#
GPP_B13/PLTRST#
RSVD2
RSVD1
VSS
TP
GPP_K16/GSXCLK
GPP_K12/GSXDOUT
GPP_K13/GSXSLOAD
GPP_K14/GSXDIN
GPP_K15/GSXSRESET#
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
SPI0_IO2
SPI0_IO3
SPI0_CS2#
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
GPP_D1/SPI1_CLK/SBK1_BK1
GPP_D0/SPI1_CS#/SBK0_BK0
GPP_D3/SPI1_MOSI/SBK3_BK3
GPP_D2/SPI1_MISO/SBK2_BK2
GPP_D22/SPI1_IO3
GPP_D21/SPI1_IO2
INTRUDER#
1 OF 13
PCH_PLTRST#
TBT_FORCE_PWR
RTD3_CIO_PWR_EN
RTD3_USB_PWR_EN
TOUCH_SCREEN_PD#
TOUCHPAD_INTR#
GC6_THM_DIS#
GPP_H15
GPP_H12
PCH_SPI_SI_R
PCH_SPI_SO_R
RH1 close to UH4
PCH_SPI_CS#
PCH_SPI_CLK_R
PCH_SPI_WP#_R
PCH_SPI_HOLD#_R
PCH_SPI_CS2#
PAD
T4940
HDD_DET#
FFS_INT2
TPM_PIRQ#
HDD_EN_PCH_H
HDD_EN_PCH
RH699 0_0201_5%
SPI ROM
PCH
RPH5 33_0804_8P4R_5%
RH104 EMI@ 15_0402_1%
PCH_SPI_CLK_R
+3VS
CH201 0.1U_0201_6.3V6K
UH3 TC7SH08FU_SSOP5
RH742 100K_0201_5%
RH199 100K_0201_5%
PLTRST#
MAIN@
RH69 10K_0201_5%
RH179 10K_0201_5%
RH573 10K_0201_5%
+RTC_CELL_PCH
RH531 1M_0402_5%
DH2 RB751S40T1G_SOD523-2
TP_WAKE_KBC#
RH687 10K_0201_5%
+3V_PCH_PRIM
RH726 100K_0201_5%
RH727 4.7K_0402_5%
RH738 100K_0201_5%
Reserve for ESD
CH222 100P_0402_50V8J
@ESD@
SPI ROM FOR ME (32MByte)
PN: SA00009RI10
CH49 0.1U_0402_16V7K
UH4
W25Q256JVEIQ_WSON8_8X6
SA00009RI10
UH15
S IC FL 128M W25Q128JVSIQ SOIC8P SPI ROM
SA00005VV20
Co-lay with UH4
Close UH4
RH708 33_0402_5% @EMI@
CH224 33P_0402_50V8J @EMI@

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: PCH (2/7) CLK,SPI,PLTRST
				Size / Document Number: LA-F611P / Rev 0.3
				Date: Thursday, March 22, 2018 / Sheet 17 of 78

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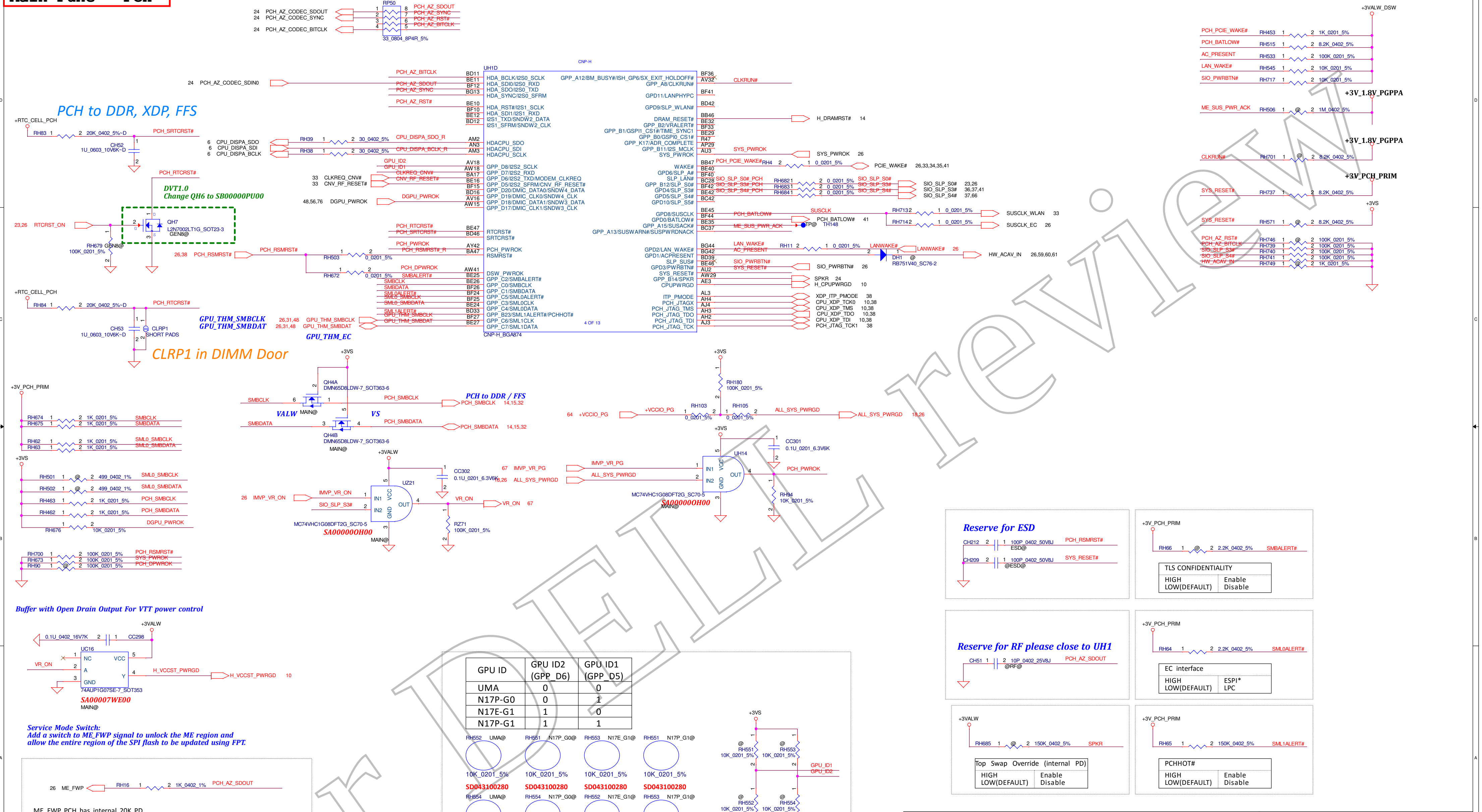
Main Func = PCH


UH1D
CNP-H
CNP-H_BGA874
4 OF 13
HDA_BCLK/I2S0_SCLK
HDA_SDI0/I2S0_RXD
HDA_SDO/I2S0_TXD
HDA_SYNC/I2S0_SFRM
HDA_RST#/I2S1_SCLK
HDA_SDI1/I2S1_RXD
I2S1_TXD/SNDW2_DATA
I2S1_SFRM/SNDW2_CLK
HDACPU_SDO
HDACPU_SDI
HDACPU_SCLK
GPP_D8/I2S2_SCLK
GPP_D7/I2S2_RXD
GPP_D6/I2S2_TXD/MODEM_CLKREQ
GPP_D5/I2S2_SFRM/CNV_RF_RESET#
GPP_D20/DMIC_DATA0/SNDW4_DATA
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_D17/DMIC_CLK1/SNDW3_CLK
RTCRST#
SRTCRST#
PCH_PWROK
RSMRST#
DSW_PWROK
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1/GSPI1_CS1#/TIME_SYNC1
GPP_B0/GSPI0_CS1#
GPP_K17/ADR_COMPLETE
GPP_B11/I2S_MCLK
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
CPUPWRGD
ITP_PMODE
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TCK
RP50
33_0804_8P4R_5%
PCH_AZ_CODEC_SDOUT
PCH_AZ_CODEC_SYNC
PCH_AZ_CODEC_BITCLK
PCH_AZ_CODEC_SDIN0
PCH_AZ_SDOUT
PCH_AZ_SYNC
PCH_AZ_RST#
PCH_AZ_BITCLK
PCH to DDR, XDP, FFS
+RTC_CELL_PCH
RH83
20K_0402_5%~D
PCH_SRTCRST#
CH52
1U_0603_10V6K~D
CPU_DISPA_SDO
CPU_DISPA_SDI
CPU_DISPA_BCLK
RH39
RH38
30_0402_5%
CPU_DISPA_SDO_R
CPU_DISPA_BCLK_R
GPU_ID2
GPU_ID1
CLKREQ_CNV#
CNV_RF_RESET#
DGPU_PWROK
PCH_RTCRST#
DVT1.0
Change QH6 to SB00000PU00
QH7
L2N7002LT1G_SOT23-3
GEN8@
RTCST_ON
RH679 GEN8@
100K_0201_5%
PCH_RSMRST#
RH503
0_0201_5%
RH672
PCH_DPWROK
SMBALERT#
SMBCLK
SMBDATA
SML0ALERT#
SML0_SMBCLK
SML0_SMBDATA
SML1ALERT#
GPU_THM_SMBCLK
GPU_THM_SMBDAT
GPU_THM_EC
RH84
CH53
CLRP1
SHORT PADS
CLRP1 in DIMM Door
CLKRUN#
H_DRAMRST#
SYS_PWROK
PCH_PCIE_WAKE#
RH4
0_0201_5%
PCIE_WAKE#
SIO_SLP_S0#_PCH
SIO_SLP_S3#_PCH
SIO_SLP_S4#_PCH
RH6821
RH6831
RH6841
SIO_SLP_S0#
SIO_SLP_S3#
SIO_SLP_S4#
SUSCLK
PCH_BATLOW#
ME_SUS_PWR_ACK
TP@ TH148
RH7132
RH7142
SUSCLK_WLAN
SUSCLK_EC
LAN_WAKE#
AC_PRESENT
RH11
LANWAKE#
DH1 @
RB751V40_SC76-2
HW_ACAV_IN
SIO_PWRBTN#
SYS_RESET#
SPKR
H_CPUPWRGD
XDP_ITP_PMODE
CPU_XDP_TCK0
CPU_XDP_TMS
CPU_XDP_TDO
CPU_XDP_TDI
PCH_JTAG_TCK1
+3VALW_DSW
RH453 1K_0201_5%
RH515 8.2K_0402_5%
RH533 100K_0201_5%
RH545 10K_0201_5%
RH717 10K_0201_5%
+3V_1.8V_PGPPA
RH506 1M_0402_5%
RH701 8.2K_0402_5%
+3V_PCH_PRIM
RH737 8.2K_0402_5%
+3VS
RH571 8.2K_0402_5%
RH746 100K_0201_5%
RH739 100K_0201_5%
RH740 100K_0201_5%
RH741 100K_0201_5%
RH749 1K_0201_5%
QH4A
DMN65D8LDW-7_SOT363-6
QH4B
MAIN@
PCH_SMBCLK
PCH_SMBDATA
PCH to DDR / FFS
VALW
VS
+3V_PCH_PRIM
RH674 1K_0201_5%
RH675 1K_0201_5%
RH62 1K_0201_5%
RH63 1K_0201_5%
SML0_SMBCLK
SML0_SMBDATA
RH501 499_0402_1%
RH502 499_0402_1%
RH463 1K_0201_5%
RH462 1K_0201_5%
RH676 10K_0201_5%
RH700 100K_0201_5%
RH673 100K_0201_5%
RH90 100K_0201_5%
PCH_RSMRST#
SYS_PWROK
PCH_DPWROK
+3VALW
CC302
0.1U_0201_6.3V6K
UZ21
IMVP_VR_ON
SIO_SLP_S3#
VR_ON
RZ71
100K_0201_5%
MC74VHC1G08DFT2G_SC70-5
SA00000OH00
+VCCIO_PG
RH103
RH105
0_0201_5%
ALL_SYS_PWRGD
RH180
100K_0201_5%
CC301
0.1U_0201_6.3V6K
UH14
IMVP_VR_PG
PCH_PWROK
RH94
10K_0201_5%
CC298
0.1U_0402_16V7K
UC16
74AUP1G07SE-7_SOT353
SA00007WE00
H_VCCST_PWRGD
RH16
1K_0402_1%
ME_FWP
PCH_AZ_SDOUT
RH552 UMA@
RH551 N17P_G0@
RH553 N17E_G1@
RH551 N17P_G1@
RH554 UMA@
RH554 N17P_G0@
RH552 N17E_G1@
RH553 N17P_G1@
10K_0201_5%
SD043100280
GPU_ID1
GPU_ID2
CH212 100P_0402_50V8J ESD@
CH209 100P_0402_50V8J @ESD@
RH66 2.2K_0402_5%
SMBALERT#
RH64 2.2K_0402_5%
SML0ALERT#
CH51 10P_0402_25V8J @RF@
RH685 150K_0402_5%
SPKR
RH65 150K_0402_5%
SML1ALERT#

GPU_THM_SMBCLK
GPU_THM_SMBDAT

CLRP1 in DIMM Door

Buffer with Open Drain Output For VTT power control

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and
allow the entire region of the SPI flash to be updated using FPT.

ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE
Disable ME Protect (ME can be updated) Enable ME Protect (ME cannot be updated)(Default posit i on)

GPU ID	GPU ID2 (GPP_D6)	GPU ID1 (GPP_D5)
UMA	0	0
N17P-G0	0	1
N17E-G1	1	0
N17P-G1	1	1

Reserve for ESD

TLS CONFIDENTIALITY	
HIGH LOW(DEFAULT)	Enable Disable

Reserve for RF please close to UH1

EC interface	
HIGH LOW(DEFAULT)	ESPI* LPC

Top Swap Override (internal PD)	
HIGH LOW(DEFAULT)	Enable Disable

PCHHOT#	
HIGH LOW(DEFAULT)	Enable Disable

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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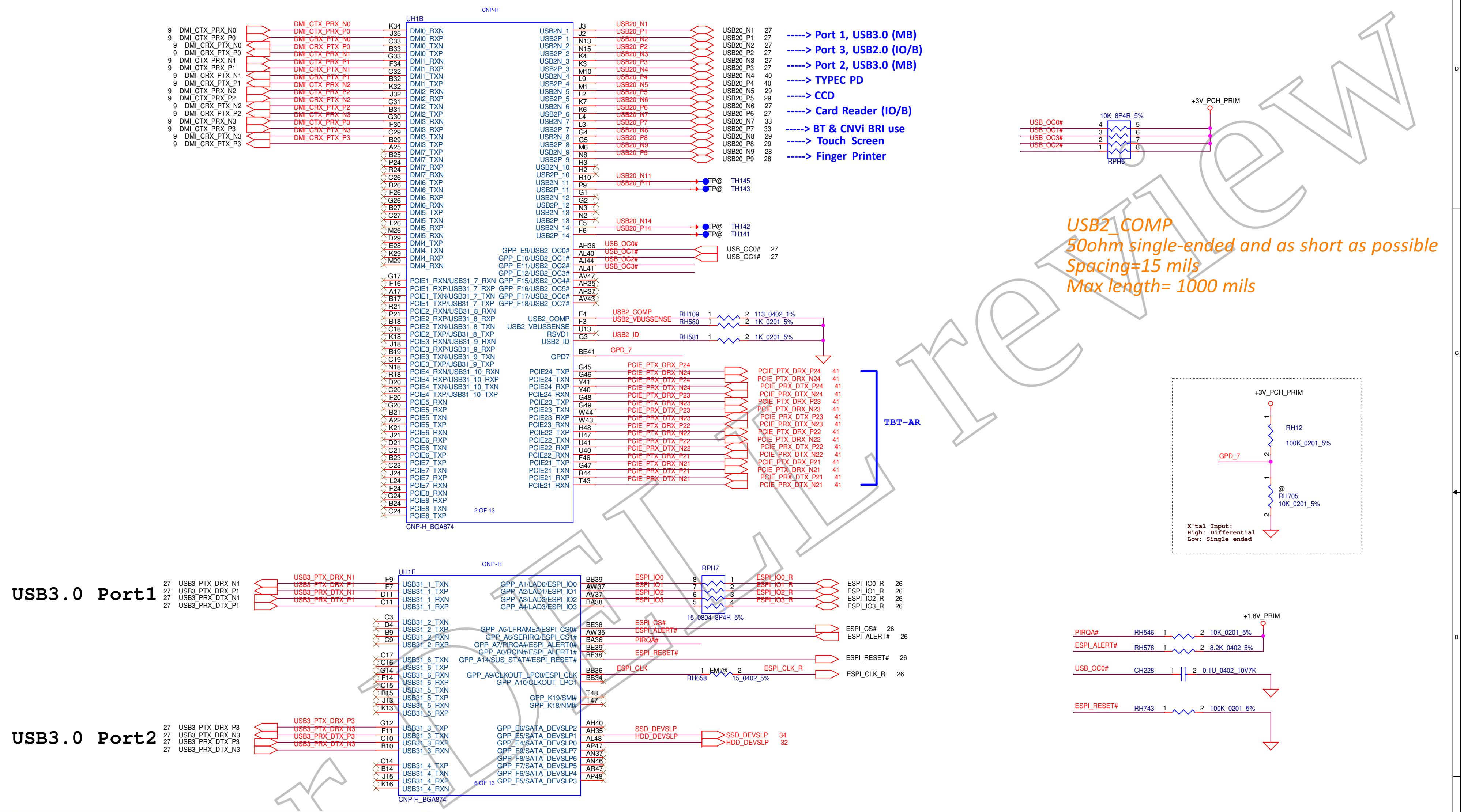
Compal Electronics, Inc.

Title
PCH (3/7) PM,HDA,SMB,JTAG
Size Document Number
LA-F611P
Rev 0.3
Date: Thursday, March 22, 2018 Sheet 18 of 78

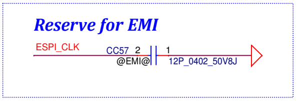
Main Func = PCH

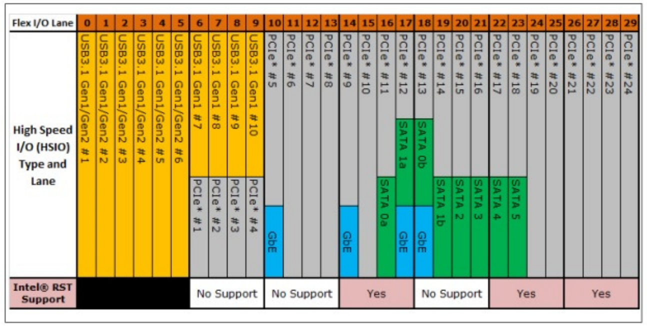
Update OK


CNP-H
UH1B
DMI0_RXN
DMI0_RXP
DMI0_TXN
DMI0_TXP
DMI1_RXN
DMI1_RXP
DMI1_TXN
DMI1_TXP
DMI2_RXN
DMI2_RXP
DMI2_TXN
DMI2_TXP
DMI3_RXN
DMI3_RXP
DMI3_TXN
DMI3_TXP
DMI_CTX_PRX_N0
DMI_CTX_PRX_P0
DMI_CRX_PTX_N0
DMI_CRX_PTX_P0
DMI_CTX_PRX_N1
DMI_CTX_PRX_P1
DMI_CRX_PTX_N1
DMI_CRX_PTX_P1
DMI_CTX_PRX_N2
DMI_CTX_PRX_P2
DMI_CRX_PTX_N2
DMI_CRX_PTX_P2
DMI_CTX_PRX_N3
DMI_CTX_PRX_P3
DMI_CRX_PTX_N3
DMI_CRX_PTX_P3
USB20_N1
USB20_P1
USB20_N2
USB20_P2
USB20_N3
USB20_P3
USB20_N4
USB20_P4
USB20_N5
USB20_P5
USB20_N6
USB20_P6
USB20_N7
USB20_P7
USB20_N8
USB20_P8
USB20_N9
USB20_P9
-----> Port 1, USB3.0 (MB)
-----> Port 3, USB2.0 (IO/B)
-----> Port 2, USB3.0 (MB)
-----> TYPEC PD
-----> CCD
-----> Card Reader (IO/B)
-----> BT & CNVi BRI use
-----> Touch Screen
-----> Finger Printer
USB20_N11
USB20_P11
TP@ TH145
TP@ TH143
USB20_N14
USB20_P14
TP@ TH142
TP@ TH141
USB_OC0#
USB_OC1#
USB_OC2#
USB_OC3#
+3V_PCH_PRIM
10K_8P4R_5%
RPH6
USB2_COMP
USB2_VBUSSENSE
USB2_ID
RH109 113_0402_1%
RH580 1K_0201_5%
RH581 1K_0201_5%
GPD_7
PCIE_PTX_DRX_P24
PCIE_PTX_DRX_N24
PCIE_PRX_DTX_P24
PCIE_PRX_DTX_N24
PCIE_PTX_DRX_P23
PCIE_PTX_DRX_N23
PCIE_PRX_DTX_P23
PCIE_PRX_DTX_N23
PCIE_PTX_DRX_P22
PCIE_PTX_DRX_N22
PCIE_PRX_DTX_P22
PCIE_PRX_DTX_N22
PCIE_PTX_DRX_P21
PCIE_PTX_DRX_N21
PCIE_PRX_DTX_P21
PCIE_PRX_DTX_N21
TBT-AR
2 OF 13
CNP-H_BGA874
+3V_PCH_PRIM
RH12 100K_0201_5%
GPD_7
@ RH705 10K_0201_5%
X'tal Input:
High: Differential
Low: Single ended
USB3.0 Port1
USB3_PTX_DRX_N1
USB3_PTX_DRX_P1
USB3_PRX_DTX_N1
USB3_PRX_DTX_P1
UH1F
RPH7
15_0804_8P4R_5%
ESPI_IO0
ESPI_IO1
ESPI_IO2
ESPI_IO3
ESPI_IO0_R
ESPI_IO1_R
ESPI_IO2_R
ESPI_IO3_R
ESPI_CS#
ESPI_ALERT#
PIRQA#
ESPI_RESET#
ESPI_CLK
RH658 15_0402_5%
ESPI_CLK_R
USB3.0 Port2
USB3_PTX_DRX_P3
USB3_PTX_DRX_N3
USB3_PRX_DTX_P3
USB3_PRX_DTX_N3
SSD_DEVSLP
HDD_DEVSLP
6 OF 13
+1.8V_PRIM
RH546 10K_0201_5%
RH578 8.2K_0402_5%
CH228 0.1U_0402_10V7K
RH743 100K_0201_5%

USB2_COMP
50ohm single-ended and as short as possible
Spacing=15 mils
Max length= 1000 mils

Reserve for EMI


ESPI_CLK
CC57
@EMI@
12P_0402_50V8J



Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7 PCIe* #1	USB3.1 Gen1 #8 PCIe* #2	USB3.1 Gen1 #9 PCIe* #3	USB3.1 Gen1 #10 PCIe* #4	PCIe* #5 GbE	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9 GbE	PCIe* #10	PCIe* #11 SATA 0a	PCIe* #12 SATA 1a GbE	PCIe* #13 SATA 0b GbE	PCIe* #14 SATA 1b	PCIe* #15 SATA 2	PCIe* #16 SATA 3	PCIe* #17 SATA 4	PCIe* #18 SATA 5	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: PCH (4/7) DMI,PCIE,USB,LPC
				Size: Document Number: LA-F611P Rev: 0.3
				Date: Thursday, March 22, 2018 Sheet 19 of 78

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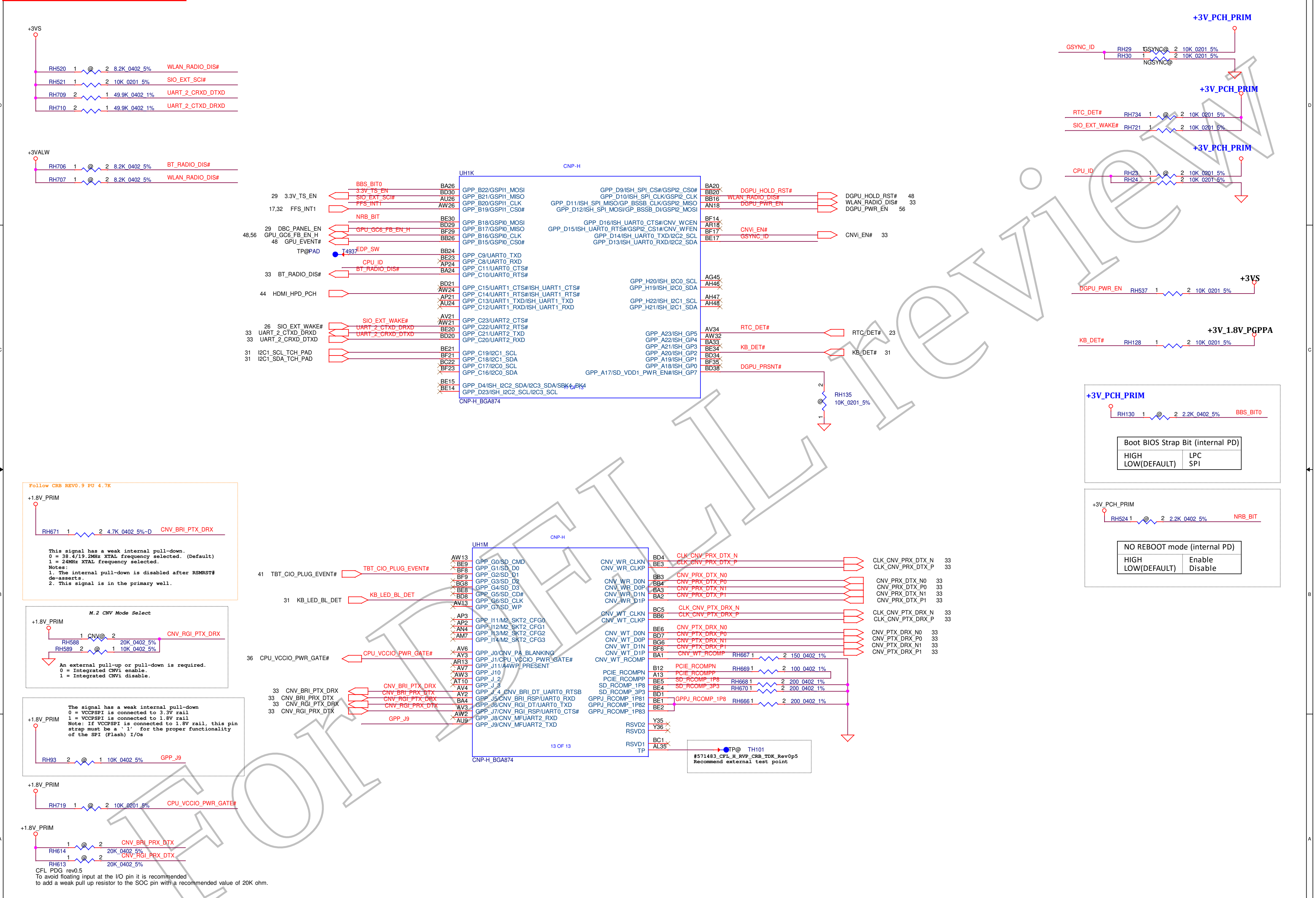
Main Func = PCH



+3VS
RH520 1 @ 2 8.2K_0402_5% WLAN_RADIO_DIS#
RH521 1 2 10K_0201_5% SIO_EXT_SCI#
RH709 2 1 49.9K_0402_1% UART_2_CRXD_DTXD
RH710 2 1 49.9K_0402_1% UART_2_CTXD_DRXD
+3VALW
RH706 1 @ 2 8.2K_0402_5% BT_RADIO_DIS#
RH707 1 @ 2 8.2K_0402_5% WLAN_RADIO_DIS#
UH1K
CNP-H
BBS_BIT0
3.3V_TS_EN
SIO_EXT_SCI#
FFS_INT1
NRB_BIT
GPU_GC6_FB_EN_H
EDP_SW
CPU_ID
BT_RADIO_DIS#
29 3.3V_TS_EN
17,32 FFS_INT1
29 DBC_PANEL_EN
48,56 GPU_GC6_FB_EN_H
48 GPU_EVENT#
TP@PAD T4937
33 BT_RADIO_DIS#
44 HDMI_HPD_PCH
26 SIO_EXT_WAKE#
33 UART_2_CTXD_DRXD
33 UART_2_CRXD_DTXD
31 I2C1_SCL_TCH_PAD
31 I2C1_SDA_TCH_PAD
SIO_EXT_WAKE#
UART_2_CTXD_DRXD
UART_2_CRXD_DTXD
BA26 GPP_B22/GSPI1_MOSI
BD30 GPP_B21/GSPI1_MISO
AU26 GPP_B20/GSPI1_CLK
AW26 GPP_B19/GSPI1_CS0#
BE30 GPP_B18/GSPI0_MOSI
BD29 GPP_B17/GSPI0_MISO
BF29 GPP_B16/GSPI0_CLK
BB26 GPP_B15/GSPI0_CS0#
BB24 GPP_C9/UART0_TXD
BE23 GPP_C8/UART0_RXD
AP24 GPP_C11/UART0_CTS#
BA24 GPP_C10/UART0_RTS#
BD21 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
AW24 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
AP21 GPP_C13/UART1_TXD/ISH_UART1_TXD
AU24 GPP_C12/UART1_RXD/ISH_UART1_RXD
AV21 GPP_C23/UART2_CTS#
AW21 GPP_C22/UART2_RTS#
BE20 GPP_C21/UART2_TXD
BD20 GPP_C20/UART2_RXD
BE21 GPP_C19/I2C1_SCL
BF21 GPP_C18/I2C1_SDA
BC22 GPP_C17/I2C0_SCL
BF23 GPP_C16/I2C0_SDA
BE15 GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4_BK4
BE14 GPP_D23/ISH_I2C2_SCL/I2C3_SCL
CNP-H_BGA874
GPP_D9/ISH_SPI_CS#/GSPI2_CS0# BA20
GPP_D10/ISH_SPI_CLK/GSPI2_CLK BB20
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO BB16
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI AN18
GPP_D16/ISH_UART0_CTS#/CNV_WCEN BF14
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN AR18
GPP_D14/ISH_UART0_TXD/I2C2_SCL BF17
GPP_D13/ISH_UART0_RXD/I2C2_SDA BE17
GPP_H20/ISH_I2C0_SCL AG45
GPP_H19/ISH_I2C0_SDA AH46
GPP_H22/ISH_I2C1_SCL AH47
GPP_H21/ISH_I2C1_SDA AH48
GPP_A23/ISH_GP5 AV34
GPP_A22/ISH_GP4 AW32
GPP_A21/ISH_GP3 BA33
GPP_A20/ISH_GP2 BE34
GPP_A19/ISH_GP1 BD34
GPP_A18/ISH_GP0 BF35
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7 BD38
DGPU_HOLD_RST#
WLAN_RADIO_DIS#
DGPU_PWR_EN
DGPU_HOLD_RST# 48
WLAN_RADIO_DIS# 33
DGPU_PWR_EN 56
CNVi_EN#
GSYNC_ID
CNVi_EN# 33
RTC_DET#
RTC_DET# 23
KB_DET#
KB_DET# 31
DGPU_PRSNT#
RH135 10K_0201_5%
+3V_PCH_PRIM
GSYNC_ID
RH29 GSYNC@ 2 10K_0201_5%
RH30 1 2 10K_0201_5%
NGSYNC@
+3V_PCH_PRIM
RTC_DET# RH734 1 @ 2 10K_0201_5%
SIO_EXT_WAKE# RH721 1 2 10K_0201_5%
+3V_PCH_PRIM
CPU_ID
RH23 1 @ 2 10K_0201_5%
RH24 1 2 10K_0201_5%
+3VS
DGPU_PWR_EN RH537 1 2 10K_0201_5%
+3V_1.8V_PGPPA
KB_DET# RH128 1 2 10K_0201_5%
+3V_PCH_PRIM
RH130 1 @ 2 2.2K_0402_5% BBS_BIT0
+3V_PCH_PRIM
RH524 1 @ 2 2.2K_0402_5% NRB_BIT
Follow CRB REV0.9 PU 4.7K
+1.8V_PRIM
RH671 1 2 4.7K_0402_5%~D CNV_BRI_PTX_DRX
UH1M
CNP-H
41 TBT_CIO_PLUG_EVENT#
TBT_CIO_PLUG_EVENT#
31 KB_LED_BL_DET
KB_LED_BL_DET
36 CPU_VCCIO_PWR_GATE#
CPU_VCCIO_PWR_GATE#
33 CNV_BRI_PTX_DRX
33 CNV_BRI_PRX_DTX
33 CNV_RGI_PTX_DRX
33 CNV_RGI_PRX_DTX
GPP_J9
AW13 GPP_G0/SD_CMD
BE9 GPP_G1/SD_D0
BF8 GPP_G2/SD_D1
BF9 GPP_G3/SD_D2
BG8 GPP_G4/SD_D3
BE8 GPP_G5/SD_CD#
BD8 GPP_G6/SD_CLK
AV13 GPP_G7/SD_WP
AP3 GPP_I11/M2_SKT2_CFG0
AP2 GPP_I12/M2_SKT2_CFG1
AN4 GPP_I13/M2_SKT2_CFG2
AM7 GPP_I14/M2_SKT2_CFG3
AV6 GPP_J0/CNV_PA_BLANKING
AY3 GPP_J1/CPU_VCCIO_PWR_GATE#
AR13 GPP_J11/A4WP_PRESENT
AV7 GPP_J10
AW3 GPP_J_2
AT10 GPP_J_3
AV4 GPP_J_4_CNV_BRI_DT_UART0_RTSB
AY2 GPP_J5/CNV_BRI_RSP/UART0_RXD
BA4 GPP_J6/CNV_RGI_DT/UART0_TXD
AY3 GPP_J7/CNV_RGI_RSP/UART0_CTS#
AW2 GPP_J8/CNV_MFUART2_RXD
AU9 GPP_J9/CNV_MFUART2_TXD
CNV_WR_CLKN BD4
CNV_WR_CLKP BE3
CNV_WR_D0N BB3
CNV_WR_D0P BB4
CNV_WR_D1N BA3
CNV_WR_D1P BA2
CNV_WT_CLKN BC5
CNV_WT_CLKP BB6
CNV_WT_D0N BE6
CNV_WT_D0P BD7
CNV_WT_D1N BG6
CNV_WT_D1P BF6
CNV_WT_RCOMP BA1
PCIE_RCOMPN B12
PCIE_RCOMPP A13
SD_RCOMP_1P8 BE5
SD_RCOMP_3P3 BE4
GPPJ_RCOMP_1P81 BD1
GPPJ_RCOMP_1P82 BE1
GPPJ_RCOMP_1P83 BE2
RSVD2 Y35
RSVD3 Y36
RSVD1 BC1
TP AL35
13 OF 13
CNP-H_BGA874
CLK_CNV_PRX_DTX_N
CLK_CNV_PRX_DTX_P
CNV_PRX_DTX_N0
CNV_PRX_DTX_P0
CNV_PRX_DTX_N1
CNV_PRX_DTX_P1
CLK_CNV_PTX_DRX_N
CLK_CNV_PTX_DRX_P
CNV_PTX_DRX_N0
CNV_PTX_DRX_P0
CNV_PTX_DRX_N1
CNV_PTX_DRX_P1
CNV_WT_RCOMP
CLK_CNV_PRX_DTX_N 33
CLK_CNV_PRX_DTX_P 33
CNV_PRX_DTX_N0 33
CNV_PRX_DTX_P0 33
CNV_PRX_DTX_N1 33
CNV_PRX_DTX_P1 33
CLK_CNV_PTX_DRX_N 33
CLK_CNV_PTX_DRX_P 33
CNV_PTX_DRX_N0 33
CNV_PTX_DRX_P0 33
CNV_PTX_DRX_N1 33
CNV_PTX_DRX_P1 33
RH667 1 2 150_0402_1%
PCIE_RCOMPN
PCIE_RCOMPP
RH669 1 2 100_0402_1%
SD_RCOMP_1P8
SD_RCOMP_3P3
RH668 1 2 200_0402_1%
RH670 1 2 200_0402_1%
GPPJ_RCOMP_1P8
RH666 1 2 200_0402_1%
TP@ TH101
M.2 CNV Mode Select
+1.8V_PRIM
1 CNV@ 2 CNV_RGI_PTX_DRX
RH588 20K_0402_5%
RH589 2 @ 1 10K_0402_5%
+1.8V_PRIM
RH93 2 @ 1 10K_0402_5% GPP_J9
+1.8V_PRIM
RH719 1 @ 2 10K_0201_5% CPU_VCCIO_PWR_GATE#
+1.8V_PRIM
1 @ 2 CNV_BRI_PRX_DTX
RH614 20K_0402_5%
1 @ 2 CNV_RGI_PRX_DTX
RH613 20K_0402_5%

Boot BIOS Strap Bit (internal PD)

HIGH	LPC
LOW(DEFAULT)	SPI

NO REBOOT mode (internal PD)

HIGH	Enable
LOW(DEFAULT)	Disable

This signal has a weak internal pull-down.
0 = 38.4/19.2MHz XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.
Notes:
1. The internal pull-down is disabled after RSMRST#
de-asserts.
2. This signal is in the primary well.

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

The signal has a weak internal pull-down
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin
strap must be a ' 1' for the proper functionality
of the SPI (Flash) I/Os

#571483_CFL_H_RVP_CRB_TDK_Rev0p5
Recommend external test point

CFL PDG rev0.5
To avoid floating input at the I/O pin it is recommended
to add a weak pull up resistor to the SOC pin with a recommended value of 20K ohm.

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: PCH (5/7) I2C,GPIO,CNVI
				Size / Document Number: LA-F611P / Rev 0.3
				Date: Thursday, March 22, 2018 / Sheet 20 of 78

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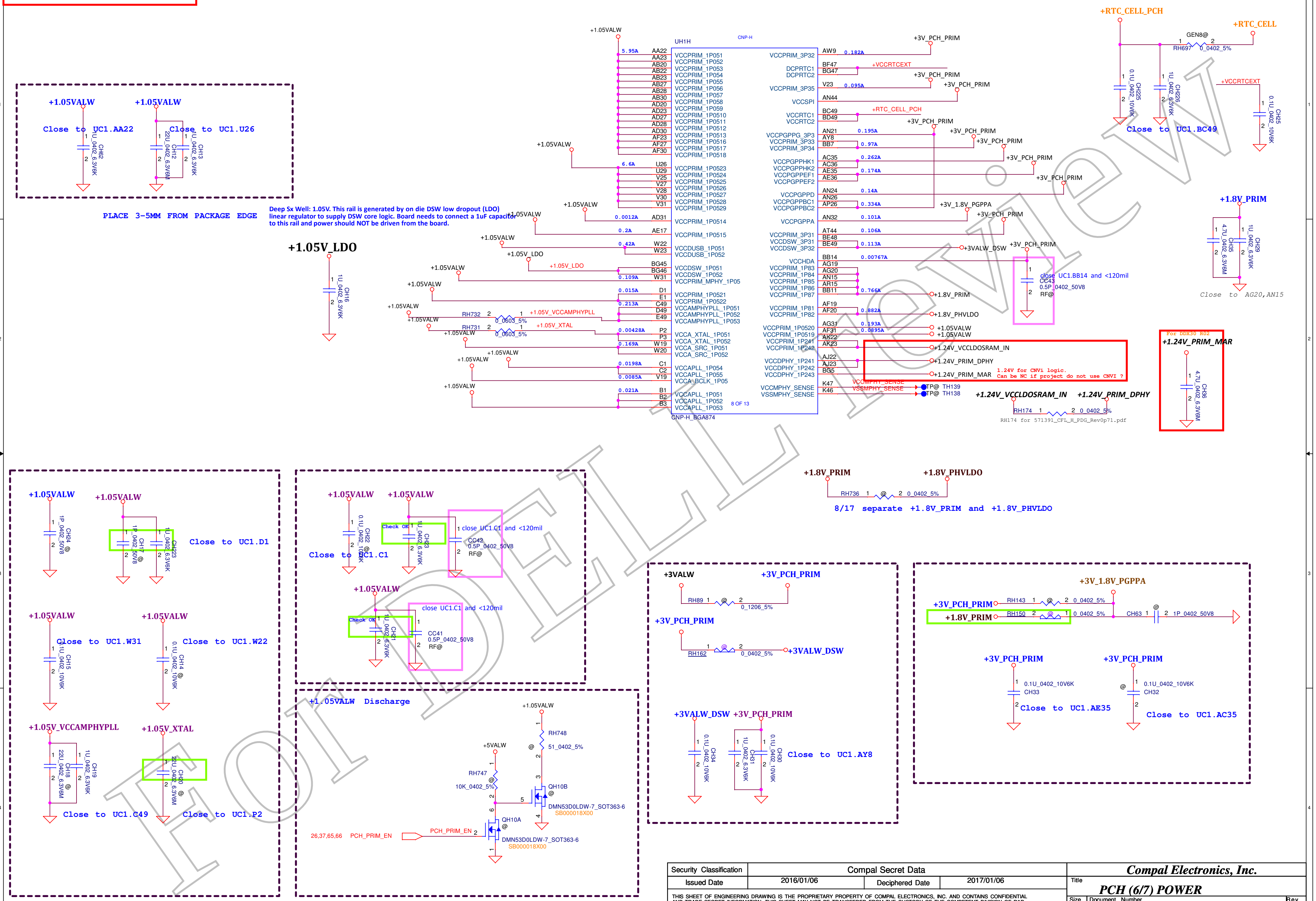
Main Func = PCH


UH1H
CNP-H
CNP-H_BGA874
8 OF 13
+1.05VALW
5.95A
AA22 AA23 AB20 AB22 AB23 AB27 AB28 AB30 AD20 AD23 AD27 AD28 AD30 AF23 AF27 AF30
VCCPRIM_1P051 … VCCPRIM_1P0518
6.6A
U26 U29 V25 V27 V28 V30 V31
VCCPRIM_1P0523 … VCCPRIM_1P0529
0.0012A AD31 VCCPRIM_1P0514
0.2A AE17 VCCPRIM_1P0515
0.42A W22 W23 VCCDUSB_1P051 VCCDUSB_1P052
+1.05V_LDO
0.109A BG45 BG46 W31 VCCDSW_1P051 VCCDSW_1P052 VCCPRIM_MPHY_1P05
0.015A D1 E1 VCCPRIM_1P0521 VCCPRIM_1P0522
0.213A C49 D49 E49 VCCAMPHYPLL_1P051 VCCAMPHYPLL_1P052 VCCAMPHYPLL_1P053
RH732 0_0603_5% +1.05V_VCCAMPHYPLL
RH731 0_0603_5% +1.05V_XTAL
0.00428A P2 P3 VCCA_XTAL_1P051 VCCA_XTAL_1P052
0.169A W19 W20 VCCA_SRC_1P051 VCCA_SRC_1P052
0.0198A C1 C2 VCCAPLL_1P054 VCCAPLL_1P055
0.0085A V19 VCCA_BCLK_1P05
0.021A B1 B2 B3 VCCAPLL_1P051 VCCAPLL_1P052 VCCAPLL_1P053
AW9 0.182A VCCPRIM_3P32 +3V_PCH_PRIM
BF47 BG47 DCPRTC1 DCPRTC2 +VCCRTCEXT
V23 0.095A VCCPRIM_3P35
AN44 VCCSPI
BC49 BD49 VCCRTC1 VCCRTC2 +RTC_CELL_PCH
AN21 0.195A VCCPGPPG_3P3
AY8 BB7 0.97A VCCPRIM_3P33 VCCPRIM_3P34
AC35 AC36 0.262A VCCPGPPHK1 VCCPGPPHK2
AE35 AE36 0.174A VCCPGPPEF1 VCCPGPPEF2
AN24 0.14A VCCPGPPD
AN26 AP26 0.334A VCCPGPPBC1 VCCPGPPBC2 +3V_1.8V_PGPPA
AN32 0.101A VCCPGPPA
AT44 0.106A VCCPRIM_3P31
BE48 BE49 0.113A VCCDSW_3P31 VCCDSW_3P32 +3VALW_DSW
BB14 0.00767A VCCHDA
AG19 AG20 AN15 AR15 BB11 0.766A VCCPRIM_1P83 … VCCPRIM_1P87 +1.8V_PRIM
AF19 AF20 0.882A VCCPRIM_1P81 VCCPRIM_1P82 +1.8V_PHVLDO
AG31 AF31 0.193A 0.0895A VCCPRIM_1P0520 VCCPRIM_1P0519
AK22 AK23 VCCPRIM_1P241 VCCPRIM_1P242 +1.24V_VCCLDOSRAM_IN
AJ22 AJ23 BG5 VCCDPHY_1P241 VCCDPHY_1P242 VCCDPHY_1P243 +1.24V_PRIM_DPHY +1.24V_PRIM_MAR
K47 K46 VCCMPHY_SENSE VSSMPHY_SENSE TP@ TH139 TP@ TH138
+1.24V_VCCLDOSRAM_IN +1.24V_PRIM_DPHY
RH174 0_0402_5%
RH174 for 571391_CFL_H_PDG_Rev0p71.pdf
+RTC_CELL_PCH +RTC_CELL GEN8@ RH697 0_0402_5%
CH225 0.1U_0402_10V6K CH226 1U_0402_6.3V6K
+VCCRTCEXT CH25 0.1U_0402_10V6K
Close to UC1.BC49
close UC1.BB14 and <120mil
CC43 0.5P_0402_50V8 RF@
+1.8V_PRIM CH35 4.7U_0402_6.3V6M CH29 1U_0402_6.3V6K
Close to AG20,AN15
For DDX30 R02
+1.24V_PRIM_MAR CH36 4.7U_0402_6.3V6M
+1.05VALW CH62 1U_0402_6.3V6K Close to UC1.AA22
+1.05VALW CH12 22U_0402_6.3V6M CH13 1U_0402_6.3V6K Close to UC1.U26
PLACE 3-5MM FROM PACKAGE EDGE
+1.05V_LDO CH16 1U_0402_6.3V6K
+1.05VALW CH24 1P_0402_50V8 @
+1.05VALW CH17 1P_0402_50V8 @ CH23 1U_0402_6.3V6K Close to UC1.D1
+1.05VALW CH15 1U_0402_10V6K Close to UC1.W31
+1.05VALW CH14 0.1U_0402_10V6K @ Close to UC1.W22
+1.05V_VCCAMPHYPLL CH18 22U_0402_6.3V6M @ CH19 1U_0402_6.3V6K Close to UC1.C49
+1.05V_XTAL CH20 22U_0402_6.3V6M @ Close to UC1.P2
+1.05VALW CH22 0.1U_0402_10V6K +1.05VALW Check OK CH43 1U_0402_6.3V6K
close UC1.C1 and <120mil CC42 0.5P_0402_50V8 RF@ Close to UC1.C1
+1.05VALW Check OK CH21 1U_0402_6.3V6K close UC1.C1 and <120mil CC41 0.5P_0402_50V8 RF@
+1.05VALW Discharge
+1.05VALW RH748 51_0402_5% @
+5VALW RH747 10K_0402_5% @
QH10B DMN53D0LDW-7_SOT363-6 SB000018X00
QH10A DMN53D0LDW-7_SOT363-6 SB000018X00
26,37,65,66 PCH_PRIM_EN PCH_PRIM_EN
+1.8V_PRIM +1.8V_PHVLDO RH736 @ 0_0402_5%
8/17 separate +1.8V_PRIM and +1.8V_PHVLDO
+3VALW +3V_PCH_PRIM RH89 @ 0_1206_5%
+3V_PCH_PRIM RH162 0_0402_5% +3VALW_DSW
+3VALW_DSW +3V_PCH_PRIM CH34 0.1U_0402_10V6K CH31 1U_0402_6.3V6K CH30 0.1U_0402_10V6K Close to UC1.AY8
+3V_1.8V_PGPPA +3V_PCH_PRIM RH143 @ 0_0402_5% +1.8V_PRIM RH150 @ 0_0402_5% CH63 @ 1P_0402_50V8
+3V_PCH_PRIM CH33 0.1U_0402_10V6K Close to UC1.AE35
+3V_PCH_PRIM CH32 0.1U_0402_10V6K @ Close to UC1.AC35
For DELL Review

Deep Sx Well: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board.

1.24V for CNVi logic.
Can be NC if project do not use CNVI ?

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: PCH (6/7) POWER

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Size Document Number LA-F611P Rev 0.3

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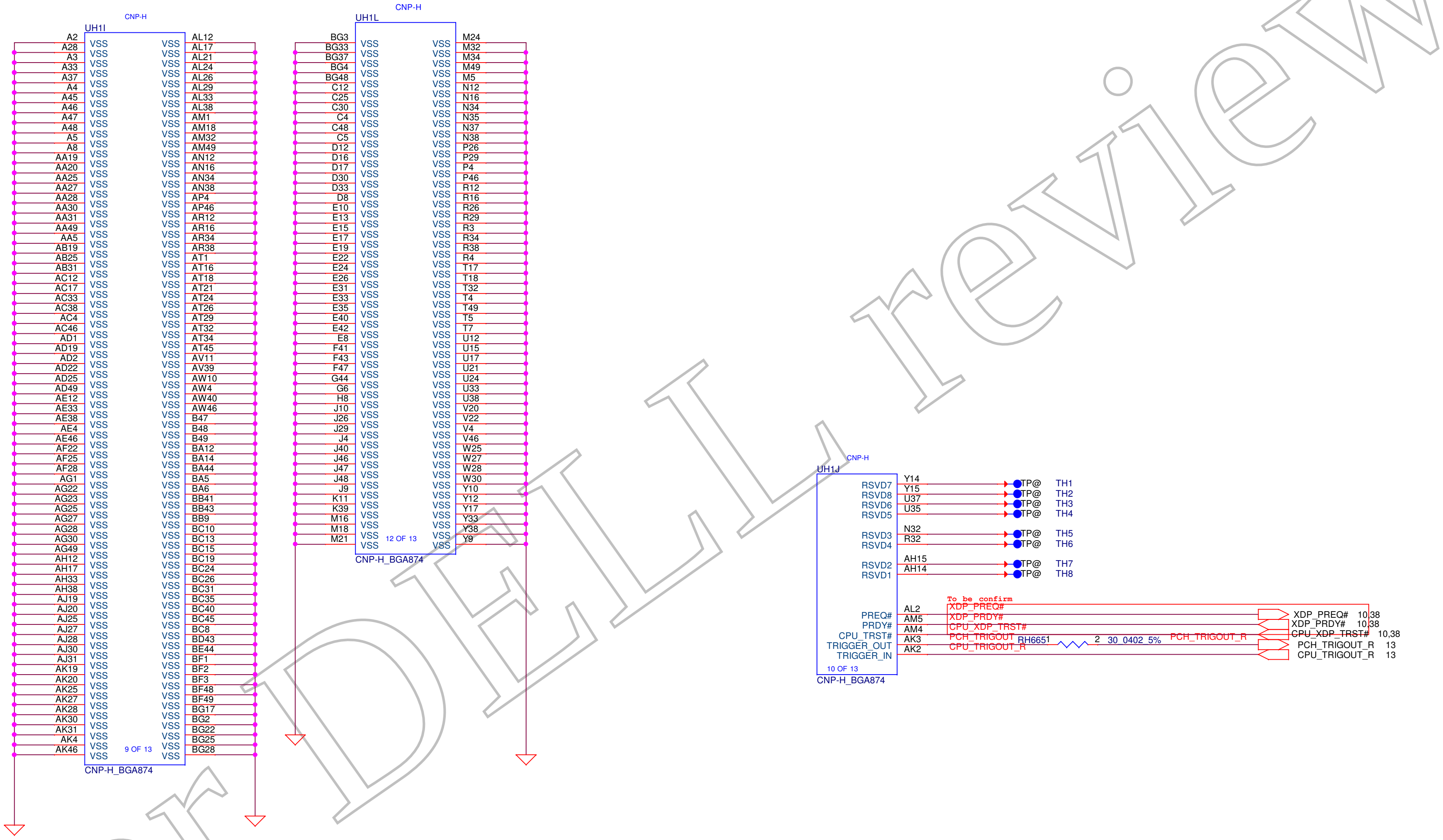
Main Func = PCH



CNP-H
UH1I
A2
A28
A3
A33
A37
A4
A45
A46
A47
A48
A5
A8
AA19
AA20
AA25
AA27
AA28
AA30
AA31
AA49
AA5
AB19
AB25
AB31
AC12
AC17
AC33
AC38
AC4
AC46
AD1
AD19
AD2
AD22
AD25
AD49
AE12
AE33
AE38
AE4
AE46
AF22
AF25
AF28
AG1
AG22
AG23
AG25
AG27
AG28
AG30
AG49
AH12
AH17
AH33
AH38
AJ19
AJ20
AJ25
AJ27
AJ28
AJ30
AJ31
AK19
AK20
AK25
AK27
AK28
AK30
AK31
AK4
AK46
VSS
AL12
AL17
AL21
AL24
AL26
AL29
AL33
AL38
AM1
AM18
AM32
AM49
AN12
AN16
AN34
AN38
AP4
AP46
AR12
AR16
AR34
AR38
AT1
AT16
AT18
AT21
AT24
AT26
AT29
AT32
AT34
AT45
AV11
AV39
AW10
AW4
AW40
AW46
B47
B48
B49
BA12
BA14
BA44
BA5
BA6
BB41
BB43
BB9
BC10
BC13
BC15
BC19
BC24
BC26
BC31
BC35
BC40
BC45
BC8
BD43
BE44
BF1
BF2
BF3
BF48
BF49
BG17
BG2
BG22
BG25
BG28
9 OF 13
CNP-H_BGA874
CNP-H
UH1L
BG3
BG33
BG37
BG4
BG48
C12
C25
C30
C4
C48
C5
D12
D16
D17
D30
D33
D8
E10
E13
E15
E17
E19
E22
E24
E26
E31
E33
E35
E40
E42
E8
F41
F43
F47
G44
G6
H8
J10
J26
J29
J4
J40
J46
J47
J48
J9
K11
K39
M16
M18
M21
M24
M32
M34
M49
M5
N12
N16
N34
N35
N37
N38
P26
P29
P4
P46
R12
R16
R26
R29
R3
R34
R38
R4
T17
T18
T32
T4
T49
T5
T7
U12
U15
U17
U21
U24
U33
U38
V20
V22
V4
V46
W25
W27
W28
W30
Y10
Y12
Y17
Y33
Y38
Y9
12 OF 13
CNP-H_BGA874
CNP-H
UH1J
RSVD7
RSVD8
RSVD6
RSVD5
RSVD3
RSVD4
RSVD2
RSVD1
Y14
Y15
U37
U35
N32
R32
AH15
AH14
TP@ TH1
TP@ TH2
TP@ TH3
TP@ TH4
TP@ TH5
TP@ TH6
TP@ TH7
TP@ TH8
PREQ#
PRDY#
CPU_TRST#
TRIGGER_OUT
TRIGGER_IN
AL2
AM5
AM4
AK3
AK2
To be confirm
XDP_PREQ#
XDP_PRDY#
CPU_XDP_TRST#
PCH_TRIGOUT
CPU_TRIGOUT_R
RH6651
2
30_0402_5%
PCH_TRIGOUT_R
XDP_PREQ# 10,38
XDP_PRDY# 10,38
CPU_XDP_TRST# 10,38
PCH_TRIGOUT_R 13
CPU_TRIGOUT_R 13
10 OF 13
CNP-H_BGA874

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title
PCH (7/7) VSS

Size Document Number
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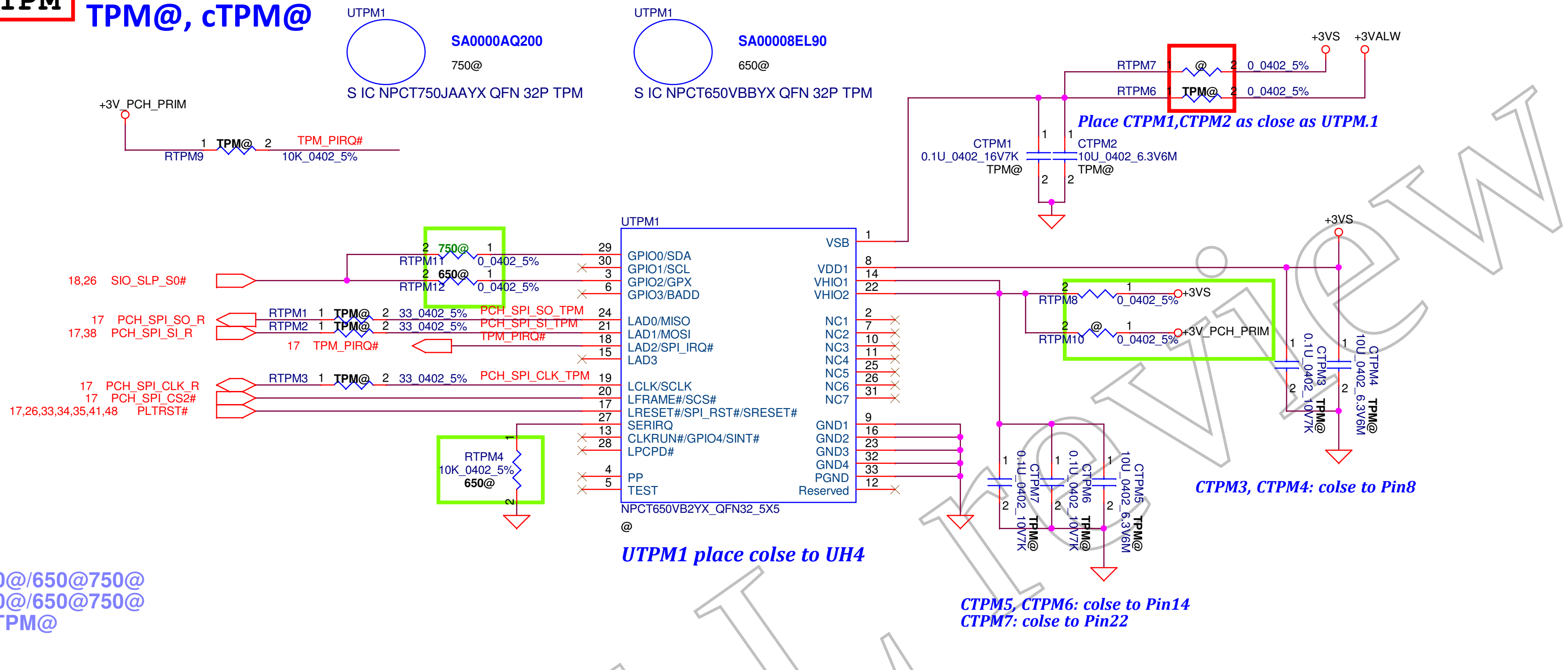
Date: Thursday, March 22, 2018 Sheet 22 of 78

Main Func = TPM

TPM@, cTPM@


UTPM1
SA0000AQ200
750@
S IC NPCT750JAAYX QFN 32P TPM
UTPM1
SA00008EL90
650@
S IC NPCT650VBBYX QFN 32P TPM
+3V_PCH_PRIM
RTPM9
1 TPM@ 2
TPM_PIRQ#
10K_0402_5%
+3VS
+3VALW
RTPM7 1 @ 2 0_0402_5%
RTPM6 1 TPM@ 2 0_0402_5%
CTPM1
0.1U_0402_16V7K
TPM@
CTPM2
10U_0402_6.3V6M
TPM@
UTPM1
VSB
VDD1
VHIO1
VHIO2
GPIO0/SDA
GPIO1/SCL
GPIO2/GPX
GPIO3/BADD
LAD0/MISO
LAD1/MOSI
LAD2/SPI_IRQ#
LAD3
LCLK/SCLK
LFRAME#/SCS#
LRESET#/SPI_RST#/SRESET#
SERIRQ
CLKRUN#/GPIO4/SINT#
LPCPD#
PP
TEST
NC1
NC2
NC3
NC4
NC5
NC6
NC7
GND1
GND2
GND3
GND4
PGND
Reserved
NPCT650VB2YX_QFN32_5X5
@
RTPM11 2 750@ 1 0_0402_5%
RTPM12 2 650@ 1 0_0402_5%
18,26 SIO_SLP_S0#
17 PCH_SPI_SO_R
17,38 PCH_SPI_SI_R
RTPM1 1 TPM@ 2 33_0402_5% PCH_SPI_SO_TPM
RTPM2 1 TPM@ 2 33_0402_5% PCH_SPI_SI_TPM
TPM_PIRQ#
17 TPM_PIRQ#
17 PCH_SPI_CLK_R
17 PCH_SPI_CS2#
17,26,33,34,35,41,48 PLTRST#
RTPM3 1 TPM@ 2 33_0402_5% PCH_SPI_CLK_TPM
RTPM4
10K_0402_5%
650@
+3VS
RTPM8 2 1 0_0402_5%
RTPM10 2 @ 1 0_0402_5%
+3V_PCH_PRIM
CTPM3
0.1U_0402_10V7K
TPM@
CTPM4
10U_0402_6.3V6M
TPM@
CTPM7
0.1U_0402_10V7K
TPM@
CTPM6
0.1U_0402_10V7K
TPM@
CTPM5
10U_0402_6.3V6M
TPM@

Place CTPM1,CTPM2 as close as UTPM1.1

CTPM3, CTPM4: colse to Pin8

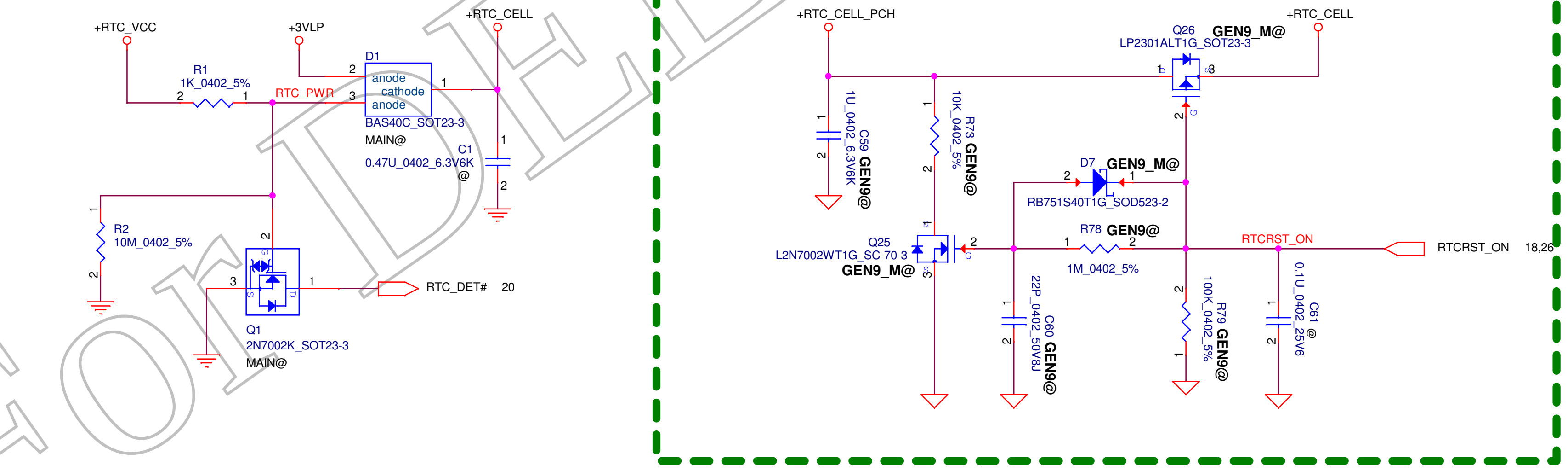
UTPM1 place colse to UH4

CTPM5, CTPM6: colse to Pin14
CTPM7: colse to Pin22

NPCT650:TPM@/650@/650@750@
NPCT750:TPM@/750@/650@750@
ChinaTPM:TPM@/cTPM@
SW TPM:fTPM@

Main Func = RTC

GEN9@


+RTC_VCC
+3VLP
+RTC_CELL
R1
1K_0402_5%
RTC_PWR
D1
anode
cathode
anode
BAS40C_SOT23-3
MAIN@
C1
0.47U_0402_6.3V6K
@
R2
10M_0402_5%
Q1
2N7002K_SOT23-3
MAIN@
RTC_DET# 20
+RTC_CELL_PCH
+RTC_CELL
Q26 GEN9_M@
LP2301ALT1G_SOT23-3
C59
1U_0402_6.3V6K
GEN9@
R73
10K_0402_5%
GEN9@
D7 GEN9_M@
RB751S40T1G_SOD523-2
R78 GEN9@
1M_0402_5%
Q25
L2N7002WT1G_SC-70-3
GEN9_M@
RTCRST_ON
RTCRST_ON 18,26
C60
22P_0402_50V8J
GEN9@
R79
100K_0402_5%
GEN9@
C61
0.1U_0402_25V6
@

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title
TPM/RTC/Screw Holes

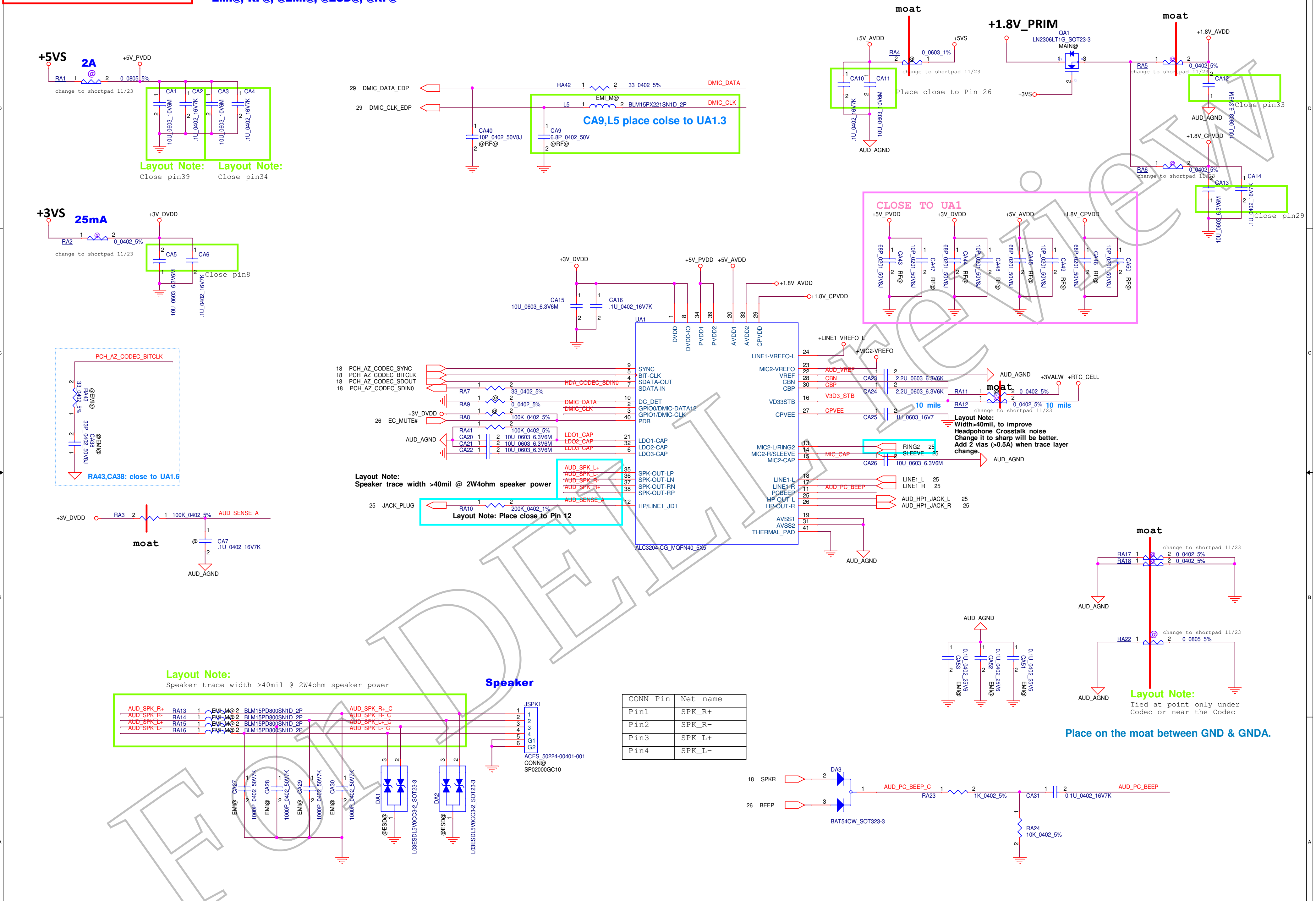
Size Document Number
LA-F611P

Rev 0.3

Date: Thursday, March 22, 2018 Sheet 23 of 78

Main Func = Audio

EMI@, RF@, @EMI@, @ESD@, @RF@



+5VS
2A
+5V_PVDD
RA1 0_0805_5%
change to shortpad 11/23
CA1 CA2 CA3 CA4
10U_0603_10V6M
.1U_0402_16V7K
Layout Note: Close pin39
Layout Note: Close pin34
+3VS
25mA
+3V_DVDD
RA2 0_0402_5%
CA5 CA6
10U_0603_6.3V6M
.1U_0402_16V7K
Close pin8
29 DMIC_DATA_EDP
29 DMIC_CLK_EDP
RA42 33_0402_5%
DMIC_DATA
DMIC_CLK
EMI_M@
L5 BLM15PX221SN1D_2P
CA40 10P_0402_50V8J @RF@
CA9 6.8P_0402_50V @RF@
CA9,L5 place colse to UA1.3
moat
+5V_AVDD
+5VS
RA4 0_0603_1%
change to shortpad 11/23
CA10 CA11
Place close to Pin 26
AUD_AGND
+1.8V_PRIM
QA1 LN2306LT1G_SOT23-3
MAIN@
+3VS
RA5 0_0402_5%
+1.8V_AVDD
CA12
Close pin33
+1.8V_CPVDD
RA6 0_0402_5%
CA13 CA14
Close pin29
CLOSE TO UA1
+5V_PVDD +3V_DVDD +5V_AVDD +1.8V_CPVDD
CA43 CA47 CA44 CA48 CA45 CA49 CA46 CA50
68P_0201_50V8J
10P_0201_50V8J
RF@
PCH_AZ_CODEC_BITCLK
RA43 33_0402_5% @EMI@
CA38 33P_0402_50V8J @EMI@
RA43,CA38: close to UA1.6
+3V_DVDD
CA15 10U_0603_6.3V6M
CA16 .1U_0402_16V7K
+5V_PVDD +5V_AVDD
+1.8V_AVDD
+1.8V_CPVDD
UA1
DVDD DVDD-IO PVDD1 PVDD2 AVDD1 AVDD2 CPVDD
18 PCH_AZ_CODEC_SYNC
18 PCH_AZ_CODEC_BITCLK
18 PCH_AZ_CODEC_SDOUT
18 PCH_AZ_CODEC_SDIN0
HDA_CODEC_SDIN0
RA7 33_0402_5%
RA9 0_0402_5%
+3V_DVDD
26 EC_MUTE#
RA8 100K_0402_5%
RA41 100K_0402_5%
AUD_AGND
CA20 CA21 CA22 10U_0603_6.3V6M
LDO1_CAP LDO2_CAP LDO3_CAP
SYNC BIT-CLK SDATA-OUT SDATA-IN
DC_DET GPIO0/DMIC-DATA12 GPIO1/DMIC-CLK PDB
LDO1-CAP LDO2-CAP LDO3-CAP
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power
AUD_SPK_L+ AUD_SPK_L- AUD_SPK_R- AUD_SPK_R+
SPK-OUT-LP SPK-OUT-LN SPK-OUT-RN SPK-OUT-RP
AUD_SENSE_A
25 JACK_PLUG
RA10 200K_0402_1%
HP/LINE1_JD1
Layout Note: Place close to Pin 12
ALC3204-CG_MQFN40_5X5
LINE1-VREFO-L
+LINE1_VREFO_L
+MIC2-VREFO
MIC2-VREFO VREF CBN CBP
AUD_VREF CBN CBP
CA23 2.2U_0603_6.3V6K
CA24 2.2U_0603_6.3V6K
AUD_AGND
+3VALW +RTC_CELL
V3D3_STB
VD33STB
RA11 0_0402_5%
RA12 0_0402_5%
10 mils
change to shortpad 11/23
CPVEE
CA25 1U_0603_16V7
Layout Note:
Width>40mil, to improve
Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer
change.
MIC2-L/RING2 MIC2-R/SLEEVE MIC2-CAP
RING2 25
SLEEVE 25
MIC_CAP
CA26 10U_0603_6.3V6M
LINE1-L LINE1-R PCBEEP HP-OUT-L HP-OUT-R
LINE1_L 25
LINE1_R 25
AUD_PC_BEEP
AUD_HP1_JACK_L 25
AUD_HP1_JACK_R 25
AVSS1 AVSS2 THERMAL_PAD
AUD_AGND
+3V_DVDD
RA3 100K_0402_5%
AUD_SENSE_A
moat
CA7 .1U_0402_16V7K
AUD_AGND
moat
change to shortpad 11/23
RA17 0_0402_5%
RA18 0_0402_5%
AUD_AGND
RA22 0_0805_5%
Layout Note:
Tied at point only under Codec or near the Codec
Place on the moat between GND & GNDA.
AUD_AGND
CA53 CA52 CA51 0.1U_0402_25V6 EMI@
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power
AUD_SPK_R+ AUD_SPK_R- AUD_SPK_L+ AUD_SPK_L-
RA13 RA14 RA15 RA16
EMI_M@ BLM15PD800SN1D_2P
AUD_SPK_R+_C AUD_SPK_R-_C AUD_SPK_L+_C AUD_SPK_L-_C
Speaker
JSPK1
ACES_50224-00401-001
CONN@
SP02000GC10
CA27 CA28 CA29 CA30 1000P_0402_50V7K EMI@
DA1 DA2 L03ESDL5V0CC3-2_SOT23-3 @ESD@
18 SPKR
26 BEEP
DA3 BAT54CW_SOT323-3
AUD_PC_BEEP_C
RA23 1K_0402_5%
CA31 0.1U_0402_16V7K
AUD_PC_BEEP
RA24 10K_0402_5%

CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

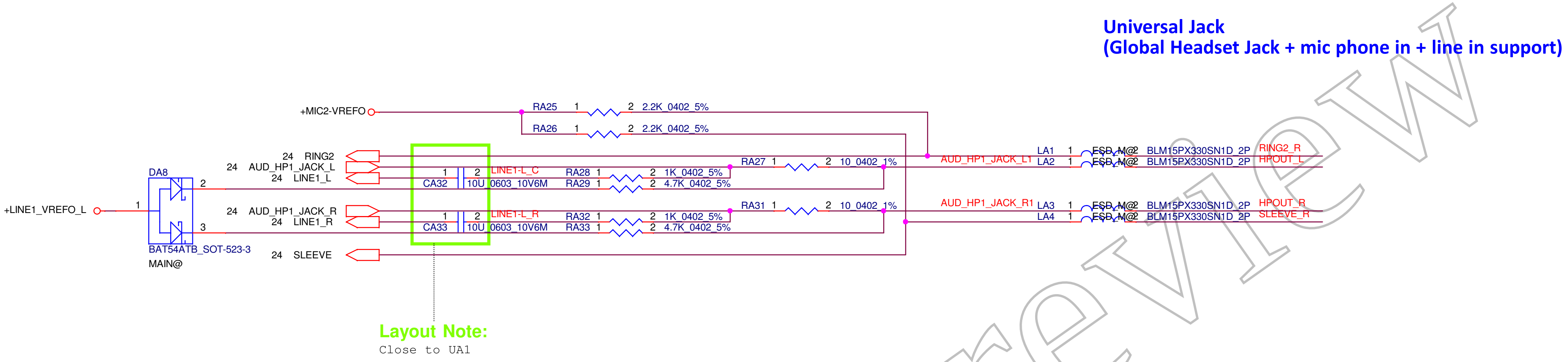
Title
Audio Codec ALC3204

Size Document Number **LA-F611P** Rev 0.3

Date: Thursday, March 22, 2018 Sheet 24 of 78

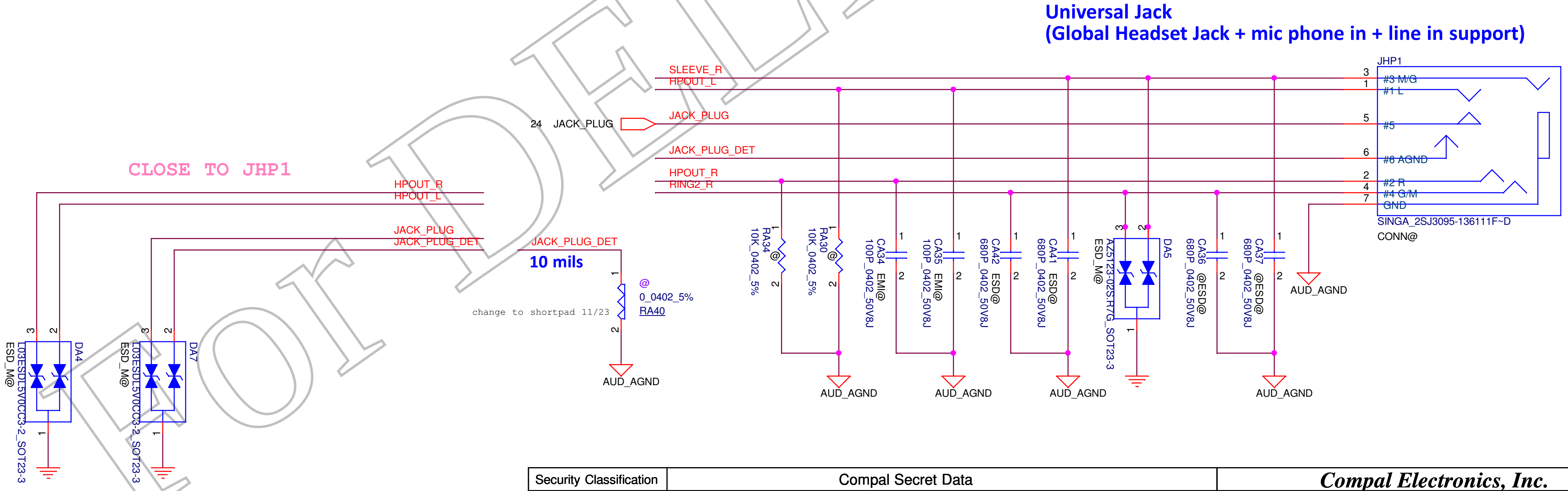
Main Func = Audio Jack

ESD@


Universal Jack
(Global Headset Jack + mic phone in + line in support)
+MIC2-VREFO
RA25 1 2 2.2K_0402_5%
RA26 1 2 2.2K_0402_5%
24 RING2
24 AUD_HP1_JACK_L
24 LINE1_L
DA8
+LINE1_VREFO_L
24 AUD_HP1_JACK_R
24 LINE1_R
BAT54ATB_SOT-523-3
MAIN@
24 SLEEVE
CA32 1 2 10U_0603_10V6M
CA33 1 2 10U_0603_10V6M
LINE1-L_C
LINE1-L_R
RA28 1 2 1K_0402_5%
RA29 1 2 4.7K_0402_5%
RA32 1 2 1K_0402_5%
RA33 1 2 4.7K_0402_5%
RA27 1 2 10_0402_1%
RA31 1 2 10_0402_1%
AUD_HP1_JACK_L1
AUD_HP1_JACK_R1
LA1 1 ESD_M@2 BLM15PX330SN1D_2P
LA2 1 ESD_M@2 BLM15PX330SN1D_2P
LA3 1 ESD_M@2 BLM15PX330SN1D_2P
LA4 1 ESD_M@2 BLM15PX330SN1D_2P
RING2_R
HPOUT_L
HPOUT_R
SLEEVE_R
Layout Note:
Close to UA1

Main Func = Audio Jack

EMI@, @ESD@, ESD@


Universal Jack
(Global Headset Jack + mic phone in + line in support)
CLOSE TO JHP1
SLEEVE_R
HPOUT_L
24 JACK_PLUG
JACK_PLUG
JACK_PLUG_DET
HPOUT_R
RING2_R
JACK_PLUG_DET
10 mils
@
0_0402_5%
RA40
change to shortpad 11/23
AUD_AGND
RA34 10K_0402_5% @
RA30 10K_0402_5% @
CA34 100P_0402_50V8J EMI@
CA35 100P_0402_50V8J EMI@
CA42 680P_0402_50V8J ESD@
CA41 680P_0402_50V8J ESD@
DA5 AZ5123-02S.R7G_SOT23-3 ESD_M@
CA36 680P_0402_50V8J @ESD@
CA37 680P_0402_50V8J @ESD@
JHP1
#3 M/G
#1 L
#5
#6 AGND
#2 R
#4 G/M
GND
SINGA_2SJ3095-136111F~D
CONN@
DA4 L03ESDL5V0CC3-2_SOT23-3 ESD_M@
DA7 L03ESDL5V0CC3-2_SOT23-3 ESD_M@

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title Audio Jack

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Size	Document Number	Rev
	LA-F611P	0.3

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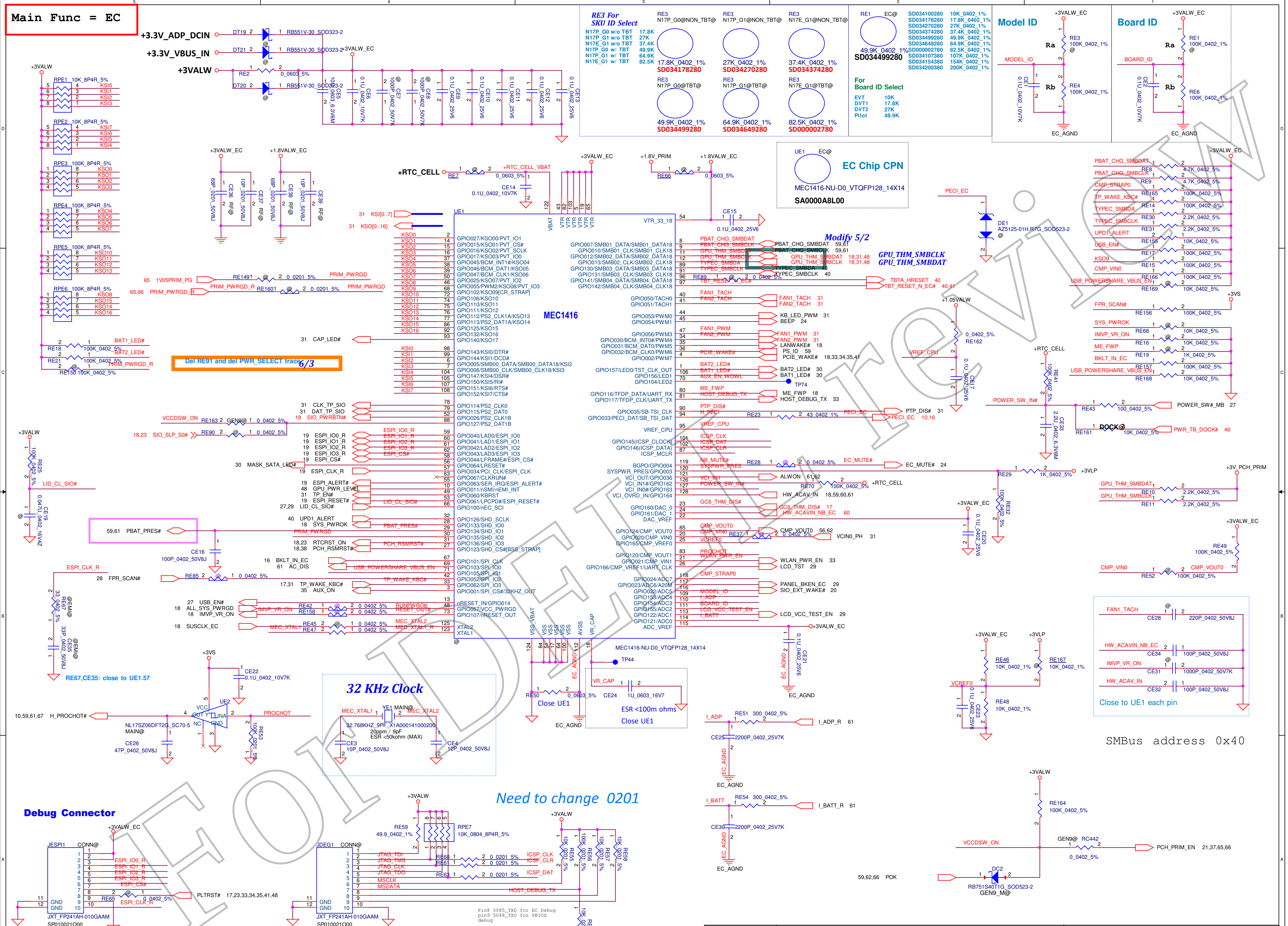
Main Func = EC
+3.3V_ADP_DCIN
+3.3V_VBUS_IN
+3VALW
RE3 For SKU ID Select
N17P_G0 w/o TBT 17.8K
N17P_G1 w/o TBT 27K
N17E_G1 w/o TBT 37.4K
N17P_G0 w/ TBT 49.9K
N17P_G1 w/ TBT 64.9K
N17E_G1 w/ TBT 82.5K
17.8K_0402_1% SD034178280
27K_0402_1% SD034270280
37.4K_0402_1% SD034374280
49.9K_0402_1% SD034499280
64.9K_0402_1% SD034649280
82.5K_0402_1% SD000002780
SD034100280 10K_0402_1%
SD034178280 17.8K_0402_1%
SD034270280 27K_0402_1%
SD034374280 37.4K_0402_1%
SD034499280 49.9K_0402_1%
SD034649280 64.9K_0402_1%
SD000002780 82.5K_0402_1%
SD034107380 107K_0402_1%
SD034154380 154K_0402_1%
SD034200380 200K_0402_1%
For Board ID Select
EVT 10K
DVT1 17.8K
DVT2 27K
Pilot 49.9K
Model ID
Board ID
MODEL_ID
BOARD_ID
EC Chip CPN
MEC1416-NU-D0_VTQFP128_14X14
SA0000A8L00
MEC1416
Modify 5/2
GPU_THM_SMBCLK
GPU_THM_SMBDAT
Del RE91 and del PWR_SELECT trace 6/3
RE67,CE35: close to UE1.57
32 KHz Clock
32.768KHZ_9PF_X1A000141000200
20ppm / 9pF
ESR <50kohm (MAX)
Close UE1
ESR <100m ohms
Close UE1
Close to UE1 each pin
SMBus address 0x40
Need to change 0201
Debug Connector
JXT_FP241AH-010GAAM
SP010021O00
Pin8 5085_TXD for EC Debug
pin9 5048_TXD for SBIOS
debug
PCH_PRIM_EN 21,37,65,66
POWER_SW#_MB 27
PWR_TB_DOCK# 40
EC_MUTE# 24
VCIN0_PH 31

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

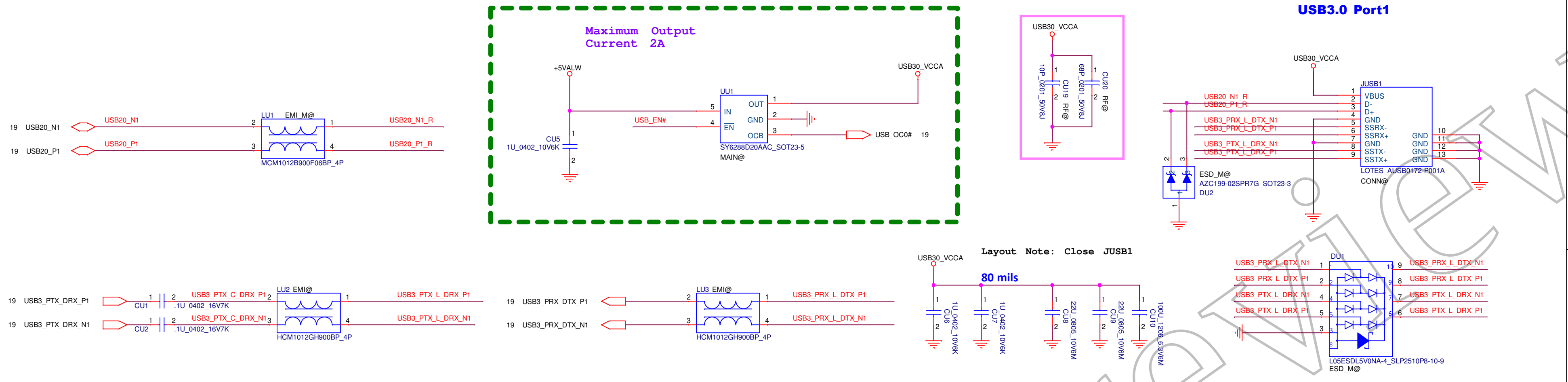
Title: EC MEC1416

Size Document Number: LA-F611P

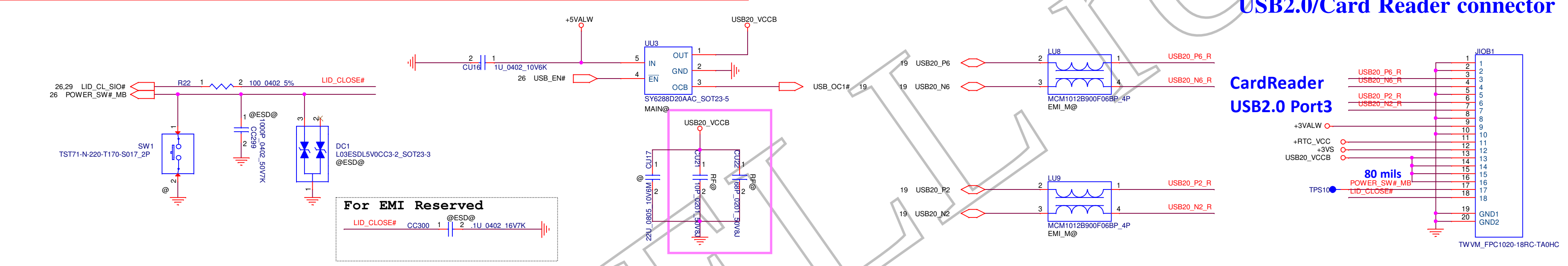
Rev: 0.3

Date: Thursday, March 22, 2018

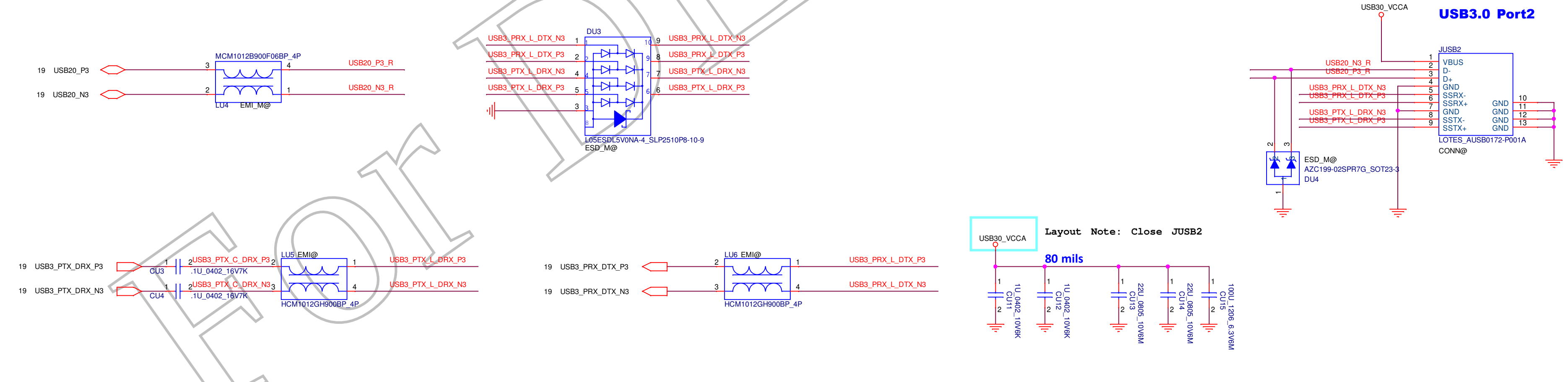
Main Func = USB3.0 Port1


Maximum Output Current 2A
+5VALW
USB30_VCCA
UU1
IN
EN
OUT
GND
OCB
SY6288D20AAC_SOT23-5
MAIN@
USB_EN#
USB_OC0# 19
CU5
1U_0402_10V6K
19 USB20_N1
19 USB20_P1
USB20_N1
USB20_P1
LU1 EMI_M@
MCM1012B900F06BP_4P
USB20_N1_R
USB20_P1_R
CU19 RF@
10P_0201_50V8J
CU20 RF@
68P_0201_50V8J
USB3.0 Port1
JUSB1
VBUS
D-
D+
GND
SSRX-
SSRX+
GND
SSTX-
SSTX+
LOTES_AUSB0172-P001A
CONN@
USB3_PRX_L_DTX_N1
USB3_PRX_L_DTX_P1
USB3_PTX_L_DRX_N1
USB3_PTX_L_DRX_P1
ESD_M@
AZC199-02SPR7G_SOT23-3
DU2
19 USB3_PTX_DRX_P1
19 USB3_PTX_DRX_N1
CU1
CU2
.1U_0402_16V7K
USB3_PTX_C_DRX_P1
USB3_PTX_C_DRX_N1
LU2 EMI@
HCM1012GH900BP_4P
19 USB3_PRX_DTX_P1
19 USB3_PRX_DTX_N1
LU3 EMI@
USB3_PRX_L_DTX_P1
USB3_PRX_L_DTX_N1
Layout Note: Close JUSB1
80 mils
CU6
CU7
1U_0402_10V6K
CU8
CU9
22U_0805_10V6M
CU10
100U_1206_6.3V6M
DU1
L05ESDL5V0NA-4_SLP2510P8-10-9
ESD_M@

Main Func = USB2.0 Port2 + Card Reader+Power BTN on IO/B


USB2.0/Card Reader connector
+5VALW
USB20_VCCB
CU16
1U_0402_10V6K
26 USB_EN#
UU3
IN
EN
OUT
GND
OCB
SY6288D20AAC_SOT23-5
MAIN@
USB_OC1# 19
26,29 LID_CL_SIO#
26 POWER_SW#_MB
R22
100_0402_5%
LID_CLOSE#
@ESD@
CC299
1000P_0402_50V7K
SW1
TST71-N-220-T170-S017_2P
DC1
L03ESDL5V0CC3-2_SOT23-3
@ESD@
For EMI Reserved
LID_CLOSE#
CC300
@ESD@
.1U_0402_16V7K
CU17
22U_0805_10V6M
CU21 RF@
10P_0201_50V8J
CU22 RF@
68P_0201_50V8J
19 USB20_P6
19 USB20_N6
LU8
MCM1012B900F06BP_4P
EMI_M@
USB20_P6_R
USB20_N6_R
19 USB20_P2
19 USB20_N2
LU9
USB20_P2_R
USB20_N2_R
CardReader
USB2.0 Port3
+3VALW
+RTC_VCC
+3VS
USB20_VCCB
80 mils
POWER_SW#_MB
LID_CLOSE#
TPS10
JIOB1
GND1
GND2
TWVM_FPC1020-18RC-TA0HC

Main Func = USB3.0 Port2


19 USB20_P3
19 USB20_N3
MCM1012B900F06BP_4P
LU4 EMI_M@
USB20_P3_R
USB20_N3_R
DU3
L05ESDL5V0NA-4_SLP2510P8-10-9
ESD_M@
USB3_PRX_L_DTX_N3
USB3_PRX_L_DTX_P3
USB3_PTX_L_DRX_N3
USB3_PTX_L_DRX_P3
USB30_VCCA
USB3.0 Port2
JUSB2
VBUS
D-
D+
GND
SSRX-
SSRX+
GND
SSTX-
SSTX+
LOTES_AUSB0172-P001A
CONN@
ESD_M@
AZC199-02SPR7G_SOT23-3
DU4
19 USB3_PTX_DRX_P3
19 USB3_PTX_DRX_N3
CU3
CU4
.1U_0402_16V7K
USB3_PTX_C_DRX_P3
USB3_PTX_C_DRX_N3
LU5 EMI@
HCM1012GH900BP_4P
19 USB3_PRX_DTX_P3
19 USB3_PRX_DTX_N3
LU6 EMI@
USB3_PRX_L_DTX_P3
USB3_PRX_L_DTX_N3
Layout Note: Close JUSB2
80 mils
CU11
CU12
1U_0402_10V6K
CU13
CU14
22U_0805_10V6M
CU15
100U_1206_6.3V6M

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: USB3.0 & I/O
				Size / Document Number: LA-F611P / Rev 0.3
				Date: Thursday, March 22, 2018 / Sheet 27 of 78

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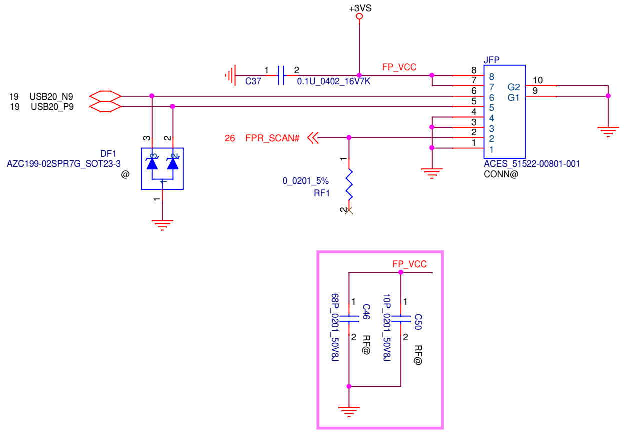
Main Func = Finger Printer


+3VS
C37
1
2
0.1U_0402_16V7K
FP_VCC
JFP
8
7
6
5
4
3
2
1
G2
G1
10
9
ACES_51522-00801-001
CONN@
19 USB20_N9
19 USB20_P9
3
2
1
DF1
AZC199-02SPR7G_SOT23-3
@
26 FPR_SCAN#
0_0201_5%
RF1
FP_VCC
C46
68P_0201_50V8J
RF@
C50
10P_0201_50V8J
RF@

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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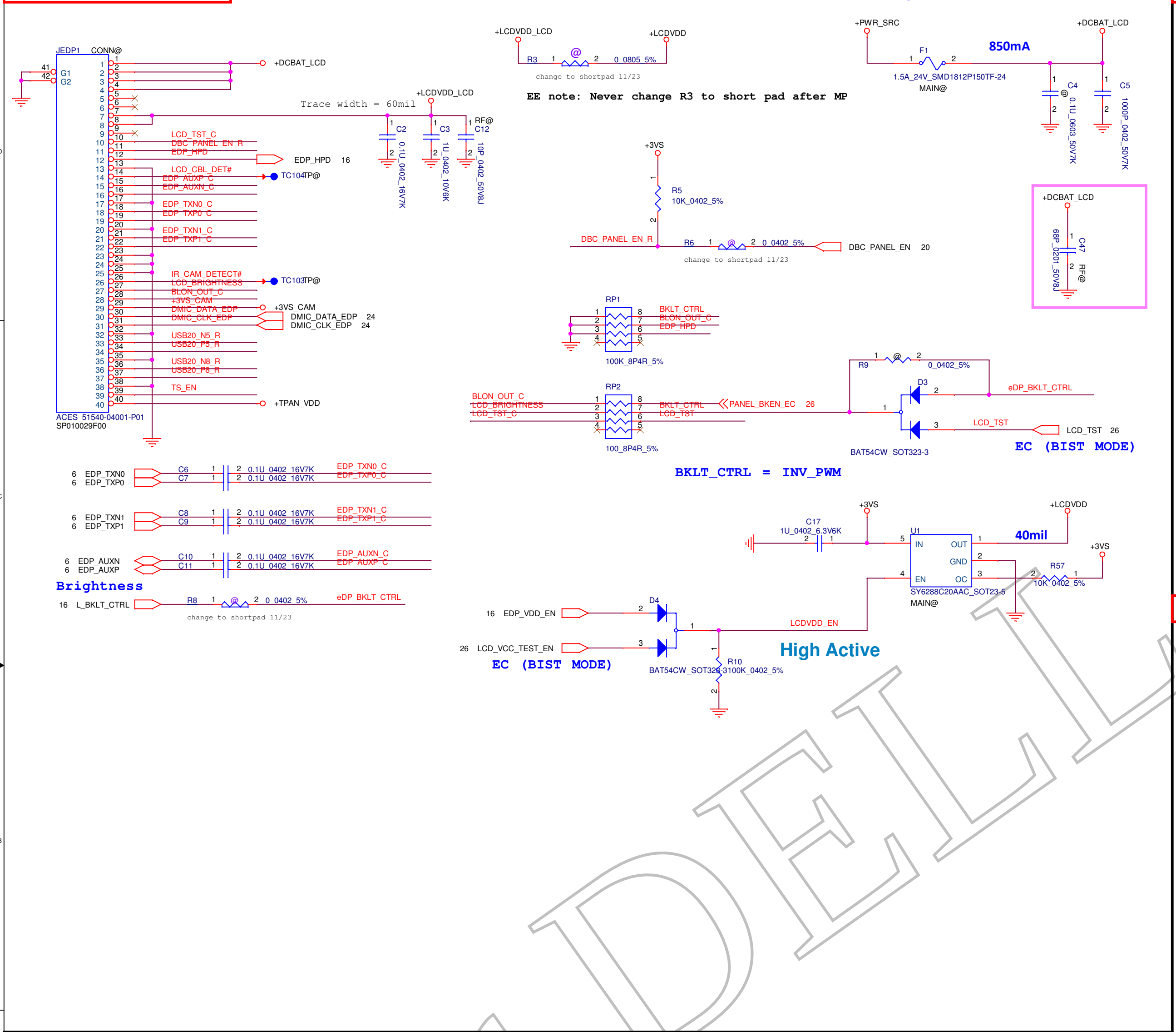
Compal Electronics, Inc.

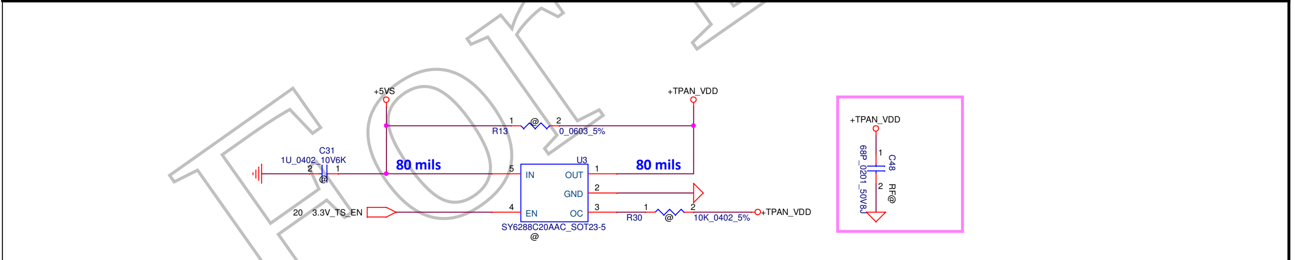
Title
Finger Print

Size	Document Number	Rev
	LA-F611P	0.3

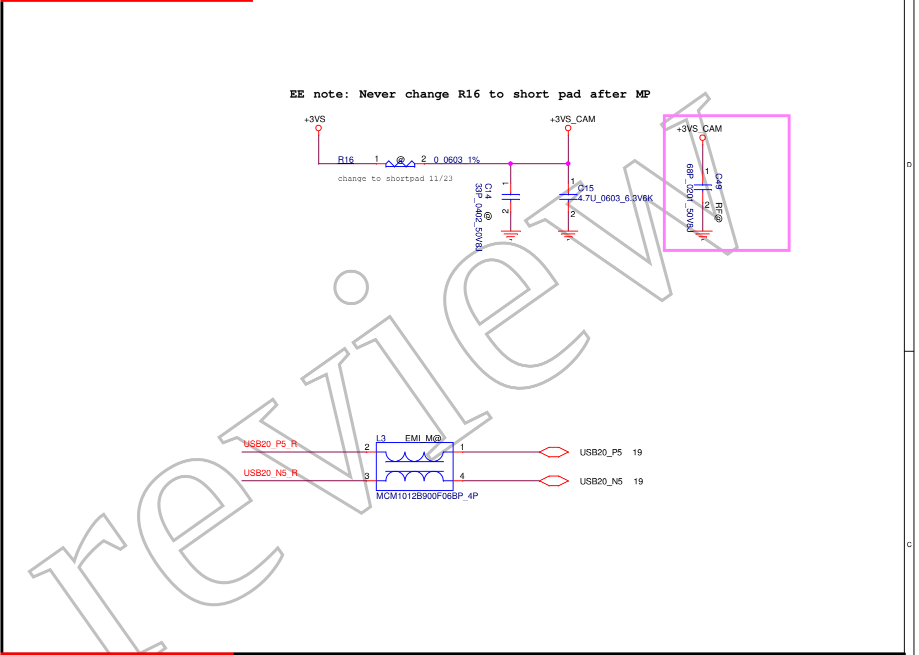
Date: Thursday, March 22, 2018 Sheet 28 of 78

Main Func = LCD

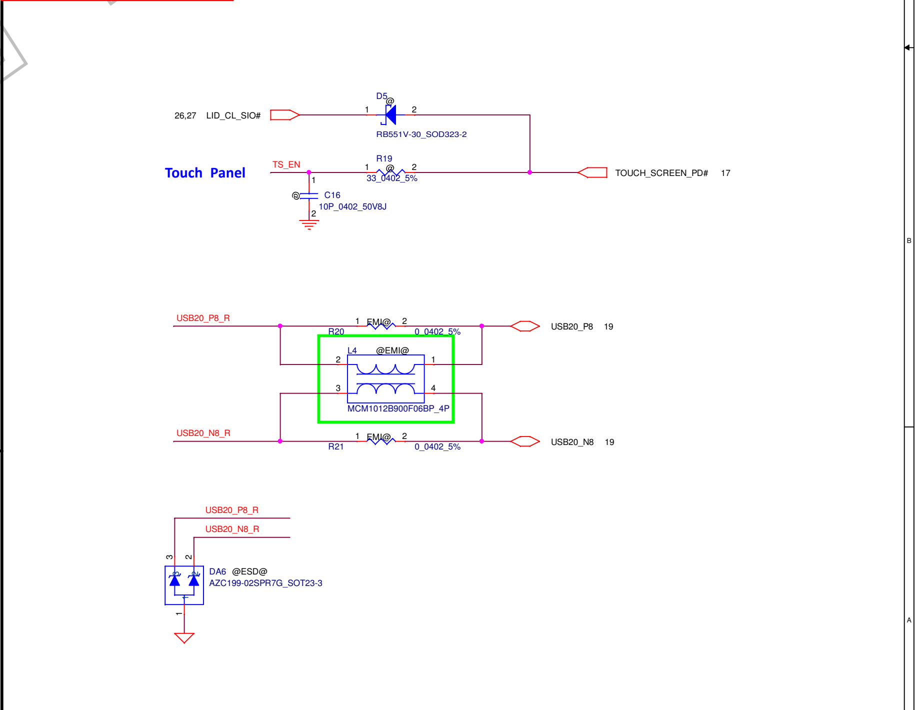

INVERTER POWER
JEDP1 CONN@
G1
G2
41
42
+DCBAT_LCD
+LCDVDD_LCD
Trace width = 60mil
C2 0.1U_0402_16V7K
C3 1U_0402_10V6K
RF@ C12 10P_0402_50V8J
LCD_TST_C
DBC_PANEL_EN_R
EDP_HPD
EDP_HPD 16
LCD_CBL_DET#
EDP_AUXP_C
EDP_AUXN_C
TC104TP@
EDP_TXN0_C
EDP_TXP0_C
EDP_TXN1_C
EDP_TXP1_C
IR_CAM_DETECT#
LCD_BRIGHTNESS
TC103TP@
BLON_OUT_C
+3VS_CAM
DMIC_DATA_EDP
DMIC_CLK_EDP
+3VS_CAM
DMIC_DATA_EDP 24
DMIC_CLK_EDP 24
USB20_N5_R
USB20_P5_R
USB20_N8_R
USB20_P8_R
TS_EN
+TPAN_VDD
ACES_51540-04001-P01
SP010029F00
6 EDP_TXN0
6 EDP_TXP0
C6 0.1U_0402_16V7K
C7 0.1U_0402_16V7K
6 EDP_TXN1
6 EDP_TXP1
C8 0.1U_0402_16V7K
C9 0.1U_0402_16V7K
6 EDP_AUXN
6 EDP_AUXP
C10 0.1U_0402_16V7K
C11 0.1U_0402_16V7K
EDP_AUXN_C
EDP_AUXP_C
Brightness
16 L_BKLT_CTRL
R8 @ 0_0402_5%
eDP_BKLT_CTRL
change to shortpad 11/23
+LCDVDD_LCD
+LCDVDD
R3 @ 0_0805_5%
change to shortpad 11/23
EE note: Never change R3 to short pad after MP
+PWR_SRC
F1
1.5A_24V_SMD1812P150TF-24
MAIN@
850mA
+DCBAT_LCD
C4 @ 0.1U_0603_50V7K
C5 1000P_0402_50V7K
+3VS
R5 10K_0402_5%
DBC_PANEL_EN_R
R6 @ 0_0402_5%
change to shortpad 11/23
DBC_PANEL_EN 20
+DCBAT_LCD
C47 68P_0201_50V8J RF@
RP1
BKLT_CTRL
BLON_OUT_C
EDP_HPD
100K_8P4R_5%
RP2
BLON_OUT_C
LCD_BRIGHTNESS
LCD_TST_C
BKLT_CTRL
LCD_TST
PANEL_BKEN_EC 26
100_8P4R_5%
R9 @ 0_0402_5%
D3
eDP_BKLT_CTRL
LCD_TST
LCD_TST 26
BAT54CW_SOT323-3
EC (BIST MODE)
BKLT_CTRL = INV_PWM
+3VS
C17 1U_0402_6.3V6K
U1
IN
OUT
GND
EN
OC
SY6288C20AAC_SOT23-5
MAIN@
+LCDVDD
40mil
+3VS
R57 10K_0402_5%
16 EDP_VDD_EN
26 LCD_VCC_TEST_EN
EC (BIST MODE)
D4
BAT54CW_SOT323-3
LCDVDD_EN
R10 100K_0402_5%
High Active


+5VS
+TPAN_VDD
R13 @ 0_0603_5%
C31 1U_0402_10V6K @
80 mils
U3
IN
OUT
GND
EN
OC
80 mils
20 3.3V_TS_EN
SY6288C20AAC_SOT23-5
@
R30 @ 10K_0402_5%
+TPAN_VDD
+TPAN_VDD
C48 68P_0201_50V8J RF@

Main Func = CAM


EE note: Never change R16 to short pad after MP
+3VS
+3VS_CAM
R16 @ 0_0603_1%
change to shortpad 11/23
C14 @ 33P_0402_50V8J
C15 4.7U_0603_6.3V6K
+3VS_CAM
C49 68P_0201_50V8J RF@
USB20_P5_R
USB20_N5_R
L3 EMI_M@
MCM1012B900F06BP_4P
USB20_P5 19
USB20_N5 19

Main Func = TS


26,27 LID_CL_SIO#
D5 @
RB551V-30_SOD323-2
Touch Panel
TS_EN
R19 @ 33_0402_5%
C16 @ 10P_0402_50V8J
TOUCH_SCREEN_PD# 17
USB20_P8_R
R20 EMI@ 0_0402_5%
USB20_P8 19
L4 @EMI@
MCM1012B900F06BP_4P
USB20_N8_R
R21 EMI@ 0_0402_5%
USB20_N8 19
USB20_P8_R
USB20_N8_R
DA6 @ESD@
AZC199-02SPR7G_SOT23-3

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title
LCD/Camera/Mic

Size
Document Number
LA-F611P
Rev
0.3

Date: Thursday, March 22, 2018
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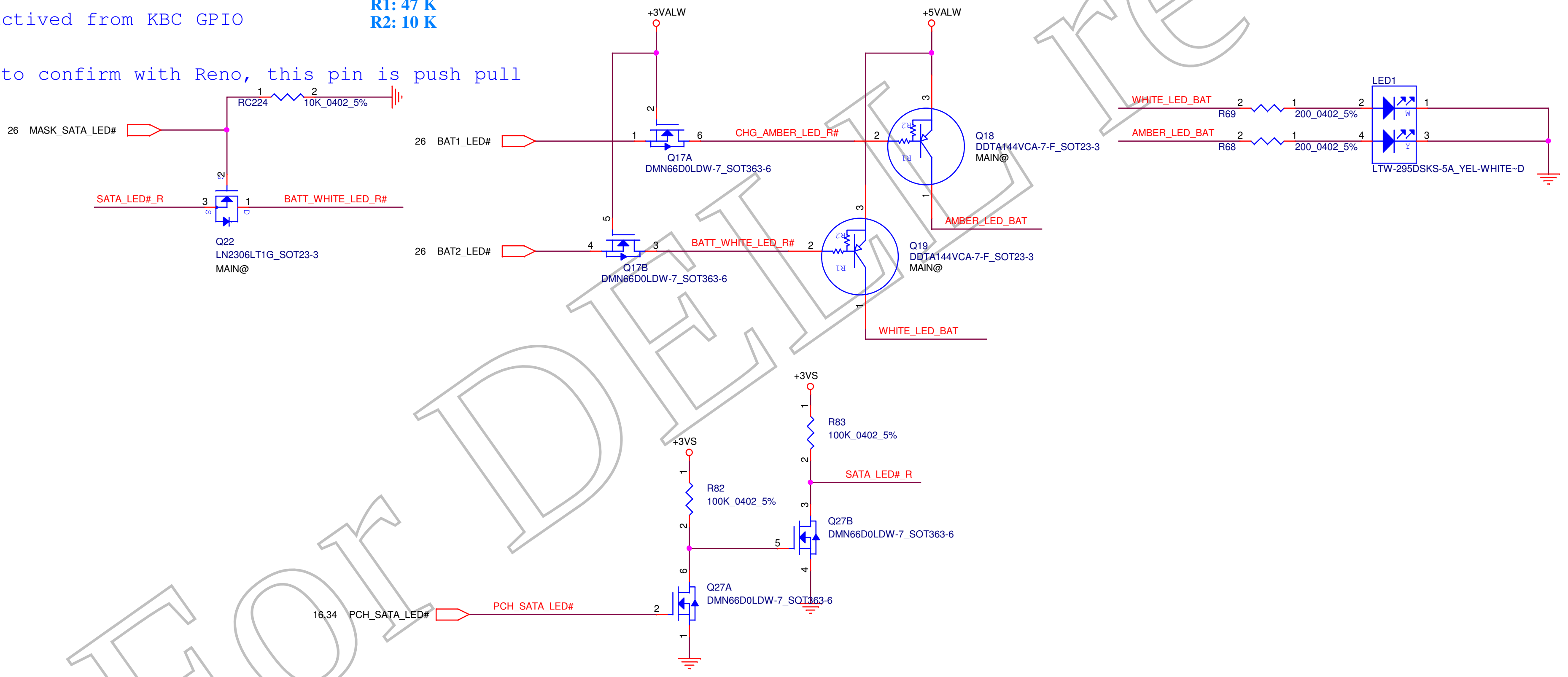
Main Func = Battery LED

BJT
R1: 47 K
R2: 10 K

Low actived from KBC GPIO

Need to confirm with Reno, this pin is push pull


+3VALW
+5VALW
RC224
10K_0402_5%
1
2
26 MASK_SATA_LED#
SATA_LED#_R
BATT_WHITE_LED_R#
Q22
LN2306LT1G_SOT23-3
MAIN@
26 BAT1_LED#
26 BAT2_LED#
Q17A
DMN66D0LDW-7_SOT363-6
Q17B
DMN66D0LDW-7_SOT363-6
CHG_AMBER_LED_R#
BATT_WHITE_LED_R#
Q18
DDTA144VCA-7-F_SOT23-3
MAIN@
Q19
DDTA144VCA-7-F_SOT23-3
MAIN@
R1
R2
AMBER_LED_BAT
WHITE_LED_BAT
WHITE_LED_BAT
AMBER_LED_BAT
R69
200_0402_5%
R68
200_0402_5%
LED1
W
Y
LTW-295DSKS-5A_YEL-WHITE~D
+3VS
R83
100K_0402_5%
SATA_LED#_R
Q27B
DMN66D0LDW-7_SOT363-6
+3VS
R82
100K_0402_5%
Q27A
DMN66D0LDW-7_SOT363-6
16,34 PCH_SATA_LED#
PCH_SATA_LED#

Security Classification | Compal Secret Data
Issued Date 2016/01/06 | Deciphered Date 2017/01/06

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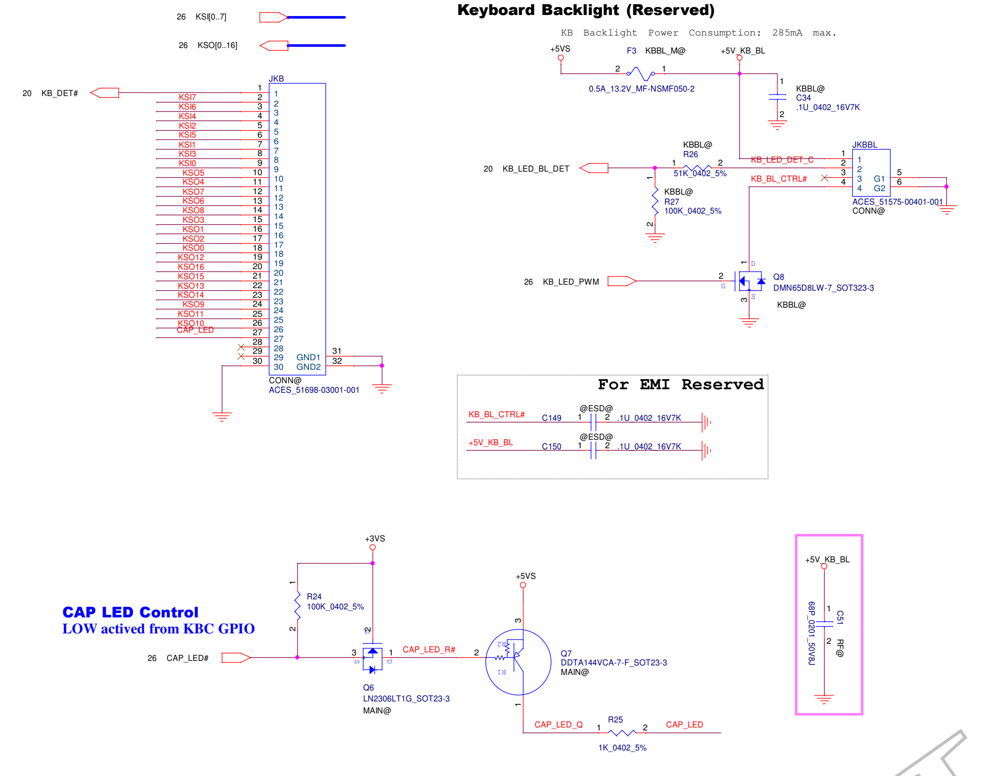
Compal Electronics, Inc.

Title ***Power Button/LED***

Size Document Number ***LA-F611P*** Rev 0.3

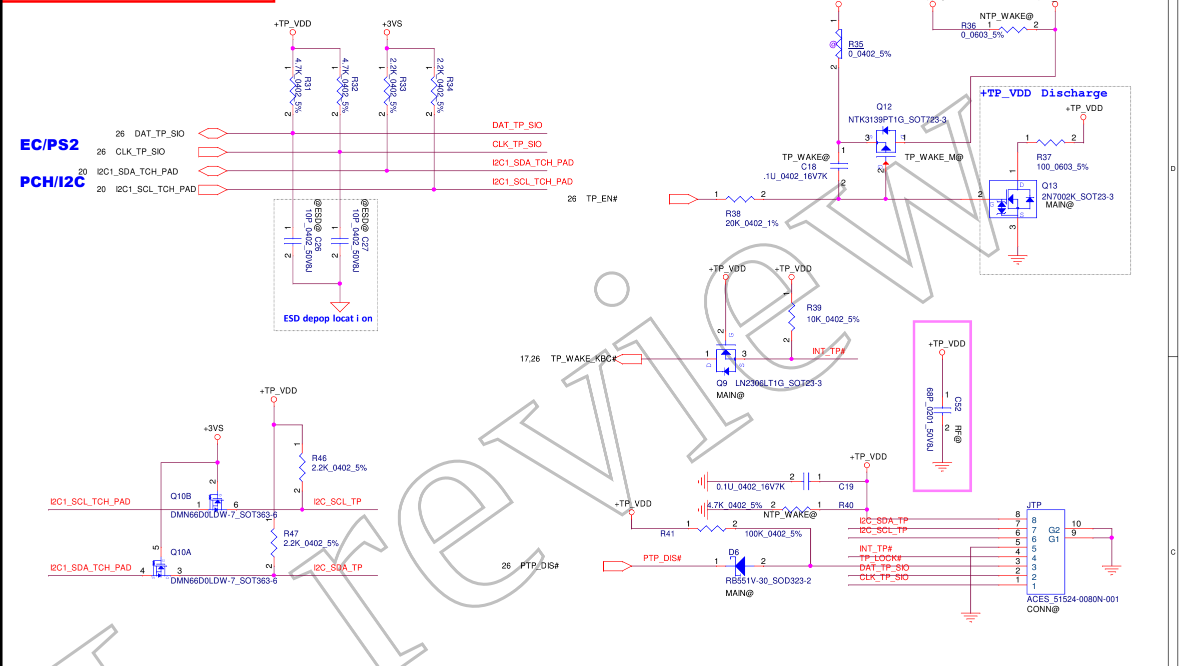
Date: Thursday, March 22, 2018 Sheet 30 of 78

Main Func = KB



Keyboard Backlight (Reserved)
KB Backlight Power Consumption: 285mA max.
26 KSI[0..7]
26 KSO[0..16]
20 KB_DET#
JKB
KSI7 KSI6 KSI4 KSI2 KSI5 KSI1 KSI3 KSI0
KSO5 KSO4 KSO7 KSO6 KSO8 KSO3 KSO1 KSO2 KSO0 KSO12 KSO16 KSO15 KSO13 KSO14 KSO9 KSO11 KSO10
CAP_LED
GND1 GND2
CONN@
ACES_51698-03001-001
+5VS
F3 KBBL_M@
0.5A_13.2V_MF-NSMF050-2
+5V_KB_BL
KBBL@ C34 .1U_0402_16V7K
KBBL@ R26 51K_0402_5%
20 KB_LED_BL_DET
KBBL@ R27 100K_0402_5%
KB_LED_DET_C
KB_BL_CTRL#
JKBBL
ACES_51575-00401-001
CONN@
26 KB_LED_PWM
Q8 DMN65D8LW-7_SOT323-3
KBBL@
For EMI Reserved
KB_BL_CTRL# C149 @ESD@ .1U_0402_16V7K
+5V_KB_BL C150 @ESD@ .1U_0402_16V7K
+3VS
R24 100K_0402_5%
CAP LED Control
LOW actived from KBC GPIO
26 CAP_LED#
Q6 LN2306LT1G_SOT23-3
MAIN@
CAP_LED_R#
+5VS
Q7 DDTA144VCA-7-F_SOT23-3
MAIN@
CAP_LED_Q
R25 1K_0402_5%
CAP_LED
+5V_KB_BL
C51 6.8P_0201_50V8J RF@

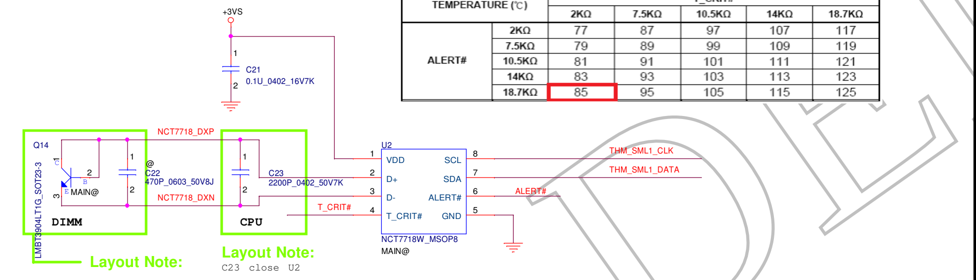
Main Func = TPAD



+TP_VDD
+3VS
R31 4.7K_0402_5%
R32 4.7K_0402_5%
R33 2.2K_0402_5%
R34 2.2K_0402_5%
EC/PS2
PCH/I2C
26 DAT_TP_SIO
26 CLK_TP_SIO
20 I2C1_SDA_TCH_PAD
20 I2C1_SCL_TCH_PAD
DAT_TP_SIO
CLK_TP_SIO
I2C1_SDA_TCH_PAD
I2C1_SCL_TCH_PAD
C26 @ESD@ 10P_0402_50V8J
C27 @ESD@ 10P_0402_50V8J
ESD depop locat i on
+3VALW
R35 0_0402_5%
+3VS
NTP_WAKE@
R36 0_0603_5%
+TP_VDD
Q12 NTK3139PT1G_SOT723-3
TP_WAKE@
C18 .1U_0402_16V7K
TP_WAKE_M@
+TP_VDD Discharge
R37 100_0603_5%
Q13 2N7002K_SOT23-3
MAIN@
26 TP_EN#
R38 20K_0402_1%
+TP_VDD
R39 10K_0402_5%
17,26 TP_WAKE_KBC#
Q9 LN2306LT1G_SOT23-3
MAIN@
INT_TP#
+TP_VDD
C52 68P_0201_50V8J RF@
+TP_VDD
+3VS
R46 2.2K_0402_5%
I2C1_SCL_TCH_PAD
Q10B DMN66D0LDW-7_SOT363-6
I2C_SCL_TP
R47 2.2K_0402_5%
Q10A DMN66D0LDW-7_SOT363-6
I2C1_SDA_TCH_PAD
I2C_SDA_TP
0.1U_0402_16V7K C19
+TP_VDD
4.7K_0402_5% R40 NTP_WAKE@
R41 100K_0402_5%
26 PTP_DIS#
PTP_DIS#
D6 RB551V-30_SOD323-2
MAIN@
JTP
I2C_SDA_TP
I2C_SCL_TP
INT_TP#
TP_LOCK#
DAT_TP_SIO
CLK_TP_SIO
G2 G1
ACES_51524-0080N-001
CONN@

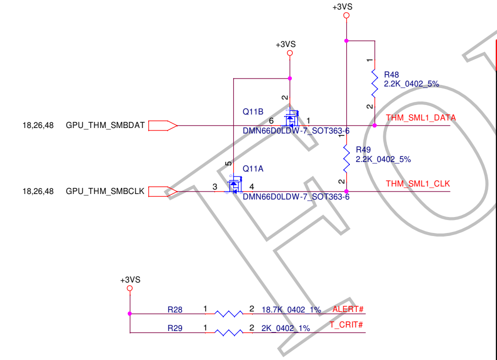
Main Func = Thermal

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



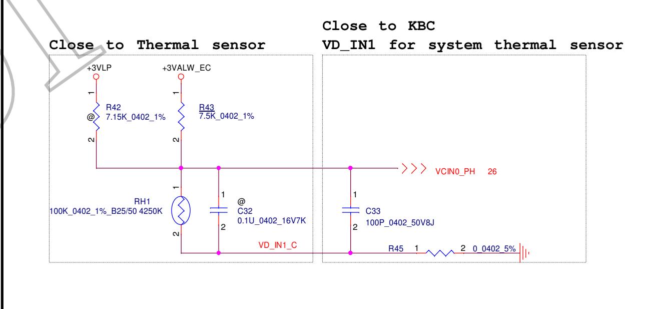
+3VS
C21 0.1U_0402_16V7K
Q14
LMBT3904LT1G_SOT23-3
MAIN@
C22 470P_0603_50V8J
DIMM
NCT7718_DXP
NCT7718_DXN
C23 2200P_0402_50V7K
CPU
T_CRIT#
U2
VDD SCL
D+ SDA
D- ALERT#
T_CRIT# GND
NCT7718W_MSOP8
MAIN@
THM_SML1_CLK
THM_SML1_DATA
ALERT#
Layout Note:
Layout Note:
C23 close U2

DXN and DXP routing width and spacing is 10 mil / 10 mil.



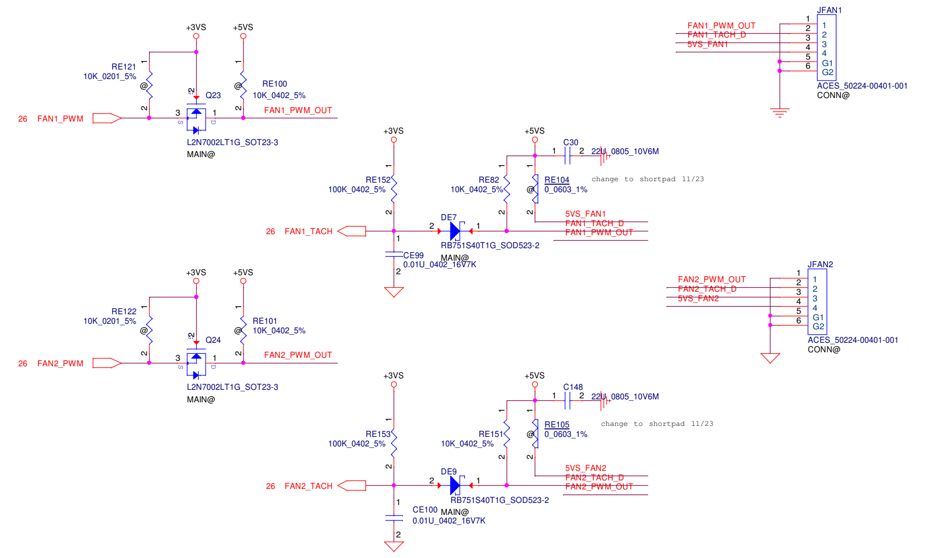
+3VS
+3VS
R48 2.2K_0402_5%
Q11B DMN66D0LDW-7_SOT363-6
18,26,48 GPU_THM_SMBDAT
THM_SML1_DATA
R49 2.2K_0402_5%
Q11A DMN66D0LDW-7_SOT363-6
18,26,48 GPU_THM_SMBCLK
THM_SML1_CLK
+3VS
R28 18.7K_0402_1%
ALERT#
R29 2K_0402_1%
T_CRIT#

Main Func = OTP



Close to Thermal sensor
Close to KBC
VD_IN1 for system thermal sensor
+3VLP
+3VALW_EC
R42 7.15K_0402_1%
R43 7.5K_0402_1%
RH1 100K_0402_1%_B25/50 4250K
C32 0.1U_0402_16V7K
VCIN0_PH 26
C33 100P_0402_50V8J
VD_IN1_C
R45 0_0402_5%

PWM FAN



+3VS
+5VS
RE121 10K_0201_5%
Q23
RE100 10K_0402_5%
26 FAN1_PWM
FAN1_PWM_OUT
L2N7002LT1G_SOT23-3
MAIN@
FAN1_PWM_OUT
FAN1_TACH_D
5VS_FAN1
JFAN1
ACES_50224-00401-001
CONN@
+3VS
+5VS
C30 22U_0805_10V6M
change to shortpad 11/23
RE152 100K_0402_5%
RE82 10K_0402_5%
RE104 0_0603_1%
26 FAN1_TACH
DE7 RB751S40T1G_SOD523-2
MAIN@
CE99 0.01U_0402_16V7K
5VS_FAN1
FAN1_TACH_D
FAN1_PWM_OUT
+3VS
+5VS
RE122 10K_0201_5%
Q24
RE101 10K_0402_5%
26 FAN2_PWM
FAN2_PWM_OUT
L2N7002LT1G_SOT23-3
MAIN@
FAN2_PWM_OUT
FAN2_TACH_D
5VS_FAN2
JFAN2
ACES_50224-00401-001
CONN@
+3VS
+5VS
C148 22U_0805_10V6M
change to shortpad 11/23
RE153 100K_0402_5%
RE151 10K_0402_5%
RE105 0_0603_1%
26 FAN2_TACH
DE9 RB751S40T1G_SOD523-2
MAIN@
CE100 0.01U_0402_16V7K
5VS_FAN2
FAN2_TACH_D
FAN2_PWM_OUT

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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: *KB/KBBL/TP/Thermal/FAN*

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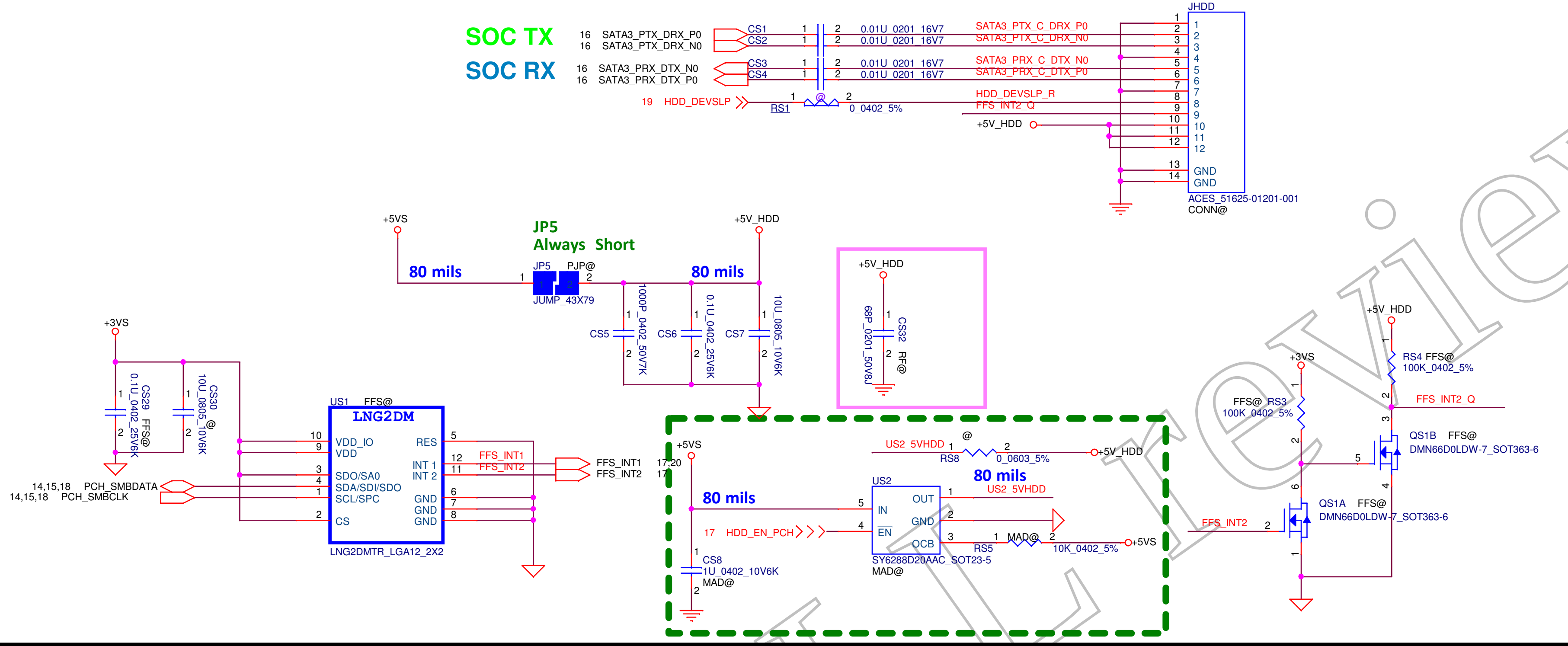
Main Func = HDD&FFS



SOC TX
SOC RX
16 SATA3_PTX_DRX_P0
16 SATA3_PTX_DRX_N0
16 SATA3_PRX_DTX_N0
16 SATA3_PRX_DTX_P0
CS1
CS2
CS3
CS4
0.01U_0201_16V7
SATA3_PTX_C_DRX_P0
SATA3_PTX_C_DRX_N0
SATA3_PRX_C_DTX_N0
SATA3_PRX_C_DTX_P0
19 HDD_DEVSLP
RS1
0_0402_5%
HDD_DEVSLP_R
FFS_INT2_Q
+5V_HDD
JHDD
GND
ACES_51625-01201-001
CONN@
+5VS
JP5
Always Short
80 mils
JP5 PJP@
JUMP_43X79
+5V_HDD
CS5
CS6
CS7
1000P_0402_50V7K
0.1U_0402_25V6K
10U_0805_10V6K
CS32
68P_0201_50V8J
RF@
+3VS
CS29
0.1U_0402_25V6K
FFS@
CS30
10U_0805_10V6K
@
US1 FFS@
LNG2DM
VDD_IO
VDD
SDO/SA0
SDA/SDI/SDO
SCL/SPC
CS
RES
INT 1
INT 2
GND
LNG2DMTR_LGA12_2X2
14,15,18 PCH_SMBDATA
14,15,18 PCH_SMBCLK
FFS_INT1
FFS_INT2
17,20
17
US2_5VHDD
RS8
0_0603_5%
US2
IN
EN
OUT
OCB
US2_5VHDD
17 HDD_EN_PCH
CS8
1U_0402_10V6K
MAD@
RS5
10K_0402_5%
SY6288D20AAC_SOT23-5
FFS@ RS3
100K_0402_5%
RS4 FFS@
100K_0402_5%
FFS_INT2_Q
QS1B FFS@
DMN66D0LDW-7_SOT363-6
QS1A FFS@
DMN66D0LDW-7_SOT363-6
FFS_INT2

CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title *HDD/FFS*

Size Document Number *LA-F611P* Rev 0.3

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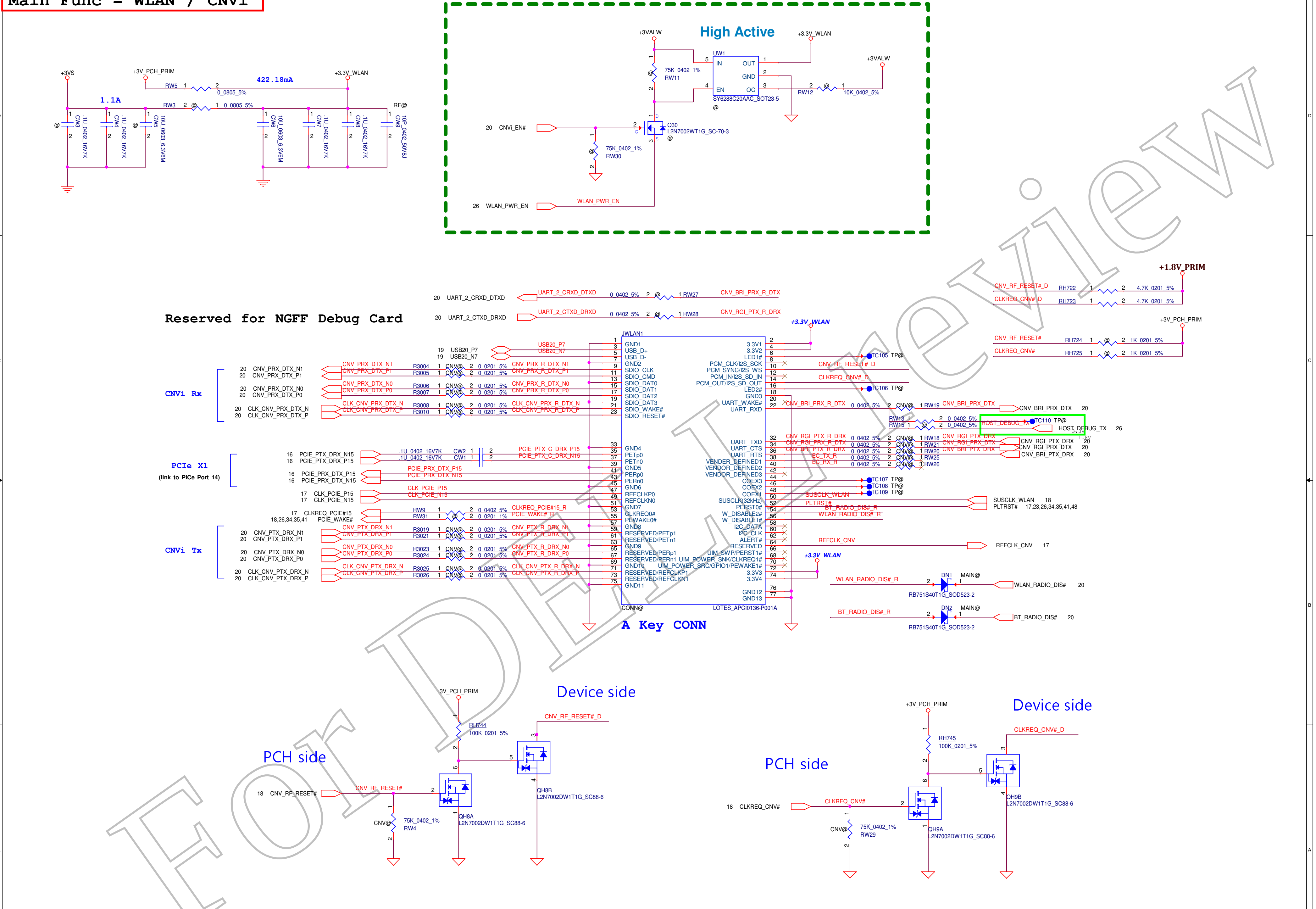
Main Func = WLAN / CNVi


High Active
+3VALW
+3.3V_WLAN
UW1
IN
OUT
GND
EN
OC
SY6288C20AAC_SOT23-5
75K_0402_1%
RW11
RW12
10K_0402_5%
20 CNVi_EN#
Q30
L2N7002WT1G_SC-70-3
75K_0402_1%
RW30
26 WLAN_PWR_EN
WLAN_PWR_EN
+3VS
+3V_PCH_PRIM
RW5
0_0805_5%
422.18mA
1.1A
RW3
0_0805_5%
RF@
CW3 .1U_0402_16V7K
CW4 .1U_0402_16V7K
CW5 10U_0603_6.3V6M
CW6 10U_0603_6.3V6M
CW7 .1U_0402_16V7K
CW8 .1U_0402_16V7K
CW9 10P_0402_50V8J
Reserved for NGFF Debug Card
20 UART_2_CRXD_DTXD
20 UART_2_CTXD_DRXD
RW27
RW28
CNV_BRI_PRX_R_DTX
CNV_RGI_PTX_R_DRX
+1.8V_PRIM
CNV_RF_RESET#_D
CLKREQ_CNV#_D
RH722 4.7K_0201_5%
RH723 4.7K_0201_5%
CNV_RF_RESET#
CLKREQ_CNV#
RH724 1K_0201_5%
RH725 1K_0201_5%
JWLAN1
CNVi Rx
PCIe X1
(link to PICe Port 14)
CNVi Tx
19 USB20_P7
19 USB20_N7
20 CNV_PRX_DTX_N1
20 CNV_PRX_DTX_P1
20 CNV_PRX_DTX_N0
20 CNV_PRX_DTX_P0
20 CLK_CNV_PRX_DTX_N
20 CLK_CNV_PRX_DTX_P
16 PCIE_PTX_DRX_N15
16 PCIE_PTX_DRX_P15
16 PCIE_PRX_DTX_P15
16 PCIE_PRX_DTX_N15
17 CLK_PCIE_P15
17 CLK_PCIE_N15
17 CLKREQ_PCIE#15
18,26,34,35,41 PCIE_WAKE#
20 CNV_PTX_DRX_N1
20 CNV_PTX_DRX_P1
20 CNV_PTX_DRX_N0
20 CNV_PTX_DRX_P0
20 CLK_CNV_PTX_DRX_N
20 CLK_CNV_PTX_DRX_P
GND1
USB_D+
USB_D-
GND2
SDIO_CLK
SDIO_CMD
SDIO_DAT0
SDIO_DAT1
SDIO_DAT2
SDIO_DAT3
SDIO_WAKE#
SDIO_RESET#
GND4
PETp0
PETn0
GND5
PERp0
PERn0
GND6
REFCLKP0
REFCLKN0
GND7
CLKREQ0#
PEWAKE0#
GND8
RESERVED/PETp1
RESERVED/PETn1
GND9
RESERVED/PERp1
RESERVED/PERn1
GND10
RESERVED/REFCLKP1
RESERVED/REFCLKN1
GND11
3.3V1
3.3V2
LED1#
PCM_CLK/I2S_SCK
PCM_SYNC/I2S_WS
PCM_IN/I2S_SD_IN
PCM_OUT/I2S_SD_OUT
LED2#
GND3
UART_WAKE#
UART_RXD
UART_TXD
UART_CTS
UART_RTS
VENDER_DEFINED1
VENDOR_DEFINED2
VENDOR_DEFINED3
COEX3
COEX2
COEX1
SUSCLK(32kHz)
PERST0#
W_DISABLE2#
W_DISABLE1#
I2C_DATA
I2C_CLK
ALERT#
RESERVED
UIM_SWP/PERST1#
UIM_POWER_SNK/CLKREQ1#
UIM_POWER_SRC/GPIO1/PEWAKE1#
3.3V3
3.3V4
GND12
GND13
CONN@
LOTES_APCI0136-P001A
A Key CONN
TC105 TP@
TC106 TP@
TC110 TP@
TC107 TP@
TC108 TP@
TC109 TP@
CNV_BRI_PRX_DTX 20
HOST_DEBUG_TX 26
CNV_RGI_PTX_DRX 20
CNV_RGI_PRX_DTX 20
CNV_BRI_PTX_DRX 20
SUSCLK_WLAN 18
PLTRST# 17,23,26,34,35,41,48
REFCLK_CNV 17
WLAN_RADIO_DIS# 20
BT_RADIO_DIS# 20
DN1
DN2
MAIN@
RB751S40T1G_SOD523-2
Device side
PCH side
18 CNV_RF_RESET#
RH744 100K_0201_5%
QH8A
QH8B
L2N7002DW1T1G_SC88-6
75K_0402_1%
RW4
18 CLKREQ_CNV#
RH745 100K_0201_5%
QH9A
QH9B
L2N7002DW1T1G_SC88-6
75K_0402_1%
RW29

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title
NGFF WLAN

Size Document Number
LA-F611P
Rev 0.3

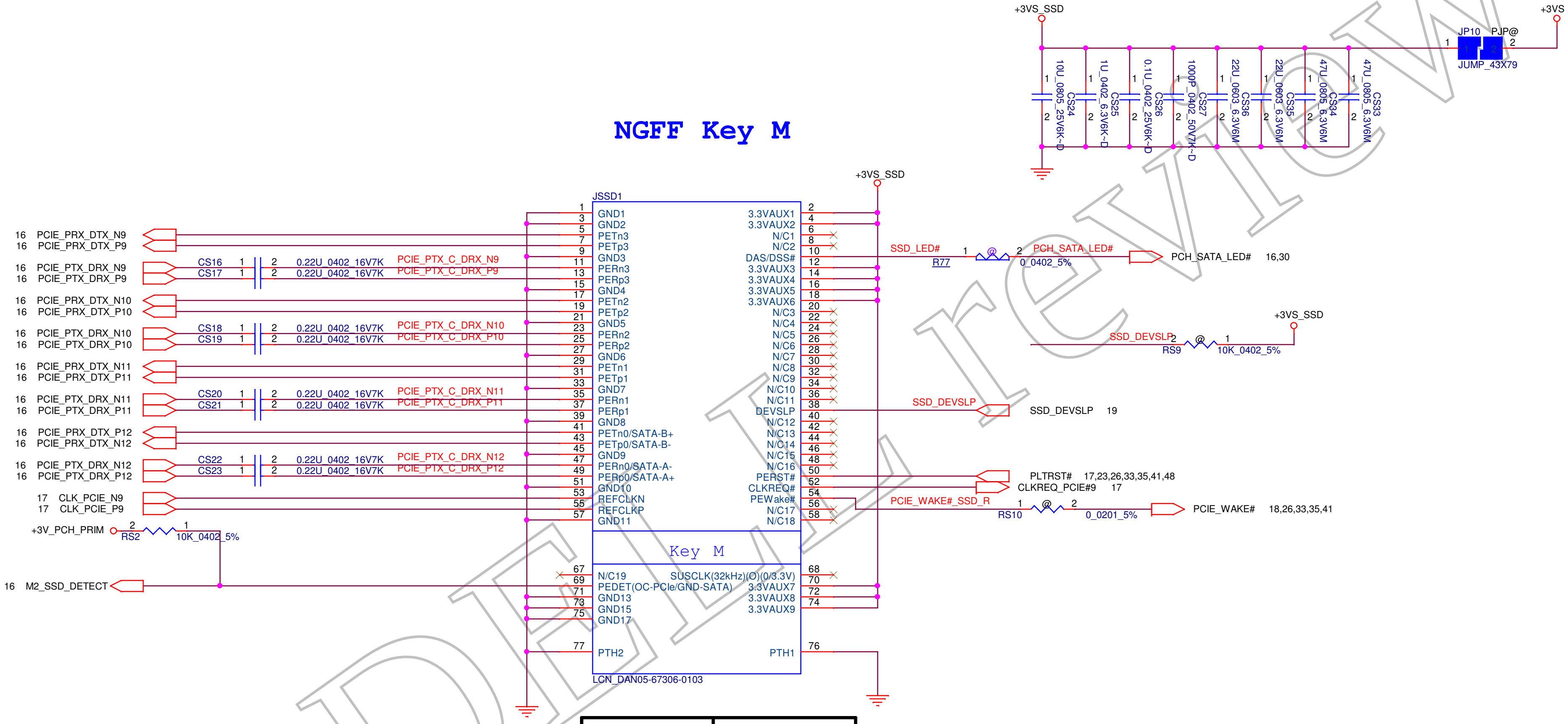
Date: Thursday, March 22, 2018 Sheet 33 of 78

Main Func = SSD

M Key CONN

Update OK

NGFF Key M


+3VS_SSD
+3VS
JP10 PJP@
JUMP_43X79
CS24 10U_0805_25V6K-D
CS25 1U_0402_6.3V6K-D
CS26 0.1U_0402_25V6K-D
CS27 1000P_0402_50V7K-D
CS36 22U_0603_6.3V6M
CS35 22U_0603_6.3V6M
CS34 47U_0805_6.3V6M
CS33 47U_0805_6.3V6M
JSSD1
GND1
GND2
PETn3
PETp3
GND3
PERn3
PERp3
GND4
PETn2
PETp2
GND5
PERn2
PERp2
GND6
PETn1
PETp1
GND7
PERn1
PERp1
GND8
PETn0/SATA-B+
PETp0/SATA-B-
GND9
PERn0/SATA-A-
PERp0/SATA-A+
GND10
REFCLKN
REFCLKP
GND11
3.3VAUX1
3.3VAUX2
N/C1
N/C2
DAS/DSS#
3.3VAUX3
3.3VAUX4
3.3VAUX5
3.3VAUX6
N/C3
N/C4
N/C5
N/C6
N/C7
N/C8
N/C9
N/C10
N/C11
DEVSLP
N/C12
N/C13
N/C14
N/C15
N/C16
PERST#
CLKREQ#
PEWake#
N/C17
N/C18
Key M
N/C19
PEDET(OC-PCIe/GND-SATA)
GND13
GND15
GND17
SUSCLK(32kHz)(O)(0/3.3V)
3.3VAUX7
3.3VAUX8
3.3VAUX9
PTH2
PTH1
LCN_DAN05-67306-0103
16 PCIE_PRX_DTX_N9
16 PCIE_PRX_DTX_P9
16 PCIE_PTX_DRX_N9
16 PCIE_PTX_DRX_P9
16 PCIE_PRX_DTX_N10
16 PCIE_PRX_DTX_P10
16 PCIE_PTX_DRX_N10
16 PCIE_PTX_DRX_P10
16 PCIE_PRX_DTX_N11
16 PCIE_PRX_DTX_P11
16 PCIE_PTX_DRX_N11
16 PCIE_PTX_DRX_P11
16 PCIE_PRX_DTX_P12
16 PCIE_PRX_DTX_N12
16 PCIE_PTX_DRX_N12
16 PCIE_PTX_DRX_P12
17 CLK_PCIE_N9
17 CLK_PCIE_P9
CS16 CS17 CS18 CS19 CS20 CS21 CS22 CS23
0.22U_0402_16V7K
PCIE_PTX_C_DRX_N9
PCIE_PTX_C_DRX_P9
PCIE_PTX_C_DRX_N10
PCIE_PTX_C_DRX_P10
PCIE_PTX_C_DRX_N11
PCIE_PTX_C_DRX_P11
PCIE_PTX_C_DRX_N12
PCIE_PTX_C_DRX_P12
+3V_PCH_PRIM
RS2 10K_0402_5%
16 M2_SSD_DETECT
SSD_LED#
R77 0_0402_5%
PCH_SATA_LED#
PCH_SATA_LED# 16,30
SSD_DEVSLP
RS9 10K_0402_5%
SSD_DEVSLP 19
PLTRST# 17,23,26,33,35,41,48
CLKREQ_PCIE#9 17
PCIE_WAKE#_SSD_R
RS10 0_0201_5%
PCIE_WAKE# 18,26,33,35,41

PEDET	Module Type
0	SATA
1	PCIE

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title

NVMe SSD

Size Document Number ***LA-F611P*** Rev 0.3

Date: Thursday, March 22, 2018 Sheet 34 of 78

Main Func = LAN

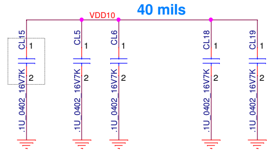
Update OK

LAN Chip (10/100/1000M & 10/100M co-layout)

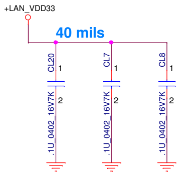
Layout:
For RTL8111H-CG
* Place CL5,CL6,CL18,CL19 close to each VDD10 pin 8, 30, 3, 22
For RTL8106E
* Place CL5,CL6 close to each VDD10 pin 8, 30

CL5: close to Pin8
CL6: close to Pin30
CL18: close to Pin3
CL19: close to Pin22

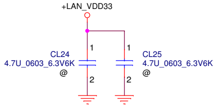
CL15,RL1:
Only for
RTL8111 LDO mode.


40 mils
VDD10
CL15 .1U_0402_16V7K
CL5 .1U_0402_16V7K
CL6 .1U_0402_16V7K
CL18 .1U_0402_16V7K
CL19 .1U_0402_16V7K

Layout:
For RTL8111H-CG
* Place CL20 and CL7 and CL8 close to each VDD33 pin 11, 32 ,23
For RTL8106E
* Place CL7 and CL8 close to each VDD33 pin 23, 32


+LAN_VDD33
40 mils
CL20 .1U_0402_16V7K
CL7 .1U_0402_16V7K
CL8 .1U_0402_16V7K

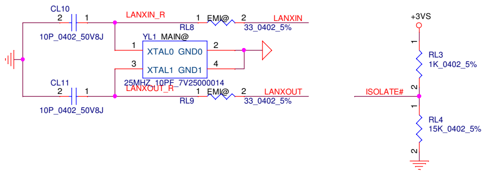
CL8: close to Pin23
CL20: close to Pin11
CL7: close to Pin32

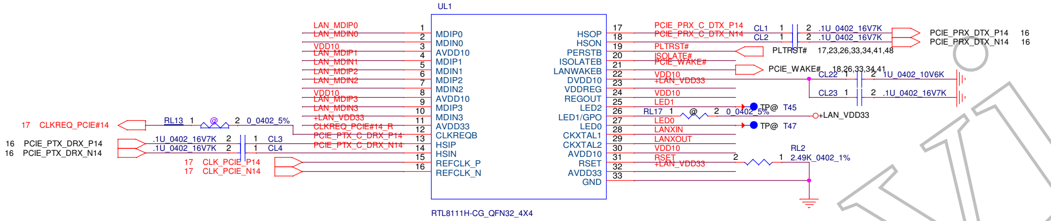

+LAN_VDD33
CL24 4.7U_0603_6.3V6K @
CL25 4.7U_0603_6.3V6K @

Layout:
CL24: close to Pin32
CL25: close to Pin11

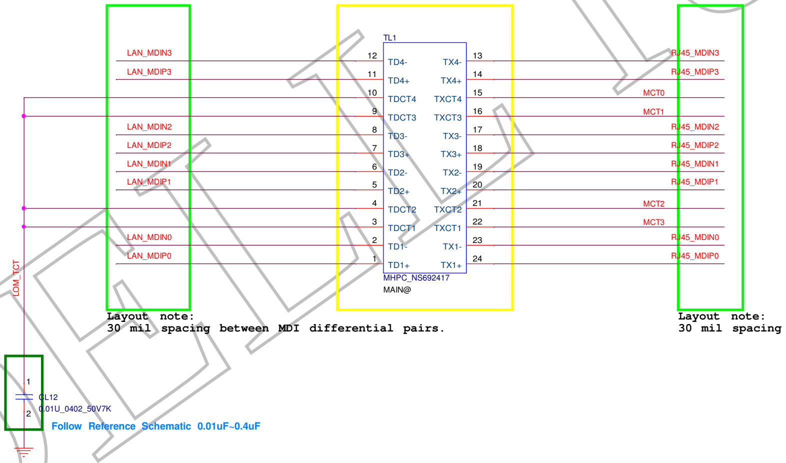
+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.

RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M


CL10 10P_0402_50V8J
CL11 10P_0402_50V8J
LANXIN_R
RL8 33_0402_5% EMI@
LANXIN
YL1 MAIN@
XTAL0 GND0
XTAL1 GND1
25MHZ_10PF_7V25000014
LANXOUT_R
RL9 33_0402_5% EMI@
LANXOUT
+3VS
RL3 1K_0402_5%
ISOLATE#
RL4 15K_0402_5%

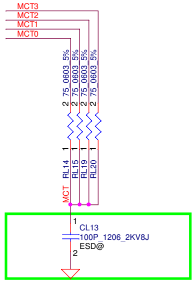

UL1
RTL8111H-CG_QFN32_4X4
LAN_MDIP0 1 MDIP0
LAN_MDIN0 2 MDIN0
VDD10 3 AVDD10
LAN_MDIP1 4 MDIP1
LAN_MDIN1 5 MDIN1
LAN_MDIP2 6 MDIP2
LAN_MDIN2 7 MDIN2
VDD10 8 AVDD10
LAN_MDIP3 9 MDIP3
LAN_MDIN3 10 MDIN3
+LAN_VDD33 11 AVDD33
CLKREQ_PCIE#14_R 12 CLKREQB
PCIE_PTX_C_DRX_P14 13 HSIP
PCIE_PTX_C_DRX_N14 14 HSIN
15 REFCLK_P
16 REFCLK_N
17 HSOP PCIE_PRX_C_DTX_P14
18 HSON PCIE_PRX_C_DTX_N14
19 PERSTB PLTRST#
20 ISOLATEB ISOLATE#
21 LANWAKEB PCIE_WAKE#
22 DVDD10 VDD10
23 VDDREG +LAN_VDD33
24 REGOUT VDD10
25 LED2 LED1
26 LED1/GPO
27 LED0 LED0
28 CKXTAL1 LANXIN
29 CKXTAL2 LANXOUT
30 AVDD10 VDD10
31 RSET RSET
32 AVDD33 +LAN_VDD33
33 GND
17 CLKREQ_PCIE#14
RL13 0_0402_5% @
16 PCIE_PTX_DRX_P14
16 PCIE_PTX_DRX_N14
CL3 .1U_0402_16V7K
CL4 .1U_0402_16V7K
17 CLK_PCIE_P14
17 CLK_PCIE_N14
CL1 .1U_0402_16V7K
CL2 .1U_0402_16V7K
PCIE_PRX_DTX_P14 16
PCIE_PRX_DTX_N14 16
PLTRST# 17,23,26,33,34,41,48
PCIE_WAKE# 18,26,33,34,41
CL22 1U_0402_10V6K
CL23 .1U_0402_16V7K
TP@ T45
TP@ T47
RL17 0_0402_5% @
+LAN_VDD33
RL2 2.49K_0402_1%

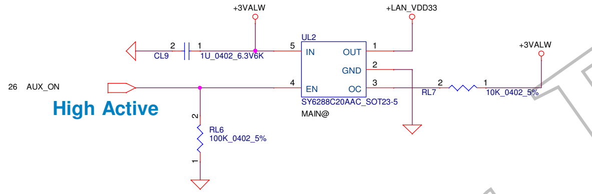
LAN TransFormer (10/100/1000M & 10/100M co-layout)


TL1
MHPC_NS692417
MAIN@
LAN_MDIN3 12 TD4- TX4- 13 RJ45_MDIN3
LAN_MDIP3 11 TD4+ TX4+ 14 RJ45_MDIP3
10 TDCT4 TXCT4 15 MCT0
9 TDCT3 TXCT3 16 MCT1
LAN_MDIN2 8 TD3- TX3- 17 RJ45_MDIN2
LAN_MDIP2 7 TD3+ TX3+ 18 RJ45_MDIP2
LAN_MDIN1 6 TD2- TX2- 19 RJ45_MDIN1
LAN_MDIP1 5 TD2+ TX2+ 20 RJ45_MDIP1
4 TDCT2 TXCT2 21 MCT2
3 TDCT1 TXCT1 22 MCT3
LAN_MDIN0 2 TD1- TX1- 23 RJ45_MDIN0
LAN_MDIP0 1 TD1+ TX1+ 24 RJ45_MDIP0
LOM_TCT
CL12 0.01U_0402_50V7K
Follow Reference Schematic 0.01uF~0.4uF

Layout note:
30 mil spacing between MDI differential pairs.

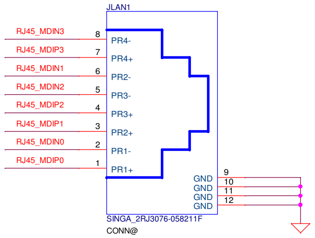
Layout note:
30 mil spacing between MDI differential pairs.


MCT3
MCT2
MCT1
MCT0
RL14 75_0603_5%
RL15 75_0603_5%
RL19 75_0603_5%
RL20 75_0603_5%
MCT
CL13 100P_1206_2KV8J ESD@


+3VALW
+LAN_VDD33
UL2
IN OUT
GND
EN OC
SY6288C20AAC_SOT23-5
MAIN@
CL9 1U_0402_6.3V6K
26 AUX_ON
RL6 100K_0402_5%
+3VALW
RL7 10K_0402_5%

High Active

	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O


JLAN1
RJ45_MDIN3 8 PR4-
RJ45_MDIP3 7 PR4+
RJ45_MDIN1 6 PR2-
RJ45_MDIN2 5 PR3-
RJ45_MDIP2 4 PR3+
RJ45_MDIP1 3 PR2+
RJ45_MDIN0 2 PR1-
RJ45_MDIP0 1 PR1+
GND 9
GND 10
GND 11
GND 12
SINGA_2RJ3076-058211F
CONN@

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: LAN RTL8111
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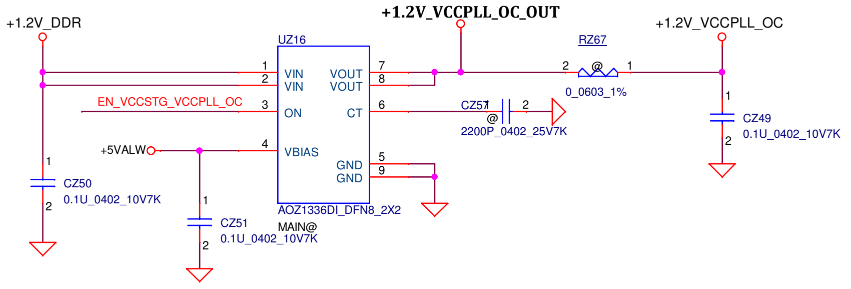
				Date: Thursday, March 22, 2018 · Sheet 35 of 78

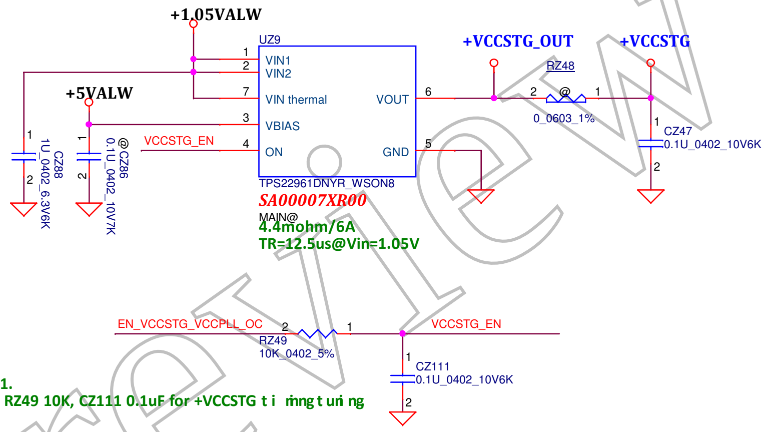
Main Func = DC/DC

+VCCPLL_OC Load Switch

H-Processor Line - Quad Core GT2
Max : 130 mA


+1.2V_DDR
+1.2V_VCCPLL_OC_OUT
+1.2V_VCCPLL_OC
UZ16
VIN
VIN
VOUT
VOUT
ON
CT
VBIAS
GND
GND
EN_VCCSTG_VCCPLL_OC
+5VALW
RZ67
0_0603_1%
CZ57
2200P_0402_25V7K
CZ49
0.1U_0402_10V7K
CZ50
0.1U_0402_10V7K
CZ51
0.1U_0402_10V7K
AOZ1336DI_DFN8_2X2
MAIN@

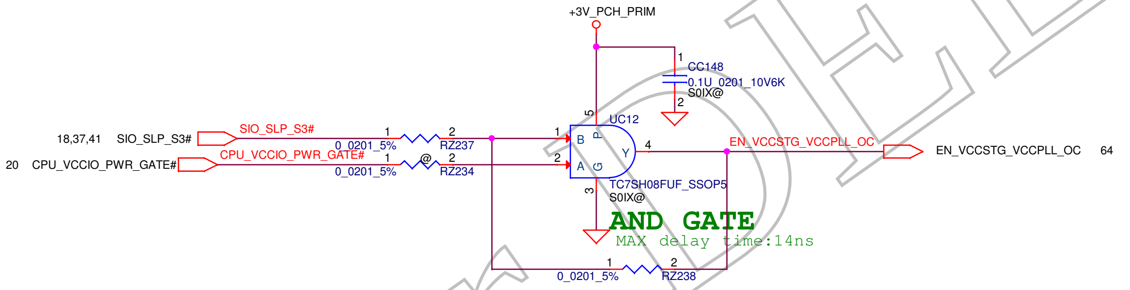
+VCCSTG Load Switch


+1.05VALW
+5VALW
+VCCSTG_OUT
+VCCSTG
UZ9
VIN1
VIN2
VIN thermal
VBIAS
ON
VOUT
GND
VCCSTG_EN
TPS22961DNYR_WSON8
SA00007XR00
MAIN@
4.4mohm/6A
TR=12.5us@Vin=1.05V
RZ48
0_0603_1%
CZ47
0.1U_0402_10V6K
CZ88
1U_0402_6.3V6K
CZ86
0.1U_0402_10V7K
EN_VCCSTG_VCCPLL_OC
RZ49
10K_0402_5%
VCCSTG_EN
CZ111
0.1U_0402_10V6K

DVT1.
Add RZ49 10K, CZ111 0.1uF for +VCCSTG timing tuning

Power Gating by Modern Standby Control

+1.05VALW TO +1.0VS_VCCSTG


+3V_PCH_PRIM
CC148
0.1U_0201_10V6K
S0IX@
18,37,41 SIO_SLP_S3#
SIO_SLP_S3#
20 CPU_VCCIO_PWR_GATE#
CPU_VCCIO_PWR_GATE#
RZ237
0_0201_5%
RZ234
0_0201_5%
UC12
B
A
Y
P
G
TC7SH08FUF_SSOP5
S0IX@
EN_VCCSTG_VCCPLL_OC
EN_VCCSTG_VCCPLL_OC 64
RZ238
0_0201_5%
AND GATE
MAX delay time:14ns

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: DC/DC(1/2)
				Size / Document Number: LA-F611P / Rev 0.3
				Date: Thursday, March 22, 2018 / Sheet 36 of 78

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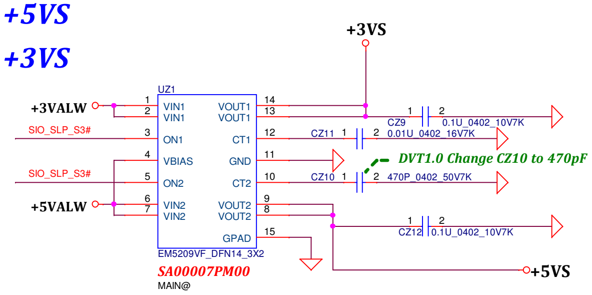
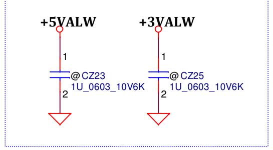
Main Func = DC/DC

+5VALW to +5VS
+3VALW to +3VS

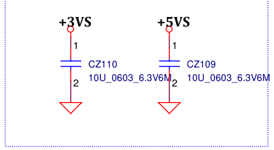

+3VS
UZ1
+3VALW
SIO_SLP_S3#
SIO_SLP_S3#
+5VALW
VIN1
VIN1
ON1
VBIAS
ON2
VIN2
VIN2
VOUT1
VOUT1
CT1
GND
CT2
VOUT2
VOUT2
GPAD
CZ9 0.01U_0402_16V7K
0.1U_0402_10V7K
CZ11
CZ10 470P_0402_50V7K
CZ12 0.1U_0402_10V7K
+5VS
EM5209VF_DFN14_3X2
SA00007PM00
MAIN@

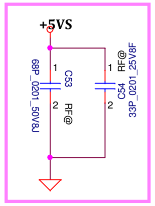
DVT1.0 Change CZ10 to 470pF

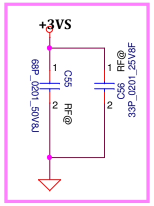
Close UZ1


+5VALW
+3VALW
@CZ23
1U_0603_10V6K
@CZ25
1U_0603_10V6K

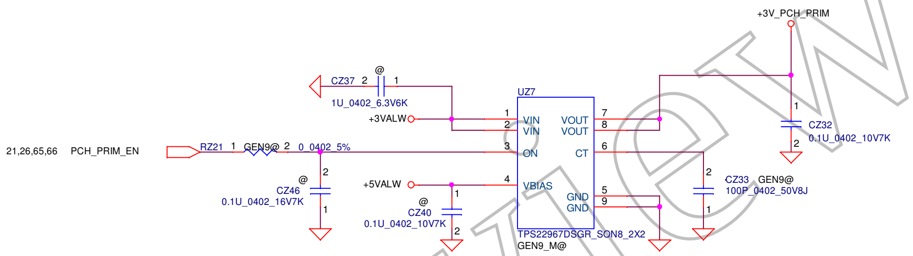
Close JPZ1 and JPZ2


+3VS
+5VS
CZ110
10U_0603_6.3V6M
CZ109
10U_0603_6.3V6M

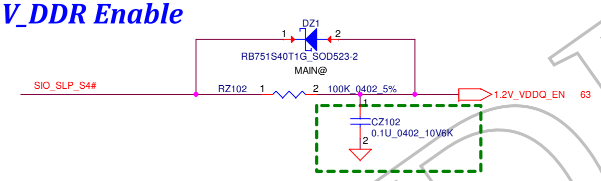

+5VS
68P_0201_50V8J
C53
RF@
RF@
C54
33P_0201_25V8F


+3VS
68P_0201_50V8J
C55
RF@
RF@
C56
33P_0201_25V8F

+3V_PCH_PRIM Load Switch

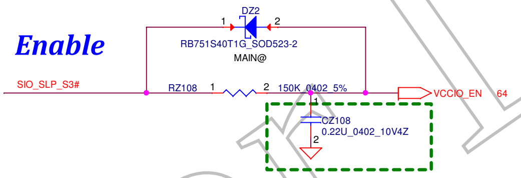

+3V_PCH_PRIM
CZ37 @
1U_0402_6.3V6K
+3VALW
21,26,65,66
PCH_PRIM_EN
RZ21 GEN9@ 0_0402_5%
CZ46 @
0.1U_0402_16V7K
+5VALW
CZ40 @
0.1U_0402_10V7K
UZ7
VIN
VIN
ON
VBIAS
VOUT
VOUT
CT
GND
GND
TPS22967DSGR_SON8_2X2
GEN9_M@
CZ32
0.1U_0402_10V7K
CZ33 GEN9@
100P_0402_50V8J

+1.2V_DDR Enable


DZ1
RB751S40T1G_SOD523-2
MAIN@
SIO_SLP_S4#
RZ102
100K_0402_5%
1.2V_VDDQ_EN
63
CZ102
0.1U_0402_10V6K

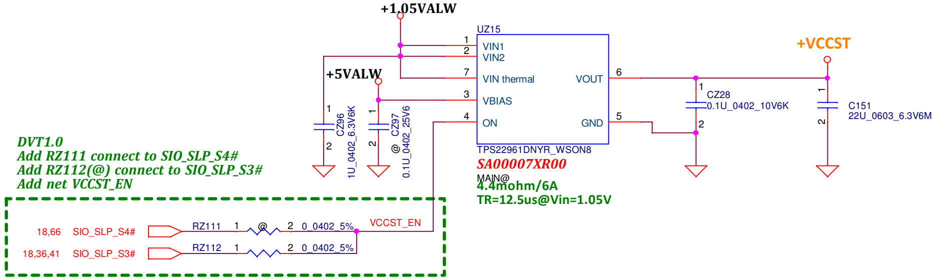
DVT1.0 Change CZ102 to 0.1uF

+VCCIO Enable


DZ2
RB751S40T1G_SOD523-2
MAIN@
SIO_SLP_S3#
RZ108
150K_0402_5%
VCCIO_EN
64
CZ108
0.22U_0402_10V4Z

DVT1.0 Change CZ108 to 0.22uF

+VCCST Load Switch


+1.05VALW
+5VALW
UZ15
VIN1
VIN2
VIN thermal
VBIAS
ON
VOUT
GND
TPS22961DNYR_WSON8
SA00007XR00
MAIN@
4.4mohm/6A
TR=12.5us@Vin=1.05V
CZ96
1U_0402_6.3V6K
CZ97 @
0.1U_0402_25V6
CZ28
0.1U_0402_10V6K
C151
22U_0603_6.3V6M
+VCCST
18,66 SIO_SLP_S4#
18,36,41 SIO_SLP_S3#
RZ111 @ 0_0402_5%
RZ112 0_0402_5%
VCCST_EN

DVT1.0
Add RZ111 connect to SIO_SLP_S4#
Add RZ112(@) connect to SIO_SLP_S3#
Add net VCCST_EN

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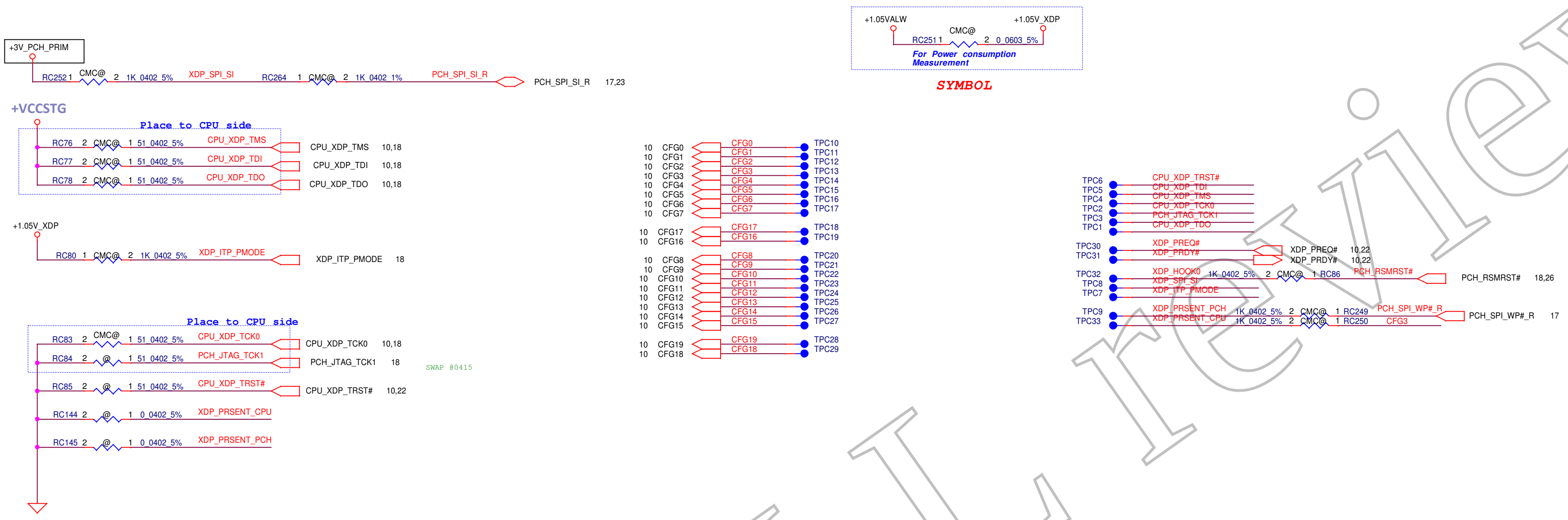
				Date: Thursday, March 22, 2018 Sheet 37 of 78

Main Func = CMC

PRIMARY CMC CONN.


+1.05VALW
+1.05V_XDP
CMC@
RC251 1
2 0_0603_5%
For Power consumption Measurement
SYMBOL
+3V_PCH_PRIM
RC252 1
CMC@
2 1K_0402_5%
XDP_SPI_SI
RC264 1
CMC@
2 1K_0402_1%
PCH_SPI_SI_R
PCH_SPI_SI_R 17,23
+VCCSTG
Place to CPU side
RC76 2 CMC@ 1 51_0402_5%
CPU_XDP_TMS
CPU_XDP_TMS 10,18
RC77 2 CMC@ 1 51_0402_5%
CPU_XDP_TDI
CPU_XDP_TDI 10,18
RC78 2 CMC@ 1 51_0402_5%
CPU_XDP_TDO
CPU_XDP_TDO 10,18
+1.05V_XDP
RC80 1 CMC@ 2 1K_0402_5%
XDP_ITP_PMODE
XDP_ITP_PMODE 18
Place to CPU side
RC83 2 CMC@ 1 51_0402_5%
CPU_XDP_TCK0
CPU_XDP_TCK0 10,18
RC84 2 @ 1 51_0402_5%
PCH_JTAG_TCK1
PCH_JTAG_TCK1 18
SWAP @0415
RC85 2 @ 1 51_0402_5%
CPU_XDP_TRST#
CPU_XDP_TRST# 10,22
RC144 2 @ 1 0_0402_5%
XDP_PRSENT_CPU
RC145 2 @ 1 0_0402_5%
XDP_PRSENT_PCH
10 CFG0
10 CFG1
10 CFG2
10 CFG3
10 CFG4
10 CFG5
10 CFG6
10 CFG7
10 CFG17
10 CFG16
10 CFG8
10 CFG9
10 CFG10
10 CFG11
10 CFG12
10 CFG13
10 CFG14
10 CFG15
10 CFG19
10 CFG18
CFG0
CFG1
CFG2
CFG3
CFG4
CFG5
CFG6
CFG7
CFG17
CFG16
CFG8
CFG9
CFG10
CFG11
CFG12
CFG13
CFG14
CFG15
CFG19
CFG18
TPC10
TPC11
TPC12
TPC13
TPC14
TPC15
TPC16
TPC17
TPC18
TPC19
TPC20
TPC21
TPC22
TPC23
TPC24
TPC25
TPC26
TPC27
TPC28
TPC29
TPC6
TPC5
TPC4
TPC2
TPC3
TPC1
CPU_XDP_TRST#
CPU_XDP_TDI
CPU_XDP_TMS
CPU_XDP_TCK0
PCH_JTAG_TCK1
CPU_XDP_TDO
TPC30
TPC31
XDP_PREQ#
XDP_PRDY#
XDP_PREQ# 10,22
XDP_PRDY# 10,22
TPC32
TPC8
TPC7
XDP_HOOK0
XDP_SPI_SI
XDP_ITP_PMODE
1K_0402_5% 2 CMC@ 1 RC86
PCH_RSMRST#
PCH_RSMRST# 18,26
TPC9
TPC33
XDP_PRSENT_PCH
XDP_PRSENT_CPU
1K_0402_5% 2 CMC@ 1 RC249
1K_0402_5% 2 CMC@ 1 RC250
PCH_SPI_WP#_R
CFG3
PCH_SPI_WP#_R 17

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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title CMC
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Main Func = Reserved

Reserved

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Title ***Reserved***

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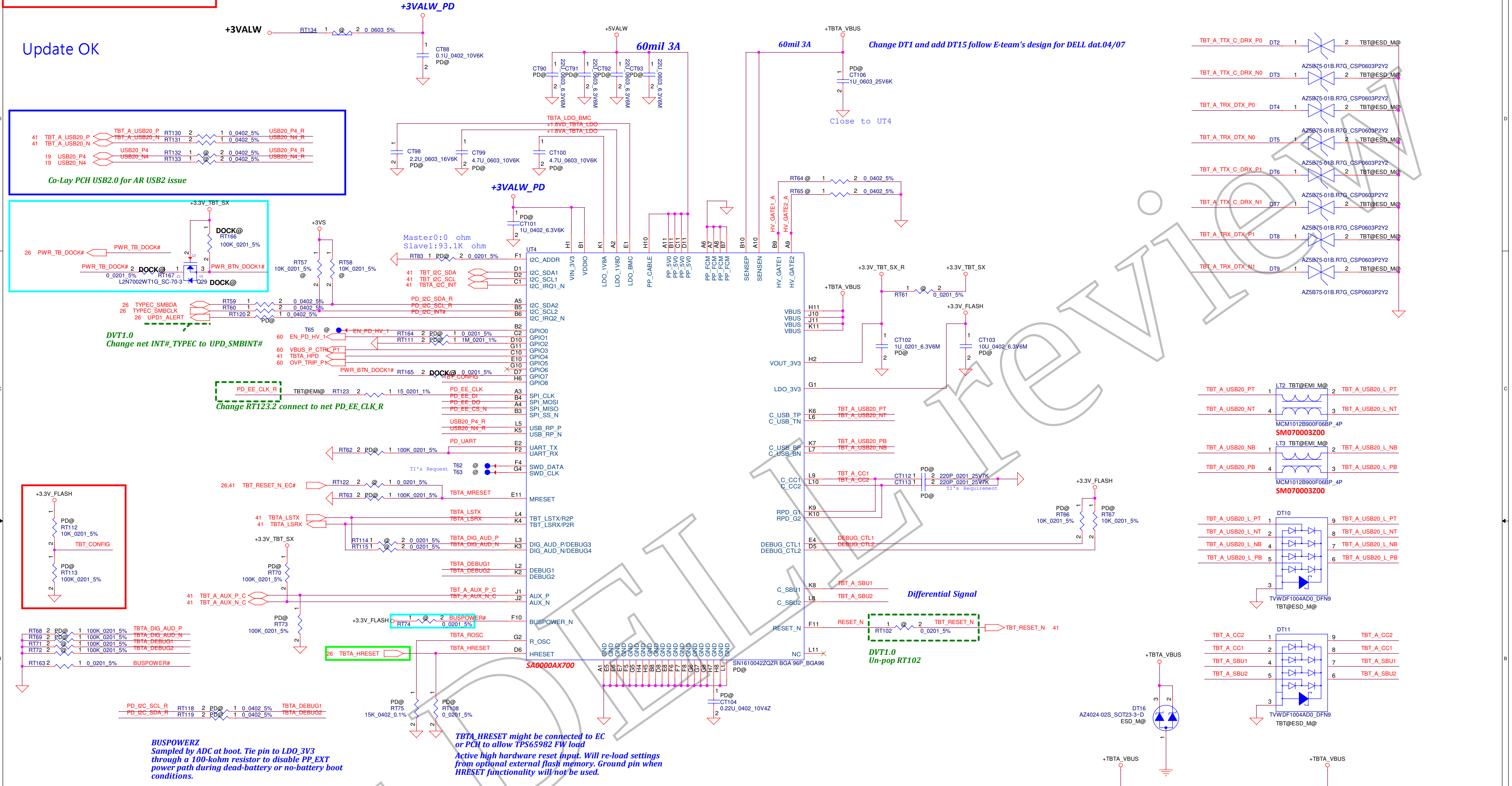
Main Func = PD + TYPE C

Update OK

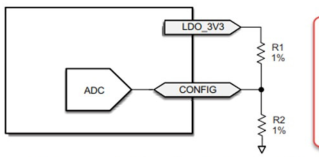

+3VALW_PD
+3VALW
RT134
0_0603_5%
CT88
0.1U_0402_10V6K
PD@
+5VALW
60mil 3A
CT90
CT91
CT92
CT93
22U_0603_6.3V6M
+TBTA_VBUS
60mil 3A
Change DT1 and add DT15 follow E-team's design for DELL dat.04/07
CT106
1U_0603_25V6K
Close to UT4
TBTA_LDO_BMC
+1.8VD_TBTA_LDO
+1.8VA_TBTA_LDO
CT98
2.2U_0603_16V6K
CT99
4.7U_0603_10V6K
CT100
4.7U_0603_10V6K
TBT_A_USB20_P
TBT_A_USB20_N
RT130
RT131
RT132
RT133
USB20_P4
USB20_N4
USB20_P4_R
USB20_N4_R
0_0402_5%
Co-Lay PCH USB2.0 for AR USB2 issue
+3.3V_TBT_SX
DOCK@
RT166
100K_0201_5%
PWR_TB_DOCK#
PWR_BTN_DOCK1#
RT167
QT29
L2N7002WT1G_SC-70-3
+3VS
RT57
RT58
10K_0201_5%
Master0:0 ohm
Slave1:93.1K ohm
RT83
0_0201_5%
CT101
1U_0402_6.3V6K
TBT_I2C_SDA
TBT_I2C_SCL
TBTA_I2C_INT
PD_I2C_SDA_R
PD_I2C_SCL_R
PD_I2C_INT#
TYPEC_SMBDA
TYPEC_SMBCLK
UPD1_ALERT
RT59
RT60
RT120
DVT1.0
Change net INT#_TYPEC to UPD_SMBINT#
EN_PD_HV_1
RT164
RT111
1M_0201_1%
VBUS_P_CTRL_P1
TBTA_HPD
OVP_TRIP_P1
PWR_BTN_DOCK1#
RT165
TBT_CONFIG
PD_EE_CLK_R
TBT@EMI@
RT123
15_0201_1%
Change RT123.2 connect to net PD_EE_CLK_R
PD_EE_CLK
PD_EE_DI
PD_EE_DO
PD_EE_CS_N
USB20_P4_R
USB20_N4_R
PD_UART
RT62
100K_0201_5%
T62
T63
TI's Request
TBT_RESET_N_EC#
RT122
RT63
TBTA_MRESET
TBTA_LSTX
TBTA_LSRX
+3.3V_TBT_SX
RT114
RT115
TBTA_DIG_AUD_P
TBTA_DIG_AUD_N
TBTA_DEBUG1
TBTA_DEBUG2
RT70
100K_0201_5%
TBT_A_AUX_P_C
TBT_A_AUX_N_C
RT73
+3.3V_FLASH
RT74
BUSPOWER#
TBTA_ROSC
TBTA_HRESET
RT112
RT113
10K_0201_5%
RT68
RT69
RT71
RT72
RT163
PD_I2C_SCL_R
PD_I2C_SDA_R
RT118
RT119
RT75
15K_0402_0.1%
RT108
UT4
I2C_ADDR
I2C_SDA1
I2C_SCL1
I2C_IRQ1_N
I2C_SDA2
I2C_SCL2
I2C_IRQ2_N
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SS_N
USB_RP_P
USB_RP_N
UART_TX
UART_RX
SWD_DATA
SWD_CLK
MRESET
TBT_LSTX/R2P
TBT_LSRX/P2R
DIG_AUD_P/DEBUG3
DIG_AUD_N/DEBUG4
DEBUG1
DEBUG2
AUX_P
AUX_N
BUSPOWER_N
R_OSC
HRESET
VIN_3V3
VDDIO
LDO_1V8A
LDO_1V8D
LDO_BMC
PP_CABLE
PP_5V0
PP_FCM
SENSEP
SENSEN
HV_GATE1
HV_GATE2
VBUS
VOUT_3V3
LDO_3V3
C_USB_TP
C_USB_TN
C_USB_BP
C_USB_BN
C_CC1
C_CC2
RPD_G1
RPD_G2
DEBUG_CTL1
DEBUG_CTL2
C_SBU1
C_SBU2
RESET_N
NC
GND
SA0000AX700
SN1610042ZQZR BGA 96P_BGA96
CT104
0.22U_0402_10V4Z
RT64
RT65
0_0402_5%
RT61
0_0201_5%
CT102
1U_0201_6.3V6M
CT103
10U_0402_6.3V6M
TBT_A_USB20_PT
TBT_A_USB20_NT
TBT_A_USB20_PB
TBT_A_USB20_NB
TBT_A_CC1
TBT_A_CC2
CT112
CT113
220P_0201_25V7K
TI's Requirement
RT66
RT67
10K_0201_5%
DEBUG_CTL1
DEBUG_CTL2
TBT_A_SBU1
TBT_A_SBU2
Differential Signal
RESET_N
RT102
TBT_RESET_N
DVT1.0
Un-pop RT102
TBT_A_TTX_C_DRX_P0
TBT_A_TTX_C_DRX_N0
TBT_A_TRX_DTX_P0
TBT_A_TRX_DTX_N0
TBT_A_TTX_C_DRX_P1
TBT_A_TTX_C_DRX_N1
TBT_A_TRX_DTX_P1
TBT_A_TRX_DTX_N1
DT2
DT3
DT4
DT5
DT6
DT7
DT8
DT9
TBT@ESD_M@
AZ5B75-01B.R7G_CSP0603P2Y2
LT2
LT3
TBT@EMI_M@
TBT_A_USB20_L_PT
TBT_A_USB20_L_NT
TBT_A_USB20_L_NB
TBT_A_USB20_L_PB
MCM1012B900F06BP_4P
SM070003Z00
DT10
DT11
TVWDF1004AD0_DFN9
TBT@ESD_M@
DT16
AZ4024-02S_SOT23-3~D
ESD_M@

BUSPOWERZ
Sampled by ADC at boot. Tie pin to LDO_3V3 through a 100-kohm resistor to disable PP_EXT power path during dead-battery or no-battery boot conditions.

TBTA_HRESET might be connected to EC or PCH to allow TPS65982 FW load

Active high hardware reset input. Will re-load settings from optional external flash memory. Ground pin when HRESET functionality will not be used.

c. GPIO 8 (CONFIG) is a dedicated GPIO that must have a pull-up and pull-down resistor option included in the HW design.
When 82D has a SPI Flash Connected, the safest option is to use the "Infinite Retry" setting, which will prevent from loading an incorrect configuration. For this setting, GPIO 8 needs to be pulled to LDO_3V3, which effectively removes the divider (DIV = 1).


LDO_3V3
R1
1%
ADC
CONFIG
R2
1%

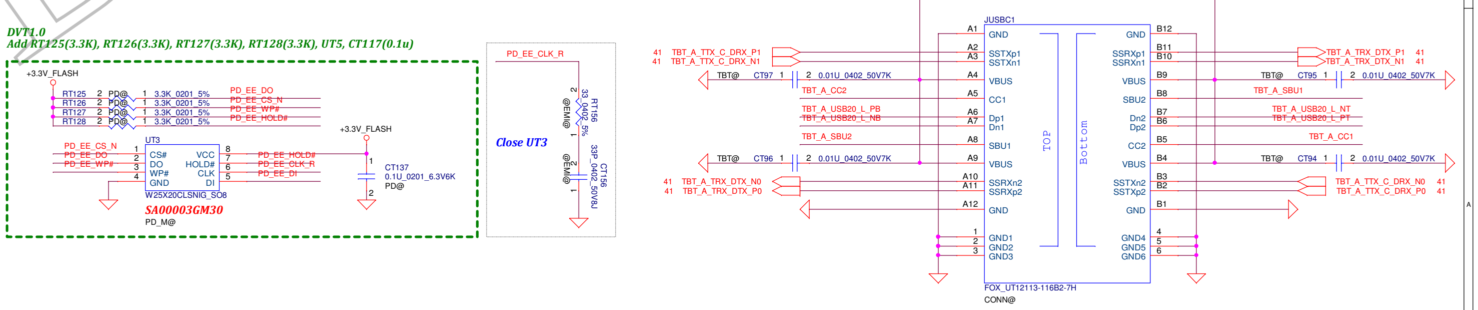
If External SPI Connected, use "Infinite Retry" Setting by pulling CONFIG (GPIO 8) to LDO_3V3

Figure 78. Factory Configuration Resistor Divider

Table 13. Factory Device Configuration Selection

DIV = R2/(R1+R2)[1]		Factory Device Configuration	Description
DIV_min	DIV_max		
■■■■■			
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

DVT1.0
Add RT125(3.3K), RT126(3.3K), RT127(3.3K), RT128(3.3K), UT5, CT117(0.1u)


+3.3V_FLASH
RT125
RT126
RT127
RT128
3.3K_0201_5%
PD_EE_DO
PD_EE_CS_N
PD_EE_WP#
PD_EE_HOLD#
UT3
CS#
DO
WP#
GND
VCC
HOLD#
CLK
DI
PD_EE_CLK_R
PD_EE_DI
W25X20CLSNIG_SO8
SA00003GM30
PD_M@
CT137
0.1U_0201_6.3V6K
RT156
33_0402_5%
CT156
33P_0402_50V8J
@EMI@
Close UT3
+TBTA_VBUS
JUSBC1
GND
SSTXp1
SSTXn1
VBUS
CC1
Dp1
Dn1
SBU1
SSRXn2
SSRXp2
GND1
GND2
GND3
SSRXp1
SSRXn1
SBU2
Dn2
Dp2
CC2
SSTXn2
SSTXp2
GND4
GND5
GND6
TOP
Bottom
CT97
CT95
CT96
CT94
0.01U_0402_50V7K
TBT@
FOX_UT12113-116B2-7H
CONN@

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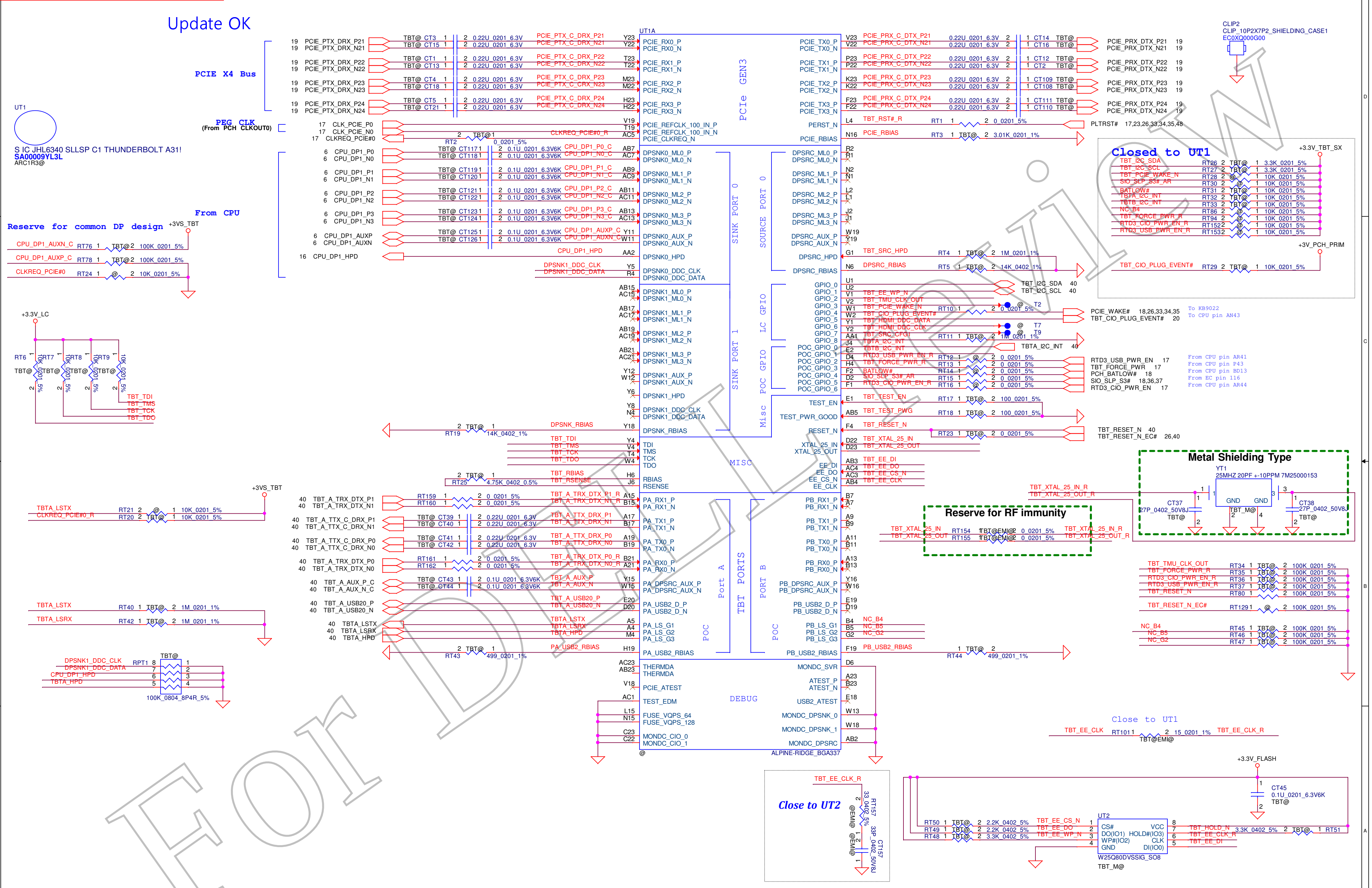
Title
PD+USB3.1 TypeC
Size Document Number LA-F611P Rev 0.3
Date: Thursday, March 22, 2018 Sheet 40 of 78

Main Func = Thunderbolt


Update OK
PCIE X4 Bus
PEG CLK (From PCH CLKOUT0)
From CPU
Reserve for common DP design
UT1
S IC JHL6340 SLLSP C1 THUNDERBOLT A31!
SA00009YL3L
ARC1R3@
UT1A
PCIe GEN3
SINK PORT 0
SOURCE PORT 0
SINK PORT 1
LC GPIO
POC GPIO
Misc
MISC
TBT PORTS
Port A
Port B
POC
DEBUG
ALPINE-RIDGE_BGA337
PCIE_RX0_P
PCIE_RX0_N
PCIE_RX1_P
PCIE_RX1_N
PCIE_RX2_P
PCIE_RX2_N
PCIE_RX3_P
PCIE_RX3_N
PCIE_REFCLK_100_IN_P
PCIE_REFCLK_100_IN_N
PCIE_CLKREQ_N
PCIE_TX0_P
PCIE_TX0_N
PCIE_TX1_P
PCIE_TX1_N
PCIE_TX2_P
PCIE_TX2_N
PCIE_TX3_P
PCIE_TX3_N
PERST_N
PCIE_RBIAS
DPSNK0_ML0_P
DPSNK0_ML0_N
DPSNK0_ML1_P
DPSNK0_ML1_N
DPSNK0_ML2_P
DPSNK0_ML2_N
DPSNK0_ML3_P
DPSNK0_ML3_N
DPSNK0_AUX_P
DPSNK0_AUX_N
DPSNK0_HPD
DPSNK0_DDC_CLK
DPSNK0_DDC_DATA
DPSRC_ML0_P
DPSRC_ML0_N
DPSRC_ML1_P
DPSRC_ML1_N
DPSRC_ML2_P
DPSRC_ML2_N
DPSRC_ML3_P
DPSRC_ML3_N
DPSRC_AUX_P
DPSRC_AUX_N
DPSRC_HPD
DPSRC_RBIAS
GPIO_0 … GPIO_8
POC_GPIO_0 … POC_GPIO_6
TEST_EN
TEST_PWR_GOOD
RESET_N
XTAL_25_IN
XTAL_25_OUT
EE_DI
EE_DO
EE_CS_N
EE_CLK
DPSNK1_ML0_P
DPSNK1_ML0_N
DPSNK1_ML1_P
DPSNK1_ML1_N
DPSNK1_ML2_P
DPSNK1_ML2_N
DPSNK1_ML3_P
DPSNK1_ML3_N
DPSNK1_AUX_P
DPSNK1_AUX_N
DPSNK1_HPD
DPSNK1_DDC_CLK
DPSNK1_DDC_DATA
DPSNK_RBIAS
TDI
TMS
TCK
TDO
RBIAS
RSENSE
PA_RX1_P
PA_RX1_N
PA_TX1_P
PA_TX1_N
PA_TX0_P
PA_TX0_N
PA_RX0_P
PA_RX0_N
PA_DPSRC_AUX_P
PA_DPSRC_AUX_N
PA_USB2_D_P
PA_USB2_D_N
PA_LS_G1
PA_LS_G2
PA_LS_G3
PA_USB2_RBIAS
PB_RX1_P
PB_RX1_N
PB_TX1_P
PB_TX1_N
PB_TX0_P
PB_TX0_N
PB_RX0_P
PB_RX0_N
PB_DPSRC_AUX_P
PB_DPSRC_AUX_N
PB_USB2_D_P
PB_USB2_D_N
PB_LS_G1
PB_LS_G2
PB_LS_G3
PB_USB2_RBIAS
THERMDA
THERMDA
PCIE_ATEST
TEST_EDM
FUSE_VQPS_64
FUSE_VQPS_128
MONDC_CIO_0
MONDC_CIO_1
MONDC_SVR
ATEST_P
ATEST_N
USB2_ATEST
MONDC_DPSNK_0
MONDC_DPSNK_1
MONDC_DPSRC
PCIE_PTX_DRX_P21 / N21 … P24 / N24
PCIE_PTX_C_DRX_P21 … N24
PCIE_PRX_C_DTX_P21 … N24
PCIE_PRX_DTX_P21 … N24
TBT@ CT3 … CT21
0.22U_0201_6.3V
CLK_PCIE_P0
CLK_PCIE_N0
CLKREQ_PCIE#0
CLKREQ_PCIE#0_R
RT2 0_0201_5%
CPU_DP1_P0 … N3
CPU_DP1_AUXP
CPU_DP1_AUXN
CPU_DP1_HPD
0.1U_0201_6.3V6K
CPU_DP1_AUXN_C
CPU_DP1_AUXP_C
RT76 100K_0201_5%
RT78 100K_0201_5%
RT24 10K_0201_5%
+3VS_TBT
+3.3V_LC
RT6 RT7 RT8 RT9 10K_0201_5%
TBT_TDI
TBT_TMS
TBT_TCK
TBT_TDO
DPSNK_RBIAS
RT19 14K_0402_1%
TBT_RBIAS
TBT_RSENSE
RT25 4.75K_0402_0.5%
TBT_RST#_R
RT1 0_0201_5%
PCIE_RBIAS
RT3 3.01K_0201_1%
PLTRST# 17,23,26,33,34,35,48
TBT_SRC_HPD
RT4 1M_0201_1%
DPSRC_RBIAS
RT5 14K_0402_1%
TBT_I2C_SDA 40
TBT_I2C_SCL 40
TBT_EE_WP_N
TBT_TMU_CLK_OUT
TBT_PCIE_WAKE_N
TBT_CIO_PLUG_EVENT#
TBT_HDMI_DDC_CLK
TBT_SRC_CFG
TBTA_I2C_INT
TBTB_I2C_INT
RT10 0_0201_5%
RT11 1M_0201_1%
T2 T7 T9
PCIE_WAKE# 18,26,33,34,35
TBT_CIO_PLUG_EVENT# 20
To KB9022
To CPU pin AN43
TBTA_I2C_INT 40
RTD3_USB_PWR_EN_R
TBT_FORCE_PWR_R
BATLOW#
SIO_SLP_S3#_AR
RTD3_CIO_PWR_EN_R
RT12 RT13 RT14 RT15 RT16 0_0201_5%
RTD3_USB_PWR_EN 17
TBT_FORCE_PWR 17
PCH_BATLOW# 18
SIO_SLP_S3# 18,36,37
RTD3_CIO_PWR_EN 17
From CPU pin AR41
From CPU pin P43
From CPU pin BD13
From EC pin 116
From CPU pin AR44
TBT_TEST_EN
RT17 100_0201_5%
TBT_TEST_PWG
RT18 100_0201_5%
TBT_RESET_N
RT23 0_0201_5%
TBT_RESET_N 40
TBT_RESET_N_EC# 26,40
TBT_XTAL_25_IN
TBT_XTAL_25_OUT
TBT_EE_DI
TBT_EE_DO
TBT_EE_CS_N
TBT_EE_CLK
CLIP2
CLIP_10P2X7P2_SHIELDING_CASE1
EC0XQ000G00
Closed to UT1
+3.3V_TBT_SX
TBT_I2C_SDA
TBT_I2C_SCL
TBT_PCIE_WAKE_N
SIO_SLP_S3#_AR
BATLOW#
TBTA_I2C_INT
TBTB_I2C_INT
NC_B4
TBT_FORCE_PWR_R
RTD3_CIO_PWR_EN_R
RTD3_USB_PWR_EN_R
RT26 RT27 3.3K_0201_5%
RT28 RT30 RT31 RT32 RT33 RT86 RT94 RT152 RT153 10K_0201_5%
+3V_PCH_PRIM
TBT_CIO_PLUG_EVENT#
RT29 10K_0201_5%
Metal Shielding Type
YT1
25MHZ 20PF +-10PPM 7M25000153
CT37 27P_0402_50V8J
CT38 27P_0402_50V8J
TBT_M@
GND
TBT_XTAL_25_IN_R
TBT_XTAL_25_OUT_R
Reserve for RF immunity
RT154 RT155 0_0201_5%
TBT@EMI@
TBTA_LSTX
CLKREQ_PCIE#0_R
RT21 RT20 10K_0201_5%
40 TBT_A_TRX_DTX_P1
40 TBT_A_TRX_DTX_N1
40 TBT_A_TTX_C_DRX_P1
40 TBT_A_TTX_C_DRX_N1
40 TBT_A_TTX_C_DRX_P0
40 TBT_A_TTX_C_DRX_N0
40 TBT_A_TRX_DTX_P0
40 TBT_A_TRX_DTX_N0
40 TBT_A_AUX_P_C
40 TBT_A_AUX_N_C
40 TBT_A_USB20_P
40 TBT_A_USB20_N
40 TBTA_LSTX
40 TBTA_LSRX
40 TBTA_HPD
RT159 RT160 RT161 RT162 0_0201_5%
TBT@ CT39 CT40 CT41 CT42 0.22U_0201_6.3V
TBT@ CT43 CT44 0.1U_0201_6.3V6K
TBT_A_TRX_DTX_P1_R
TBT_A_TRX_DTX_N1_R
TBT_A_TTX_DRX_P1
TBT_A_TTX_DRX_N1
TBT_A_TTX_DRX_P0
TBT_A_TTX_DRX_N0
TBT_A_TRX_DTX_P0_R
TBT_A_TRX_DTX_N0_R
TBT_A_AUX_P
TBT_A_AUX_N
TBT_A_USB20_P
TBT_A_USB20_N
TBTA_LSTX
TBTA_LSRX
TBTA_HPD
RT40 1M_0201_1%
TBTA_LSRX
RT42 1M_0201_1%
PA_USB2_RBIAS
RT43 499_0201_1%
PB_USB2_RBIAS
RT44 499_0201_1%
NC_B4
NC_B5
NC_G2
TBT_TMU_CLK_OUT
TBT_FORCE_PWR_R
RTD3_CIO_PWR_EN_R
RTD3_USB_PWR_EN_R
TBT_RESET_N
RT34 RT35 RT36 RT37 RT80 100K_0201_5%
TBT_RESET_N_EC#
RT1291 100K_0201_5%
RT45 RT46 RT47 100K_0201_5%
DPSNK1_DDC_CLK
DPSNK1_DDC_DATA
CPU_DP1_HPD
TBTA_HPD
RPT1
100K_0804_8P4R_5%
Close to UT1
TBT_EE_CLK
RT1011 15_0201_1%
TBT_EE_CLK_R
+3.3V_FLASH
CT45
0.1U_0201_6.3V6K
TBT@
Close to UT2
TBT_EE_CLK_R
RT157 33_0402_5%
CT157 33P_0402_50V8J
@EMI@
RT50 2.2K_0402_5%
RT49 2.2K_0402_5%
RT48 3.3K_0402_5%
TBT_EE_CS_N
TBT_EE_DO
TBT_EE_WP_N
UT2
CS#
DO(IO1)
WP#(IO2)
GND
VCC
HOLD#(IO3)
CLK
DI(IO0)
W25Q80DVSSIG_SO8
TBT_M@
TBT_HOLD_N
RT51 3.3K_0402_5%
TBT_EE_CLK_R
TBT_EE_DI

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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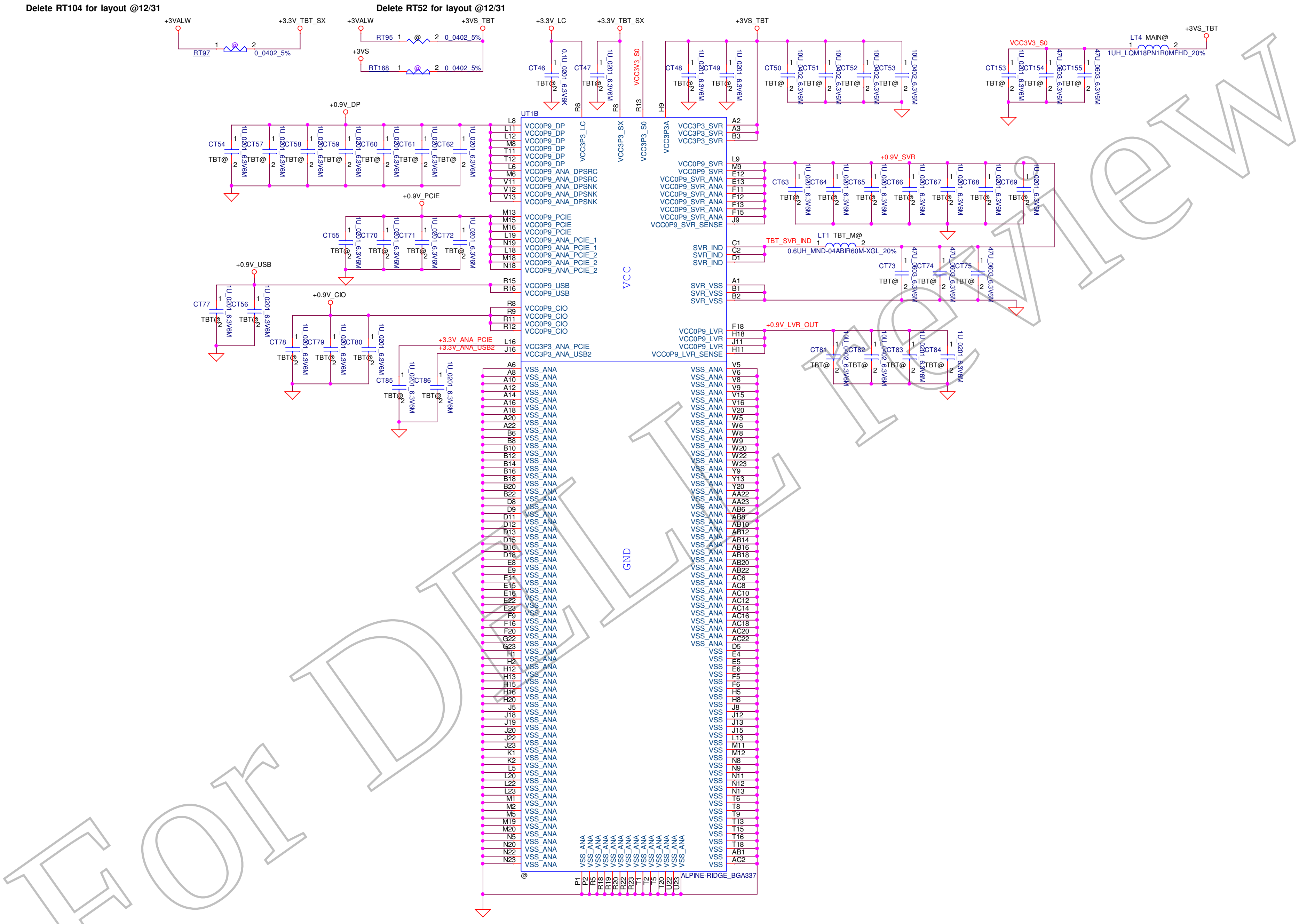
Compal Electronics, Inc.

Title
Thunderbolt (1/2)

Size Document Number Rev
LA-F611P 0.3

Date: Thursday, March 22, 2018 Sheet 41 of 78

Main Func = Thunderbolt


Delete RT104 for layout @12/31
Delete RT52 for layout @12/31
+3VALW
+3.3V_TBT_SX
RT97
0_0402_5%
RT95
RT168
+3VS
+3VS_TBT
+3.3V_LC
CT46
CT47
VCC3V3_S0
CT48
CT49
CT50
CT51
CT52
CT53
10U_0402_6.3V6M
1U_0201_6.3V6M
VCC3V3_S0
CT153
CT154
CT155
47U_0603_6.3V6M
LT4 MAIN@
1UH_LQM18PN1R0MFHD_20%
+0.9V_DP
CT54
CT57
CT58
CT59
CT60
CT61
CT62
TBT@
UT1B
VCC0P9_DP
VCC0P9_ANA_DPSRC
VCC0P9_ANA_DPSNK
+0.9V_PCIE
CT55
CT70
CT71
CT72
VCC0P9_PCIE
VCC0P9_ANA_PCIE_1
VCC0P9_ANA_PCIE_2
+0.9V_USB
CT77
CT56
VCC0P9_USB
+0.9V_CIO
CT78
CT79
CT80
VCC0P9_CIO
+3.3V_ANA_PCIE
+3.3V_ANA_USB2
CT85
CT86
VCC3P3_ANA_PCIE
VCC3P3_ANA_USB2
VCC3P3_LC
VCC3P3_SX
VCC3P3_S0
VCC3P3A
VCC3P3_SVR
VCC
+0.9V_SVR
VCC0P9_SVR
VCC0P9_SVR_ANA
VCC0P9_SVR_SENSE
CT63
CT64
CT65
CT66
CT67
CT68
CT69
TBT_SVR_IND
LT1 TBT_M@
0.6UH_MND-04ABIR60M-XGL_20%
SVR_IND
CT73
CT74
CT75
SVR_VSS
+0.9V_LVR_OUT
VCC0P9_LVR
VCC0P9_LVR_SENSE
CT81
CT82
CT83
CT84
VSS_ANA
VSS
GND
ALPINE-RIDGE_BGA337

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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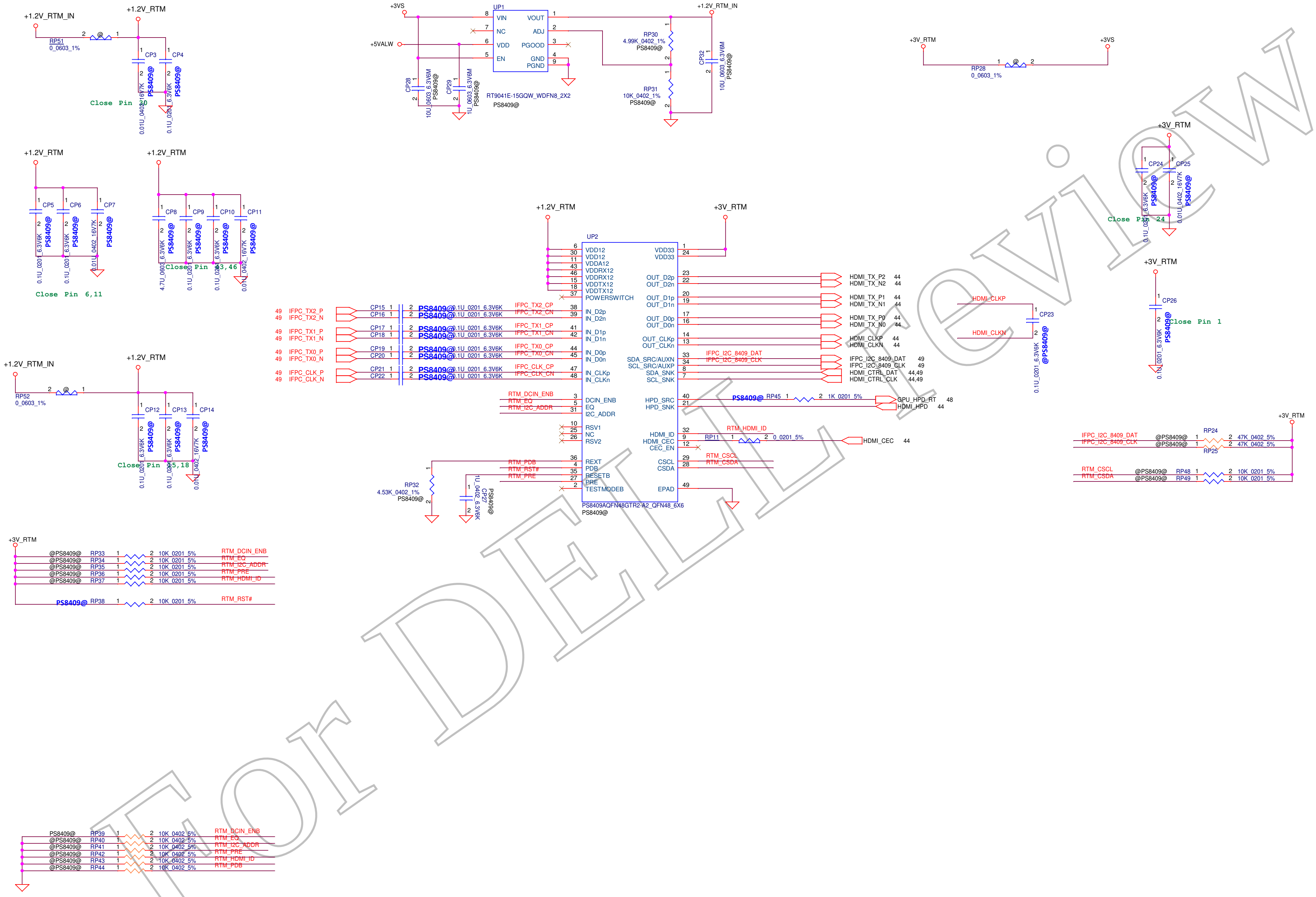
Compal Electronics, Inc.

Title
Thunderbolt (2/2)

Size Document Number
LA-F611P
Rev 0.3

Date: Thursday, March 22, 2018 Sheet 42 of 78

Main Func = Retimer



+1.2V_RTM_IN
+1.2V_RTM
RP51
0_0603_1%
CP3
CP4
PS8409@
0.01U_0402_16V7K
0.1U_0201_6.3V6K
Close Pin 20
+3VS
+5VALW
UP1
VIN
NC
VDD
EN
VOUT
ADJ
PGOOD
GND
PGND
RT9041E-15GQW_WDFN8_2X2
PS8409@
CP28
CP29
10U_0603_6.3V6M
1U_0603_6.3V6M
RP30
4.99K_0402_1%
RP31
10K_0402_1%
CP32
+3V_RTM
RP28
0_0603_1%
CP5
CP6
CP7
Close Pin 6,11
CP8
CP9
CP10
CP11
4.7U_0603_6.3V6K
Close Pin 43,46
CP24
CP25
Close Pin 24
UP2
VDD12
VDDA12
VDDRX12
VDDTX12
POWERSWITCH
VDD33
OUT_D2p
OUT_D2n
OUT_D1p
OUT_D1n
OUT_D0p
OUT_D0n
OUT_CLKp
OUT_CLKn
IN_D2p
IN_D2n
IN_D1p
IN_D1n
IN_D0p
IN_D0n
IN_CLKp
IN_CLKn
SDA_SRC/AUXN
SCL_SRC/AUXP
SDA_SNK
SCL_SNK
DCIN_ENB
EQ
I2C_ADDR
HPD_SRC
HPD_SNK
RSV1
NC
RSV2
HDMI_ID
HDMI_CEC
CEC_EN
REXT
PDB
RESETB
PRE
TESTMODEB
CSCL
CSDA
EPAD
PS8409AQFN48GTR2-A2_QFN48_6X6
49 IFPC_TX2_P
49 IFPC_TX2_N
49 IFPC_TX1_P
49 IFPC_TX1_N
49 IFPC_TX0_P
49 IFPC_TX0_N
49 IFPC_CLK_P
49 IFPC_CLK_N
CP15
CP16
CP17
CP18
CP19
CP20
CP21
CP22
0.1U_0201_6.3V6K
IFPC_TX2_CP
IFPC_TX2_CN
IFPC_TX1_CP
IFPC_TX1_CN
IFPC_TX0_CP
IFPC_TX0_CN
IFPC_CLK_CP
IFPC_CLK_CN
HDMI_TX_P2 44
HDMI_TX_N2 44
HDMI_TX_P1 44
HDMI_TX_N1 44
HDMI_TX_P0 44
HDMI_TX_N0 44
HDMI_CLKP 44
HDMI_CLKN 44
IFPC_I2C_8409_DAT
IFPC_I2C_8409_CLK
IFPC_I2C_8409_DAT 49
IFPC_I2C_8409_CLK 49
HDMI_CTRL_DAT 44,49
HDMI_CTRL_CLK 44,49
RTM_DCIN_ENB
RTM_EQ
RTM_I2C_ADDR
PS8409@ RP45
1K_0201_5%
GPU_HPD_RT 48
HDMI_HPD 44
RTM_HDMI_ID
RP11
0_0201_5%
HDMI_CEC 44
RTM_CSCL
RTM_CSDA
RTM_PDB
RTM_RST#
RTM_PRE
RP32
4.53K_0402_1%
CP27
1U_0402_6.3V6K
HDMI_CLKP
HDMI_CLKN
CP23
0.1U_0201_6.3V6K
@PS8409@
CP26
Close Pin 1
RP52
0_0603_1%
CP12
CP13
CP14
Close Pin 15,18
RP24
47K_0402_5%
RP25
RP48
RP49
10K_0201_5%
@PS8409@
RP33
RP34
RP35
RP36
RP37
RP38
10K_0201_5%
RTM_DCIN_ENB
RTM_EQ
RTM_I2C_ADDR
RTM_PRE
RTM_HDMI_ID
RTM_RST#
PS8409@
RP39
RP40
RP41
RP42
RP43
RP44
10K_0402_5%
RTM_PDB

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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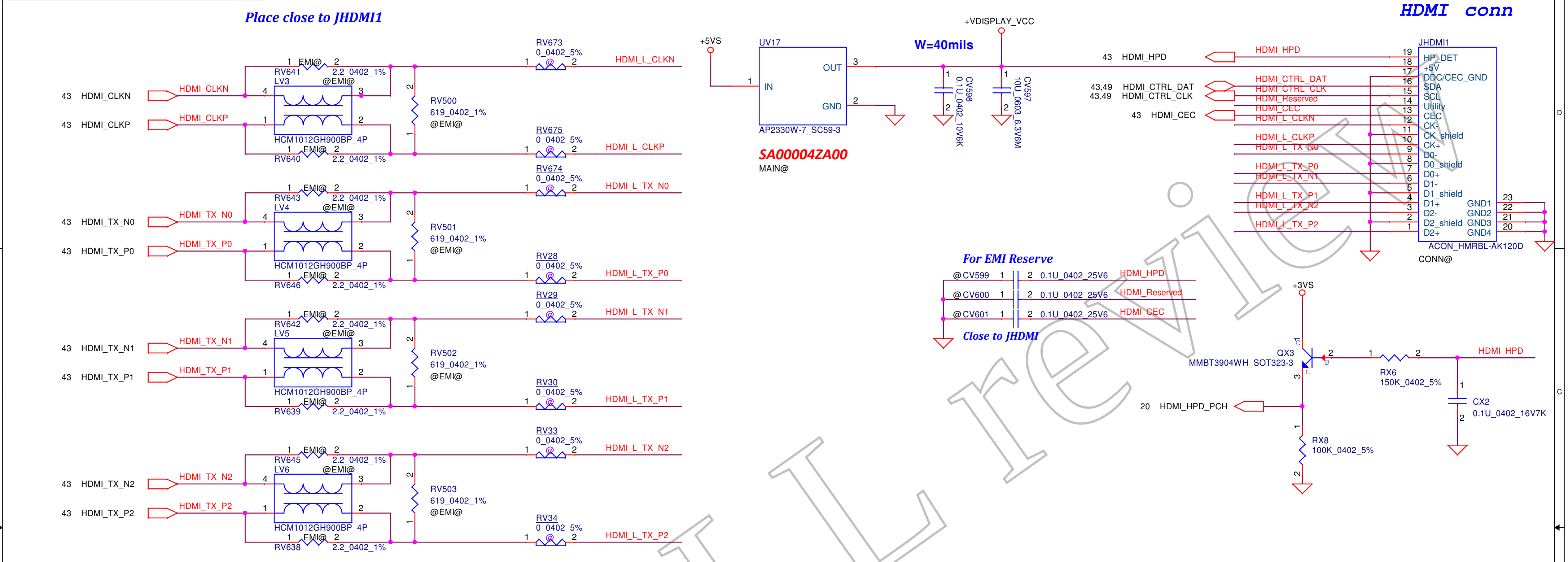
Compal Electronics, Inc.

Title
Re-Timer 8409A

Size | Document Number **LA-F611P** | Rev 0.3

Date: Thursday, March 22, 2018 | Sheet 43 of 78

Main Func = HDMI



Place close to JHDMI1
43 HDMI_CLKN
43 HDMI_CLKP
HDMI_CLKN
HDMI_CLKP
RV641 1 EMI@ 2 2.2_0402_1%
LV3 @EMI@
HCM1012GH900BP_4P
RV640 1 EMI@ 2 2.2_0402_1%
RV500 619_0402_1% @EMI@
RV673 0_0402_5%
HDMI_L_CLKN
RV675 0_0402_5%
HDMI_L_CLKP
43 HDMI_TX_N0
43 HDMI_TX_P0
HDMI_TX_N0
HDMI_TX_P0
RV643 1 EMI@ 2 2.2_0402_1%
LV4 @EMI@
HCM1012GH900BP_4P
RV646 1 EMI@ 2 2.2_0402_1%
RV501 619_0402_1% @EMI@
RV674 0_0402_5%
HDMI_L_TX_N0
RV28 0_0402_5%
HDMI_L_TX_P0
43 HDMI_TX_N1
43 HDMI_TX_P1
HDMI_TX_N1
HDMI_TX_P1
RV642 1 EMI@ 2 2.2_0402_1%
LV5 @EMI@
HCM1012GH900BP_4P
RV639 1 EMI@ 2 2.2_0402_1%
RV502 619_0402_1% @EMI@
RV29 0_0402_5%
HDMI_L_TX_N1
RV30 0_0402_5%
HDMI_L_TX_P1
43 HDMI_TX_N2
43 HDMI_TX_P2
HDMI_TX_N2
HDMI_TX_P2
RV645 1 EMI@ 2 2.2_0402_1%
LV6 @EMI@
HCM1012GH900BP_4P
RV638 1 EMI@ 2 2.2_0402_1%
RV503 619_0402_1% @EMI@
RV33 0_0402_5%
HDMI_L_TX_N2
RV34 0_0402_5%
HDMI_L_TX_P2
+5VS
UV17
IN
OUT
GND
AP2330W-7_SC59-3
SA00004ZA00
MAIN@
W=40mils
+VDISPLAY_VCC
CV598 0.1U_0402_10V6K
CV597 10U_0603_6.3V6M
HDMI conn
43 HDMI_HPD
43,49 HDMI_CTRL_DAT
43,49 HDMI_CTRL_CLK
43 HDMI_CEC
HDMI_HPD
HDMI_CTRL_DAT
HDMI_CTRL_CLK
HDMI_Reserved
HDMI_CEC
HDMI_L_CLKN
HDMI_L_CLKP
HDMI_L_TX_N0
HDMI_L_TX_P0
HDMI_L_TX_N1
HDMI_L_TX_P1
HDMI_L_TX_N2
HDMI_L_TX_P2
JHDMI1
HP_DET
+5V
DDC/CEC_GND
SDA
SCL
Utility
CEC
CK-
CK_shield
CK+
D0-
D0_shield
D0+
D1-
D1_shield
D1+
D2-
D2_shield
D2+
GND1
GND2
GND3
GND4
ACON_HMRBL-AK120D
CONN@
For EMI Reserve
@CV599 1 2 0.1U_0402_25V6 HDMI_HPD
@CV600 1 2 0.1U_0402_25V6 HDMI_Reserved
@CV601 1 2 0.1U_0402_25V6 HDMI_CEC
Close to JHDMI
+3VS
QX3
MMBT3904WH_SOT323-3
RX6 150K_0402_5%
HDMI_HPD
CX2 0.1U_0402_16V7K
20 HDMI_HPD_PCH
RX8 100K_0402_5%

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: HDMI

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Size | Document Number: LA-F611P | Rev 0.3

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Main Func = 2nd source list

Ref	Option	Part No.	Description
UG25	2ND@	SA00001OF00	S IC TC7SZ32FU SSOP 5P OR 0.65A
UG27	2ND@	SA00001OF00	S IC TC7SZ32FU SSOP 5P OR 0.65A
UG22	2ND@	SA00001DG90	S IC TC7SZ08FU SSOP 5P AND
UG31	2ND@	SA00001DG90	S IC TC7SZ08FU SSOP 5P AND
UV14	2ND@	SA00001DG90	S IC TC7SZ08FU SSOP 5P AND
UV19	2ND@	SA00001DG90	S IC TC7SZ08FU SSOP 5P AND
UV20	2ND@	SA00001DG90	S IC TC7SZ08FU SSOP 5P AND
UE2	2ND@	SA00004H300	S IC TC7SZ05FU SSOP 5P INVERTER OD
UV17	2ND@	SA000080300	S IC G5250Q1T73U SOT-23 3P POWER SWITCH
UG12	2ND@	SA00007QK00	S IC G5016KD1U TDFN2X3 14P LOAD SWITCH
UZ16	2ND@	SA00009PI00	S IC FA7607OTR DFN 8P LOAD SWITCH
UZ7	GEN9_2@	SA00009PI00	S IC FA7607OTR DFN 8P LOAD SWITCH
U1	2ND@	SA00008R900	S IC EM5203AJ-20 SOT23 5P LOAD SWITCH
UL2	2ND@	SA00008R900	S IC EM5203AJ-20 SOT23 5P LOAD SWITCH
UU1	2ND@	SA00008RA00	S IC EM5203J-20 SOT23 5P LOAD SWITCH
UU3	2ND@	SA00008RA00	S IC EM5203J-20 SOT23 5P LOAD SWITCH
UZ1	2ND@	SA00007QK00	S IC G5016KD1U TDFN2X3 14P LOAD SWITCH
UC10	2ND@	SA00005U600	S IC 74AUP1G07GW TSSOP 5P BUFFER
UC16	2ND@	SA00005U600	S IC 74AUP1G07GW TSSOP 5P BUFFER
UZ9	2ND@	SA00008A800	S IC AOZ1334DI-01 DFN 8P SINGLE LOAD SW
UZ15	2ND@	SA00008A800	S IC AOZ1334DI-01 DFN 8P SINGLE LOAD SW
UH3	2ND@	SA007080180	S IC SN74AHC1G08DCKR SC-70 5P AND
DU2	ESD_2@	SCA00001L00	S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD
DU4	ESD_2@	SCA00001L00	S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD
Q1	2ND@	SB00000M700	S TR ME2N7002D-G 1N SOT-23-3 ESD 2KV
Q13	2ND@	SB00000M700	S TR ME2N7002D-G 1N SOT-23-3 ESD 2KV
Q12	TP_WAKE_2@	SB00000PJ00	S TR DMG2301U-7 1P SOT23-3
Q14	2ND@	SB000006A00	S TR MMBT3904 NPN SOT23-3 T/R-3K
D1	2ND@	SCS00009E00	S SCH DIO LBAS40-05LT1G SOT23
YV1	N17P_2@	SJ10000B300	S CRYSTAL 27MHZ 10PF X3G027000BA1H-U
Q25	GEN9_2@	SB00000UO00	DMN65D8LW-7 1N SOT323-3
D7	GEN9_2@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DC2	GEN9_2@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DV9	N17P_2@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DV11	N17P_2@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DE7	2ND@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DE9	2ND@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DG3	2ND@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DG4	2ND@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DG7	2ND@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DG10	2ND@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DH2	2ND@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DN1	2ND@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DN2	2ND@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DZ1	2ND@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
DZ2	2ND@	SCS00008100	S SCH DIO LRB521S-40T1G SOD523-2
YL1	2ND@	SJ10000DE00	S CRYSTAL 25MHZ 10PF X3G025000DA1H-X
YE1	2ND@	SJ10000SX00	S CRYSTAL 32.768KHZ 9PF EXS00A-MU00688
F1	2ND@	SP040001G00	S FUSE 1812L150/24MR 1.5A 24V UL/TUV
TL1	2ND@	SP050006P00	S XFORM_ IH-115-F LAN
CD27	2ND@	SGA00002680	S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9
DU1	ESD_2@	SC300001Y00	AZ1045-04F
DU3	ESD_2@	SC300001Y00	AZ1045-04F
DA5	ESD_2@	SCA00003400	S ZEN ROW L18E3V3CC3-2C 3P C/A SOT-23
DA4	ESD_2@	SCA00002M00	MESC5V02BD03
DA7	ESD_2@	SCA00002M00	MESC5V02BD03
RA13	EMI_2@	SM01000NX00	S SUPPRE_ TAI-TECH HCB1005KF-800T20 0402
RA14	EMI_2@	SM01000NX00	S SUPPRE_ TAI-TECH HCB1005KF-800T20 0402
RA15	EMI_2@	SM01000NX00	S SUPPRE_ TAI-TECH HCB1005KF-800T20 0402
RA16	EMI_2@	SM01000NX00	S SUPPRE_ TAI-TECH HCB1005KF-800T20 0402
L5	EMI_2@	SM01000Q500	S SUPPRE_ TAI-TECH HCB1005KF-221T15 0402
LA1	ESD_2@	SM01000OZ00	S SUPPRE_ TAI-TECH HCB1005PF-330T30 0402
LA2	ESD_2@	SM01000OZ00	S SUPPRE_ TAI-TECH HCB1005PF-330T30 0402
LA3	ESD_2@	SM01000OZ00	S SUPPRE_ TAI-TECH HCB1005PF-330T30 0402
LA4	ESD_2@	SM01000OZ00	S SUPPRE_ TAI-TECH HCB1005PF-330T30 0402
L3	EMI_2@	SM070004400	S COM FI_ PANASONIC EXC24CQ900U
LU1	EMI_2@	SM070004400	S COM FI_ PANASONIC EXC24CQ900U
LU4	EMI_2@	SM070004400	S COM FI_ PANASONIC EXC24CQ900U
LU8	EMI_2@	SM070004400	S COM FI_ PANASONIC EXC24CQ900U
LU9	EMI_2@	SM070004400	S SUPPRE_ TAI-TECH HCB1005KF-221T15 0402
LT2	TBT@EMI_2@	SM070004400	S COM FI_ PANASONIC EXC24CQ900U
LT3	TBT@EMI_2@	SM070004400	S COM FI_ PANASONIC EXC24CQ900U
Q7	2ND@	SB00001H300	S TR LDTA144VLT1G PNP SOT23-3
Q18	2ND@	SB00001H300	S TR LDTA144VLT1G PNP SOT23-3
Q19	2ND@	SB00001H300	S TR LDTA144VLT1G PNP SOT23-3
D6	2ND@	SCS00007H00	S SCH DIO LRB551V-30T1G SOD323-2
DT2	TBT@ESD_2@	SC40000DM00	PESD5V0C1BSF
DT3	TBT@ESD_2@	SC40000DM00	PESD5V0C1BSF
DT4	TBT@ESD_2@	SC40000DM00	PESD5V0C1BSF
DT5	TBT@ESD_2@	SC40000DM00	PESD5V0C1BSF
DT6	TBT@ESD_2@	SC40000DM00	PESD5V0C1BSF
DT7	TBT@ESD_2@	SC40000DM00	PESD5V0C1BSF
DT8	TBT@ESD_2@	SC40000DM00	PESD5V0C1BSF
DT9	TBT@ESD_2@	SC40000DM00	PESD5V0C1BSF
QV10	2ND@	SB000013D00	S TR BSS138PS 2N SC88-6
QG502	2ND@	SB00001DD00	S TR PJT138K 2N SOT363-6
QG503	2ND@	SB00001DD00	S TR PJT138K 2N SOT363-6
QG504	2ND@	SB00001DD00	S TR PJT138K 2N SOT363-6
QG505	2ND@	SB00001DD00	S TR PJT138K 2N SOT363-6
QV1	N17P_2@	SB00001DD00	S TR PJT138K 2N SOT363-6
LT1	TBT_2@	SH00001BK00	S COIL 0.6UH TMPC404012HB-R60MG-Z02 6.6A
LT4	2ND@	SHI0000NV00	S INDUC_ 1UH +-20% CPI160809UF-1R0M-0A7
LG8	N17P_2@	SM01000HU00	S SUPPRE_ TAI-TECH HCB1608KF-300T20 0603
UH14	2ND@	SA007080120	S IC TC7SH08FU SSOP 5P AND
UZ21	2ND@	SA007080120	S IC TC7SH08FU SSOP 5P AND
U2	2ND@	SA007810140	S IC G781P8F MSOP 8P TEMP. SENSOR
Q6	2ND@	SB00000QM00	S TR AP2324GN-HF 1N SOT-23-3
Q9	2ND@	SB00000QM00	S TR AP2324GN-HF 1N SOT-23-3
Q22	2ND@	SB00000QM00	S TR AP2324GN-HF 1N SOT-23-3
QA1	2ND@	SB00000QM00	S TR AP2324GN-HF 1N SOT-23-3
F3	KBBL_2@	SP040006R00	S FUSE 1206L050/15YR 0.5A 15V UL/TUV
QV3	N17P_2@	SB00000S700	S TR MESS138W-G 1N SOT323-3
QV20	N17P_2@	SB00000S700	S TR MESS138W-G 1N SOT323-3
QV21	N17P_2@	SB00000S700	S TR MESS138W-G 1N SOT323-3
Q23	2ND@	SB00000EN00	S TR 2N7002K 1N SOT23-3 PANJIT
Q24	2ND@	SB00000EN00	S TR 2N7002K 1N SOT23-3 PANJIT
Q26	GEN9_2@	SB00000T900	S TR PJ2301 1P SOT23-3
QH4	2ND@	SB00000PV00	S TR L2N7002DW1T1G 2N SC88-6
QG23	N17P_2@	SB00001FN00	S TR LBSS139DW1T1G 2N SOT-363-6 ESD
DT10	TBT@ESD_2@	SC300002C00	S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD
DT11	TBT@ESD_2@	SC300002C00	S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD
LV7	N17P_2@	SM01000NV00	S SUPPRE_ TAI-TECH HCB1005KF-300T25 0402
LV13	N17P_2@	SM01000NV00	S SUPPRE_ TAI-TECH HCB1005KF-300T25 0402

YH2 CH47 CH48 2nd X76 control
X7676731L78

Ref	Option	Part No.	Description
YH2	XTAL_2@	SJ10000YS00	S CRYSTAL 24MHZ 12PF X3S024000BC1H-HU
CH47	XTAL_2@	SE071120J80	S CER CAP 12P 50V J NPO 0402
CH48	XTAL_2@	SE071120J80	S CER CAP 12P 50V J NPO 0402
UT2	TBT_2@	SA000041O00	S IC FL 8M MX25L8006EM2I-12G SOP 8P 3V
QG10	N17P_2@	SB00001GC00	S TR LBSS139WT1G 1N SC70-3
DT16	ESD_2@	SCA00000R00	S ZEN ROW PESD24VS2UT 3P C/A SOT23
DA8	2ND@	SCS00009K00	S SCH DIO BAT54AT-7-F SOT-523

YH1 CH45 CH46 2nd X76 control
X7676731L92

Ref	Option	Part No.	Description
YH1	XTAL_2@	SJ10000SX00	S CRYSTAL 32.768KHZ 9PF EXS00A-MU00688
CH45	XTAL_2@	SE07168AC80	S CER CAP 6.8P 50V C NPO 0402
CH46	XTAL_2@	SE07168AC80	S CER CAP 6.8P 50V C NPO 0402
YT1	TBT_2@	SJ10000U200	S CRYSTAL 25MHZ 20PF X3S025000BK1H-CHV

Ref	Option	Part No.	Description
UH15	2ND@	SA0000A8J10	S IC FL 128M GD25B127DSIGR SOP 8P SPI
UT3	PD_2@	SA00007XO10	S IC FL 2M GD25Q20CTIGR SOP 8P SPI ROM

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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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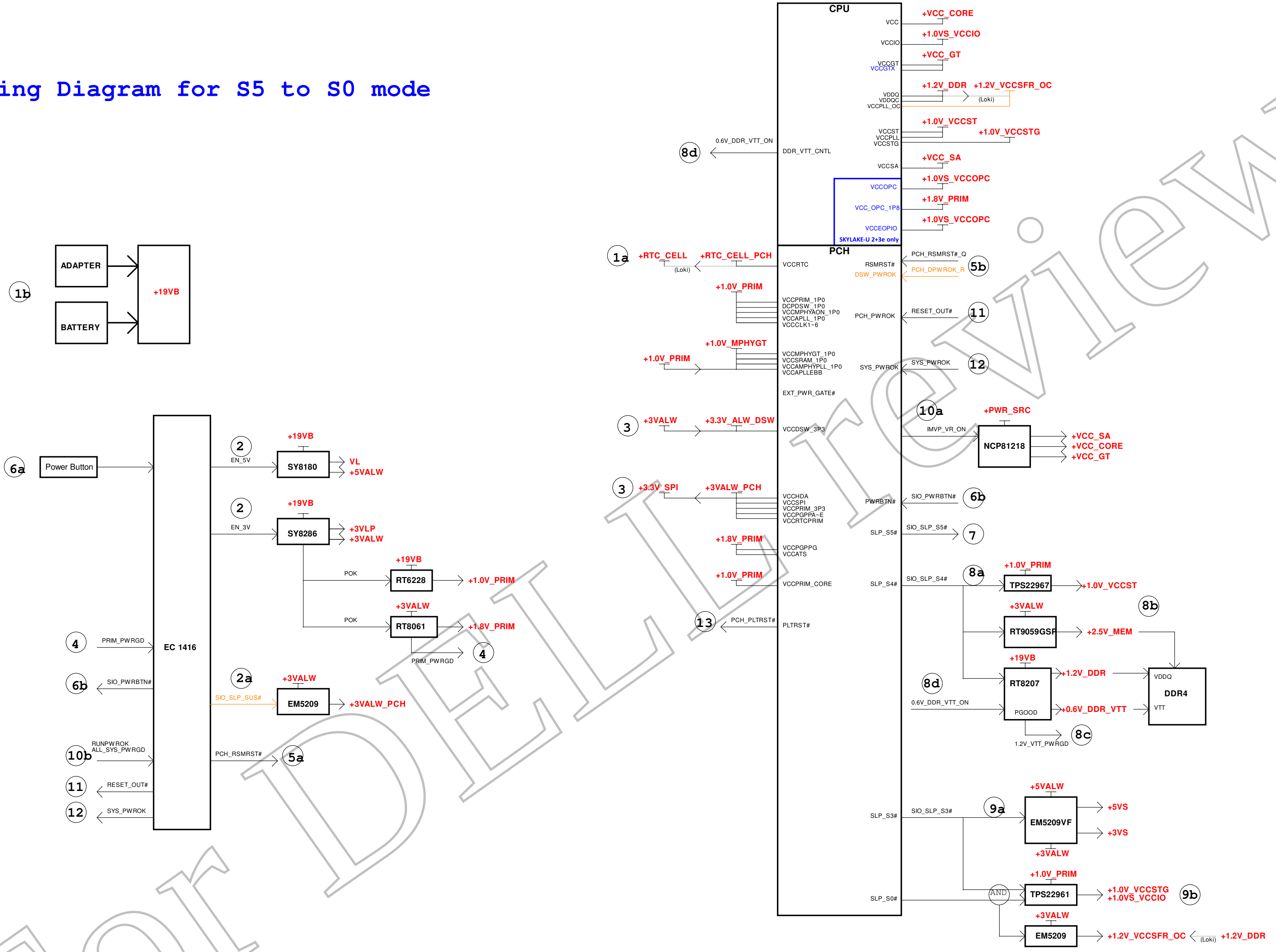
Timing Diagram for S5 to S0 mode



CPU
VCC
+VCC_CORE
VCCIO
+1.0VS_VCCIO
VCCGT
VCCGTX
+VCC_GT
VDDQ
VDDQC
VCCPLL_OC
+1.2V_DDR
+1.2V_VCCSFR_OC
(Loki)
VCCST
VCCPLL
VCCSTG
+1.0V_VCCST
+1.0V_VCCSTG
8d
0.6V_DDR_VTT_ON
DDR_VTT_CNTL
VCCSA
+VCC_SA
VCCOPC
+1.0VS_VCCOPC
VCC_OPC_1P8
+1.8V_PRIM
VCCEOPIO
+1.0VS_VCCOPC
SKYLAKE-U 2+3e only
PCH
1a
+RTC_CELL
(Loki)
+RTC_CELL_PCH
VCCRTC
RSMRST#
PCH_RSMRST#_Q
DSW_PWROK
PCH_DPWROK_R
5b
+1.0V_PRIM
VCCPRIM_1P0
DCPDSW_1P0
VCCMPHYAON_1P0
VCCAPLL_1P0
VCCCLK1~6
PCH_PWROK
RESET_OUT#
11
+1.0V_MPHYGT
+1.0V_PRIM
VCCMPHYGT_1P0
VCCSRAM_1P0
VCCAMPHYPLL_1P0
VCCAPLLEBB
SYS_PWROK
SYS_PWROK
12
EXT_PWR_GATE#
3
+3VALW
+3.3V_ALW_DSW
VCCDSW_3P3
10a
+PWR_SRC
IMVP_VR_ON
NCP81218
+VCC_SA
+VCC_CORE
+VCC_GT
3
+3.3V_SPI
+3VALW_PCH
VCCHDA
VCCSPI
VCCPRIM_3P3
VCCPGPPA~E
VCCRTCPRIM
PWRBTN#
SIO_PWRBTN#
6b
SLP_S5#
SIO_SLP_S5#
7
+1.8V_PRIM
VCCPGPPG
VCCATS
+1.0V_PRIM
VCCPRIM_CORE
SLP_S4#
SIO_SLP_S4#
8a
+1.0V_PRIM
TPS22967
+1.0V_VCCST
8b
+3VALW
RT9059GSP
+2.5V_MEM
13
PCH_PLTRST#
PLTRST#
+19VB
RT8207
+1.2V_DDR
8d
0.6V_DDR_VTT_ON
PGOOD
+0.6V_DDR_VTT
1.2V_VTT_PWRGD
8c
VDDQ
DDR4
VTT
SLP_S3#
SIO_SLP_S3#
9a
+5VALW
EM5209VF
+5VS
+3VS
+3VALW
+1.0V_PRIM
SLP_S0#
AND
TPS22961
+1.0V_VCCSTG
+1.0VS_VCCIO
9b
+3VALW
EM5209
+1.2V_VCCSFR_OC
(Loki)
+1.2V_DDR
1b
ADAPTER
BATTERY
+19VB
6a
Power Button
EC 1416
2
+19VB
EN_5V
SY8180
VL
+5VALW
2
+19VB
EN_3V
SY8286
+3VLP
+3VALW
+19VB
POK
RT6228
+1.0V_PRIM
+3VALW
POK
RT8061
+1.8V_PRIM
PRIM_PWRGD
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PRIM_PWRGD
6b
SIO_PWRBTN#
2a
+3VALW
SIO_SLP_SUS#
EM5209
+3VALW_PCH
10b
RUNPWROK
ALL_SYS_PWRGD
PCH_RSMRST#
5a
11
RESET_OUT#
12
SYS_PWROK

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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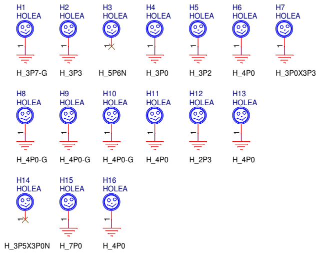
Main Func = Screw hole

Screw hole/FD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H_3P7-G
H2
HOLEA
H_3P3
H3
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H_5P6N
H4
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H_3P0
H5
HOLEA
H_3P2
H6
HOLEA
H_4P0
H7
HOLEA
H_3P0X3P3
H8
HOLEA
H_4P0-G
H9
HOLEA
H_4P0-G
H10
HOLEA
H_4P0-G
H11
HOLEA
H_4P0
H12
HOLEA
H_2P3
H13
HOLEA
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H15
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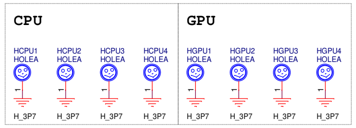
H_4P0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GPU
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HOLEA
H_3P7
HCPU2
HOLEA
H_3P7
HCPU3
HOLEA
H_3P7
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HOLEA
H_3P7
HGPU1
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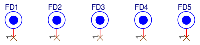
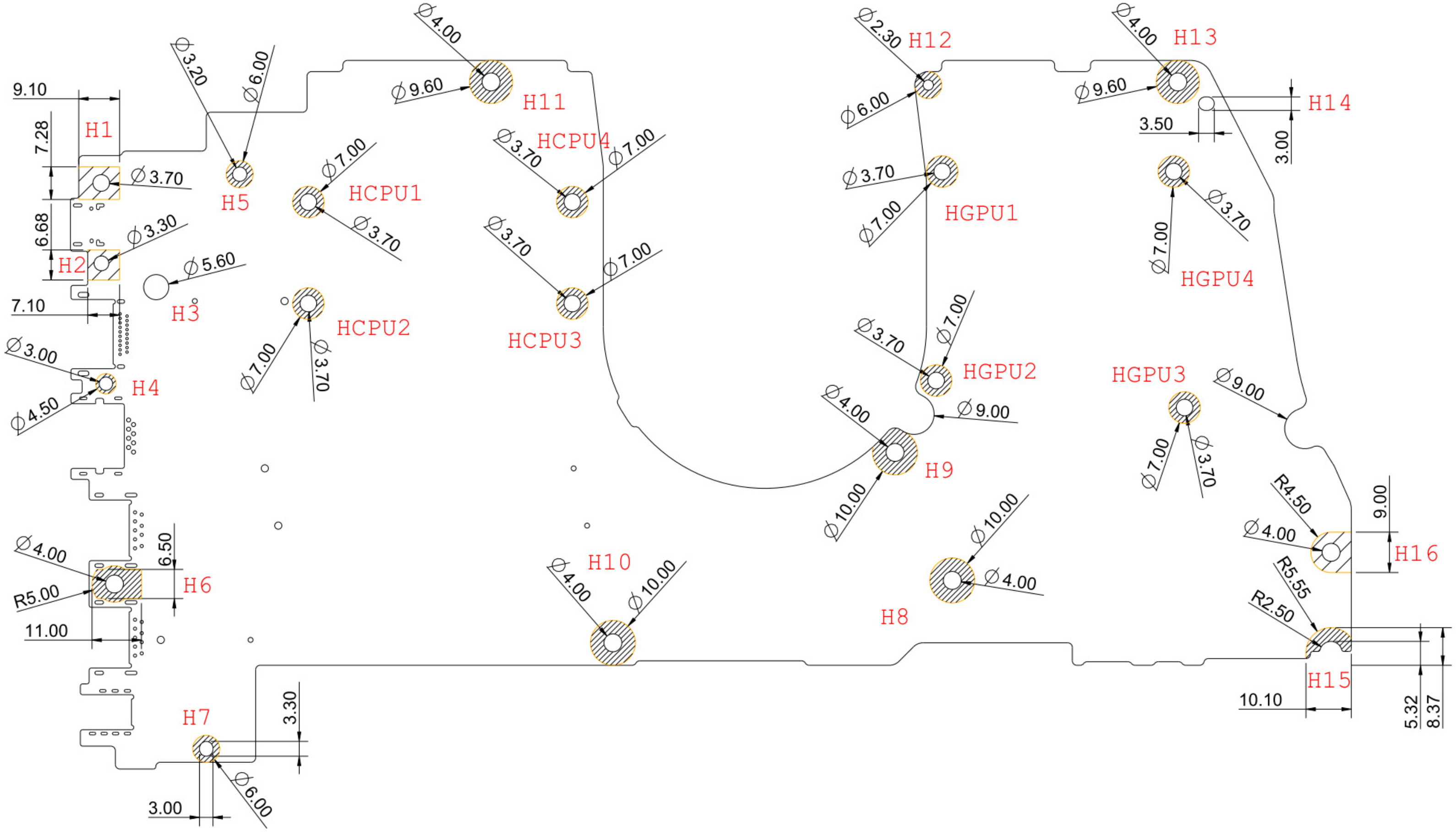
HGPU4
HOLEA
H_3P7


FD1
FD2
FD3
FD4
FD5

Preview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H4
∅3.20
∅6.00
H5
∅4.00
R5.00
6.50
11.00
H6
H7
3.30
3.00
∅6.00
∅4.00
∅9.60
H11
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∅4.00
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H12
∅6.00
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HGPU1
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∅9.00
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∅4.00
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H13
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H14
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3.00
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HGPU4
HGPU3
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∅7.00
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R4.50
∅4.00
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H16
R5.55
R2.50
H15
10.10
5.32
8.37

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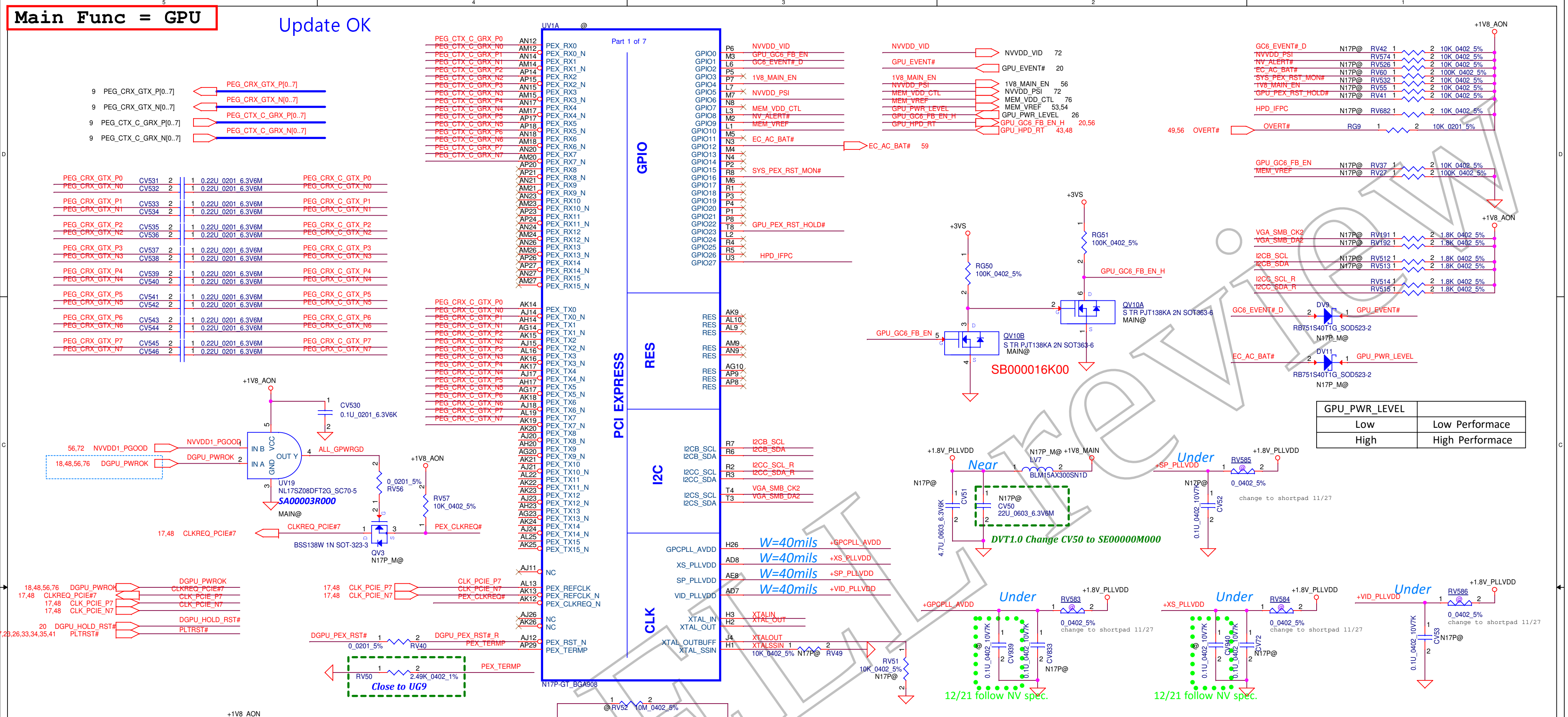
Main Func = GPU

Update OK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Part 1 of 7
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PEG_CRX_GTX_N[0..7]
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PEG_CTX_C_GRX_N[0..7]
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PEX_TX0 … PEX_TX15_N
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PEX_REFCLK_N
PEX_CLKREQ_N
PEX_RST_N
PEX_TERMP
GPIO0 … GPIO27
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GC6_EVENT#_D
1V8_MAIN_EN
NVVDD_PSI
MEM_VDD_CTL
NV_ALERT#
MEM_VREF
EC_AC_BAT#
SYS_PEX_RST_MON#
GPU_PEX_RST_HOLD#
HPD_IFPC
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I2CB_SDA
I2CC_SCL
I2CC_SDA
I2CS_SCL
I2CS_SDA
GPCPLL_AVDD
XS_PLLVDD
SP_PLLVDD
VID_PLLVDD
XTAL_IN
XTAL_OUT
XTAL_OUTBUFF
XTAL_SSIN
W=40mils
+1V8_AON
NVVDD1_PGOOD
DGPU_PWROK
ALL_GPWRGD
UV19
NL17SZ08DFT2G_SC70-5
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MAIN@
CLKREQ_PCIE#7
QV3
BSS138W 1N SOT-323-3
N17P_M@
CLK_PCIE_P7
CLK_PCIE_N7
DGPU_HOLD_RST#
PLTRST#
DGPU_PEX_RST#
RV50
2.49K_0402_1%
Close to UG9
N17P-GT_BGA908
QV10A
QV10B
S TR PJT138KA 2N SOT363-6
SB000016K00
GPU_GC6_FB_EN_H
DV9
DV11
RB751S40T1G_SOD523-2
GPU_EVENT#
GPU_PWR_LEVEL
OVERT#
+3VS
+1V8_AON
+1.8V_PLLVDD
Near
Under
LV7
BLM15AX300SN1D
CV50
22U_0603_6.3V6M
DVT1.0 Change CV50 to SE00000M000
change to shortpad 11/27
12/21 follow NV spec.

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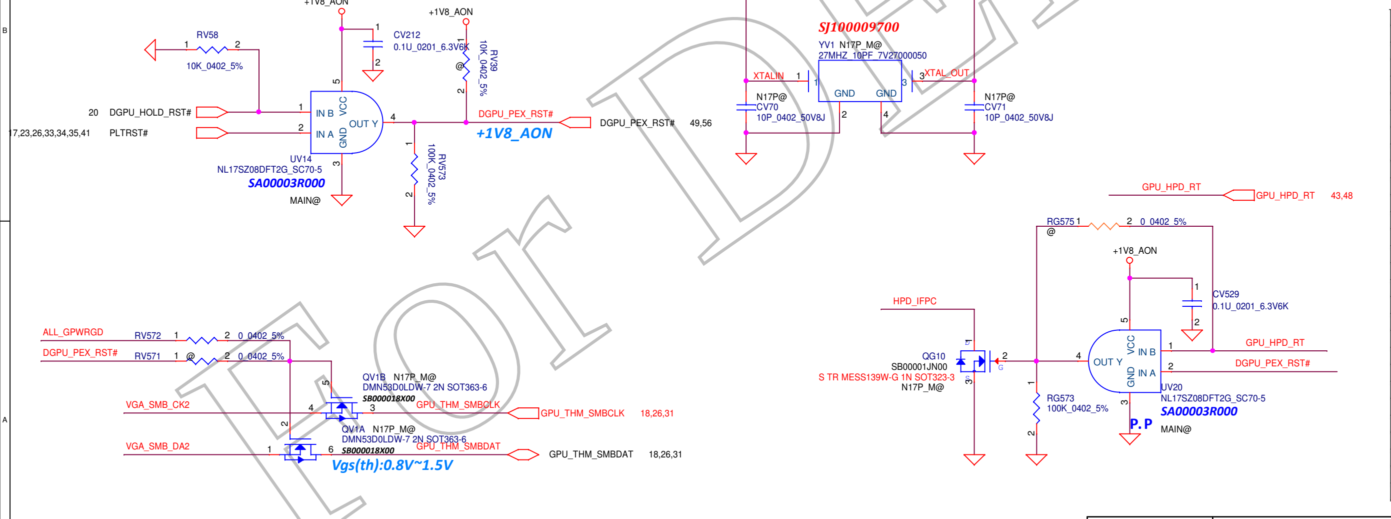
Low	Low Performance
High	High Performance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XTALIN
XTAL_OUT
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CV71
10P_0402_50V8J
UV14
NL17SZ08DFT2G_SC70-5
SA00003R000
DGPU_HOLD_RST#
PLTRST#
DGPU_PEX_RST#
+1V8_AON
RV573
100K_0402_5%
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DGPU_PEX_RST#
QV1B
QV1A
DMN53D0LDW-7 2N SOT363-6
SB000018X00
VGA_SMB_CK2
VGA_SMB_DA2
GPU_THM_SMBCLK
GPU_THM_SMBDAT
Vgs(th):0.8V~1.5V
HPD_IFPC
QG10
SB00001JN00
S TR MESS139W-G 1N SOT323-3
GPU_HPD_RT
RG575
RG573
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UV20
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P.P
MAIN@
CV529
0.1U_0201_6.3V6K

GPIO Number	I/O	GPIO Name	Function Description
GPIO0	O	NVVDD_PWM	PWM Output to control NVVDD(0 to1V8 PWM output)
GPIO1	O	GC6M:GC6_FB_EN	FB Enable for GC6 2.1
GPIO2	I	GC6M:GPU_EVENT*/WAKE*	GPU wake signal for GC6 2.1
GPIO3	O	NVVDDS_PWM	For MAX-Q detection.
GPIO4	O	GC6M:1V8_MAIN_EN	GPU power sequencing for GC6 2.1
GPIO5	I	FRM_CLK*	Active low Frame Lock
GPIO6		NVVDD_PSI*/NVVDDS_PSI*	Phase Shedding(Optional, check with VR Spec)
GPIO7	O	LCD_BL_PWM	Panel Backlight enable Control signal to turn on a logo LED
GPIO8	O	MEM_VDD_CTL	Memory voltage control
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert
GPIO10	O	MEM_VREF_CTL	Memory VREF Control
GPIO11	O	LCD_VDD	Panel Power enable(100 kΩ PD)
GPIO12	I	PWM_LEVEL	AC power detect for PWR supply overdraw input
GPIO13	O	LCD_BLEN	LCD Panel Backlight
GPIO14	I	HPD_IFPA*	Hot Plug Detect for IFPA(Inverted input)
GPIO15	I	HPD_IFPB*	Hot Plug Detect for IFPB(Inverted input)
GPIO16	O	GC6M:SYS_PEX_RST_MON*	System side PCIe reset monitor
GPIO17	I	HPD_IFPD*	Hot Plug Detect for IFPD(Inverted input)
GPIO18	I	HPD_IFPE*	Hot Plug Detect for IFPE(Inverted input)
GPIO19	O	3D Vision/STEREO	3D Vision L/R Signal
GPIO20	I/O	GC5_MODE	Phase Shedding,Optional, check with VR Spec.
GPIO21	I/O	UNUSED	
GPIO22	I/O	UNUSED	
GPIO23	I/O	GC6M:GPU_PEX_RST_HOLD*	GPU PCIe self-reset control
GPIO24	I	HPD_IFPF*	Hot Plug Detect for IFPF(Inverted input)
GPIO25	I/O	UNUSED	
GPIO26	I/O	UNUSED	
GPIO27	I	HPD_IFPC*	Hot Plug Detect for IFPC(Inverted input)

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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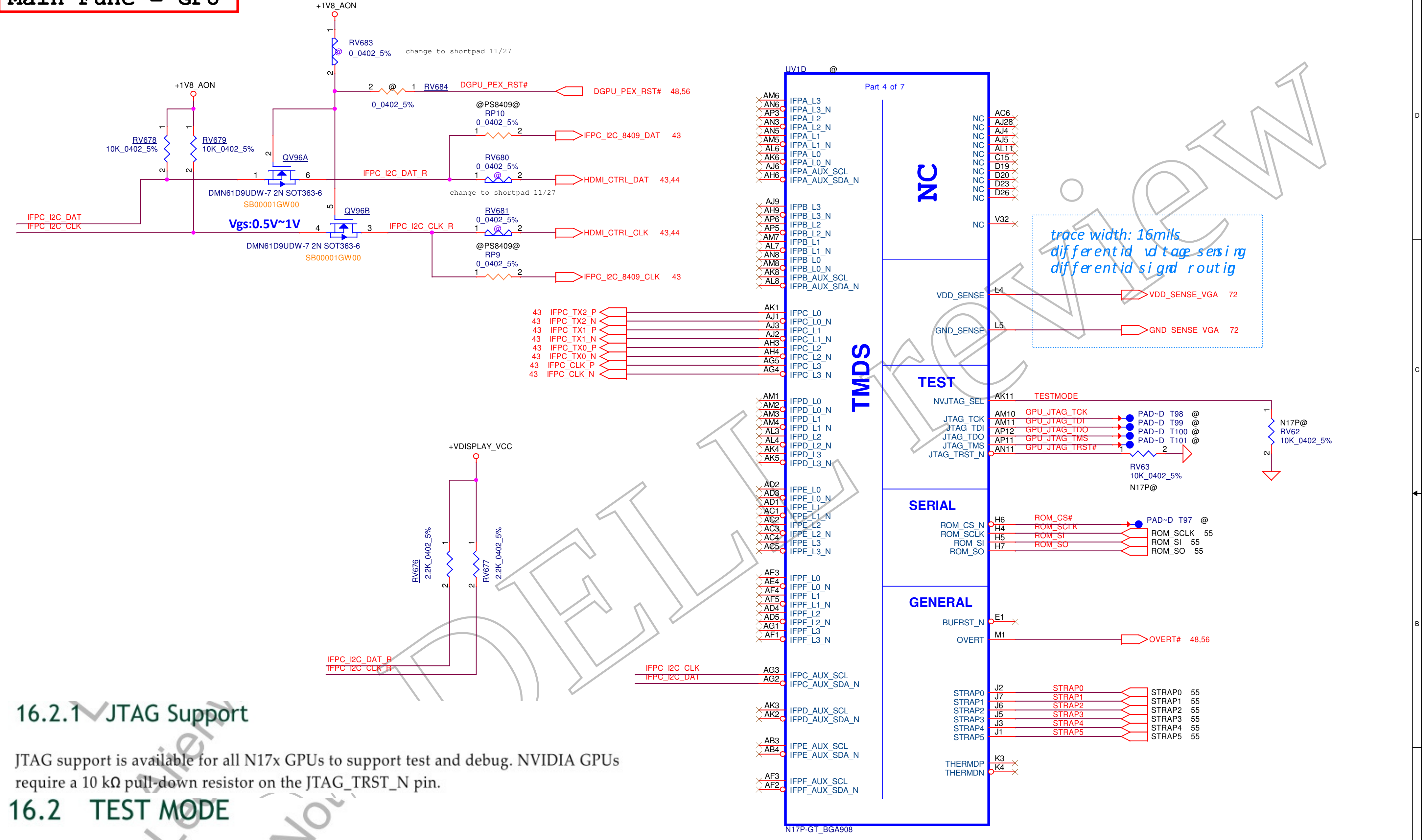
Compal Electronics, Inc.

Title
N17P-G1(1/9)PCIE/DAC/GPIO

Size
Document Number
LA-F611P
Rev
0.3

Date: Thursday, March 22, 2018

Main Func = GPU



+1V8_AON
RV683
0_0402_5%
change to shortpad 11/27
RV684
DGPU_PEX_RST#
0_0402_5%
DGPU_PEX_RST# 48,56
@PS8409@
RP10
0_0402_5%
IFPC_I2C_8409_DAT 43
+1V8_AON
RV678
10K_0402_5%
RV679
10K_0402_5%
QV96A
DMN61D9UDW-7 2N SOT363-6
SB00001GW00
IFPC_I2C_DAT_R
RV680
0_0402_5%
HDMI_CTRL_DAT 43,44
change to shortpad 11/27
IFPC_I2C_DAT
IFPC_I2C_CLK
Vgs:0.5V~1V
QV96B
IFPC_I2C_CLK_R
RV681
0_0402_5%
HDMI_CTRL_CLK 43,44
DMN61D9UDW-7 2N SOT363-6
SB00001GW00
@PS8409@
RP9
0_0402_5%
IFPC_I2C_8409_CLK 43
43 IFPC_TX2_P
43 IFPC_TX2_N
43 IFPC_TX1_P
43 IFPC_TX1_N
43 IFPC_TX0_P
43 IFPC_TX0_N
43 IFPC_CLK_P
43 IFPC_CLK_N
+VDISPLAY_VCC
RV676
2.2K_0402_5%
RV677
2.2K_0402_5%
IFPC_I2C_DAT_R
IFPC_I2C_CLK_R
IFPC_I2C_CLK
IFPC_I2C_DAT
UV1D @
Part 4 of 7
IFPA_L3
IFPA_L3_N
IFPA_L2
IFPA_L2_N
IFPA_L1
IFPA_L1_N
IFPA_L0
IFPA_L0_N
IFPA_AUX_SCL
IFPA_AUX_SDA_N
IFPB_L3
IFPB_L3_N
IFPB_L2
IFPB_L2_N
IFPB_L1
IFPB_L1_N
IFPB_L0
IFPB_L0_N
IFPB_AUX_SCL
IFPB_AUX_SDA_N
IFPC_L0
IFPC_L0_N
IFPC_L1
IFPC_L1_N
IFPC_L2
IFPC_L2_N
IFPC_L3
IFPC_L3_N
IFPD_L0
IFPD_L0_N
IFPD_L1
IFPD_L1_N
IFPD_L2
IFPD_L2_N
IFPD_L3
IFPD_L3_N
IFPE_L0
IFPE_L0_N
IFPE_L1
IFPE_L1_N
IFPE_L2
IFPE_L2_N
IFPE_L3
IFPE_L3_N
IFPF_L0
IFPF_L0_N
IFPF_L1
IFPF_L1_N
IFPF_L2
IFPF_L2_N
IFPF_L3
IFPF_L3_N
IFPC_AUX_SCL
IFPC_AUX_SDA_N
IFPD_AUX_SCL
IFPD_AUX_SDA_N
IFPE_AUX_SCL
IFPE_AUX_SDA_N
IFPF_AUX_SCL
IFPF_AUX_SDA_N
TMDS
NC
VDD_SENSE
GND_SENSE
VDD_SENSE_VGA 72
GND_SENSE_VGA 72
trace width: 16mils
differential voltage sensing
differential signal routing
TEST
NVJTAG_SEL
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST_N
TESTMODE
GPU_JTAG_TCK
GPU_JTAG_TDI
GPU_JTAG_TDO
GPU_JTAG_TMS
GPU_JTAG_TRST#
PAD~D T98 @
PAD~D T99 @
PAD~D T100 @
PAD~D T101 @
N17P@
RV62
10K_0402_5%
RV63
10K_0402_5%
N17P@
SERIAL
ROM_CS_N
ROM_SCLK
ROM_SI
ROM_SO
ROM_CS#
PAD~D T97 @
ROM_SCLK 55
ROM_SI 55
ROM_SO 55
GENERAL
BUFRST_N
OVERT
OVERT# 48,56
STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
STRAP5
STRAP0 55
STRAP1 55
STRAP2 55
STRAP3 55
STRAP4 55
STRAP5 55
THERMDP
THERMDN
N17P-GT_BGA908

16.2.1 JTAG Support

JTAG support is available for all N17x GPUs to support test and debug. NVIDIA GPUs require a 10 kΩ pull-down resistor on the JTAG_TRST_N pin.

16.2 TEST MODE

By default, pull-down the TESTMODE pin (pin name is NVJTAG_SEL in some N17x pinouts) to GND with a 10 kΩ resistor. For ICT/boundary scan requirements, contact your NVIDIA AE.

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

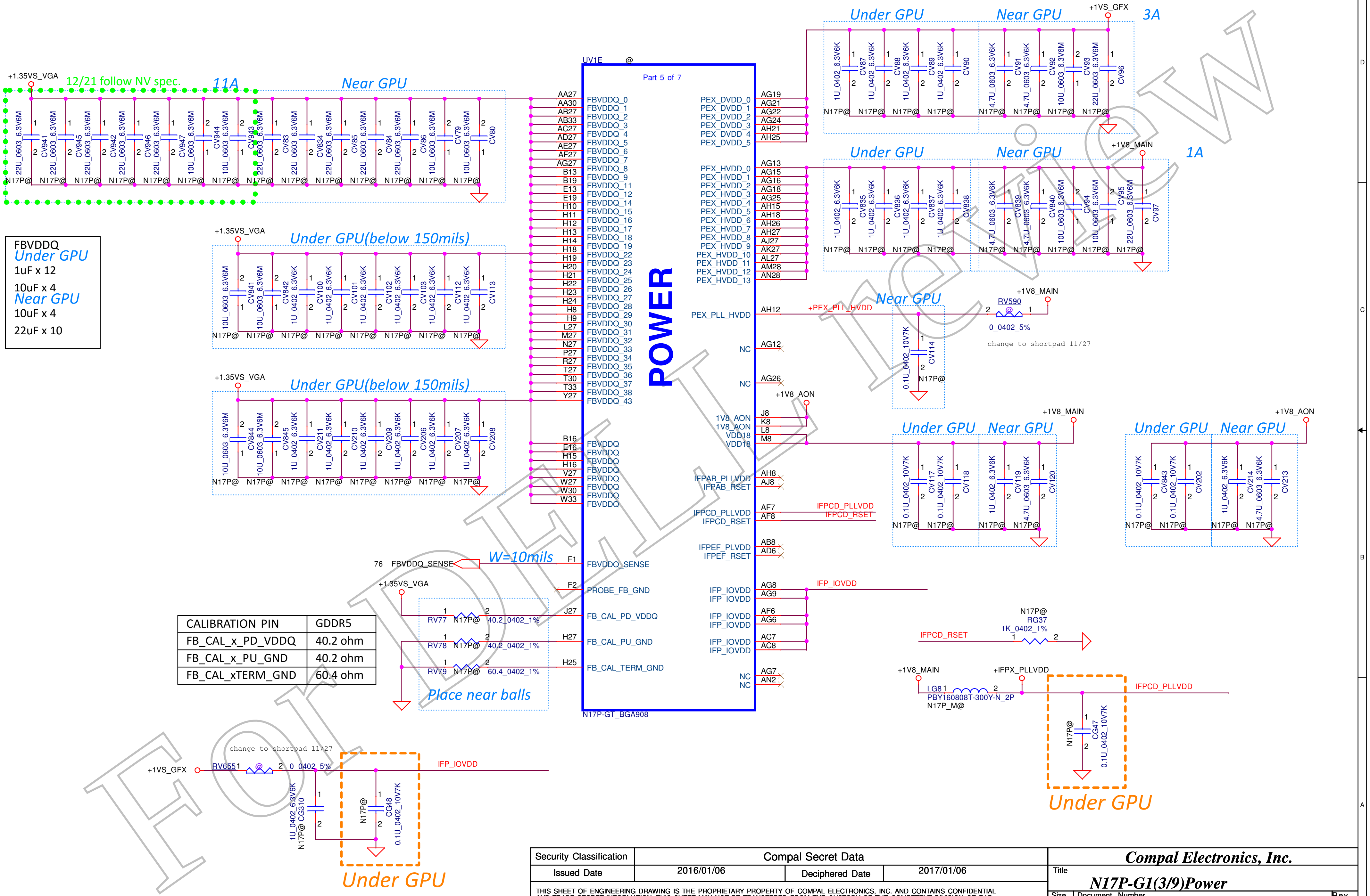
Title
N17P-G1(2/9)eDP/HDMI/mDP

Size Document Number
LA-F611P

Rev
0.3

Date: Thursday, March 22, 2018 Sheet 49 of 78

Main Func = GPU



UV1E
Part 5 of 7
POWER
N17P-GT_BGA908
+1.35VS_VGA
12/21 follow NV spec.
11A
Near GPU
Under GPU(below 150mils)
Under GPU
3A
1A
+1VS_GFX
+1V8_MAIN
+1V8_AON
+PEX_PLL_HVDD
RV590
0_0402_5%
change to shortpad 11/27
FBVDDQ_0
FBVDDQ_43
FBVDDQ
PEX_DVDD_0
PEX_DVDD_5
PEX_HVDD_0
PEX_HVDD_13
PEX_PLL_HVDD
NC
1V8_AON
VDD18
IFPAB_PLLVDD
IFPAB_RSET
IFPCD_PLLVDD
IFPCD_RSET
IFPEF_PLVDD
IFPEF_RSET
IFP_IOVDD
76
FBVDDQ_SENSE
W=10mils
PROBE_FB_GND
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
RV77
RV78
RV79
40.2_0402_1%
60.4_0402_1%
Place near balls
N17P@
RG37
1K_0402_1%
+IFPX_PLLVDD
LG8
PBY160808T-300Y-N_2P
N17P_M@
CG47
0.1U_0402_10V7K
RV6551
2_0_0402_5%
CG310
CG48
1U_0402_6.3V6K
22U_0603_6.3V6M
10U_0603_6.3V6M
4.7U_0603_6.3V6K

FBVDDQ
Under GPU
1uF x 12
10uF x 4
Near GPU
10uF x 4
22uF x 10

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm

Under GPU

Under GPU

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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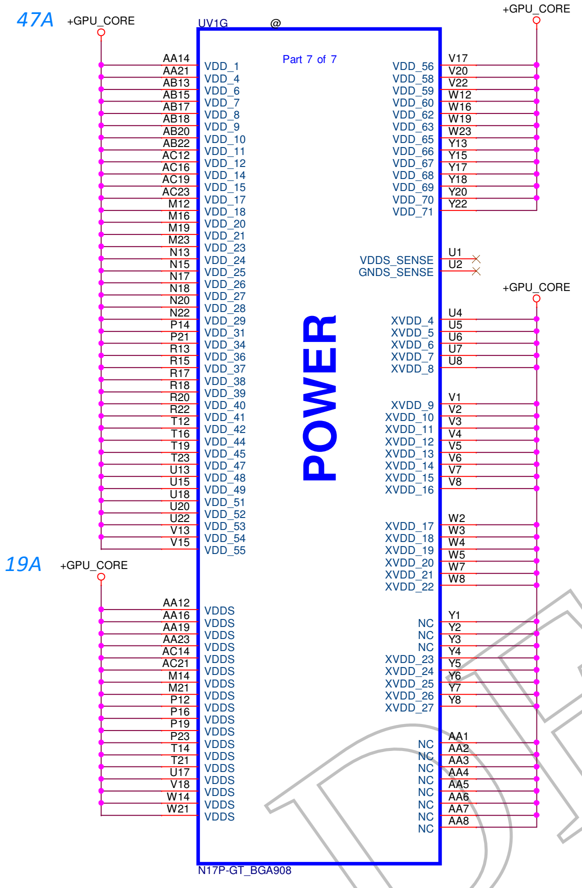
Compal Electronics, Inc.

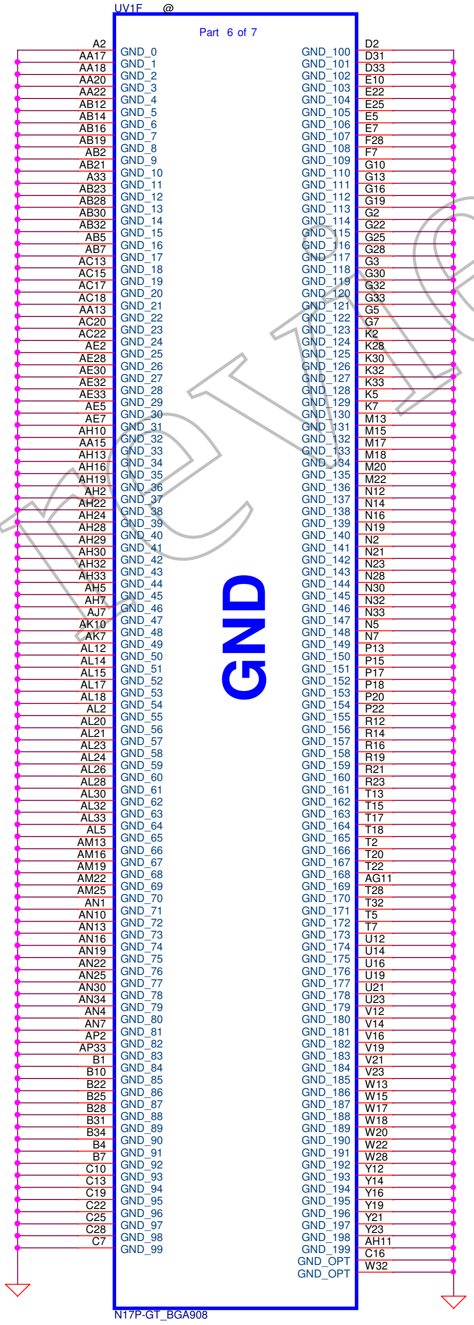
Title *N17P-G1(3/9)Power*

Size Document Number *LA-F611P* Rev 0.3

Date: Thursday, March 22, 2018 Sheet 50 of 78

Main Func = GPU


47A
+GPU_CORE
UV1G
@
Part 7 of 7
POWER
AA14 VDD_1
AA21 VDD_4
AB13 VDD_6
AB15 VDD_7
AB17 VDD_8
AB18 VDD_9
AB20 VDD_10
AB22 VDD_11
AC12 VDD_12
AC16 VDD_14
AC19 VDD_15
AC23 VDD_17
M12 VDD_18
M16 VDD_20
M19 VDD_21
M23 VDD_23
N13 VDD_24
N15 VDD_25
N17 VDD_26
N18 VDD_27
N20 VDD_28
N22 VDD_29
P14 VDD_31
P21 VDD_34
R13 VDD_36
R15 VDD_37
R17 VDD_38
R18 VDD_39
R20 VDD_40
R22 VDD_41
T12 VDD_42
T16 VDD_44
T19 VDD_45
T23 VDD_47
U13 VDD_48
U15 VDD_49
U18 VDD_51
U20 VDD_52
U22 VDD_53
V13 VDD_54
V15 VDD_55
19A
+GPU_CORE
AA12 VDDS
AA16 VDDS
AA19 VDDS
AA23 VDDS
AC14 VDDS
AC21 VDDS
M14 VDDS
M21 VDDS
P12 VDDS
P16 VDDS
P19 VDDS
P23 VDDS
T14 VDDS
T21 VDDS
U17 VDDS
V18 VDDS
W14 VDDS
W21 VDDS
+GPU_CORE
VDD_56 V17
VDD_58 V20
VDD_59 V22
VDD_60 W12
VDD_62 W16
VDD_63 W19
VDD_65 W23
VDD_66 Y13
VDD_67 Y15
VDD_68 Y17
VDD_69 Y18
VDD_70 Y20
VDD_71 Y22
VDDS_SENSE U1
GNDS_SENSE U2
+GPU_CORE
XVDD_4 U4
XVDD_5 U5
XVDD_6 U6
XVDD_7 U7
XVDD_8 U8
XVDD_9 V1
XVDD_10 V2
XVDD_11 V3
XVDD_12 V4
XVDD_13 V5
XVDD_14 V6
XVDD_15 V7
XVDD_16 V8
XVDD_17 W2
XVDD_18 W3
XVDD_19 W4
XVDD_20 W5
XVDD_21 W7
XVDD_22 W8
NC Y1
NC Y2
NC Y3
XVDD_23 Y4
XVDD_24 Y5
XVDD_25 Y6
XVDD_26 Y7
XVDD_27 Y8
NC AA1
NC AA2
NC AA3
NC AA4
NC AA5
NC AA6
NC AA7
NC AA8
N17P-GT_BGA908


UV1F
@
Part 6 of 7
GND
A2 GND_0
AA17 GND_1
AA18 GND_2
AA20 GND_3
AA22 GND_4
AB12 GND_5
AB14 GND_6
AB16 GND_7
AB19 GND_8
AB2 GND_9
AB21 GND_10
A33 GND_11
AB23 GND_12
AB28 GND_13
AB30 GND_14
AB32 GND_15
AB5 GND_16
AB7 GND_17
AC13 GND_18
AC15 GND_19
AC17 GND_20
AC18 GND_21
AA13 GND_22
AC20 GND_23
AC22 GND_24
AE2 GND_25
AE28 GND_26
AE30 GND_27
AE32 GND_28
AE33 GND_29
AE5 GND_30
AE7 GND_31
AH10 GND_32
AA15 GND_33
AH13 GND_34
AH16 GND_35
AH19 GND_36
AH2 GND_37
AH22 GND_38
AH24 GND_39
AH28 GND_40
AH29 GND_41
AH30 GND_42
AH32 GND_43
AH33 GND_44
AH5 GND_45
AH7 GND_46
AJ7 GND_47
AK10 GND_48
AK7 GND_49
AL12 GND_50
AL14 GND_51
AL15 GND_52
AL17 GND_53
AL18 GND_54
AL2 GND_55
AL20 GND_56
AL21 GND_57
AL23 GND_58
AL24 GND_59
AL26 GND_60
AL28 GND_61
AL30 GND_62
AL32 GND_63
AL33 GND_64
AL5 GND_65
AM13 GND_66
AM16 GND_67
AM19 GND_68
AM22 GND_69
AM25 GND_70
AN1 GND_71
AN10 GND_72
AN13 GND_73
AN16 GND_74
AN19 GND_75
AN22 GND_76
AN25 GND_77
AN30 GND_78
AN34 GND_79
AN4 GND_80
AN7 GND_81
AP2 GND_82
AP33 GND_83
B1 GND_84
B10 GND_85
B22 GND_86
B25 GND_87
B28 GND_88
B31 GND_89
B34 GND_90
B4 GND_91
B7 GND_92
C10 GND_93
C13 GND_94
C19 GND_95
C22 GND_96
C25 GND_97
C28 GND_98
C7 GND_99
GND_100 D2
GND_101 D31
GND_102 D33
GND_103 E10
GND_104 E22
GND_105 E25
GND_106 E5
GND_107 E7
GND_108 F28
GND_109 F7
GND_110 G10
GND_111 G13
GND_112 G16
GND_113 G19
GND_114 G2
GND_115 G22
GND_116 G25
GND_117 G28
GND_118 G3
GND_119 G30
GND_120 G32
GND_121 G33
GND_122 G5
GND_123 G7
GND_124 K2
GND_125 K28
GND_126 K30
GND_127 K32
GND_128 K33
GND_129 K5
GND_130 K7
GND_131 M13
GND_132 M15
GND_133 M17
GND_134 M18
GND_135 M20
GND_136 M22
GND_137 N12
GND_138 N14
GND_139 N16
GND_140 N19
GND_141 N2
GND_142 N21
GND_143 N23
GND_144 N28
GND_145 N30
GND_146 N32
GND_147 N33
GND_148 N5
GND_149 N7
GND_150 P13
GND_151 P15
GND_152 P17
GND_153 P18
GND_154 P20
GND_155 P22
GND_156 R12
GND_157 R14
GND_158 R16
GND_159 R19
GND_160 R21
GND_161 R23
GND_162 T13
GND_163 T15
GND_164 T17
GND_165 T18
GND_166 T2
GND_167 T20
GND_168 T22
GND_169 AG11
GND_170 T28
GND_171 T32
GND_172 T5
GND_173 T7
GND_174 U12
GND_175 U14
GND_176 U16
GND_177 U19
GND_178 U21
GND_179 U23
GND_180 V12
GND_181 V14
GND_182 V16
GND_183 V19
GND_184 V21
GND_185 V23
GND_186 W13
GND_187 W15
GND_188 W17
GND_189 W18
GND_190 W20
GND_191 W22
GND_192 W28
GND_193 Y12
GND_194 Y14
GND_195 Y16
GND_196 Y19
GND_197 Y21
GND_198 Y23
GND_199 AH11
GND_OPT C16
GND_OPT W32
N17P-GT_BGA908

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title N17P-G1(4/9)VGA CORE/GND
				Size Document Number LA-F611P Rev 0.3
				Date: Thursday, March 22, 2018 Sheet 51 of 78

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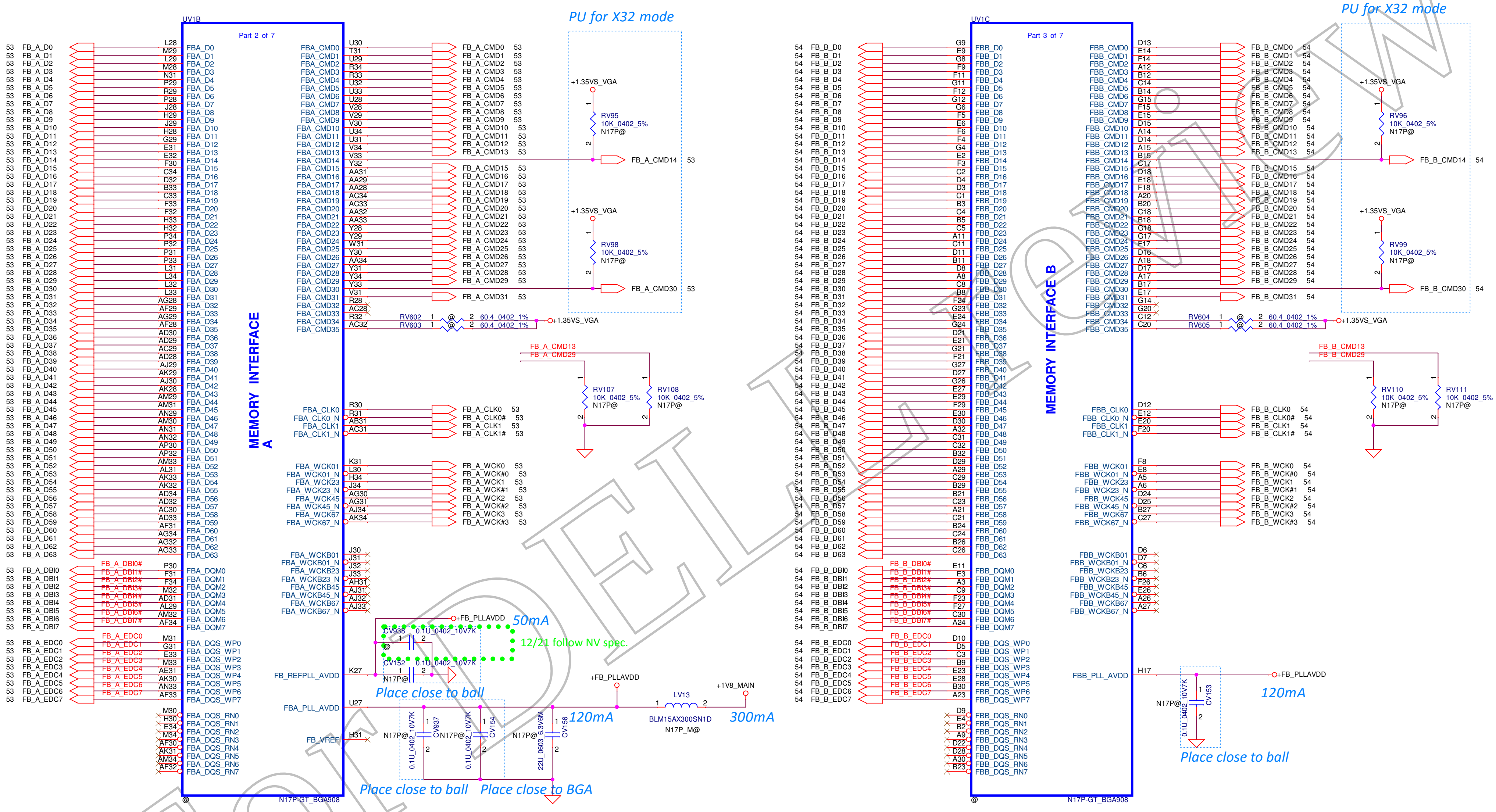
Main Func = GPU


UV1B
Part 2 of 7
MEMORY INTERFACE A
FBA_D0 … FBA_D63
FB_A_D0 … FB_A_D63
FBA_CMD0 … FBA_CMD35
FB_A_CMD0 … FB_A_CMD31
FBA_CLK0
FBA_CLK0_N
FBA_CLK1
FBA_CLK1_N
FB_A_CLK0
FB_A_CLK0#
FB_A_CLK1
FB_A_CLK1#
FBA_WCK01
FBA_WCK01_N
FBA_WCK23
FBA_WCK23_N
FBA_WCK45
FBA_WCK45_N
FBA_WCK67
FBA_WCK67_N
FB_A_WCK0
FB_A_WCK#0
FB_A_WCK1
FB_A_WCK#1
FB_A_WCK2
FB_A_WCK#2
FB_A_WCK3
FB_A_WCK#3
FBA_WCKB01
FBA_WCKB01_N
FBA_WCKB23
FBA_WCKB23_N
FBA_WCKB45
FBA_WCKB45_N
FBA_WCKB67
FBA_WCKB67_N
FBA_DQM0 … FBA_DQM7
FB_A_DBI0 … FB_A_DBI7
FB_A_DBI0# … FB_A_DBI7#
FBA_DQS_WP0 … FBA_DQS_WP7
FB_A_EDC0 … FB_A_EDC7
FBA_DQS_RN0 … FBA_DQS_RN7
FB_REFPLL_AVDD
FBA_PLL_AVDD
FB_VREF
N17P-GT_BGA908
PU for X32 mode
+1.35VS_VGA
RV95
RV98
10K_0402_5%
N17P@
FB_A_CMD14
FB_A_CMD30
RV602
RV603
60.4_0402_1%
FB_A_CMD13
FB_A_CMD29
RV107
RV108
+FB_PLLAVDD
50mA
CV938
0.1U_0402_10V7K
12/21 follow NV spec.
CV152
Place close to ball
+FB_PLLAVDD
LV13
BLM15AX300SN1D
N17P_M@
+1V8_MAIN
120mA
300mA
CV937
CV154
CV156
22U_0603_6.3V6M
Place close to ball
Place close to BGA
UV1C
Part 3 of 7
MEMORY INTERFACE B
FBB_D0 … FBB_D63
FB_B_D0 … FB_B_D63
FBB_CMD0 … FBB_CMD35
FB_B_CMD0 … FB_B_CMD31
FBB_CLK0
FBB_CLK0_N
FBB_CLK1
FBB_CLK1_N
FB_B_CLK0
FB_B_CLK0#
FB_B_CLK1
FB_B_CLK1#
FBB_WCK01 … FBB_WCK67_N
FB_B_WCK0 … FB_B_WCK#3
FBB_WCKB01 … FBB_WCKB67_N
FBB_DQM0 … FBB_DQM7
FB_B_DBI0 … FB_B_DBI7
FBB_DQS_WP0 … FBB_DQS_WP7
FB_B_EDC0 … FB_B_EDC7
FBB_DQS_RN0 … FBB_DQS_RN7
FBB_PLL_AVDD
PU for X32 mode
RV96
RV99
FB_B_CMD14
FB_B_CMD30
RV604
RV605
FB_B_CMD13
FB_B_CMD29
RV110
RV111
CV153
120mA
Place close to ball
N17P-GT_BGA908

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title N17P-G1(5/9)MEM Interface
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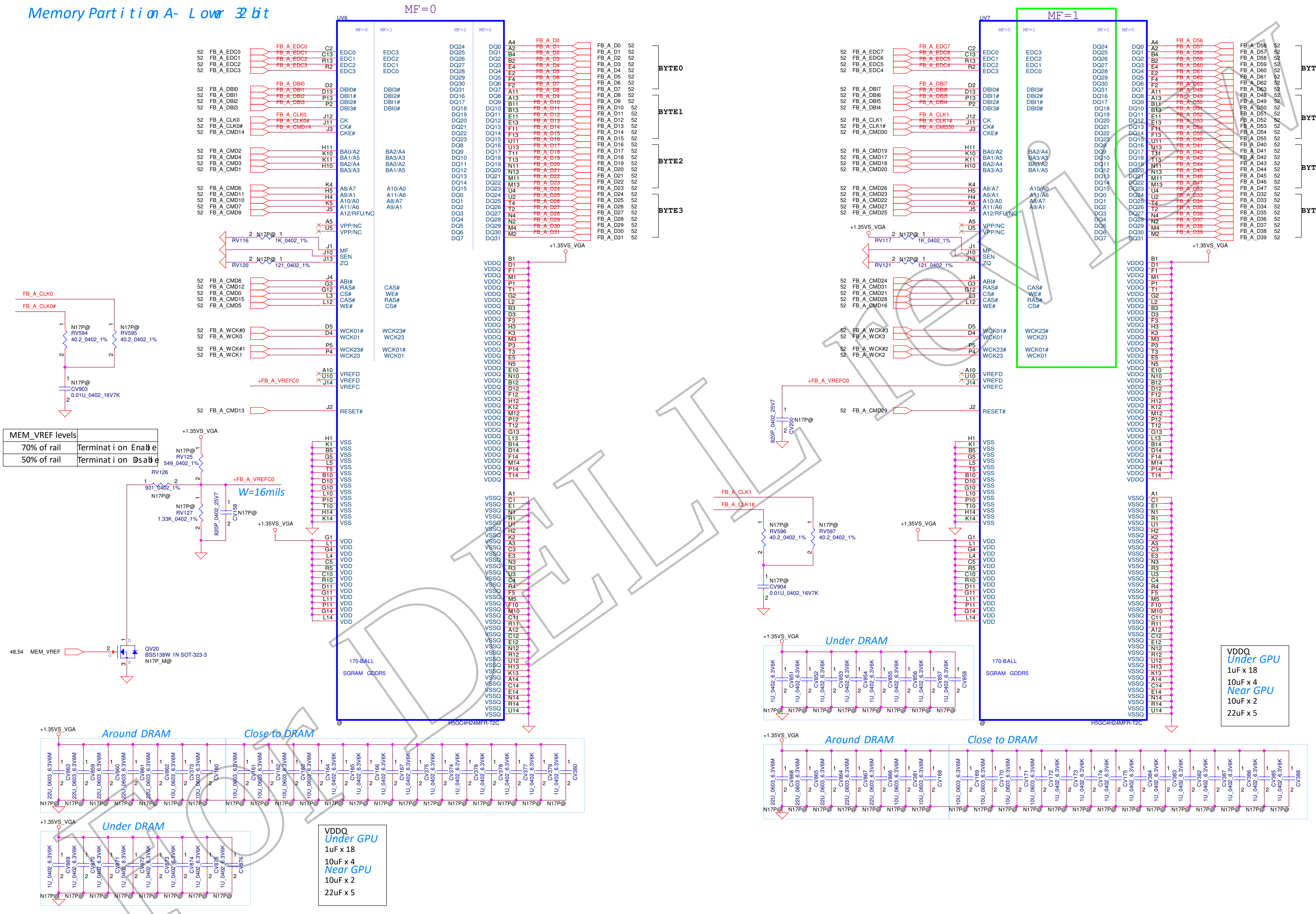
				Date: Thursday, March 22, 2018 Sheet 52 of 78

Main Func = GDDR5



Memory Partition A - Lower 32 bit
MF=0
MF=1
UV6
UV7
BYTE0
BYTE1
BYTE2
BYTE3
BYTE4
BYTE5
BYTE6
BYTE7
FB_A_CLK0
FB_A_CLK0#
FB_A_CLK1
FB_A_CLK1#
+FB_A_VREFC0
W=16mils
MEM_VREF levels
70% of rail
Terminati on Enable
50% of rail
Terminati on Disable
+1.35VS_VGA
48,54 MEM_VREF
QV20
BSS138W 1N SOT-323-3
N17P_M@
RV594 40.2_0402_1%
RV595 40.2_0402_1%
RV596 40.2_0402_1%
RV597 40.2_0402_1%
RV116 1K_0402_1%
RV120 121_0402_1%
RV117 1K_0402_1%
RV121 121_0402_1%
RV125 549_0402_1%
RV126 931_0402_1%
RV127 1.33K_0402_1%
CV903 0.01U_0402_16V7K
CV904 0.01U_0402_16V7K
CV158 820P_0402_25V7
CV200 820P_0402_25V7
170-BALL
SGRAM GDDR5
H5GC4H24MFR-T2C
Around DRAM
Close to DRAM
Under DRAM
VDDQ
Under GPU
1uF x 18
10uF x 4
Near GPU
10uF x 2
22uF x 5

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Title
N17P-G1(6/9)GDDR5_A

Size Document Number
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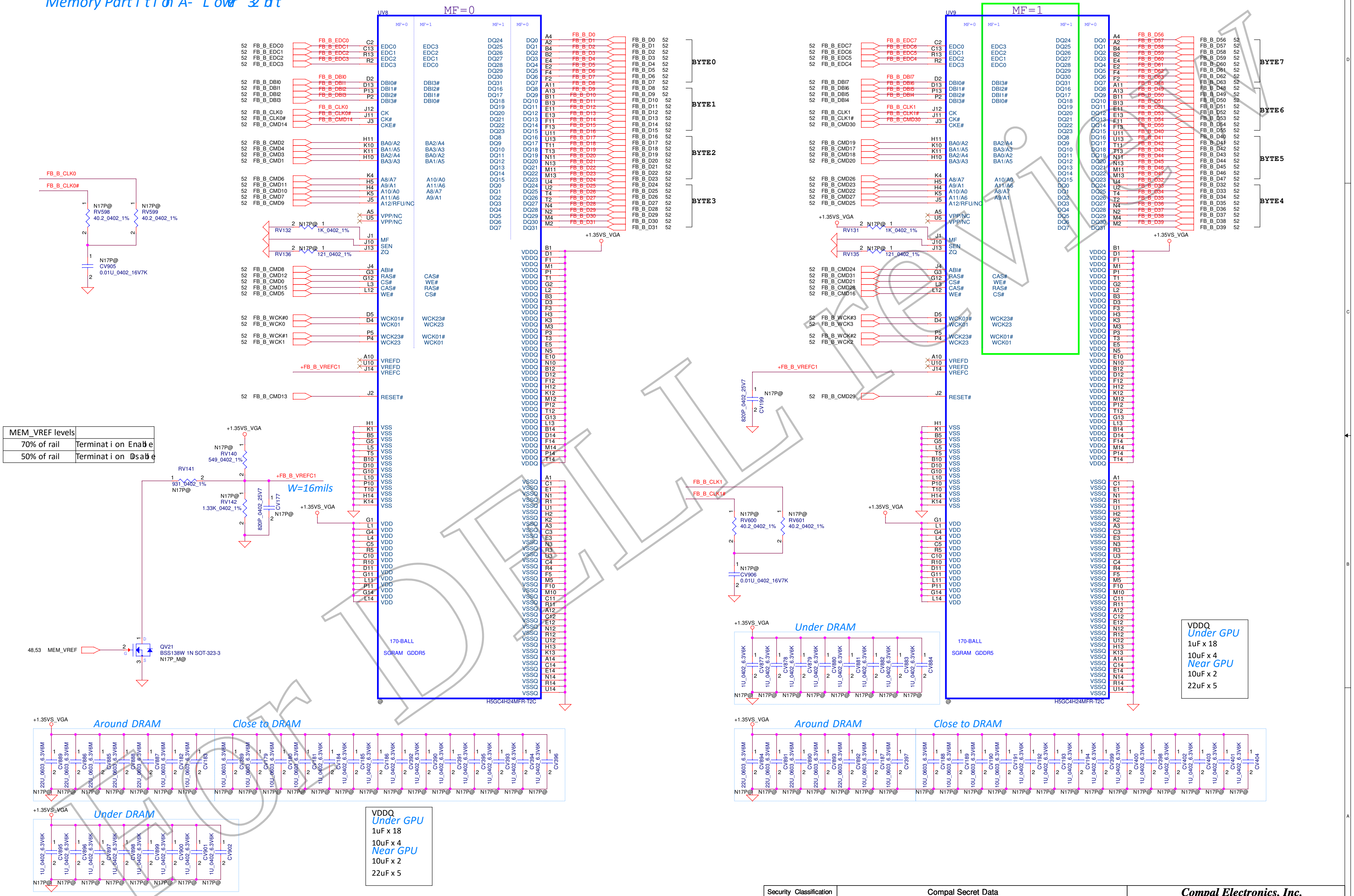
Main Func = GDDR5

Memory Partition A- Lower 32 bit



UV8
MF=0
UV9
MF=1
BYTE0
BYTE1
BYTE2
BYTE3
BYTE4
BYTE5
BYTE6
BYTE7
170-BALL
SGRAM GDDR5
H5GC4H24MFR-T2C
+1.35VS_VGA
+FB_B_VREFC1
W=16mils
FB_B_CLK0
FB_B_CLK0#
FB_B_CLK1
FB_B_CLK1#
RV598 40.2_0402_1%
RV599 40.2_0402_1%
RV600 40.2_0402_1%
RV601 40.2_0402_1%
CV905 0.01U_0402_16V7K
CV906 0.01U_0402_16V7K
RV132 1K_0402_1%
RV136 121_0402_1%
RV131 1K_0402_1%
RV135 121_0402_1%
RV140 549_0402_1%
RV141 931_0402_1%
RV142 1.33K_0402_1%
CV177 820P_0402_25V7
CV199 820P_0402_25V7
QV21 BSS138W 1N SOT-323-3
N17P_M@
48,53 MEM_VREF
N17P@
Around DRAM
Close to DRAM
Under DRAM

MEM_VREF levels	
70% of rail	Termination Enable
50% of rail	Termination Disable

VDDQ
Under GPU
1uF x 18
10uF x 4
Near GPU
10uF x 2
22uF x 5

VDDQ
Under GPU
1uF x 18
10uF x 4
Near GPU
10uF x 2
22uF x 5

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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Title
N17P-G1(7/9)GDDR5_B

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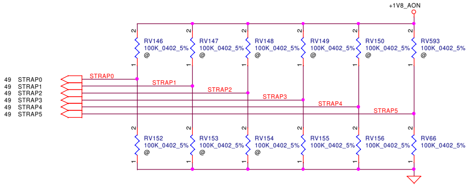

+1V8_AON
RV146 100K_0402_5% @
RV147 100K_0402_5% @
RV148 100K_0402_5% @
RV149 100K_0402_5% @
RV150 100K_0402_5% @
RV593 100K_0402_5% @
49 STRAP0
49 STRAP1
49 STRAP2
49 STRAP3
49 STRAP4
49 STRAP5
STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
STRAP5
RV152 100K_0402_5% @
RV153 100K_0402_5% @
RV154 100K_0402_5% @
RV155 100K_0402_5%
RV156 100K_0402_5%
RV66 100K_0402_5%
2
1

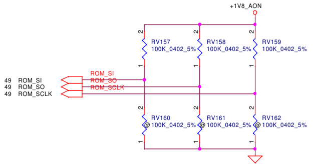

+1V8_AON
RV157 100K_0402_5%
RV158 100K_0402_5%
RV159 100K_0402_5%
49 ROM_SI
49 ROM_SO
49 ROM_SCLK
ROM_SI
ROM_SO
ROM_SCLK
RV160 @ 100K_0402_5%
RV161 @ 100K_0402_5%
RV162 @ 100K_0402_5%
2
1

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V²	Samsung	K4G80325FB-HC28	B-die	0x0	Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	Gbps	N/A	N/A	Substitution allowed with waiver³
			Micron	MT51J256M32HF-70:A	A-die	0x1	Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	Gbps	N/A	N/A	Substitution allowed with waiver³
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	Gbps	N/A	N/A	Substitution allowed with waiver³
4 Gb	128Mx32	1.35V and 1.5V²	Samsung	K4G41325FE-HC28	E-die	0x7	Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	Gbps	N/A	N/A	Substitution allowed with waiver³
		1.35V and 1.5V²	Hynix	H5GC4H24AJR-R0C	A-die	0x6	Gbps	N/A	Full	Production ready
			Hynix	H5GQ4H24AJR-R4C	A-die	0x6	Gbps	N/A	N/A	Substitution allowed with waiver³

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
		1.35V and 1.55V²	Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production ready

SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU

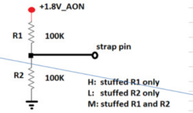
DEVID_SEL	
Low	Original Device ID
High	Re-brand Device ID

VGA_DEVICE	
Low	3D Device
High	VGA Device

PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude

Display SOR			GPU Config			VRAM Config		
ROM_SO	ROM_SI	ROM_SCLK	STRAP5	STRAP4	STRAP3	STRAP2	STRAP1	STRAP0
H	H	H	L	L	L	L	L	L

Display Link/Config						
IFPA	IFPB	IFPC	IFPD(eDP only)	IFPE	IFPF	
NA	NA	HDMI	NA	NA	N/A	<= Fill in displaytype


+1.8V_AON
R1
100K
strap pin
R2
100K

H: stuffed R1 only
L: stuffed R2 only
M: stuffed R1 and R2

Display SOR

ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
H	H	H	Enable	Disable	Disable	Disable

GPU config

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR_EN	DEVID_SEL	PCIE_CFG	VGA_DEVICE
			0: Single GPU	0: Dedicate GPU DID	0: Full swimming (default)	0: 3D (PCI class code 0x302) MSHybrid/Optimus
			1:Multi GPUs	1: Alternated GPU DID (ex.GSYNC)	1: Reduce amplitude	1: VGA (PCI class code 0x300) Discrete
L	L	L	0	0	0	0

Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is IFPD used? (Only supports eDP.)	See This Row of Table 5.5
4	4	NO	15
4	3	YES	13
3	3	NO	14
3	2	YES	12
2	2	NO	12
2	1	YES	8
1	1	NO	8
1	0	YES	0
No other configurations are supported.			

Select your display config

8

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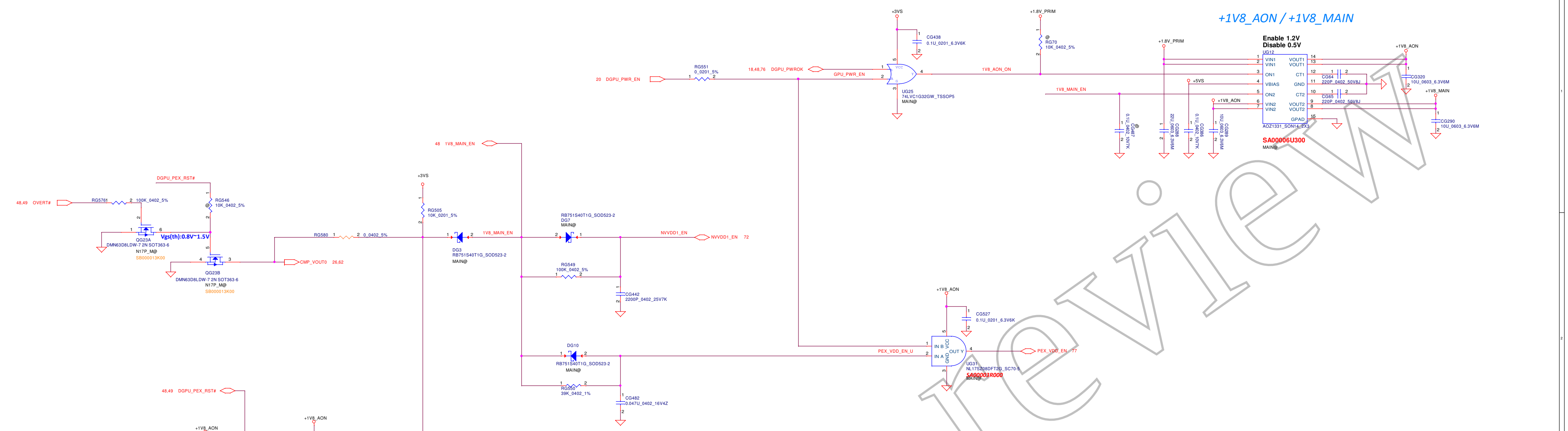
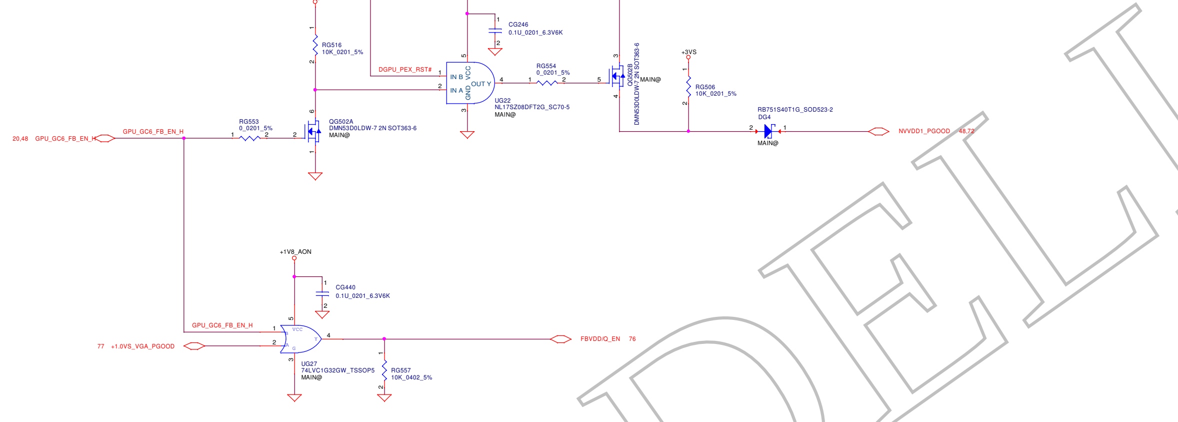
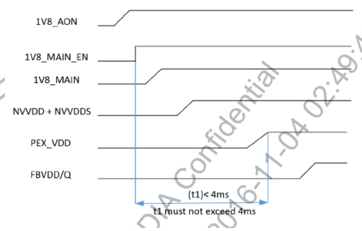
Main Func = DC/DC

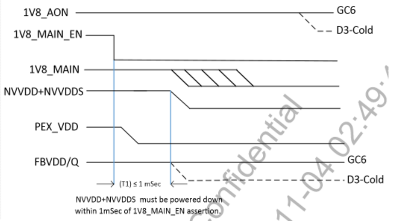

+1V8_AON / +1V8_MAIN
Enable 1.2V
Disable 0.5V
UG12
AOZ1331_SON14_2X3
SA00006U300
MAIN@
VIN1
VOUT1
ON1
CT1
VBIAS
GND
ON2
CT2
VIN2
VOUT2
GPAD
CG320
10U_0603_6.3V6M
CG290
10U_0603_6.3V6M
CG64
220P_0402_50V8J
CG65
220P_0402_50V8J
+1.8V_PRIM
+5VS
+1V8_AON
+1V8_MAIN
1V8_AON_ON
1V8_MAIN_EN
+3VS
CG438
0.1U_0201_6.3V6K
RG70
10K_0402_5%
UG25
74LVC1G32GW_TSSOP5
MAIN@
GPU_PWR_EN
18,48,76 DGPU_PWROK
20 DGPU_PWR_EN
RG551
0_0201_5%
48 1V8_MAIN_EN
DGPU_PEX_RST#
48,49 OVERT#
RG5761
100K_0402_5%
RG546
10K_0402_5%
QG23A
DMN63D8LDW-7 2N SOT363-6
N17P_M@
SB000013K00
Vgs(th):0.8V~1.5V
QG23B
DMN63D8LDW-7 2N SOT363-6
N17P_M@
SB000013K00
CMP_VOUT0 26,62
RG580
0_0402_5%
RG505
10K_0201_5%
DG3
RB751S40T1G_SOD523-2
MAIN@
DG7
RB751S40T1G_SOD523-2
MAIN@
NVVDD1_EN
NVVDD1_EN 72
RG549
100K_0402_5%
CG442
2200P_0402_25V7K
+1V8_AON
CG527
0.1U_0201_6.3V6K
UG31
NL17SZ08DFT2G_SC70-5
SA00003R000
MAIN@
PEX_VDD_EN_U
PEX_VDD_EN 77
DG10
RB751S40T1G_SOD523-2
MAIN@
RG550
39K_0402_1%
CG482
0.047U_0402_16V4Z
48,49 DGPU_PEX_RST#


+1V8_AON
RG516
10K_0201_5%
CG246
0.1U_0201_6.3V6K
DGPU_PEX_RST#
UG22
NL17SZ08DFT2G_SC70-5
MAIN@
RG554
0_0201_5%
QG502B
DMN53D0LDW-7 2N SOT363-6
MAIN@
+3VS
RG506
10K_0201_5%
RG553
0_0201_5%
QG502A
DMN53D0LDW-7 2N SOT363-6
MAIN@
20,48 GPU_GC6_FB_EN_H
GPU_GC6_FB_EN_H
DG4
RB751S40T1G_SOD523-2
MAIN@
NVVDD1_PGOOD 48,72
CG440
0.1U_0201_6.3V6K
UG27
74LVC1G32GW_TSSOP5
MAIN@
77 +1.0VS_VGA_PGOOD
FBVDDQ_EN 76
RG557
10K_0402_5%

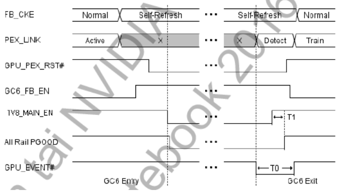
GPU Power Up Sequence


1V8_AON
1V8_MAIN_EN
1V8_MAIN
NVVDD + NVVDDS
PEX_VDD
FBVDD/Q
(t1)< 4ms
t1 must not exceed 4ms

GPU Power Down Sequence


1V8_AON
GC6
D3-Cold
1V8_MAIN_EN
1V8_MAIN
NVVDD+NVVDDS
PEX_VDD
FBVDD/Q
GC6
D3-Cold
(T1) ≤ 1 mSec
NVVDD+NVVDDS must be powered down
within 1mSec of 1V8_MAIN_EN assertion.

GPU GC6 Entry/Exit Sequence


FB_CKE
Normal
Self-Refresh
Self-Refresh
Normal
PEX_LINK
Active
X
X
Detect
Train
GPU_PEX_RST#
GC6_FB_EN
1V8_MAIN_EN
T1
All Rail PGOOD
GPU_EVENT#
T0
GC6 Entry
GC6 Exit

Optimus Sequence

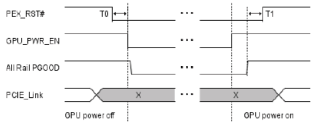

PEX_RST#
T0
T1
GPU_PWR_EN
All Rail PGOOD
PCIE_Link
X
X
GPU power off
GPU power on

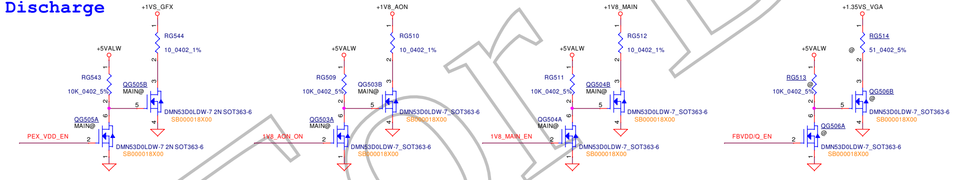
Table 8.1 Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Table 8.2 GC6 2.1 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Discharge


+1VS_GFX
+1V8_AON
+1V8_MAIN
+1.35VS_VGA
+5VALW
RG544
10_0402_1%
RG510
10_0402_1%
RG512
10_0402_1%
RG514
51_0402_5%
RG543
10K_0402_5%
RG509
10K_0402_5%
RG511
10K_0402_5%
RG513
10K_0402_5%
QG505B
QG503B
QG504B
QG506B
QG505A
QG503A
QG504A
QG506A
MAIN@
DMN53D0LDW-7 2N SOT363-6
DMN53D0LDW-7_SOT363-6
SB000018X00
PEX_VDD_EN
1V8_AON_ON
1V8_MAIN_EN
FBVDD/Q_EN

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Title: GPU power control

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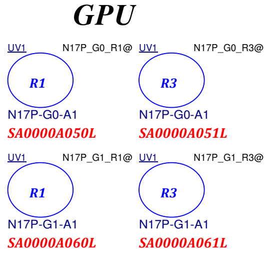
MODEL NAME : *CALXX/CALXX*
PCB NO : *LA-F611P*

Bom Structure

GPU


UV1
N17P_G0_R1@
R1
N17P-G0-A1
SA0000A050L
UV1
N17P_G0_R3@
R3
N17P-G0-A1
SA0000A051L
UV1
N17P_G1_R1@
R1
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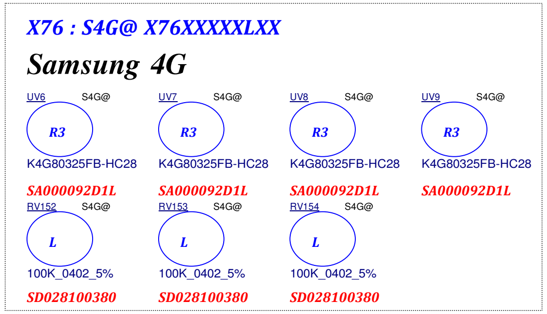
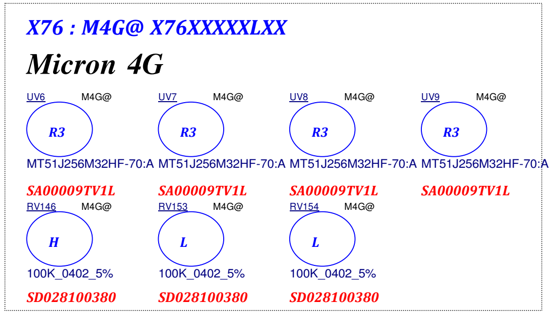
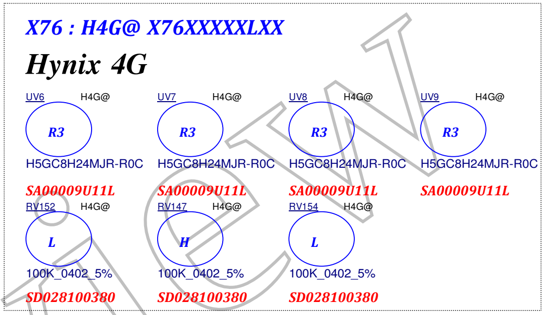
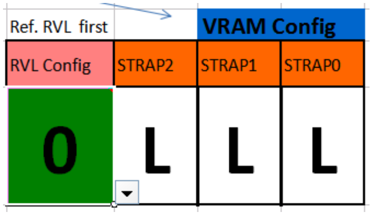
SA0000A060L
UV1
N17P_G1_R3@
R3
N17P-G1-A1
SA0000A061L


X76 : S4G@ X76XXXXXLXX
Samsung 4G
UV6 S4G@ R3 K4G80325FB-HC28 SA000092D1L
UV7 S4G@ R3 K4G80325FB-HC28 SA000092D1L
UV8 S4G@ R3 K4G80325FB-HC28 SA000092D1L
UV9 S4G@ R3 K4G80325FB-HC28 SA000092D1L
RV152 S4G@ L 100K_0402_5% SD028100380
RV153 S4G@ L 100K_0402_5% SD028100380
RV154 S4G@ L 100K_0402_5% SD028100380


X76 : M4G@ X76XXXXXLXX
Micron 4G
UV6 M4G@ R3 MT51J256M32HF-70:A SA000009TV1L
UV7 M4G@ R3 MT51J256M32HF-70:A SA000009TV1L
UV8 M4G@ R3 MT51J256M32HF-70:A SA000009TV1L
UV9 M4G@ R3 MT51J256M32HF-70:A SA000009TV1L
RV146 M4G@ H 100K_0402_5% SD028100380
RV153 M4G@ L 100K_0402_5% SD028100380
RV154 M4G@ L 100K_0402_5% SD028100380

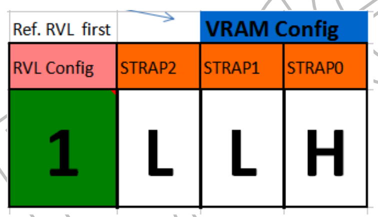

X76 : H4G@ X76XXXXXLXX
Hynix 4G
UV6 H4G@ R3 H5GC8H24MJR-R0C SA000009U11L
UV7 H4G@ R3 H5GC8H24MJR-R0C SA000009U11L
UV8 H4G@ R3 H5GC8H24MJR-R0C SA000009U11L
UV9 H4G@ R3 H5GC8H24MJR-R0C SA000009U11L
RV152 H4G@ L 100K_0402_5% SD028100380
RV147 H4G@ H 100K_0402_5% SD028100380
RV154 H4G@ L 100K_0402_5% SD028100380

Samsung 4G



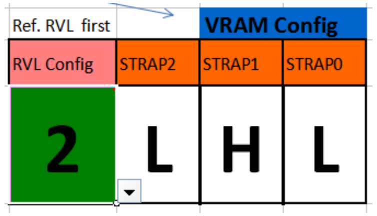
Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
0	L	L	L

Micron 4G



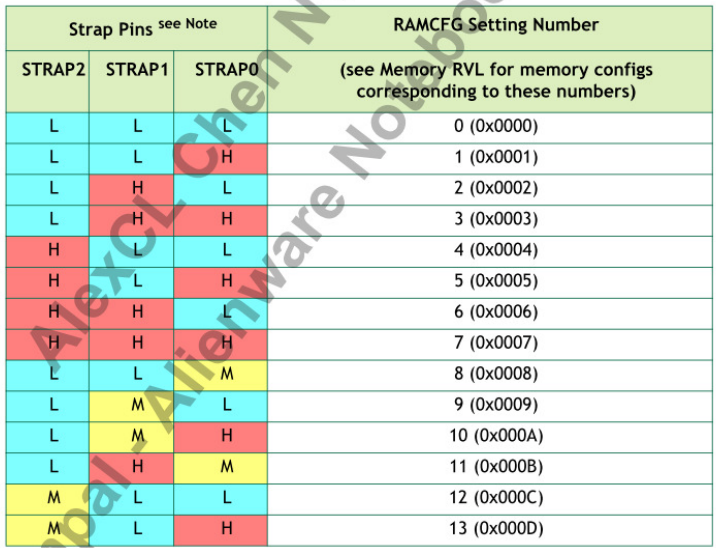
Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
1	L	L	H

Hynix 4G



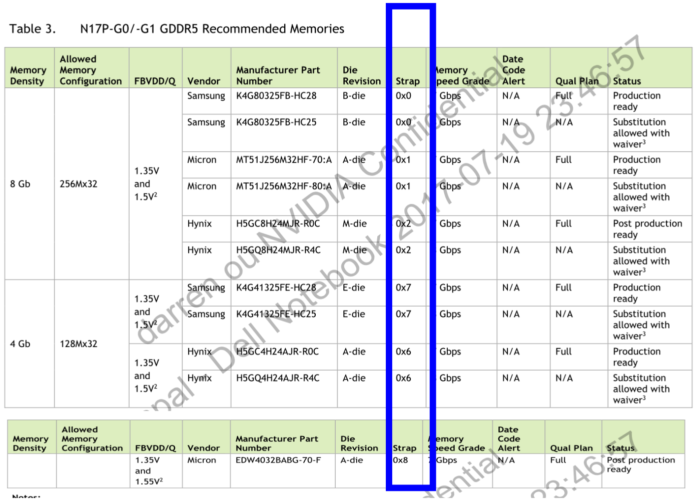
Ref. RVL first	VRAM Config		
RVL Config	STRAP2	STRAP1	STRAP0
2	L	H	L

Table 5.2 RAMCFG



Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories



Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V²	Samsung	K4G80325FB-HC28	B-die	0x0	Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	Gbps	N/A	N/A	Substitution allowed with waiver³
			Micron	MT51J256M32HF-70:A	A-die	0x1	Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	Gbps	N/A	N/A	Substitution allowed with waiver³
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	Gbps	N/A	N/A	Substitution allowed with waiver³
4 Gb	128Mx32	1.35V and 1.5V²	Samsung	K4G41325FE-HC28	E-die	0x7	Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	Gbps	N/A	N/A	Substitution allowed with waiver³
		1.35V and 1.5V²	Hynix	H5GC4H24AJR-R0C	A-die	0x6	Gbps	N/A	Full	Production ready
			Hynix	H5GQ4H24AJR-R4C	A-die	0x6	Gbps	N/A	N/A	Substitution allowed with waiver³

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
		1.35V and 1.55V²	Micron	EDW4032BABG-70-F	A-die	0x8	Gbps	N/A	Full	Post production ready

Notes:

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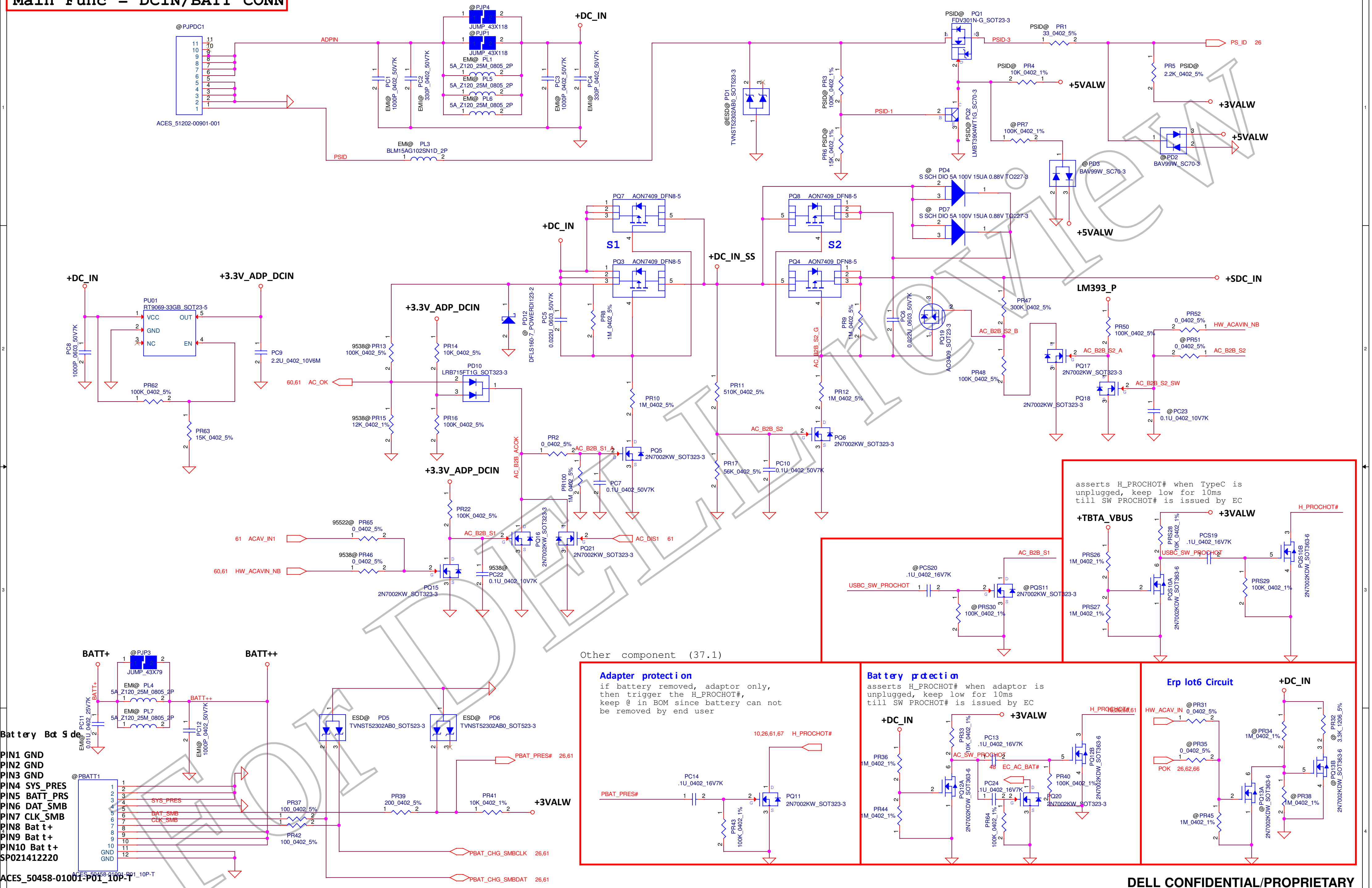

@PJPDC1
ACES_51202-00901-001
ADPIN
PSID
EMI@ PL3
BLM15AG102SN1D_2P
@PJP4
JUMP_43X118
@PJP1
JUMP_43X118
EMI@ PL1
5A_Z120_25M_0805_2P
EMI@ PL5
5A_Z120_25M_0805_2P
EMI@ PL6
5A_Z120_25M_0805_2P
EMI@ PC1 1000P_0402_50V7K
EMI@ PC2 330P_0402_50V7K
EMI@ PC3 1000P_0402_50V7K
EMI@ PC4 330P_0402_50V7K
+DC_IN
@ESD@ PD1
TVNST52302AB0_SOT523-3
PSID@ PR3 100K_0402_1%
PR6 PSID@ 15K_0402_1%
PSID-1
PSID@ PQ1
FDV301N-G_SOT23-3
PSID-3
PSID@ PR1
33_0402_5%
PS_ID 26
PSID@ PR4
10K_0402_1%
+5VALW
PSID@ PQ2
LMBT3904WT1G_SC70-3
@PR7
100K_0402_1%
PR5 PSID@
2.2K_0402_5%
+3VALW
@PD2
BAV99W_SC70-3
@PD3
BAV99W_SC70-3
@ PD4
S SCH DIO 5A 100V 15UA 0.88V TO227-3
@ PD7
S SCH DIO 5A 100V 15UA 0.88V TO227-3
PQ7 AON7409_DFN8-5
PQ3 AON7409_DFN8-5
PQ8 AON7409_DFN8-5
PQ4 AON7409_DFN8-5
S1
S2
+DC_IN_SS
+SDC_IN
+3.3V_ADP_DCIN
PU01
RT9069-33GB_SOT23-5
VCC
OUT
GND
NC
EN
PC8 1000P_0603_50V7K
PC9 2.2U_0402_10V6M
PR62 100K_0402_5%
PR63 15K_0402_5%
9538@ PR13 100K_0402_5%
9538@ PR15 12K_0402_1%
PR14 10K_0402_5%
PR16 100K_0402_5%
PD10
LRB715FT1G_SOT323-3
60,61 AC_OK
@ PD12 DFLS160-7_POWERDI123-2
PC5 0.022U_0603_50V7K
PR8 1M_0402_5%
PR10 1M_0402_5%
PR11 510K_0402_5%
PR9 1M_0402_5%
PC6 0.022U_0603_50V7K
PQ19 AO3409_SOT23-3
PR47 300K_0402_5%
PR48 100K_0402_5%
AC_B2B_S2_B
AC_B2B_S2_A
PQ17 2N7002KW_SOT323-3
PQ18 2N7002KW_SOT323-3
AC_B2B_S2_SW
LM393_P
PR50 100K_0402_5%
PR52 0_0402_5%
HW_ACAVIN_NB
@PR51 0_0402_5%
AC_B2B_S2
@PC23 0.1U_0402_10V7K
PR12 1M_0402_5%
PQ6 2N7002KW_SOT323-3
PR17 56K_0402_5%
PC10 0.1U_0402_50V7K
PR2 0_0402_5%
AC_B2B_S1
AC_B2B_ACOK
PQ5 2N7002KW_SOT323-3
PR100 1M_0402_5%
PC7 0.1U_0402_50V7K
PR22 100K_0402_5%
95522@ PR65 0_0402_5%
61 ACAV_IN1
9538@ PR46 0_0402_5%
60,61 HW_ACAVIN_NB
PQ15 2N7002KW_SOT323-3
9538@ PC22 0.1U_0402_10V7K
PQ16 2N7002KW_SOT323-3
PQ21 2N7002KW_SOT323-3
AC_DIS1 61
@PCS20 .1U_0402_16V7K
USBC_SW_PROCHOT
@PQS11 2N7002KW_SOT323-3
@PRS30 100K_0402_1%
+TBTA_VBUS
PRS26 1M_0402_1%
PRS27 1M_0402_1%
PRS28 10K_0402_1%
PCS19 .1U_0402_16V7K
PQS10A 2N7002KDW_SOT363-6
PQS10B 2N7002KDW_SOT363-6
PRS29 100K_0402_1%
H_PROCHOT#
BATT+
BATT++
@PJP3
JUMP_43X79
EMI@ PL4
5A_Z120_25M_0805_2P
EMI@ PL7
5A_Z120_25M_0805_2P
EMI@ PC11 0.01U_0402_25V7K
EMI@ PC12 1000P_0402_50V7K
ESD@ PD5 TVNST52302AB0_SOT523-3
ESD@ PD6 TVNST52302AB0_SOT523-3
PBAT_PRES# 26,61
@PBATT1
ACES_50458-01001-P01_10P-T
SYS_PRES
DAT_SMB
CLK_SMB
PR37 100_0402_5%
PR42 100_0402_5%
PR39 200_0402_5%
PR41 10K_0402_1%
PBAT_CHG_SMBCLK 26,61
PBAT_CHG_SMBDAT 26,61
10,26,61,67 H_PROCHOT#
PC14 .1U_0402_16V7K
PBAT_PRES#
PQ11 2N7002KW_SOT323-3
PR43 100K_0402_1%
PR33 10K_0402_1%
PR36 1M_0402_1%
PR44 1M_0402_1%
PC13 .1U_0402_16V7K
AC_SW_PROCHOT
48 EC_AC_BAT#
PC24 .1U_0402_16V7K
PR64 100K_0402_1%
PQ20 2N7002KW_SOT323-3
PR40 100K_0402_1%
PQ12A 2N7002KDW_SOT363-6
PQ12B 2N7002KDW_SOT363-6
HW_ACAV_IN
@PR31 0_0402_5%
@PR35 0_0402_5%
POK 26,62,66
@PR34 1M_0402_1%
@PR45 1M_0402_1%
@PR32 3.3K_1206_5%
@PR38 1M_0402_1%
@PQ13A 2N7002KDW_SOT363-6
@PQ13B 2N7002KDW_SOT363-6

asserts H_PROCHOT# when TypeC is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC

Other component (37.1)

Adapter protection

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user

Battery protection

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC

Erp lot6 Circuit

Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRES
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220

ACES_50458-01001-P01_10P-T

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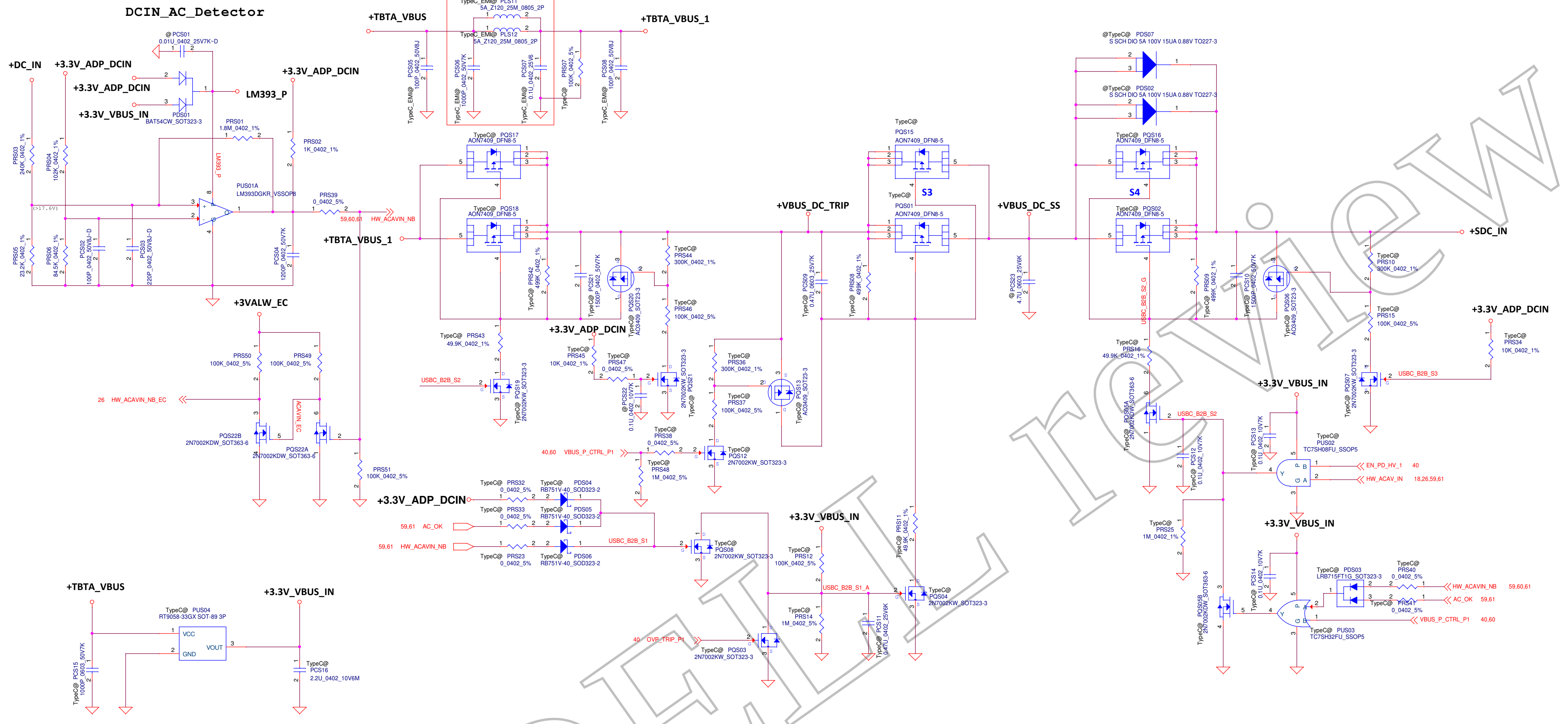

DCIN_AC_Detector
+DC_IN
+3.3V_ADP_DCIN
+3.3V_VBUS_IN
LM393_P
PCS01 0.01U_0402_25V7K-D
PDS01 BAT54CW_SOT323-3
PRS01 1.8M_0402_1%
PRS02 1K_0402_1%
PUS01A LM393DGKR_VSSOP8
PRS39 0_0402_5%
59,60,61 HW_ACAVIN_NB
PRS03 240K_0402_1%
PRS04 102K_0402_1%
PRS05 23.2K_0402_1%
PRS06 84.5K_0402_1%
PCS02 100P_0402_50V8J-D
PCS03 220P_0402_50V8J-D
PCS04 1200P_0402_50V7K
+TBTA_VBUS_1
+3VALW_EC
PRS50 100K_0402_5%
PRS49 100K_0402_5%
26 HW_ACAVIN_NB_EC
ACAVIN_EC
PQS22B 2N7002KDW_SOT363-6
PQS22A 2N7002KDW_SOT363-6
PRS51 100K_0402_5%
+TBTA_VBUS
EMI Part
TypeC_EMI@ PLS11 5A_Z120_25M_0805_2P
TypeC_EMI@ PLS12 5A_Z120_25M_0805_2P
PCS05 100P_0402_50V8J
PCS06 1000P_0402_50V7K
PCS07 0.1U_0402_25V6
PRS07 100K_0402_5%
PCS08 100P_0402_50V8J
TypeC@ PQS17 AON7409_DFN8-5
TypeC@ PQS18 AON7409_DFN8-5
PRS42 499K_0402_1%
PCS21 1500P_0402_50V7K
PQS20 AO3409_SOT23-3
PRS44 300K_0402_1%
PRS46 100K_0402_5%
PRS43 49.9K_0402_1%
USBC_B2B_S2
PQS19 2N7002KW_SOT323-3
PRS45 10K_0402_1%
PRS47 0_0402_5%
PCS22 0.1U_0402_10V7K
PQS21 2N7002KW_SOT323-3
PRS36 300K_0402_1%
PRS37 100K_0402_5%
PQS13 AO3409_SOT23-3
PRS38 0_0402_5%
40,60 VBUS_P_CTRL_P1
PRS48 1M_0402_5%
PQS12 2N7002KW_SOT323-3
+VBUS_DC_TRIP
PCS09 0.47U_0603_25V7K
PRS08 499K_0402_1%
TypeC@ PQS15 AON7409_DFN8-5
S3
PQS01 AON7409_DFN8-5
+VBUS_DC_SS
PCS23 4.7U_0603_25V6K
@TypeC@ PDS07 S SCH DIO 5A 100V 15UA 0.88V TO227-3
@TypeC@ PDS02 S SCH DIO 5A 100V 15UA 0.88V TO227-3
PQS16 AON7409_DFN8-5
S4
PQS02 AON7409_DFN8-5
PRS09 499K_0402_1%
PCS10 1500P_0402_50V7K
PQS06 AO3409_SOT23-3
+SDC_IN
PRS10 300K_0402_1%
PRS15 100K_0402_5%
PRS16 49.9K_0402_1%
USBC_B2B_S2_G
PQS05A 2N7002KDW_SOT363-6
PQS07 2N7002KW_SOT323-3
USBC_B2B_S3
PRS34 10K_0402_1%
PCS13 0.1U_0402_10V7K
PCS12 0.1U_0402_10V7K
PUS02 TC7SH08FU_SSOP5
EN_PD_HV_1 40
HW_ACAV_IN 18,26,59,61
PRS25 1M_0402_1%
PRS32 0_0402_5%
PDS04 RB751V-40_SOD323-2
PRS33 0_0402_5%
PDS05 RB751V-40_SOD323-2
59,61 AC_OK
59,61 HW_ACAVIN_NB
PRS23 0_0402_5%
PDS06 RB751V-40_SOD323-2
USBC_B2B_S1
PQS08 2N7002KW_SOT323-3
PRS12 100K_0402_5%
USBC_B2B_S1_A
PRS11 49.9K_0402_1%
PQS04 2N7002KW_SOT323-3
PRS14 1M_0402_5%
PCS11 0.47U_0402_25V6K
40 OVP_TRIP_P1
PQS03 2N7002KW_SOT323-3
PCS14 0.1U_0402_10V7K
PQS05B 2N7002KDW_SOT363-6
PDS03 LRB715FT1G_SOT323-3
PRS40 0_0402_5%
HW_ACAVIN_NB 59,60,61
PRS41 0_0402_5%
AC_OK 59,61
VBUS_P_CTRL_P1 40,60
PUS03 TC7SH32FU_SSOP5
PUS04 RT9058-33GX SOT-89 3P
VCC
GND
VOUT
PCS15 1000P_0603_50V7K
PCS16 2.2U_0402_10V6M

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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: PWR_Type-C PD Selector
				Size / Document Number: LA-F611P / Rev 0.1
				Date: Thursday, March 22, 2018 / Sheet 60 of 78

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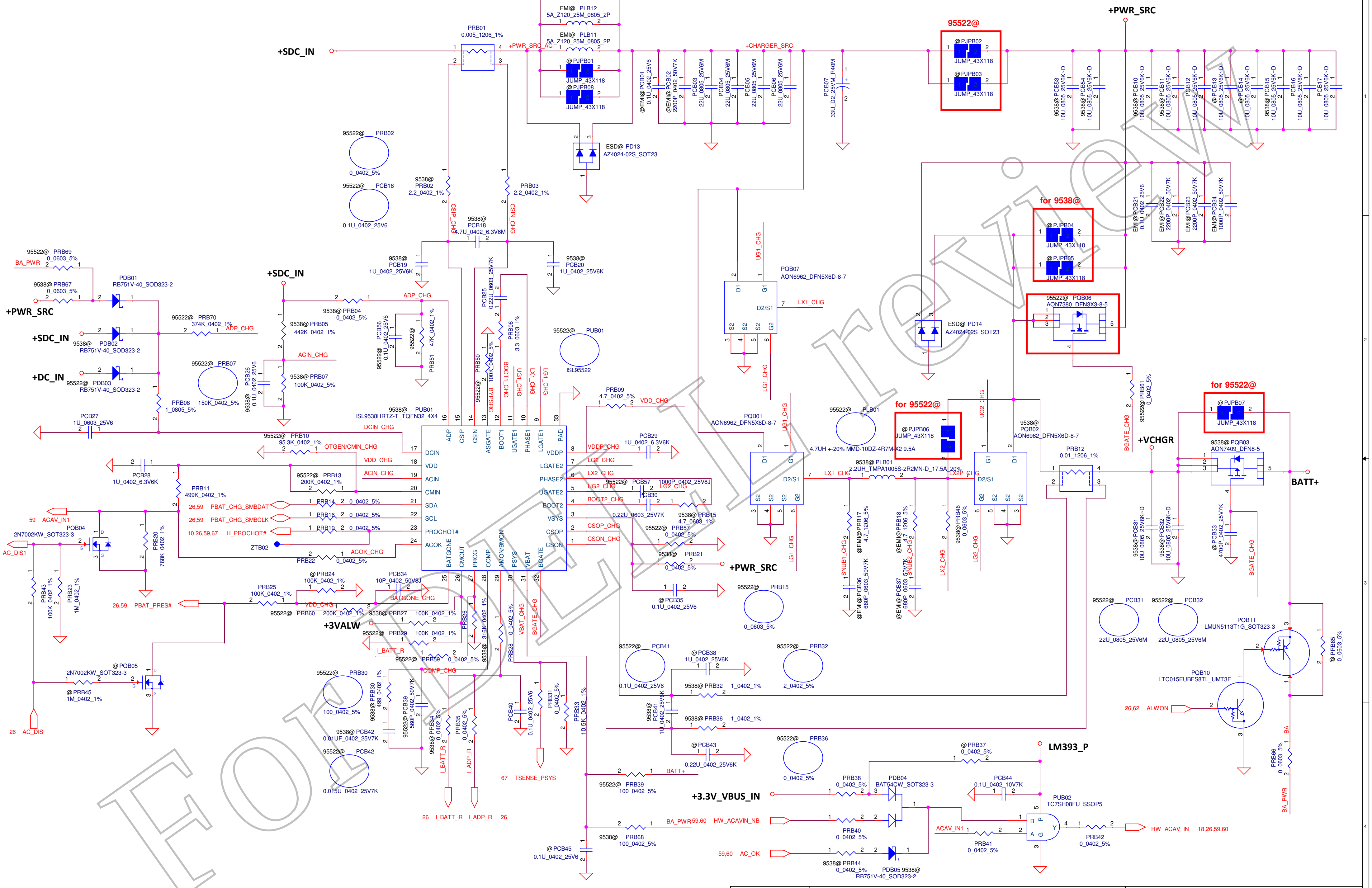

+SDC_IN
PRB01 0.005_1206_1%
+PWR_SRC_AC
EMI@ PLB13 5A_Z120_25M_0805_2P
EMI@ PLB12 5A_Z120_25M_0805_2P
EMI@ PLB11 5A_Z120_25M_0805_2P
@PJPB01 JUMP_43X118
@PJPB08 JUMP_43X118
ESD@ PD13 AZ4024-02S_SOT23
+CHARGER_SRC
@EMI@PCB01 0.1U_0402_25V6
@EMI@PCB02 2200P_0402_50V7K
PCB03 22U_0805_25V6M
PCB04 22U_0805_25V6M
PCB05 22U_0805_25V6M
PCB06 22U_0805_25V6M
PCB07 33U_D2_25VM_R40M
95522@
@PJPB02 JUMP_43X118
@PJPB03 JUMP_43X118
+PWR_SRC
9538@PCB53 10U_0805_25V6K-D
9538@PCB54 10U_0805_25V6K-D
9538@PCB10 10U_0805_25V6K-D
9538@PCB11 10U_0805_25V6K-D
9538@PCB12 10U_0805_25V6K-D
9538@PCB13 10U_0805_25V6K-D
9538@PCB14 10U_0805_25V6K-D
9538@PCB15 10U_0805_25V6K-D
9538@PCB16 10U_0805_25V6K-D
9538@PCB17 10U_0805_25V6K-D
95522@ PRB02 0_0402_5%
95522@ PCB18 0.1U_0402_25V6
9538@ PRB02 2.2_0402_1%
PRB03 2.2_0402_1%
CSIP_CHG
CSIN_CHG
9538@ PCB18 4.7U_0402_6.3V6M
9538@ PCB19 1U_0402_25V6K
9538@ PCB20 1U_0402_25V6K
EMI@PCB21 0.1U_0402_25V6
EMI@PCB22 2200P_0402_50V7K
EMI@PCB23 2200P_0402_50V7K
EMI@PCB24 1000P_0402_50V7K
for 9538@
@PJPB04 JUMP_43X118
@PJPB05 JUMP_43X118
95522@ PQB06 AON7380_DFN3X3-8-5
ESD@ PD14 AZ4024-02S_SOT23
PQB07 AON6962_DFN5X6D-8-7
UG1_CHG
LX1_CHG
LG1_CHG
95522@ PRB69 0_0603_5%
BA_PWR
9538@ PRB67 0_0603_5%
PDB01 RB751V-40_SOD323-2
+PWR_SRC
+SDC_IN
9538@ PDB02 RB751V-40_SOD323-2
+DC_IN
95522@ PDB03 RB751V-40_SOD323-2
95522@ PRB70 374K_0402_1%
ADP_CHG
9538@ PRB04 0_0402_5%
9538@ PRB05 442K_0402_1%
ACIN_CHG
9538@ PRB07 100K_0402_5%
95522@ PRB07 150K_0402_5%
PCB26 0.1U_0402_25V6
PRB08 1_0805_5%
PCB27 1U_0603_25V6
PCB56 0.1U_0402_25V6
95522@ PRB51 47K_0402_1%
PCB25 0.22U_0603_25V7K
PRB06 3.3_0603_1%
PRB50 100K_0402_5%
BYPSRC
BOOT1_CHG
UG1_CHG
LX1_CHG
LG1_CHG
95522@ PUB01 ISL95522
9538@ PUB01 ISL9538HRTZ-T_TQFN32_4X4
ADP CSIP CSIN ASGATE BOOT1 UGATE1 PHASE1 LGATE1 PAD
DCIN VDD ACIN CMIN SDA SCL PROCHOT# ACOK
VDDP LGATE2 PHASE2 UGATE2 BOOT2 VSYS CSOP CSON
BATGONE CMOUT PROG COMP AMON/BMON PSYS VBAT BGATE
DCIN_CHG
95522@ PRB10 95.3K_0402_1%
OTGEN/CMIN_CHG
VDD_CHG
ACIN_CHG
PCB28 1U_0402_6.3V6K
95522@ PRB13 200K_0402_1%
PRB11 499K_0402_1%
26,59 PBAT_CHG_SMBDAT
26,59 PBAT_CHG_SMBCLK
10,26,59,67 H_PROCHOT#
PRB14 0_0402_5%
PRB16 0_0402_5%
PRB19 0_0402_5%
ZTB02
ACOK_CHG
PRB22 0_0402_5%
59 ACAV_IN1
PQB04 2N7002KW_SOT323-3
59 AC_DIS1
PRB20 768K_0402_1%
PRB43 100K_0402_1%
PRB23 1M_0402_1%
26,59 PBAT_PRES#
PRB25 100K_0402_1%
@PRB24 100K_0402_1%
PCB34 10P_0402_50V8J
VDD_CHG
BATGONE_CHG
95522@ PRB60 200K_0402_1%
9538@ PRB27 100K_0402_1%
+3VALW
95522@ PRB29 100K_0402_1%
I_BATT_R
95522@ PRB59 0_0402_5%
PRB26 316K_0402_1%
COMP_CHG
@PQB05 2N7002KW_SOT323-3
@PRB45 1M_0402_1%
26 AC_DIS
95522@ PRB30 100_0402_5%
9538@ PRB30 499_0402_1%
95522@ PCB39 560P_0402_50V7K
9538@ PCB42 0.01UF_0402_25V7K
95522@ PCB42 0.015U_0402_25V7K
9538@ PRB34 0_0402_5%
PRB35 0_0402_5%
PCB40 0.1U_0402_25V6
PRB31 0_0402_5%
PRB33 10.5K_0402_1%
VBAT_CHG
BGATE_CHG
PRB28 0_0402_5%
26 I_BATT_R I_ADP_R 26
67 TSENSE_PSYS
PRB09 4.7_0402_5%
VDD_CHG
PCB29 1U_0402_6.3V6K
LG2_CHG
LX2_CHG
95522@ PCB57 1000P_0402_25V8J
UG2_CHG
PCB30 0.22U_0603_25V7K
BOOT2_CHG
9538@ PRB15 4.7_0603_1%
CSOP_CHG
CSON_CHG
95522@ PRB57 0_0402_5%
9538@ PRB21 0_0402_5%
+PWR_SRC
@PCB35 0.1U_0402_25V6
95522@ PRB15 0_0603_5%
95522@ PCB41 0.1U_0402_25V6
9538@ PCB41 1U_0402_25V6K
@PCB38 1U_0402_25V6K
9538@ PRB32 1_0402_1%
95522@ PRB32 2_0402_5%
9538@ PRB36 1_0402_1%
@PCB43 0.22U_0402_25V6K
95522@ PRB36 0_0402_5%
BATT+
95522@ PRB39 100_0402_5%
9538@ PRB68 100_0402_5%
BA_PWR
@PCB45 0.1U_0402_25V6
PQB01 AON6962_DFN5X6D-8-7
95522@ PLB01 4.7UH +-20% MMD-10DZ-4R7M-X2 9.5A
for 95522@
@PJPB06 JUMP_43X118
9538@ PLB01 2.2UH_TMPA1005S-2R2MN-D_17.5A_20%
LX1_CHG
LX2_CHG
9538@ PQB02 AON6962_DFN5X6D-8-7
UG2_CHG
LG2_CHG
SNUB1_CHG
@EMI@PRB17 4.7_1206_5%
@EMI@PCB36 680P_0603_50V7K
@EMI@PRB18 4.7_1206_5%
@EMI@PCB37 680P_0603_50V7K
SNUB2_CHG
9538@ PRB46 0_0603_5%
95522@ PRB61 0_0402_5%
BGATE_CHG
+VCHGR
PRB12 0.01_1206_1%
for 95522@
@PJPB07 JUMP_43X118
9538@ PQB03 AON7409_DFN8-5
BATT+
9538@ PCB31 10U_0805_25V6K-D
9538@ PCB32 10U_0805_25V6K-D
@PCB33 4700P_0402_25V7K
95522@ PCB31 22U_0805_25V6M
95522@ PCB32 22U_0805_25V6M
PQB11 LMUN5113T1G_SOT323-3
@PRB65 0_0603_5%
PQB10 LTC015EUBFS8TL_UMT3F
26,62 ALWON
PRB66 0_0603_5%
BA
BA_PWR
LM393_P
@PRB37 0_0402_5%
+3.3V_VBUS_IN
PRB38 0_0402_5%
PDB04 BAT54CW_SOT323-3
PCB44 0.1U_0402_10V7K
PUB02 TC7SH08FU_SSOP5
59,60 HW_ACAVIN_NB
PRB40 0_0402_5%
ACAV_IN1
PRB41 0_0402_5%
PRB42 0_0402_5%
HW_ACAV_IN 18,26,59,60
59,60 AC_OK
9538@ PRB44 0_0402_5%
PDB05 9538@ RB751V-40_SOD323-2

For LLL review

Security Classification | Compal Secret Data
Issued Date 2016/01/06 | Deciphered Date 2017/01/06

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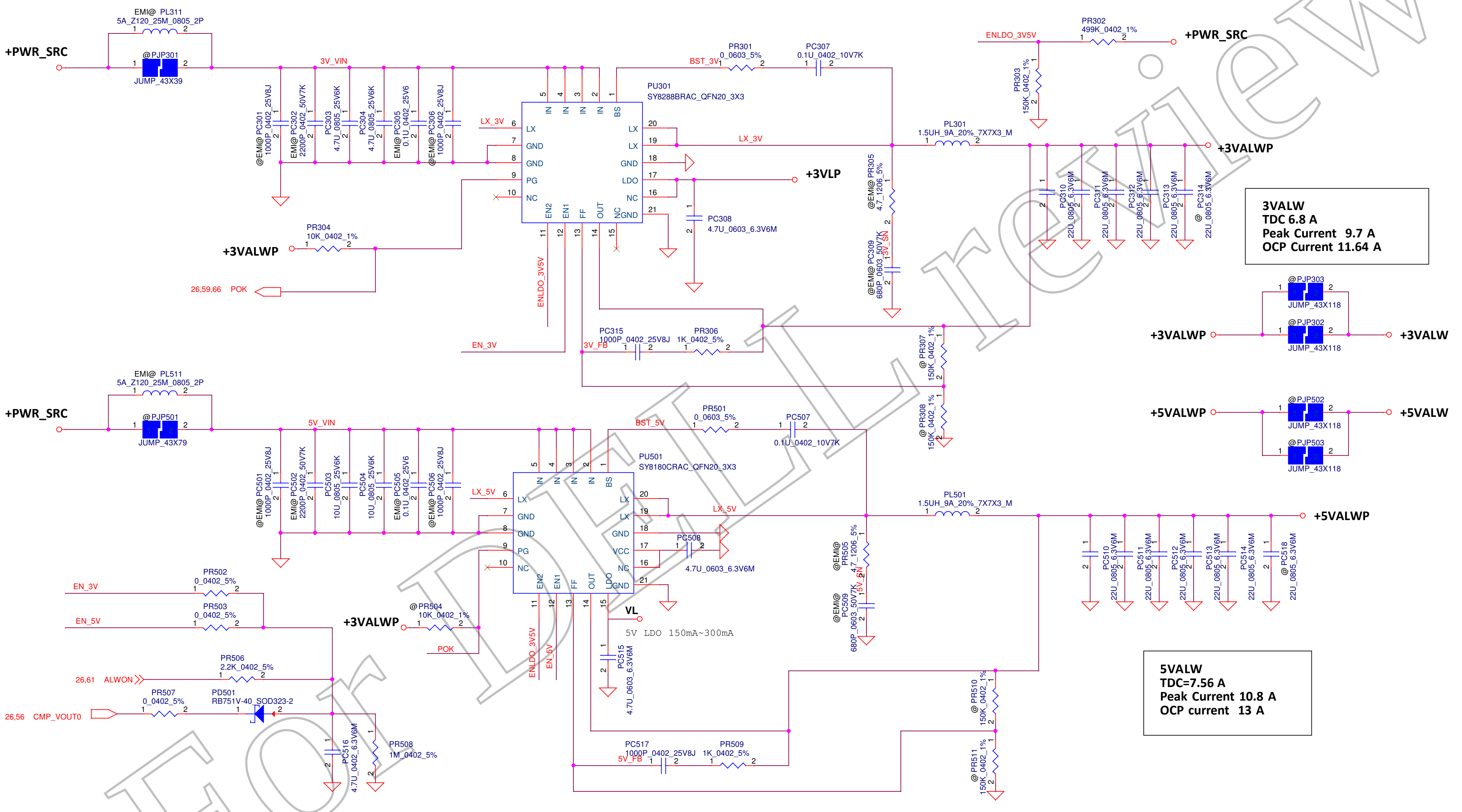
Compal Electronics, Inc.

Title ***PWR_CHARGER***

Size | Document Number ***LA-F611P*** | Rev 0.1

Date: Thursday, March 22, 2018 | Sheet 61 of 78

Main Func = 3.3VALW/5VALW



+PWR_SRC
EMI@ PL311
5A_Z120_25M_0805_2P
@PJP301
JUMP_43X39
3V_VIN
@EMI@ PC301 1000P_0402_25V8J
EMI@ PC302 2200P_0402_50V7K
PC303 4.7U_0805_25V6K
PC304 4.7U_0805_25V6K
EMI@ PC305 0.1U_0402_25V6
@EMI@ PC306 1000P_0402_25V8J
PU301
SY8288BRAC_QFN20_3X3
IN
BS
LX
GND
PG
NC
EN2
EN1
FF
OUT
LDO
LX_3V
BST_3V
PR301 0_0603_5%
PC307 0.1U_0402_10V7K
+3VLP
PC308 4.7U_0603_6.3V6M
PR304 10K_0402_1%
+3VALWP
26,59,66 POK
ENLDO_3V5V
EN_3V
PC315 1000P_0402_25V8J
PR306 1K_0402_5%
3V_FB
ENLDO_3V5V
PR302 499K_0402_1%
PR303 150K_0402_1%
PL301 1.5UH_9A_20%_7X7X3_M
@EMI@ PR305 4.7_1206_5%
@EMI@ PC309 680P_0603_50V7K
3V_SN
PC310 22U_0805_6.3V6M
PC311 22U_0805_6.3V6M
PC312 22U_0805_6.3V6M
PC313 22U_0805_6.3V6M
@ PC314 22U_0805_6.3V6M
@ PR307 150K_0402_1%
@ PR308 150K_0402_1%
@PJP303 JUMP_43X118
@PJP302 JUMP_43X118
+3VALWP
+3VALW
EMI@ PL511
5A_Z120_25M_0805_2P
@PJP501
JUMP_43X79
5V_VIN
@EMI@ PC501 1000P_0402_25V8J
EMI@ PC502 2200P_0402_50V7K
PC503 10U_0805_25V6K
PC504 10U_0805_25V6K
EMI@ PC505 0.1U_0402_25V6
@EMI@ PC506 1000P_0402_25V8J
PU501
SY8180CRAC_QFN20_3X3
VCC
LX_5V
BST_5V
PR501 0_0603_5%
PC507 0.1U_0402_10V7K
PC508 4.7U_0603_6.3V6M
PL501 1.5UH_9A_20%_7X7X3_M
+5VALWP
@EMI@ PR505 4.7_1206_5%
@EMI@ PC509 680P_0603_50V7K
5V_SN
PC510 22U_0805_6.3V6M
PC511 22U_0805_6.3V6M
PC512 22U_0805_6.3V6M
PC513 22U_0805_6.3V6M
PC514 22U_0805_6.3V6M
@PC518 22U_0805_6.3V6M
@PJP502 JUMP_43X118
@PJP503 JUMP_43X118
+5VALW
EN_3V
PR502 0_0402_5%
EN_5V
PR503 0_0402_5%
@PR504 10K_0402_1%
POK
26,61 ALWON
PR506 2.2K_0402_5%
26,56 CMP_VOUT0
PR507 0_0402_5%
PD501 RB751V-40_SOD323-2
PC516 4.7U_0402_6.3V6M
PR508 1M_0402_5%
VL
5V LDO 150mA~300mA
PC515 4.7U_0603_6.3V6M
PC517 1000P_0402_25V8J
PR509 1K_0402_5%
5V_FB
@ PR510 150K_0402_1%
@ PR511 150K_0402_1%

3VALW
TDC 6.8 A
Peak Current 9.7 A
OCP Current 11.64 A

5VALW
TDC=7.56 A
Peak Current 10.8 A
OCP current 13 A

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: PWR_3.3VALW/5VALW
				Size / Document Number: LA-F611P / Rev 0.1
				Date: Thursday, March 22, 2018 / Sheet 62 of 78

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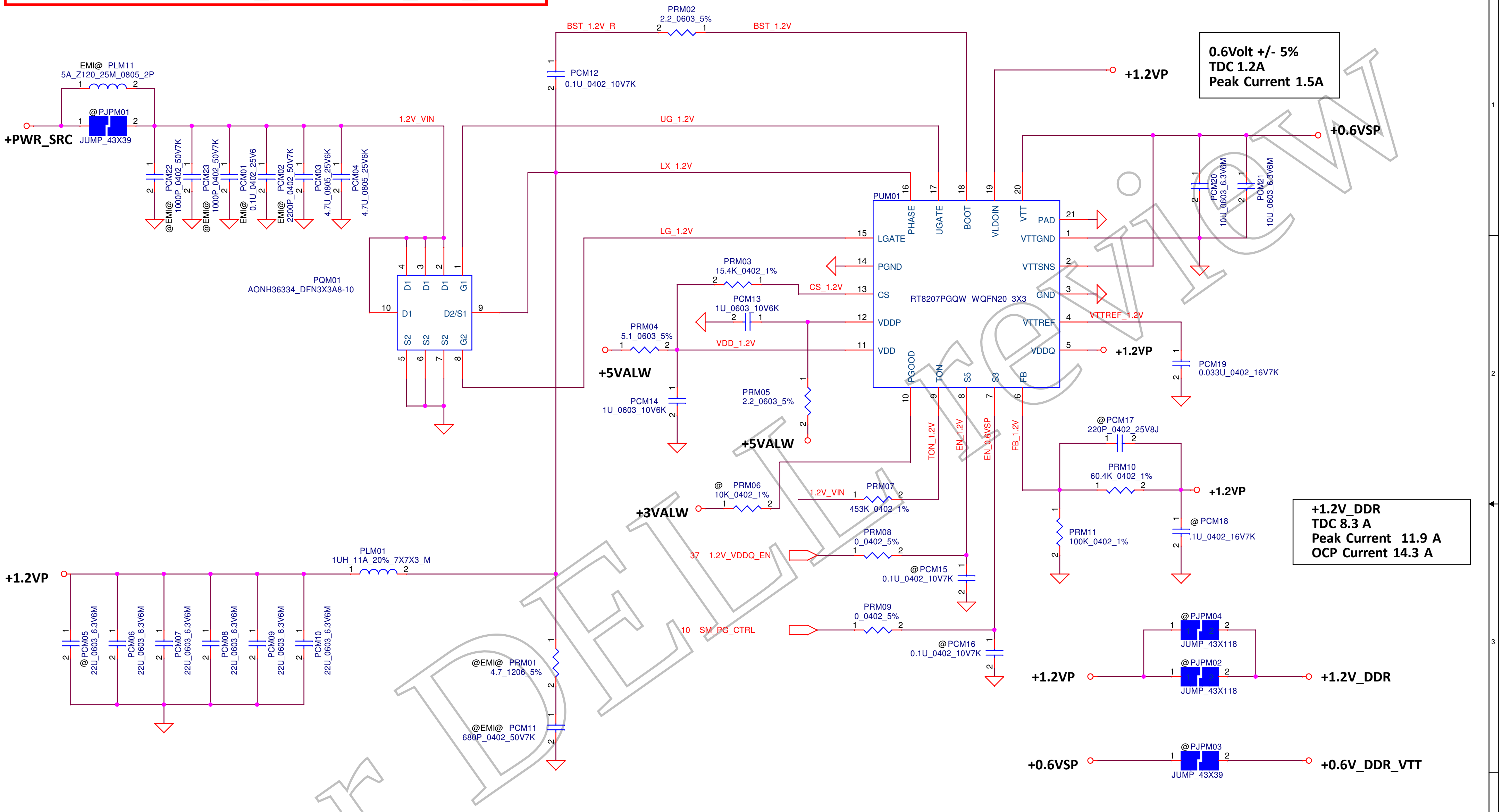
Main Func = 1.2V_DDR/+0.6V_DDR_VTT



+PWR_SRC
EMI@ PLM11
5A_Z120_25M_0805_2P
@PJPM01
JUMP_43X39
1.2V_VIN
@EMI@ PCM22 1000P_0402_50V7K
@EMI@ PCM23 1000P_0402_50V7K
EMI@ PCM01 0.1U_0402_25V6
EMI@ PCM02 2200P_0402_50V7K
PCM03 4.7U_0805_25V6K
PCM04 4.7U_0805_25V6K
PQM01
AONH36334_DFN3X3A8-10
D1 D1 D1 G1 D1 D2/S1 S2 S2 S2 G2
BST_1.2V_R
PRM02
2.2_0603_5%
BST_1.2V
PCM12
0.1U_0402_10V7K
UG_1.2V
LX_1.2V
LG_1.2V
PUM01
PHASE UGATE BOOT VLDOIN VTT
PAD VTTGND VTTSNS GND VTTREF VDDQ
LGATE PGND CS VDDP VDD
PGOOD TON S5 S3 FB
RT8207PGQW_WQFN20_3X3
+1.2VP
PRM03
15.4K_0402_1%
CS_1.2V
PCM13
1U_0603_10V6K
PRM04
5.1_0603_5%
VDD_1.2V
+5VALW
PCM14
1U_0603_10V6K
PRM05
2.2_0603_5%
+5VALW
+0.6VSP
PCM20 10U_0603_6.3V6M
PCM21 10U_0603_6.3V6M
VTTREF_1.2V
PCM19
0.033U_0402_16V7K
+1.2VP
TON_1.2V
EN_1.2V
EN_0.6VSP
FB_1.2V
@PCM17
220P_0402_25V8J
PRM10
60.4K_0402_1%
+1.2VP
PRM11
100K_0402_1%
@PCM18
.1U_0402_16V7K
+3VALW
@ PRM06
10K_0402_1%
1.2V_VIN
PRM07
453K_0402_1%
PRM08
0_0402_5%
37 1.2V_VDDQ_EN
@PCM15
0.1U_0402_10V7K
PRM09
0_0402_5%
10 SM_PG_CTRL
@PCM16
0.1U_0402_10V7K
+1.2VP
PLM01
1UH_11A_20%_7X7X3_M
@PCM05 22U_0603_6.3V6M
PCM06 22U_0603_6.3V6M
PCM07 22U_0603_6.3V6M
PCM08 22U_0603_6.3V6M
PCM09 22U_0603_6.3V6M
PCM10 22U_0603_6.3V6M
@EMI@ PRM01
4.7_1206_5%
@EMI@ PCM11
680P_0402_50V7K
@PJPM04
JUMP_43X118
@PJPM02
JUMP_43X118
+1.2VP
+1.2V_DDR
@PJPM03
JUMP_43X39
+0.6VSP
+0.6V_DDR_VTT

0.6Volt +/- 5%
TDC 1.2A
Peak Current 1.5A

+1.2V_DDR
TDC 8.3 A
Peak Current 11.9 A
OCP Current 14.3 A

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title
PWR_+1.2V_DDR/+0.6V_DDR_VTT

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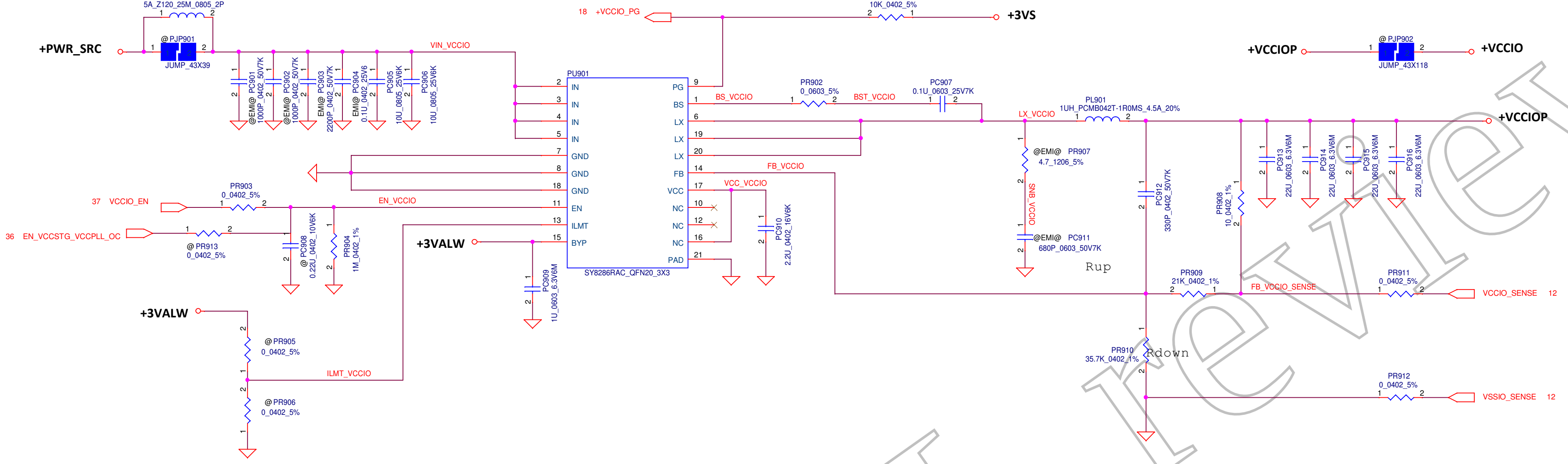
Main Func = VCCIO

+VCCIO (0.95V)
TDC 4.5 A
Peak Current 6.4 A
OCP Current 9 A Fix by IC



+PWR_SRC
EMI@ PL911
5A_Z120_25M_0805_2P
@ PJP901
JUMP_43X39
VIN_VCCIO
@EMI@ PC901 1000P_0402_50V7K
@EMI@ PC902 1000P_0402_50V7K
EMI@ PC903 2200P_0402_50V7K
EMI@ PC904 0.1U_0402_25V6
PC905 10U_0805_25V6K
PC906 10U_0805_25V6K
18 +VCCIO_PG
@ PR901
10K_0402_5%
+3VS
PU901
IN
GND
EN
ILMT
BYP
PG
BS
LX
FB
VCC
NC
PAD
SY8286RAC_QFN20_3X3
BS_VCCIO
PR902
0_0603_5%
BST_VCCIO
PC907
0.1U_0603_25V7K
LX_VCCIO
PL901
1UH_PCMB042T-1R0MS_4.5A_20%
FB_VCCIO
VCC_VCCIO
PC910 2.2U_0402_16V6K
37 VCCIO_EN
PR903
0_0402_5%
EN_VCCIO
36 EN_VCCSTG_VCCPLL_OC
@ PR913
0_0402_5%
@ PC908 0.22U_0402_10V6K
PR904 1M_0402_1%
+3VALW
PC909 1U_0603_6.3V6M
@EMI@ PR907
4.7_1206_5%
SNB_VCCIO
@EMI@ PC911
680P_0603_50V7K
PC912 330P_0402_50V7K
Rup
PR908 10_0402_1%
PC913 22U_0603_6.3V6M
PC914 22U_0603_6.3V6M
PC915 22U_0603_6.3V6M
PC916 22U_0603_6.3V6M
+VCCIOP
@ PJP902
JUMP_43X118
+VCCIO
PR909
21K_0402_1%
FB_VCCIO_SENSE
PR911
0_0402_5%
VCCIO_SENSE 12
PR910
35.7K_0402_1%
Rdown
PR912
0_0402_5%
VSSIO_SENSE 12
+3VALW
@ PR905
0_0402_5%
ILMT_VCCIO
@ PR906
0_0402_5%

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: PWR_+VCCIO

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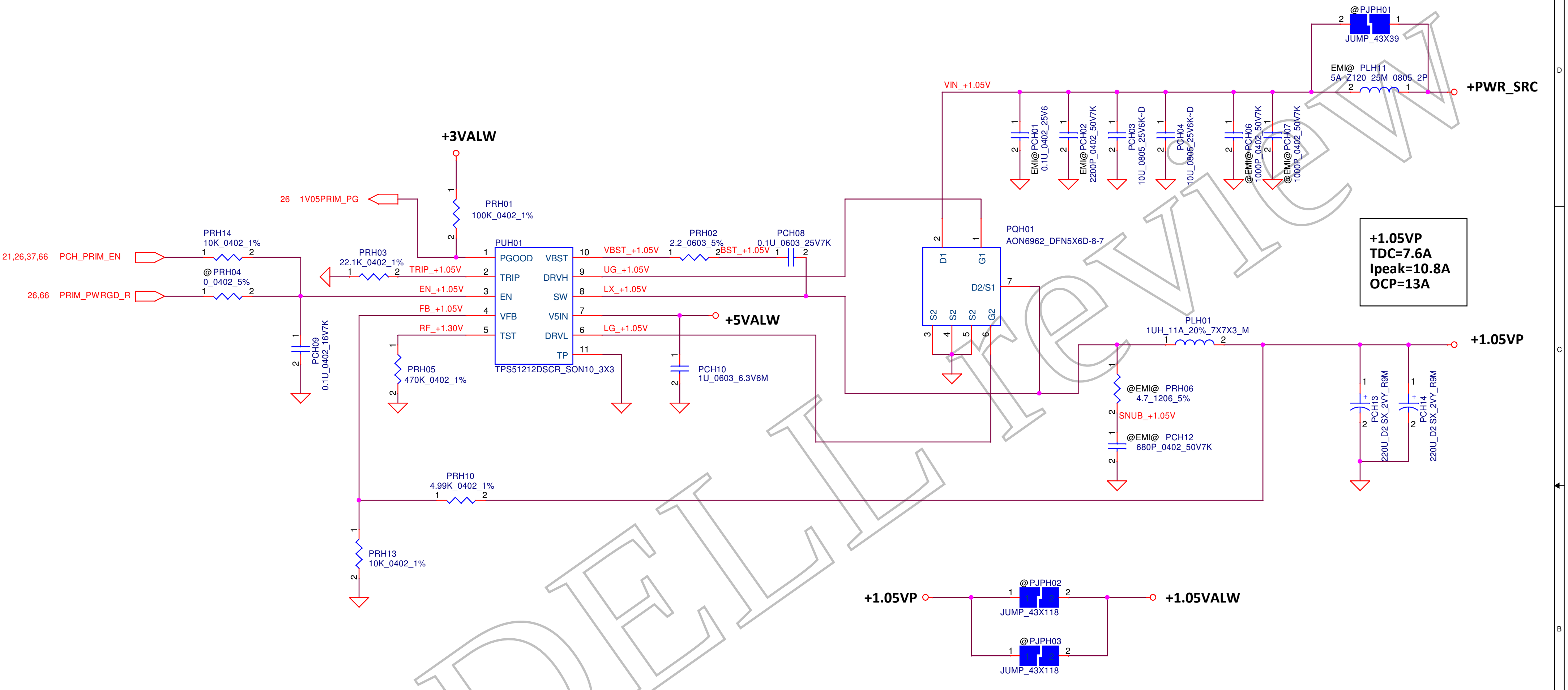
Size Document Number LA-F611P Rev 0.1

Date: Thursday, March 22, 2018

Main Func = 1.05VALW


+3VALW
PRH01
100K_0402_1%
26 1V05PRIM_PG
PRH14
10K_0402_1%
21,26,37,66 PCH_PRIM_EN
@PRH04
0_0402_5%
26,66 PRIM_PWRGD_R
PRH03
22.1K_0402_1%
TRIP_+1.05V
EN_+1.05V
FB_+1.05V
RF_+1.30V
PCH09
0.1U_0402_16V7K
PRH05
470K_0402_1%
PUH01
PGOOD
TRIP
EN
VFB
TST
VBST
DRVH
SW
V5IN
DRVL
TP
TPS51212DSCR_SON10_3X3
VBST_+1.05V
UG_+1.05V
LX_+1.05V
LG_+1.05V
PRH02
2.2_0603_5%
BST_+1.05V
PCH08
0.1U_0603_25V7K
+5VALW
PCH10
1U_0603_6.3V6M
VIN_+1.05V
PQH01
AON6962_DFN5X6D-8-7
D1
G1
D2/S1
S2
G2
EMI@ PCH01
0.1U_0402_25V6
EMI@ PCH02
2200P_0402_50V7K
PCH03
10U_0805_25V6K-D
PCH04
10U_0805_25V6K-D
@EMI@ PCH06
1000P_0402_50V7K
@EMI@ PCH07
1000P_0402_50V7K
@PJPH01
JUMP_43X39
EMI@ PLH11
5A_Z120_25M_0805_2P
+PWR_SRC
PLH01
1UH_11A_20%_7X7X3_M
+1.05VP
@EMI@ PRH06
4.7_1206_5%
SNUB_+1.05V
@EMI@ PCH12
680P_0402_50V7K
PCH13
220U_D2 SX_2VY_R9M
PCH14
220U_D2 SX_2VY_R9M
PRH10
4.99K_0402_1%
PRH13
10K_0402_1%
+1.05VP
@PJPH02
JUMP_43X118
@PJPH03
JUMP_43X118
+1.05VALW

+1.05VP
TDC=7.6A
Ipeak=10.8A
OCP=13A

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title PWR-1.05VALW
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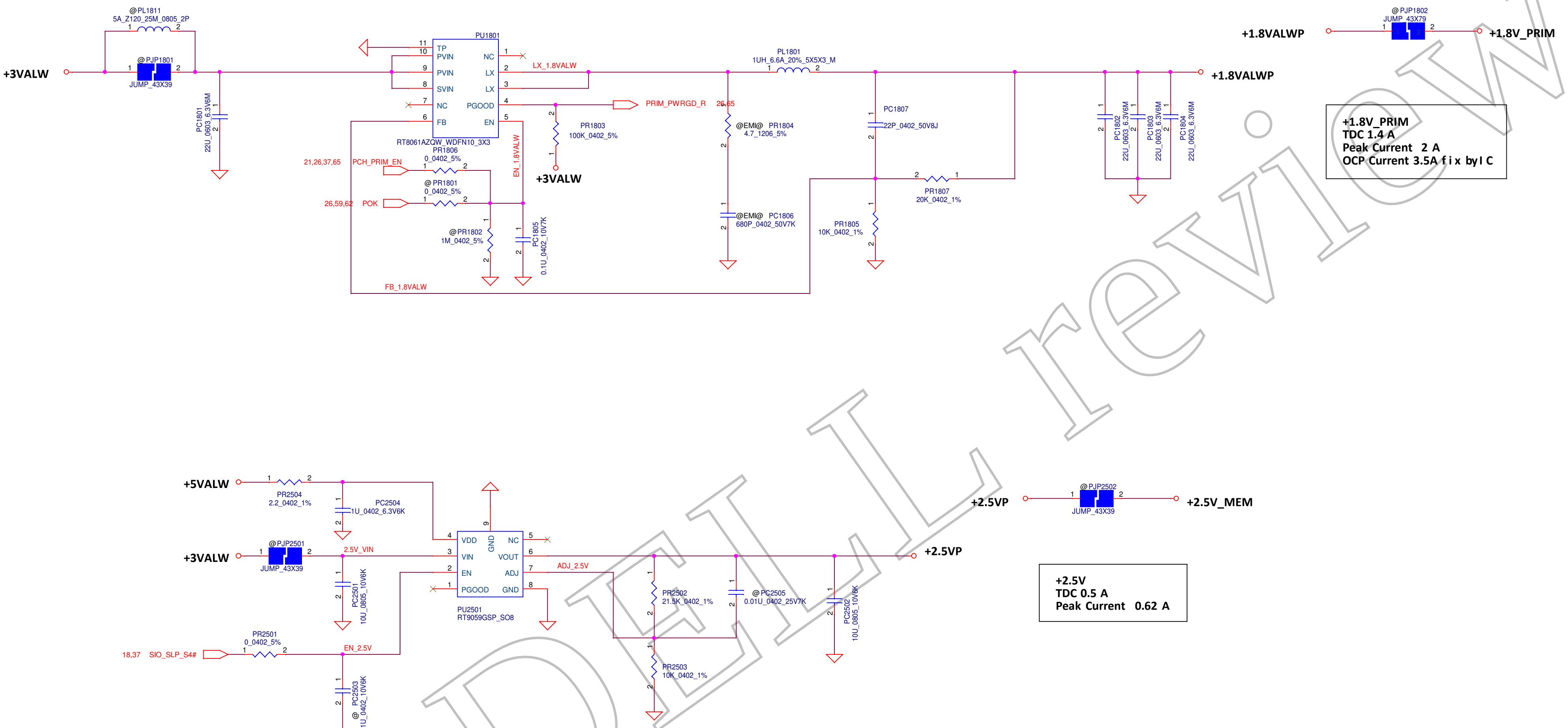
Main Func = +1.8V_PRIM/+2.5V_MEM


+3VALW
@PL1811
5A_Z120_25M_0805_2P
@PJP1801
JUMP_43X39
PC1801
22U_0603_6.3V6M
PU1801
TP
PVIN
PVIN
SVIN
NC
FB
NC
LX
LX
PGOOD
EN
RT8061AZQW_WDFN10_3X3
LX_1.8VALW
PRIM_PWRGD_R
26,65
PR1803
100K_0402_5%
+3VALW
EN_1.8VALW
PR1806
0_0402_5%
21,26,37,65
PCH_PRIM_EN
@PR1801
0_0402_5%
26,59,62
POK
@PR1802
1M_0402_5%
PC1805
0.1U_0402_10V7K
FB_1.8VALW
PL1801
1UH_6.6A_20%_5X5X3_M
@EMI@ PR1804
4.7_1206_5%
@EMI@ PC1806
680P_0402_50V7K
PC1807
22P_0402_50V8J
PR1807
20K_0402_1%
PR1805
10K_0402_1%
PC1802
22U_0603_6.3V6M
PC1803
22U_0603_6.3V6M
PC1804
22U_0603_6.3V6M
+1.8VALWP
+1.8VALWP
@PJP1802
JUMP_43X79
+1.8V_PRIM
+5VALW
PR2504
2.2_0402_1%
PC2504
1U_0402_6.3V6K
+3VALW
@PJP2501
JUMP_43X39
2.5V_VIN
PC2501
10U_0805_10V6K
PR2501
0_0402_5%
18,37
SIO_SLP_S4#
EN_2.5V
@ PC2503
0.1U_0402_10V6K
VDD
VIN
EN
PGOOD
GND
NC
VOUT
ADJ
GND
PU2501
RT9059GSP_SO8
ADJ_2.5V
PR2502
21.5K_0402_1%
PR2503
10K_0402_1%
@PC2505
0.01U_0402_25V7K
PC2502
10U_0805_10V6K
+2.5VP
+2.5VP
@PJP2502
JUMP_43X39
+2.5V_MEM

+1.8V_PRIM
TDC 1.4 A
Peak Current 2 A
OCP Current 3.5A fix by IC

+2.5V
TDC 0.5 A
Peak Current 0.62 A

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title PWR_+1.8V_PRIM/+2.5V_MEM
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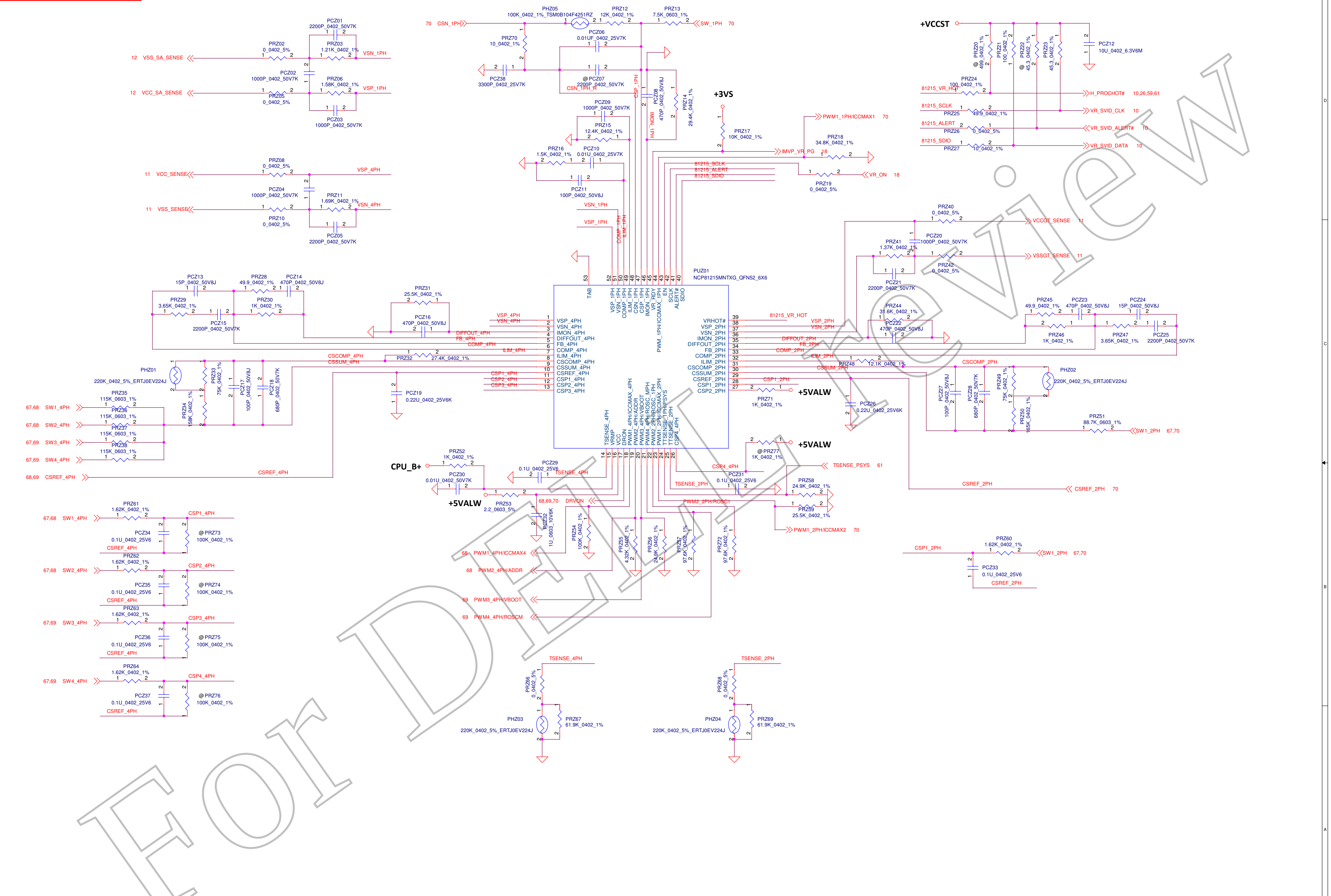
Main Func = VCORE


PUZ01
NCP81215MNTXG_QFN52_6X6
+VCCST
+3VS
+5VALW
CPU_B+
70 CSN_1PH
SW_1PH 70
PHZ05 100K_0402_1%_TSM0B104F4251RZ
PRZ12 12K_0402_1%
PRZ13 7.5K_0603_1%
PRZ70 10_0402_1%
PCZ06 0.01UF_0402_25V7K
PCZ38 3300P_0402_25V7K
@PCZ07 2200P_0402_50V7K
CSN_1PH_R
CSP_1PH
PCZ08 470P_0402_50V8J
PRZ14 29.4K_0402_1%
IPH_NOW
PCZ09 1000P_0402_50V7K
PRZ15 12.4K_0402_1%
PRZ16 1.5K_0402_1%
PCZ10 0.01U_0402_25V7K
PCZ11 100P_0402_50V8J
PRZ17 10K_0402_1%
PWM1_1PH/ICCMAX1 70
IMVP_VR_PG 18
PRZ18 34.8K_0402_1%
81215_SCLK
81215_ALERT
81215_SDIO
VR_ON 18
PRZ19 0_0402_5%
12 VSS_SA_SENSE
12 VCC_SA_SENSE
PCZ01 2200P_0402_50V7K
PRZ02 0_0402_5%
PRZ03 1.21K_0402_1%
VSN_1PH
PCZ02 1000P_0402_50V7K
PRZ06 1.58K_0402_1%
VSP_1PH
PRZ05 0_0402_5%
PCZ03 1000P_0402_50V7K
11 VCC_SENSE
PRZ08 0_0402_5%
VSP_4PH
PCZ04 1000P_0402_50V7K
PRZ11 1.69K_0402_1%
VSN_4PH
11 VSS_SENSE
PRZ10 0_0402_5%
PCZ05 2200P_0402_50V7K
PRZ20 499_0402_1%
PRZ21 100_0402_1%
PRZ22 45.3_0402_1%
PRZ23 45.3_0402_1%
PCZ12 10U_0402_6.3V6M
81215_VR_HOT
PRZ24 100_0402_1%
H_PROCHOT# 10,26,59,61
81215_SCLK PRZ25 49.9_0402_1% VR_SVID_CLK 10
81215_ALERT PRZ26 0_0402_5% VR_SVID_ALERT# 10
81215_SDIO PRZ27 10_0402_1% VR_SVID_DATA 10
PRZ40 0_0402_5%
VCCGT_SENSE 11
PCZ20 1000P_0402_50V7K
PRZ41 1.37K_0402_1%
VSSGT_SENSE 11
PRZ42 0_0402_5%
PCZ21 2200P_0402_50V7K
PCZ13 15P_0402_50V8J
PRZ28 49.9_0402_1%
PCZ14 470P_0402_50V8J
PRZ29 3.65K_0402_1%
PRZ30 1K_0402_1%
PCZ15 2200P_0402_50V7K
PRZ31 25.5K_0402_1%
PCZ16 470P_0402_50V8J
DIFFOUT_4PH
FB_4PH
COMP_4PH
ILIM_4PH
CSCOMP_4PH
CSSUM_4PH
PRZ32 27.4K_0402_1%
PCZ19 0.22U_0402_25V6K
CSP1_4PH
CSP2_4PH
CSP3_4PH
PHZ01 220K_0402_5%_ERTJ0EV224J
PRZ33 75K_0402_1%
PRZ34 158K_0402_1%
PCZ17 100P_0402_50V8J
PCZ18 680P_0402_50V7K
67,68 SW1_4PH PRZ35 115K_0603_1%
67,68 SW2_4PH PRZ36 115K_0603_1%
67,69 SW3_4PH PRZ37 115K_0603_1%
67,69 SW4_4PH PRZ38 115K_0603_1%
68,69 CSREF_4PH
VSP_4PH VSN_4PH IMON_4PH DIFFOUT_4PH FB_4PH COMP_4PH ILIM_4PH CSCOMP_4PH CSSUM_4PH CSREF_4PH CSP1_4PH CSP2_4PH CSP3_4PH
TAB
VSP_1PH VSN_1PH COMP_1PH ILIM_1PH CSN_1PH CSP_1PH IMON_1PH VR_RDY PWM_1PH/ICCMAX_1PH EN SCLK ALERT# SDIO
VRHOT# VSP_2PH VSN_2PH IMON_2PH DIFFOUT_2PH FB_2PH COMP_2PH ILIM_2PH CSCOMP_2PH CSSUM_2PH CSREF_2PH CSP1_2PH CSP2_2PH
TSENSE_4PH VRMP VCC DRON PWM1_4PH/ICCMAX_4PH PWM2_4PH/ADDR PWM3_4PH/VBOOT PWM4_4PH/ROSC_1MPH PWM2_2PH/ROSC_1PH PWM1_2PH/ICCMAX_2PH TTSENSE_1PH/PSYS TSENSE_2PH CSP4_4PH
81215_VR_HOT
VSP_2PH
VSN_2PH
DIFFOUT_2PH
FB_2PH
COMP_2PH
ILIM_2PH
CSSUM_2PH
CSP1_2PH
PRZ48 12.1K_0402_1%
PRZ71 1K_0402_1%
PCZ26 0.22U_0402_25V6K
PRZ44 31.6K_0402_1%
PCZ22 470P_0402_50V8J
PRZ45 49.9_0402_1%
PCZ23 470P_0402_50V8J
PCZ24 15P_0402_50V8J
PRZ46 1K_0402_1%
PRZ47 3.65K_0402_1%
PCZ25 2200P_0402_50V7K
CSCOMP_2PH
PHZ02 220K_0402_5%_ERTJ0EV224J
PCZ27 100P_0402_50V8J
PCZ28 680P_0402_50V7K
PRZ49 75K_0402_1%
PRZ50 165K_0402_1%
PRZ51 88.7K_0603_1%
SW1_2PH 67,70
@PRZ77 1K_0402_1%
TSENSE_PSYS 61
PRZ58 24.9K_0402_1%
PRZ59 25.5K_0402_1%
CSREF_2PH
CSREF_2PH 70
PWM1_2PH/ICCMAX2 70
PWM2_2PH/ROSC1
TSENSE_2PH
PCZ31 0.1U_0402_25V6
CSP4_4PH
PRZ52 1K_0402_1%
PCZ29 0.1U_0402_25V6
TSENSE_4PH
PCZ30 0.01U_0402_50V7K
PRZ53 2.2_0603_5%
PCZ32 1U_0603_10V6K
68,69,70 DRVON
PRZ54 100K_0402_1%
PRZ55 4.32K_0402_1%
PRZ56 24.9K_0402_1%
PRZ57 97.6K_0402_1%
PRZ72 97.6K_0402_1%
68 PWM1_4PH/ICCMAX4
68 PWM2_4PH/ADDR
69 PWM3_4PH/VBOOT
69 PWM4_4PH/ROSCM
67,68 SW1_4PH PRZ61 1.62K_0402_1% CSP1_4PH
PCZ34 0.1U_0402_25V6
@PRZ73 100K_0402_1%
CSREF_4PH
67,68 SW2_4PH PRZ62 1.62K_0402_1% CSP2_4PH
PCZ35 0.1U_0402_25V6
@PRZ74 100K_0402_1%
CSREF_4PH
67,69 SW3_4PH PRZ63 1.62K_0402_1% CSP3_4PH
PCZ36 0.1U_0402_25V6
@PRZ75 100K_0402_1%
CSREF_4PH
67,69 SW4_4PH PRZ64 1.62K_0402_1% CSP4_4PH
PCZ37 0.1U_0402_25V6
@PRZ76 100K_0402_1%
CSREF_4PH
CSP1_2PH
PRZ60 1.62K_0402_1%
SW1_2PH 67,70
PCZ33 0.1U_0402_25V6
CSREF_2PH
TSENSE_4PH
PRZ66 0_0402_5%
PHZ03 220K_0402_5%_ERTJ0EV224J
PRZ67 61.9K_0402_1%
TSENSE_2PH
PRZ68 0_0402_5%
PHZ04 220K_0402_5%_ERTJ0EV224J
PRZ69 61.9K_0402_1%

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

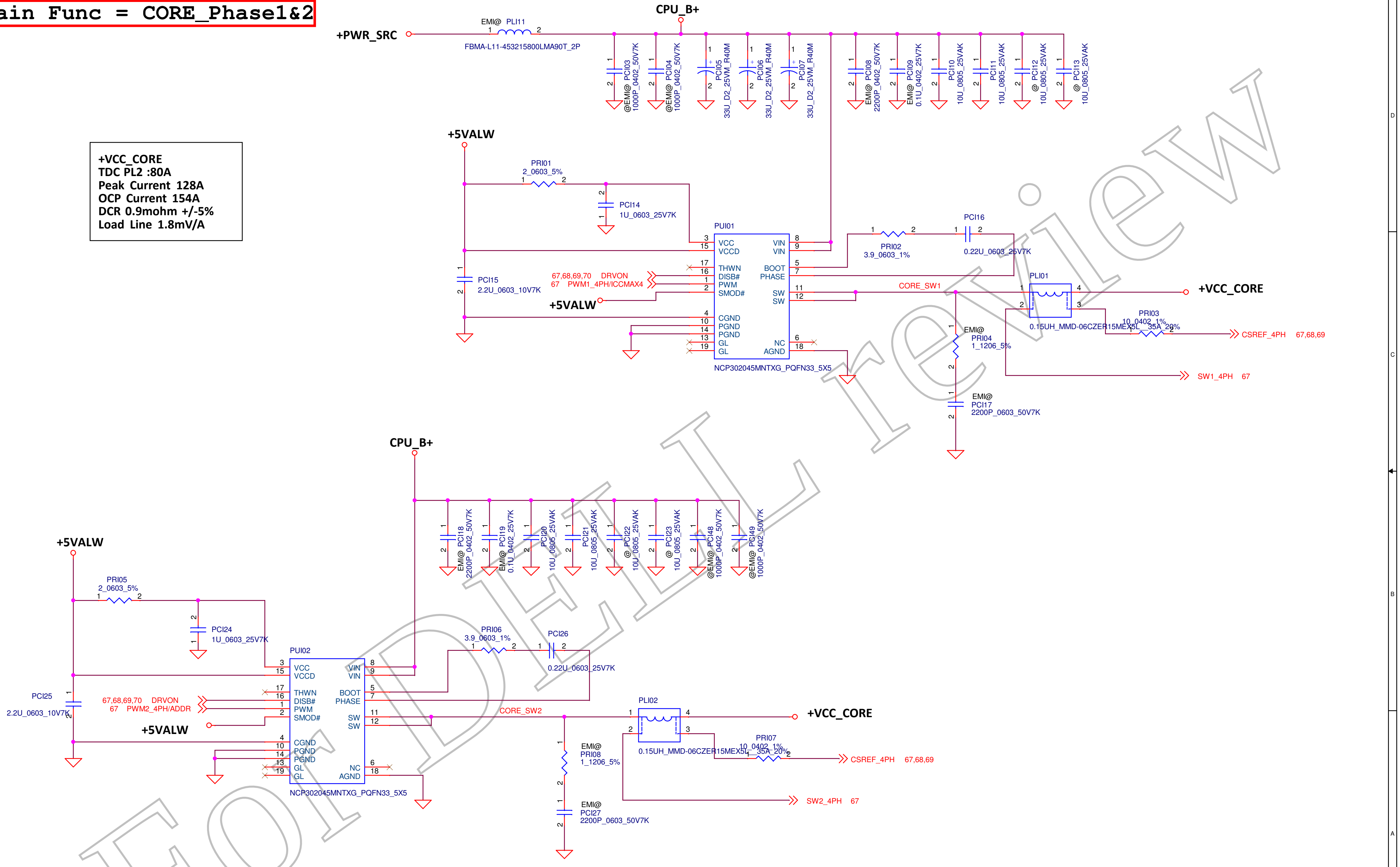
Title
+VCORE_NCP81215

Size Document Number
LA-F611P
Rev 0.1

Date: Thursday, March 22, 2018

Main Func = CORE_Phase1&2

+VCC_CORE
TDC PL2 :80A
Peak Current 128A
OCP Current 154A
DCR 0.9mohm +/-5%
Load Line 1.8mV/A


CPU_B+
+PWR_SRC
EMI@ PLI11
FBMA-L11-453215800LMA90T_2P
@EMI@ PCI03 1000P_0402_50V7K
@EMI@ PCI04 1000P_0402_50V7K
PCI05 33U_D2_25VM_R40M
PCI06 33U_D2_25VM_R40M
PCI07 33U_D2_25VM_R40M
EMI@ PCI08 2200P_0402_50V7K
EMI@ PCI09 0.1U_0402_25V7K
PCI10 10U_0805_25VAK
PCI11 10U_0805_25VAK
@ PCI12 10U_0805_25VAK
@ PCI13 10U_0805_25VAK
+5VALW
PRI01 2_0603_5%
PCI14 1U_0603_25V7K
PUI01
VCC VCCD THWN DISB# PWM SMOD# CGND PGND PGND GL GL
VIN VIN BOOT PHASE SW SW NC AGND
NCP302045MNTXG_PQFN33_5X5
PCI15 2.2U_0603_10V7K
67,68,69,70 DRVON
67 PWM1_4PH/ICCMAX4
+5VALW
PRI02 3.9_0603_1%
PCI16 0.22U_0603_25V7K
CORE_SW1
PLI01
0.15UH_MMD-06CZER15MEX5L 35A_20%
+VCC_CORE
PRI03 10_0402_1%
CSREF_4PH 67,68,69
SW1_4PH 67
EMI@ PRI04 1_1206_5%
EMI@ PCI17 2200P_0603_50V7K
CPU_B+
EMI@ PCI18 2200P_0402_50V7K
EMI@ PCI19 0.1U_0402_25V7K
PCI20 10U_0805_25VAK
PCI21 10U_0805_25VAK
@ PCI22 10U_0805_25VAK
@ PCI23 10U_0805_25VAK
@EMI@ PCI48 1000P_0402_50V7K
@EMI@ PCI49 1000P_0402_50V7K
+5VALW
PRI05 2_0603_5%
PCI24 1U_0603_25V7K
PUI02
NCP302045MNTXG_PQFN33_5X5
PCI25 2.2U_0603_10V7K
67,68,69,70 DRVON
67 PWM2_4PH/ADDR
+5VALW
PRI06 3.9_0603_1%
PCI26 0.22U_0603_25V7K
CORE_SW2
PLI02
0.15UH_MMD-06CZER15MEX5L 35A_20%
+VCC_CORE
PRI07 10_0402_1%
CSREF_4PH 67,68,69
SW2_4PH 67
EMI@ PRI08 1_1206_5%
EMI@ PCI27 2200P_0603_50V7K

Security Classification | Compal Secret Data
Issued Date 2016/01/06 | Deciphered Date 2017/01/06

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Compal Electronics, Inc.
Title *+VCC_CORE_Phase1&2*
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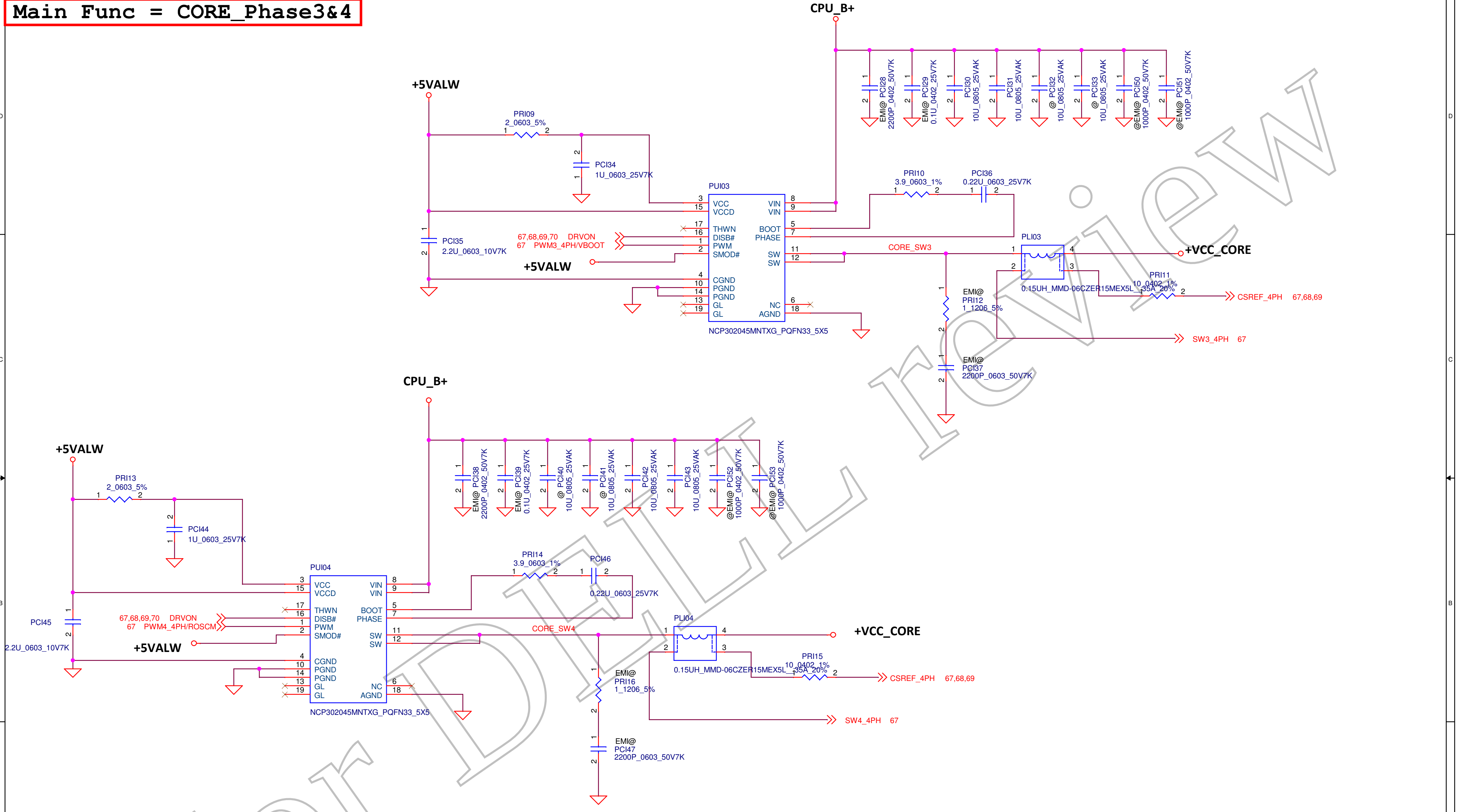
Main Func = CORE_Phase3&4



CPU_B+
PCI28 2200P_0402_50V7K EMI@
PCI29 0.1U_0402_25V7K EMI@
PCI30 10U_0805_25VAK
PCI31 10U_0805_25VAK
PCI32 10U_0805_25VAK @
PCI33 10U_0805_25VAK @
PCI50 1000P_0402_50V7K @EMI@
PCI51 1000P_0402_50V7K @EMI@
+5VALW
PRI09 2_0603_5%
PCI34 1U_0603_25V7K
PUI03
VCC
VCCD
THWN
DISB#
PWM
SMOD#
CGND
PGND
PGND
GL
GL
VIN
VIN
BOOT
PHASE
SW
SW
NC
AGND
NCP302045MNTXG_PQFN33_5X5
PCI35 2.2U_0603_10V7K
67,68,69,70 DRVON
67 PWM3_4PH/VBOOT
+5VALW
PRI10 3.9_0603_1%
PCI36 0.22U_0603_25V7K
CORE_SW3
PLI03
0.15UH_MMD-06CZER15MEX5L_35A_20%
+VCC_CORE
PRI11 10_0402_1%
CSREF_4PH 67,68,69
EMI@ PRI12 1_1206_5%
SW3_4PH 67
EMI@ PCI37 2200P_0603_50V7K
CPU_B+
PCI38 2200P_0402_50V7K EMI@
PCI39 0.1U_0402_25V7K EMI@
PCI40 10U_0805_25VAK @
PCI41 10U_0805_25VAK @
PCI42 10U_0805_25VAK
PCI43 10U_0805_25VAK
PCI52 1000P_0402_50V7K @EMI@
PCI53 1000P_0402_50V7K @EMI@
+5VALW
PRI13 2_0603_5%
PCI44 1U_0603_25V7K
PUI04
NCP302045MNTXG_PQFN33_5X5
PCI45 2.2U_0603_10V7K
67,68,69,70 DRVON
67 PWM4_4PH/ROSCM
+5VALW
PRI14 3.9_0603_1%
PCI46 0.22U_0603_25V7K
CORE_SW4
PLI04
0.15UH_MMD-06CZER15MEX5L_35A_20%
+VCC_CORE
PRI15 10_0402_1%
CSREF_4PH 67,68,69
EMI@ PRI16 1_1206_5%
SW4_4PH 67
EMI@ PCI47 2200P_0603_50V7K

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title +VCC_CORE_Phase3&4
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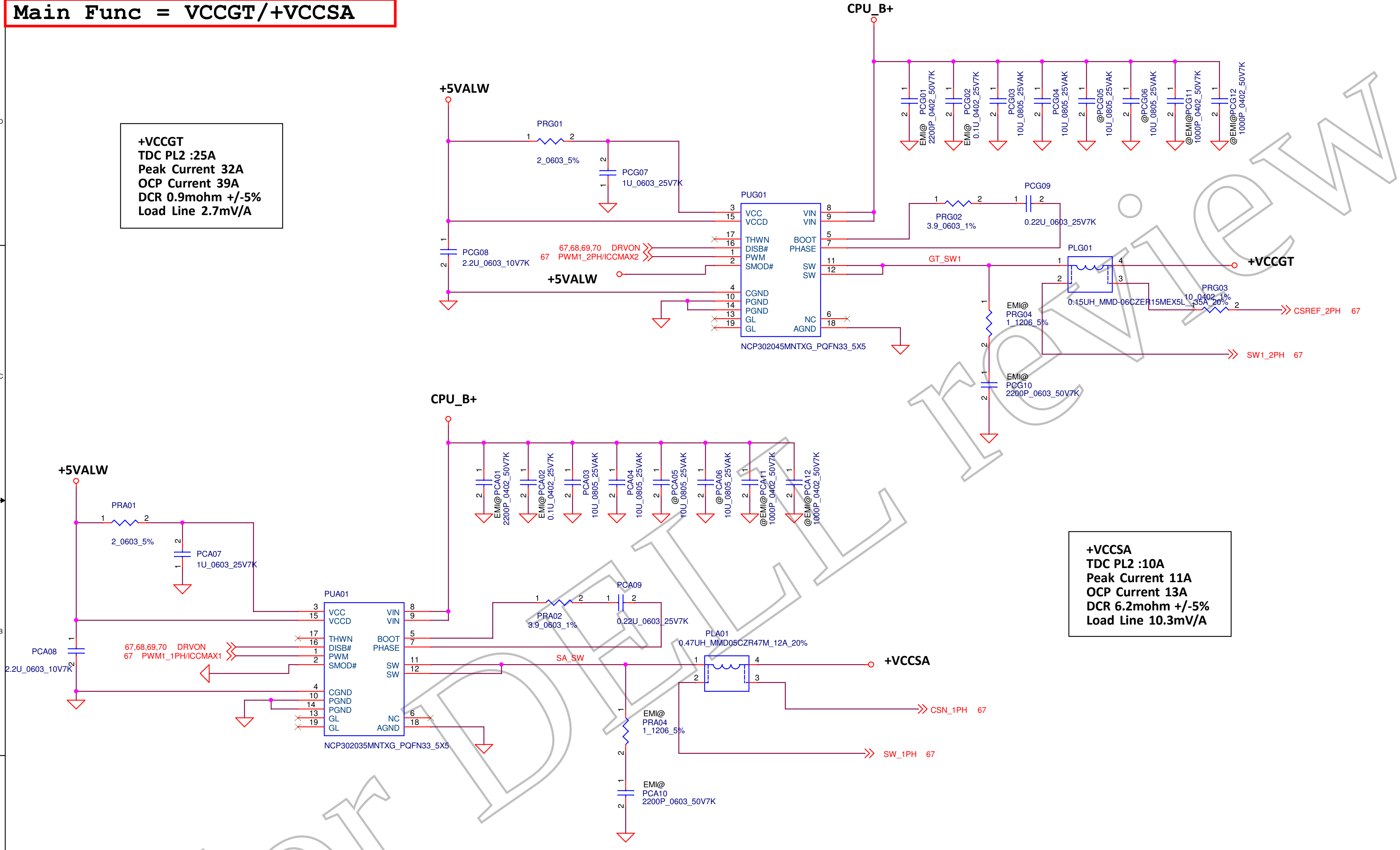
Main Func = VCCGT/+VCCSA


CPU_B+
PCG01
EMI@
2200P_0402_50V7K
PCG02
EMI@
0.1U_0402_25V7K
PCG03
10U_0805_25VAK
PCG04
10U_0805_25VAK
@PCG05
10U_0805_25VAK
@PCG06
10U_0805_25VAK
@EMI@PCG11
1000P_0402_50V7K
@EMI@PCG12
1000P_0402_50V7K
+5VALW
PRG01
2_0603_5%
PCG07
1U_0603_25V7K
PUG01
VCC
VCCD
THWN
DISB#
PWM
SMOD#
CGND
PGND
PGND
GL
GL
VIN
VIN
BOOT
PHASE
SW
SW
NC
AGND
NCP302045MNTXG_PQFN33_5X5
PCG08
2.2U_0603_10V7K
67,68,69,70 DRVON
67 PWM1_2PH/ICCMAX2
+5VALW
PRG02
3.9_0603_1%
PCG09
0.22U_0603_25V7K
GT_SW1
PLG01
0.15UH_MMD-06CZER15MEX5L_35A_20%
+VCCGT
PRG03
10_0402_1%
CSREF_2PH 67
EMI@
PRG04
1_1206_5%
SW1_2PH 67
EMI@
PCG10
2200P_0603_50V7K
CPU_B+
EMI@PCA01
2200P_0402_50V7K
EMI@PCA02
0.1U_0402_25V7K
PCA03
10U_0805_25VAK
PCA04
10U_0805_25VAK
@PCA05
10U_0805_25VAK
@PCA06
10U_0805_25VAK
@EMI@PCA11
1000P_0402_50V7K
@EMI@PCA12
1000P_0402_50V7K
+5VALW
PRA01
2_0603_5%
PCA07
1U_0603_25V7K
PUA01
VCC
VCCD
THWN
DISB#
PWM
SMOD#
CGND
PGND
PGND
GL
GL
VIN
VIN
BOOT
PHASE
SW
SW
NC
AGND
NCP302035MNTXG_PQFN33_5X5
PCA08
2.2U_0603_10V7K
67,68,69,70 DRVON
67 PWM1_1PH/ICCMAX1
PRA02
3.9_0603_1%
PCA09
0.22U_0603_25V7K
SA_SW
PLA01
0.47UH_MMD05CZR47M_12A_20%
+VCCSA
CSN_1PH 67
EMI@
PRA04
1_1206_5%
SW_1PH 67
EMI@
PCA10
2200P_0603_50V7K

+VCCGT
TDC PL2 :25A
Peak Current 32A
OCP Current 39A
DCR 0.9mohm +/-5%
Load Line 2.7mV/A

+VCCSA
TDC PL2 :10A
Peak Current 11A
OCP Current 13A
DCR 6.2mohm +/-5%
Load Line 10.3mV/A

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title ***+VCC_GT/+VCC_SA***

Size Document Number ***LA-F611P*** Rev 0.1

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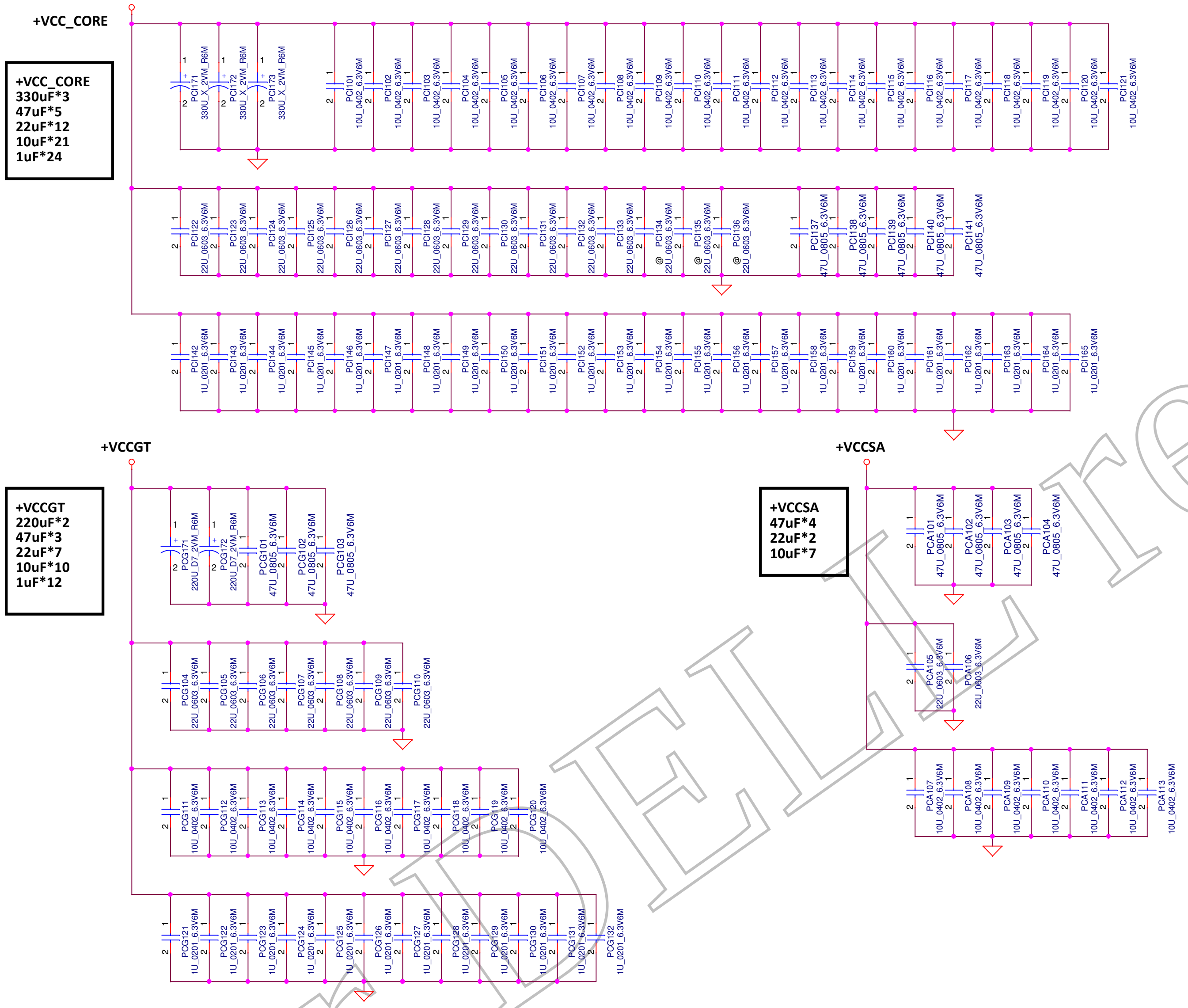
Main Func = PWR_CPU DECOUPLING


+VCC_CORE
+VCC_CORE
330uF*3
47uF*5
22uF*12
10uF*21
1uF*24
PCI171 330U_X_2VM_R6M
PCI172 330U_X_2VM_R6M
PCI173 330U_X_2VM_R6M
PCI101 10U_0402_6.3V6M
PCI102 10U_0402_6.3V6M
PCI103 10U_0402_6.3V6M
PCI104 10U_0402_6.3V6M
PCI105 10U_0402_6.3V6M
PCI106 10U_0402_6.3V6M
PCI107 10U_0402_6.3V6M
PCI108 10U_0402_6.3V6M
PCI109 10U_0402_6.3V6M
PCI110 10U_0402_6.3V6M
PCI111 10U_0402_6.3V6M
PCI112 10U_0402_6.3V6M
PCI113 10U_0402_6.3V6M
PCI114 10U_0402_6.3V6M
PCI115 10U_0402_6.3V6M
PCI116 10U_0402_6.3V6M
PCI117 10U_0402_6.3V6M
PCI118 10U_0402_6.3V6M
PCI119 10U_0402_6.3V6M
PCI120 10U_0402_6.3V6M
PCI121 10U_0402_6.3V6M
PCI122 22U_0603_6.3V6M
PCI123 22U_0603_6.3V6M
PCI124 22U_0603_6.3V6M
PCI125 22U_0603_6.3V6M
PCI126 22U_0603_6.3V6M
PCI127 22U_0603_6.3V6M
PCI128 22U_0603_6.3V6M
PCI129 22U_0603_6.3V6M
PCI130 22U_0603_6.3V6M
PCI131 22U_0603_6.3V6M
PCI132 22U_0603_6.3V6M
PCI133 22U_0603_6.3V6M
@ PCI134 22U_0603_6.3V6M
@ PCI135 22U_0603_6.3V6M
@ PCI136 22U_0603_6.3V6M
PCI137 47U_0805_6.3V6M
PCI138 47U_0805_6.3V6M
PCI139 47U_0805_6.3V6M
PCI140 47U_0805_6.3V6M
PCI141 47U_0805_6.3V6M
PCI142 1U_0201_6.3V6M
PCI143 1U_0201_6.3V6M
PCI144 1U_0201_6.3V6M
PCI145 1U_0201_6.3V6M
PCI146 1U_0201_6.3V6M
PCI147 1U_0201_6.3V6M
PCI148 1U_0201_6.3V6M
PCI149 1U_0201_6.3V6M
PCI150 1U_0201_6.3V6M
PCI151 1U_0201_6.3V6M
PCI152 1U_0201_6.3V6M
PCI153 1U_0201_6.3V6M
PCI154 1U_0201_6.3V6M
PCI155 1U_0201_6.3V6M
PCI156 1U_0201_6.3V6M
PCI157 1U_0201_6.3V6M
PCI158 1U_0201_6.3V6M
PCI159 1U_0201_6.3V6M
PCI160 1U_0201_6.3V6M
PCI161 1U_0201_6.3V6M
PCI162 1U_0201_6.3V6M
PCI163 1U_0201_6.3V6M
PCI164 1U_0201_6.3V6M
PCI165 1U_0201_6.3V6M
+VCCGT
+VCCGT
220uF*2
47uF*3
22uF*7
10uF*10
1uF*12
PCG171 220U_D7_2VM_R6M
PCG172 220U_D7_2VM_R6M
PCG101 47U_0805_6.3V6M
PCG102 47U_0805_6.3V6M
PCG103 47U_0805_6.3V6M
PCG104 22U_0603_6.3V6M
PCG105 22U_0603_6.3V6M
PCG106 22U_0603_6.3V6M
PCG107 22U_0603_6.3V6M
PCG108 22U_0603_6.3V6M
PCG109 22U_0603_6.3V6M
PCG110 22U_0603_6.3V6M
PCG111 10U_0402_6.3V6M
PCG112 10U_0402_6.3V6M
PCG113 10U_0402_6.3V6M
PCG114 10U_0402_6.3V6M
PCG115 10U_0402_6.3V6M
PCG116 10U_0402_6.3V6M
PCG117 10U_0402_6.3V6M
PCG118 10U_0402_6.3V6M
PCG119 10U_0402_6.3V6M
PCG120 10U_0402_6.3V6M
PCG121 1U_0201_6.3V6M
PCG122 1U_0201_6.3V6M
PCG123 1U_0201_6.3V6M
PCG124 1U_0201_6.3V6M
PCG125 1U_0201_6.3V6M
PCG126 1U_0201_6.3V6M
PCG127 1U_0201_6.3V6M
PCG128 1U_0201_6.3V6M
PCG129 1U_0201_6.3V6M
PCG130 1U_0201_6.3V6M
PCG131 1U_0201_6.3V6M
PCG132 1U_0201_6.3V6M
+VCCSA
+VCCSA
47uF*4
22uF*2
10uF*7
PCA101 47U_0805_6.3V6M
PCA102 47U_0805_6.3V6M
PCA103 47U_0805_6.3V6M
PCA104 47U_0805_6.3V6M
PCA105 22U_0603_6.3V6M
PCA106 22U_0603_6.3V6M
PCA107 10U_0402_6.3V6M
PCA108 10U_0402_6.3V6M
PCA109 10U_0402_6.3V6M
PCA110 10U_0402_6.3V6M
PCA111 10U_0402_6.3V6M
PCA112 10U_0402_6.3V6M
PCA113 10U_0402_6.3V6M

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title PWR-CPU DECOUPLING

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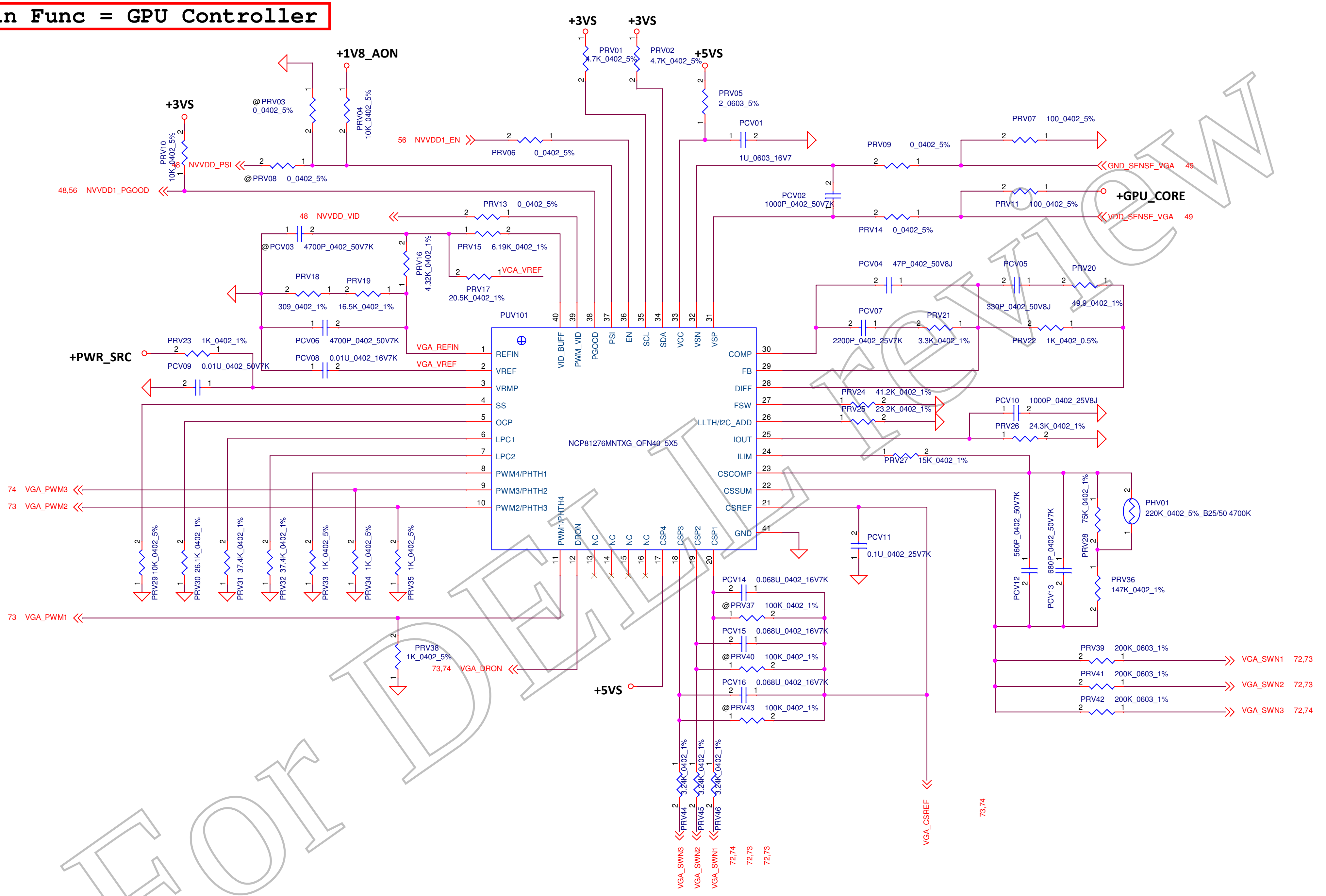
Main Func = GPU Controller



+3VS
+3VS
+1V8_AON
+5VS
+3VS
PRV01 4.7K_0402_5%
PRV02 4.7K_0402_5%
PRV05 2_0603_5%
PCV01 1U_0603_16V7
@PRV03 0_0402_5%
PRV04 10K_0402_5%
PRV10 10K_0402_5%
56 NVVDD1_EN
PRV06 0_0402_5%
48 NVVDD_PSI
@PRV08 0_0402_5%
48,56 NVVDD1_PGOOD
PRV07 100_0402_5%
PRV09 0_0402_5%
GND_SENSE_VGA 49
PCV02 1000P_0402_50V7K
+GPU_CORE
PRV11 100_0402_5%
PRV14 0_0402_5%
VDD_SENSE_VGA 49
48 NVVDD_VID
PRV13 0_0402_5%
@PCV03 4700P_0402_50V7K
PRV16 4.32K_0402_1%
PRV15 6.19K_0402_1%
PRV17 20.5K_0402_1%
VGA_VREF
PRV18 309_0402_1%
PRV19 16.5K_0402_1%
PUV101
PCV06 4700P_0402_50V7K
PCV08 0.01U_0402_16V7K
VGA_REFIN
VGA_VREF
+PWR_SRC
PRV23 1K_0402_1%
PCV09 0.01U_0402_50V7K
PCV04 47P_0402_50V8J
PCV05 330P_0402_50V8J
PRV20 49.9_0402_1%
PCV07 2200P_0402_25V7K
PRV21 3.3K_0402_1%
PRV22 1K_0402_0.5%
VID_BUFF
PWM_VID
PGOOD
PSI
EN
SCL
SDA
VCC
VSN
VSP
REFIN
VREF
VRMP
SS
OCP
LPC1
LPC2
PWM4/PHTH1
PWM3/PHTH2
PWM2/PHTH3
COMP
FB
DIFF
FSW
LLTH/I2C_ADD
IOUT
ILIM
CSCOMP
CSSUM
CSREF
GND
PWM1/PHTH4
DRON
NC
NC
NC
NC
CSP4
CSP3
CSP2
CSP1
NCP81276MNTXG_QFN40_5X5
PRV24 41.2K_0402_1%
PRV25 23.2K_0402_1%
PCV10 1000P_0402_25V8J
PRV26 24.3K_0402_1%
PRV27 15K_0402_1%
PCV12 560P_0402_50V7K
PCV13 680P_0402_50V7K
PRV28 75K_0402_1%
PHV01 220K_0402_5%_B25/50 4700K
PRV36 147K_0402_1%
PCV11 0.1U_0402_25V7K
74 VGA_PWM3
73 VGA_PWM2
PRV29 10K_0402_5%
PRV30 26.1K_0402_1%
PRV31 37.4K_0402_1%
PRV32 37.4K_0402_1%
PRV33 1K_0402_5%
PRV34 1K_0402_5%
PRV35 1K_0402_5%
73 VGA_PWM1
PRV38 1K_0402_5%
73,74 VGA_DRON
+5VS
PCV14 0.068U_0402_16V7K
@PRV37 100K_0402_1%
PCV15 0.068U_0402_16V7K
@PRV40 100K_0402_1%
PCV16 0.068U_0402_16V7K
@PRV43 100K_0402_1%
PRV39 200K_0603_1%
VGA_SWN1 72,73
PRV41 200K_0603_1%
VGA_SWN2 72,73
PRV42 200K_0603_1%
VGA_SWN3 72,74
PRV44 3.24K_0402_1%
PRV45 3.24K_0402_1%
PRV46 3.24K_0402_1%
VGA_SWN3 72,74
VGA_SWN2 72,73
VGA_SWN1 72,73
VGA_CSREF 73,74

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title PWR_GPU Controller

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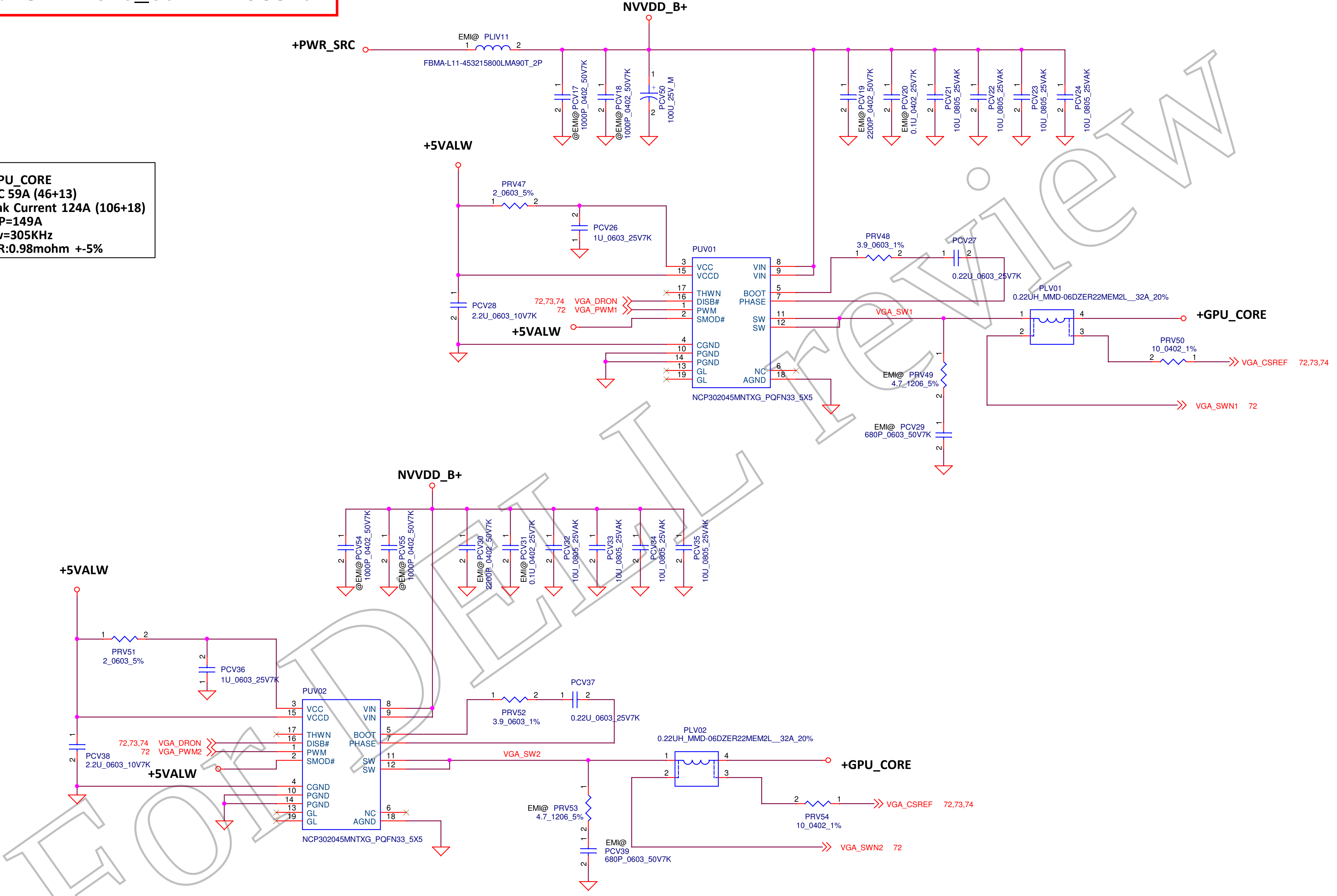
Main Func = +GPU_CORE Phase1&2

+GPU_CORE
TDC 59A (46+13)
Peak Current 124A (106+18)
OCP=149A
Fsw=305KHz
DCR:0.98mohm +-5%



NVVDD_B+
+PWR_SRC
EMI@ PLIV11
FBMA-L11-453215800LMA90T_2P
@EMI@PCV17 1000P_0402_50V7K
@EMI@PCV18 1000P_0402_50V7K
PCV50 100U_25V_M
EMI@PCV19 2200P_0402_50V7K
EMI@PCV20 0.1U_0402_25V7K
PCV21 10U_0805_25VAK
PCV22 10U_0805_25VAK
PCV23 10U_0805_25VAK
PCV24 10U_0805_25VAK
+5VALW
PRV47 2_0603_5%
PCV26 1U_0603_25V7K
PUV01
VCC
VCCD
THWN
DISB#
PWM
SMOD#
CGND
PGND
PGND
GL
GL
VIN
VIN
BOOT
PHASE
SW
SW
NC
AGND
NCP302045MNTXG_PQFN33_5X5
PCV28 2.2U_0603_10V7K
72,73,74 VGA_DRON
72 VGA_PWM1
+5VALW
PRV48 3.9_0603_1%
PCV27 0.22U_0603_25V7K
PLV01 0.22UH_MMD-06DZER22MEM2L__32A_20%
VGA_SW1
+GPU_CORE
PRV50 10_0402_1%
VGA_CSREF 72,73,74
EMI@ PRV49 4.7_1206_5%
VGA_SWN1 72
EMI@ PCV29 680P_0603_50V7K
NVVDD_B+
@EMI@PCV54 1000P_0402_50V7K
@EMI@PCV55 1000P_0402_50V7K
EMI@PCV30 2200P_0402_50V7K
EMI@PCV31 0.1U_0402_25V7K
PCV32 10U_0805_25VAK
PCV33 10U_0805_25VAK
PCV34 10U_0805_25VAK
PCV35 10U_0805_25VAK
+5VALW
PRV51 2_0603_5%
PCV36 1U_0603_25V7K
PUV02
PCV38 2.2U_0603_10V7K
72,73,74 VGA_DRON
72 VGA_PWM2
+5VALW
NCP302045MNTXG_PQFN33_5X5
PRV52 3.9_0603_1%
PCV37 0.22U_0603_25V7K
PLV02 0.22UH_MMD-06DZER22MEM2L__32A_20%
VGA_SW2
+GPU_CORE
EMI@ PRV53 4.7_1206_5%
EMI@ PCV39 680P_0603_50V7K
PRV54 10_0402_1%
VGA_CSREF 72,73,74
VGA_SWN2 72

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Title
PWR_+GPU_CORE Phase1&2

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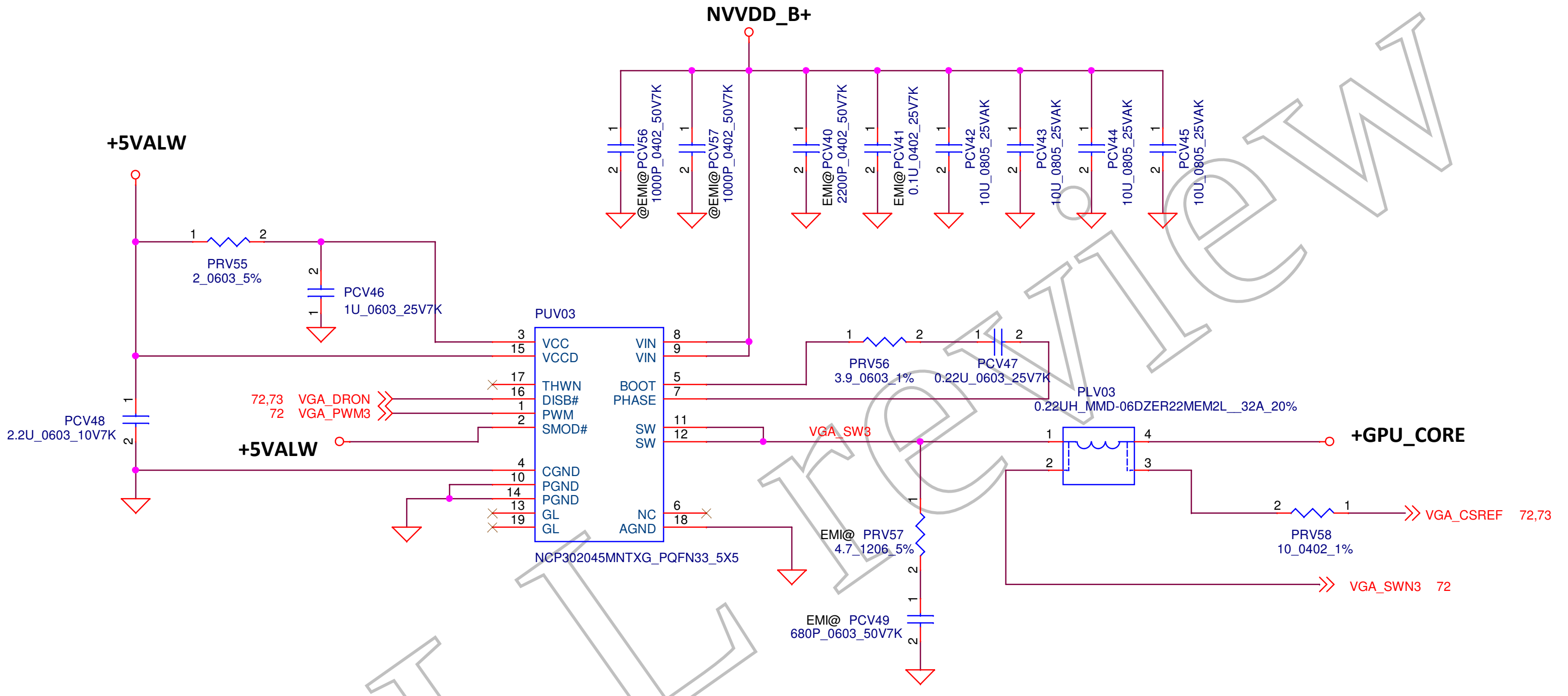
Main Func = +GPU_CORE Phase3


NVVDD_B+
+5VALW
PRV55
2_0603_5%
PCV46
1U_0603_25V7K
PUV03
VCC
VCCD
THWN
DISB#
PWM
SMOD#
CGND
PGND
PGND
GL
GL
VIN
VIN
BOOT
PHASE
SW
SW
NC
AGND
NCP302045MNTXG_PQFN33_5X5
PCV48
2.2U_0603_10V7K
72,73 VGA_DRON
72 VGA_PWM3
+5VALW
@EMI@PCV56
1000P_0402_50V7K
@EMI@PCV57
1000P_0402_50V7K
EMI@PCV40
2200P_0402_50V7K
EMI@PCV41
0.1U_0402_25V7K
PCV42
10U_0805_25VAK
PCV43
10U_0805_25VAK
PCV44
10U_0805_25VAK
PCV45
10U_0805_25VAK
PRV56
3.9_0603_1%
PCV47
0.22U_0603_25V7K
PLV03
0.22UH_MMD-06DZER22MEM2L__32A_20%
VGA_SW3
+GPU_CORE
EMI@ PRV57
4.7_1206_5%
EMI@ PCV49
680P_0603_50V7K
PRV58
10_0402_1%
VGA_CSREF 72,73
VGA_SWN3 72

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title
PWR_+GPU_CORE Phase3

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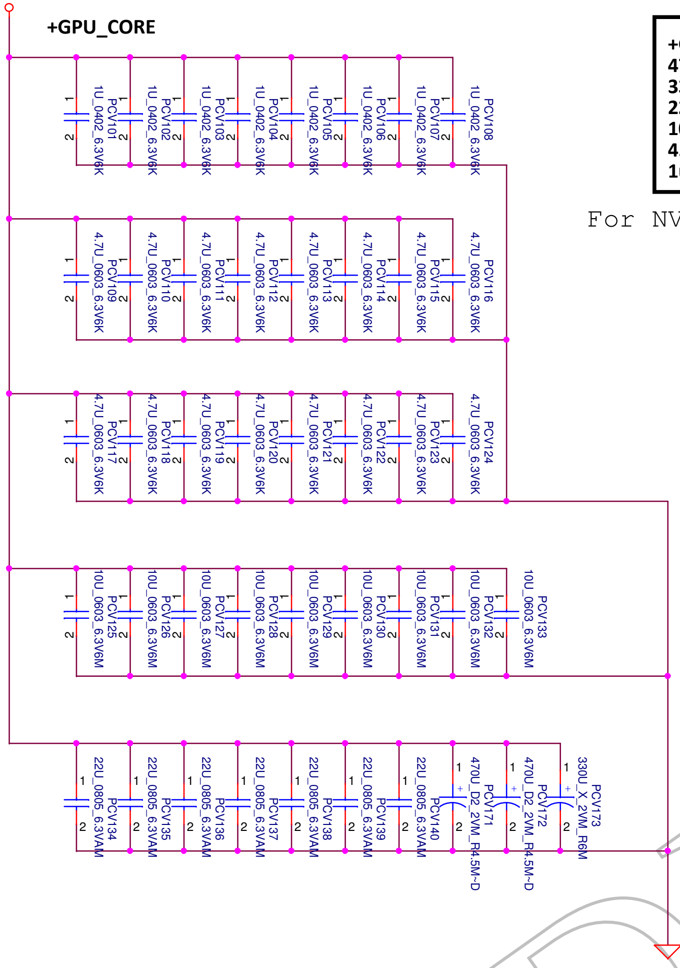
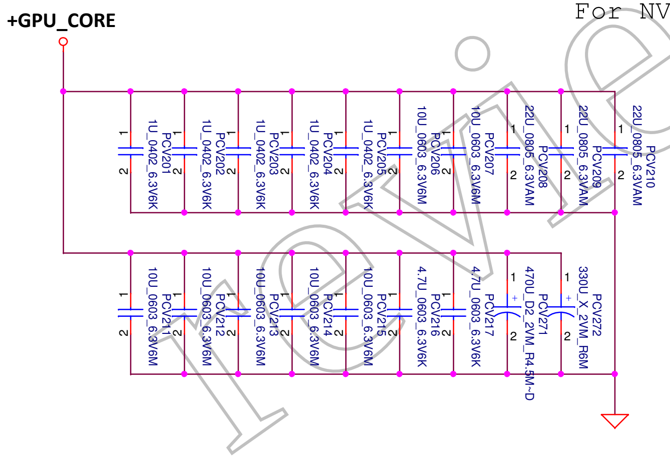
Main Func = VGA DECOUPLING



+GPU_CORE
PCV101 1U_0402_6.3V6K
PCV102 1U_0402_6.3V6K
PCV103 1U_0402_6.3V6K
PCV104 1U_0402_6.3V6K
PCV105 1U_0402_6.3V6K
PCV106 1U_0402_6.3V6K
PCV107 1U_0402_6.3V6K
PCV108 1U_0402_6.3V6K
PCV109 4.7U_0603_6.3V6K
PCV110 4.7U_0603_6.3V6K
PCV111 4.7U_0603_6.3V6K
PCV112 4.7U_0603_6.3V6K
PCV113 4.7U_0603_6.3V6K
PCV114 4.7U_0603_6.3V6K
PCV115 4.7U_0603_6.3V6K
PCV116 4.7U_0603_6.3V6K
PCV117 4.7U_0603_6.3V6K
PCV118 4.7U_0603_6.3V6K
PCV119 4.7U_0603_6.3V6K
PCV120 4.7U_0603_6.3V6K
PCV121 4.7U_0603_6.3V6K
PCV122 4.7U_0603_6.3V6K
PCV123 4.7U_0603_6.3V6K
PCV124 4.7U_0603_6.3V6K
PCV125 10U_0603_6.3V6M
PCV126 10U_0603_6.3V6M
PCV127 10U_0603_6.3V6M
PCV128 10U_0603_6.3V6M
PCV129 10U_0603_6.3V6M
PCV130 10U_0603_6.3V6M
PCV131 10U_0603_6.3V6M
PCV132 10U_0603_6.3V6M
PCV133 10U_0603_6.3V6M
PCV134 22U_0805_6.3VAM
PCV135 22U_0805_6.3VAM
PCV136 22U_0805_6.3VAM
PCV137 22U_0805_6.3VAM
PCV138 22U_0805_6.3VAM
PCV139 22U_0805_6.3VAM
PCV140 22U_0805_6.3VAM
PCV171 470U_D2_2VM_R4.5M~D
PCV172 470U_D2_2VM_R4.5M~D
PCV173 330U_X_2VM_R6M
1
2

+GPU_CORE (NVVDD)
470uF X 2
330uF X 1
22uF_0805 X 7
10uF_0603 X 9
4.7uF_0603 X 16
1uF_0402 X 8

For NV N17P latest spec



+GPU_CORE
PCV201 1U_0402_6.3V6K
PCV202 1U_0402_6.3V6K
PCV203 1U_0402_6.3V6K
PCV204 1U_0402_6.3V6K
PCV205 1U_0402_6.3V6K
PCV206 10U_0603_6.3V6M
PCV207 10U_0603_6.3V6M
PCV208 22U_0805_6.3VAM
PCV209 22U_0805_6.3VAM
PCV210 22U_0805_6.3VAM
PCV211 10U_0603_6.3V6M
PCV212 10U_0603_6.3V6M
PCV213 10U_0603_6.3V6M
PCV214 10U_0603_6.3V6M
PCV215 10U_0603_6.3V6M
PCV216 4.7U_0603_6.3V6K
PCV217 4.7U_0603_6.3V6K
PCV271 470U_D2_2VM_R4.5M~D
PCV272 330U_X_2VM_R6M
1
2

+GPU_CORE (NVVDDS)
470uF X 1
330uF X 1
22uF_0805 X 3
10uF_0603 X 7
4.7uF_0603 X 2
1uF_0402 X 5

For NV N17P latest spec

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Title
VGA DECOUPLING

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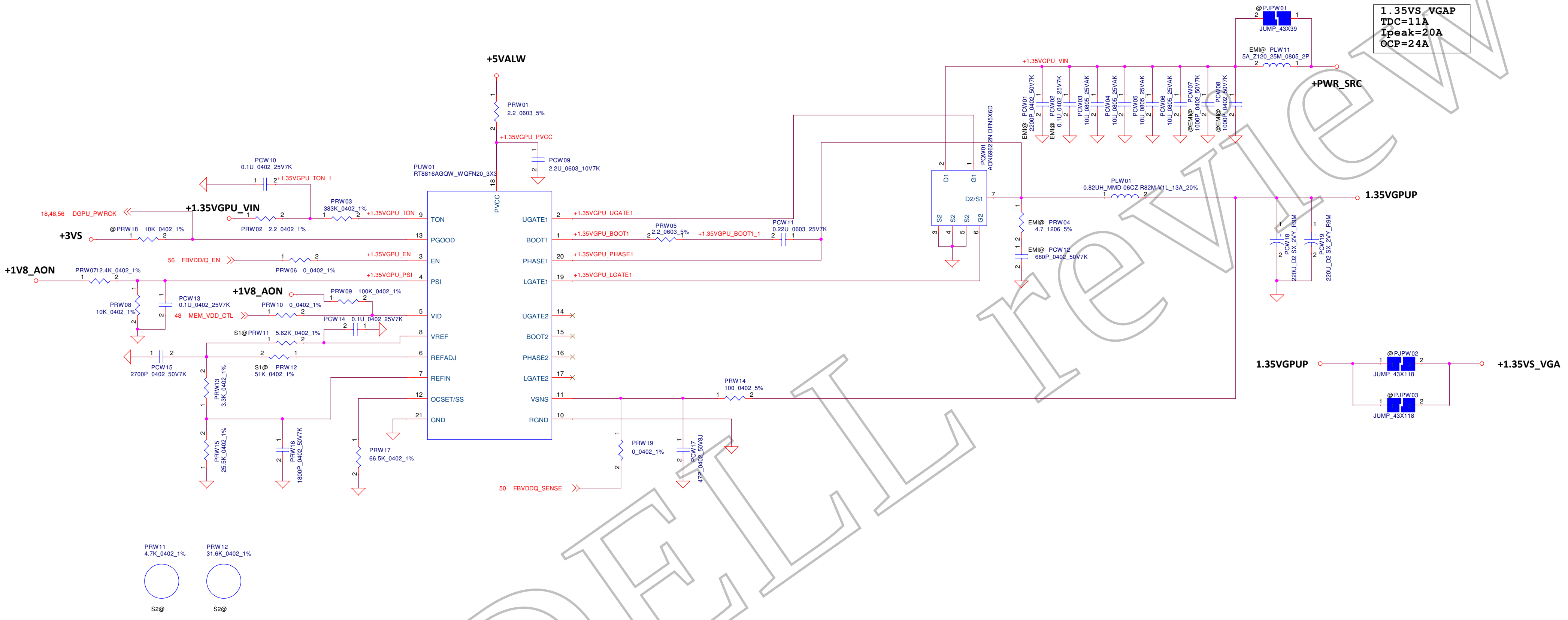
Main Func = +1.35VGPUP

1.35VS_VGAP
TDC=11A
Ipeak=20A
OCP=24A



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+3VS
@PRW18 10K_0402_1%
56 FBVDD/Q_EN
PRW06 0_0402_1%
+1.35VGPU_EN
+1V8_AON
PRW0712.4K_0402_1%
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PRW08
10K_0402_1%
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+1V8_AON
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PRW10 0_0402_1%
PCW14 0.1U_0402_25V7K
S1@PRW11 5.62K_0402_1%
PCW15
2700P_0402_50V7K
S1@ PRW12
51K_0402_1%
PRW13
3.3K_0402_1%
PRW15
25.5K_0402_1%
PRW16
1800P_0402_50V7K
PRW17
66.5K_0402_1%
TON
PGOOD
EN
PSI
VID
VREF
REFADJ
REFIN
OCSET/SS
GND
UGATE1
BOOT1
PHASE1
LGATE1
UGATE2
BOOT2
PHASE2
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VSNS
RGND
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0_0402_1%
PCW17
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2200P_0402_50V7K
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5A_Z120_25M_0805_2P
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AON6962 2N DFN5X6D
D1
G1
D2/S1
S2
S2
S2
G2
PLW01
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EMI@ PRW04
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PCW18
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PCW19
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+1.35VS_VGA
PRW11
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PRW12
31.6K_0402_1%
S2@
S2@

BOM config	GPU type	VRAM memory	VRAM vender	RVL	PRW11	PRW12
S1@ (4G)	N17P-G0/G1	256Mx32	Micron	1.35V & 1.5V	5.62K	51K
S1@ (4G)	N17P-G0/G1	256Mx32	Hynix	1.35V & 1.5V	5.62K	51K
S1@ (4G)	N17P-G0/G1	256Mx32	Samsung	1.35V & 1.5V	5.62K	51K
S2@ (3G/6G)	N17E-G1 Max-Q	128M/256M x32	Hynix	1.35V & 1.55V	4.7K	31.6K
S2@ (3G/6G)	N17E-G1 Max-Q	128M/256M x32	Samsung	1.35V & 1.55V	4.7K	31.6K

MEM_VDD_CTL	+MVDD
L	1.35V
H	1.5V/1.55V

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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Title
+1.35VGPUP

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Document Number
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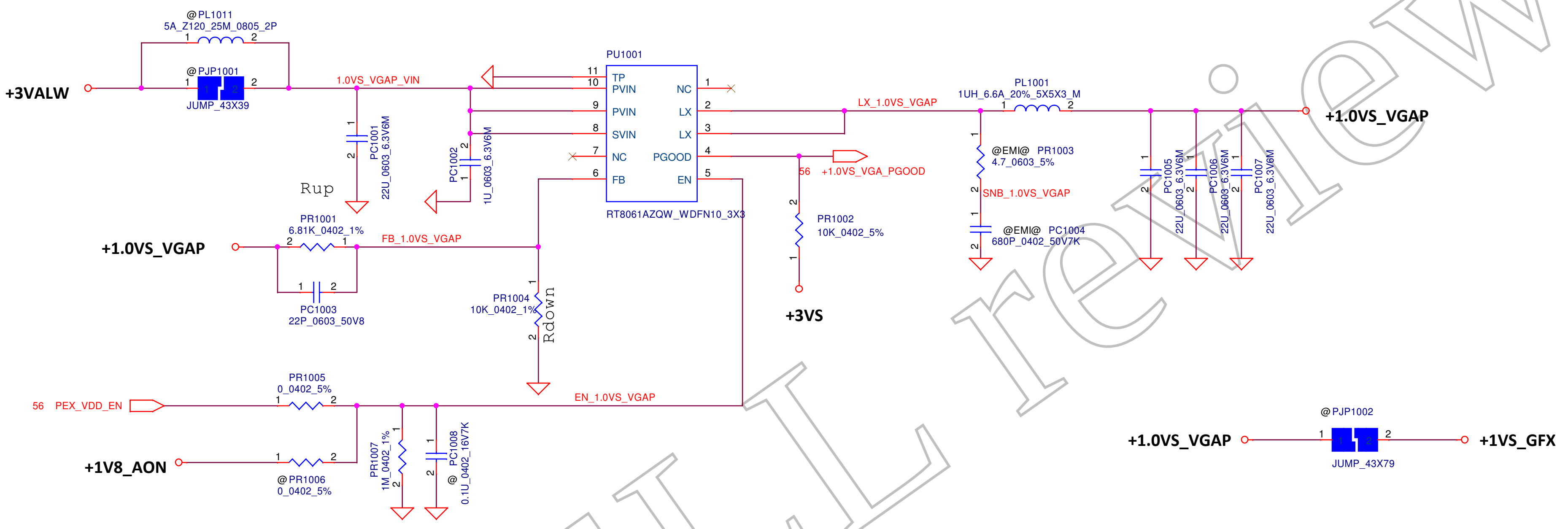
Date: Thursday, March 22, 2018

Main Func = 1VS_GFX

+1VS_GFX
TDC 0.88A
Peak Current 1.1A
OCP current 4A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1U_0603_6.3V6M
Rup
PU1001
TP
PVIN
PVIN
SVIN
NC
FB
NC
LX
LX
PGOOD
EN
RT8061AZQW_WDFN10_3X3
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PL1001
1UH_6.6A_20%_5X5X3_M
+1.0VS_VGAP
@EMI@ PR1003
4.7_0603_5%
SNB_1.0VS_VGAP
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680P_0402_50V7K
PC1005
22U_0603_6.3V6M
PC1006
22U_0603_6.3V6M
PC1007
22U_0603_6.3V6M
56 +1.0VS_VGA_PGOOD
PR1002
10K_0402_5%
+3VS
+1.0VS_VGAP
PR1001
6.81K_0402_1%
FB_1.0VS_VGAP
PC1003
22P_0603_50V8
PR1004
10K_0402_1%
Rdown
56 PEX_VDD_EN
PR1005
0_0402_5%
EN_1.0VS_VGAP
+1V8_AON
@PR1006
0_0402_5%
PR1007
1M_0402_1%
@ PC1008
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+1.0VS_VGAP
@PJP1002
JUMP_43X79
+1VS_GFX

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Title *PWR_+1VS_GFX*

Size Document Number *LA-F611P* Rev 0.1

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Version Change List (P. I. R. List)

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Security Classification	Compal Secret Data		
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Title: **Changed-List PWR History**

Size | Document Number | Rev 0.1

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