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HSF Property: ROHS or Halogen-Free

DAKAR10F/FG (45W CPU) MP(A02) BUILD

2012.03.23

DATE	CHANGE NO.	REV
21-FEB-2009		

EE	DATE	POWER	DATE
DRAWER	LOREN	2012.03.23	EDISON
DESIGN	LOREN	2012.03.23	EDISON
CHECK	REYAN	2012.03.23	RY
RESPONSIBLE	REYAN	2012.03.23	RY
SIZE:			
FILE NAME:			
PN	XXX		1310

INVENTEC

MODEL PROJECT FUNCTION
DAKAR10F/FG MAIN BOARD



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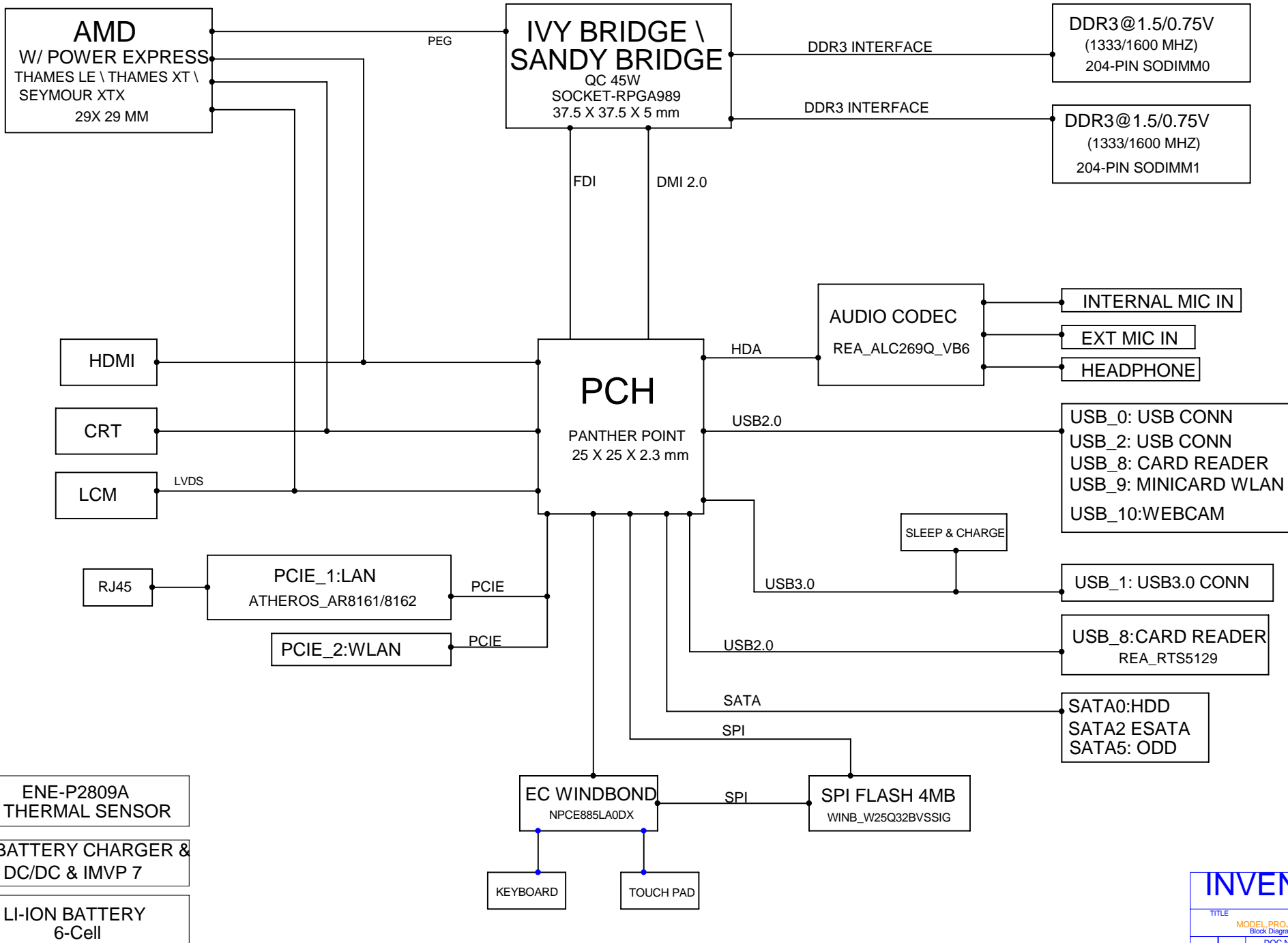
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TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01

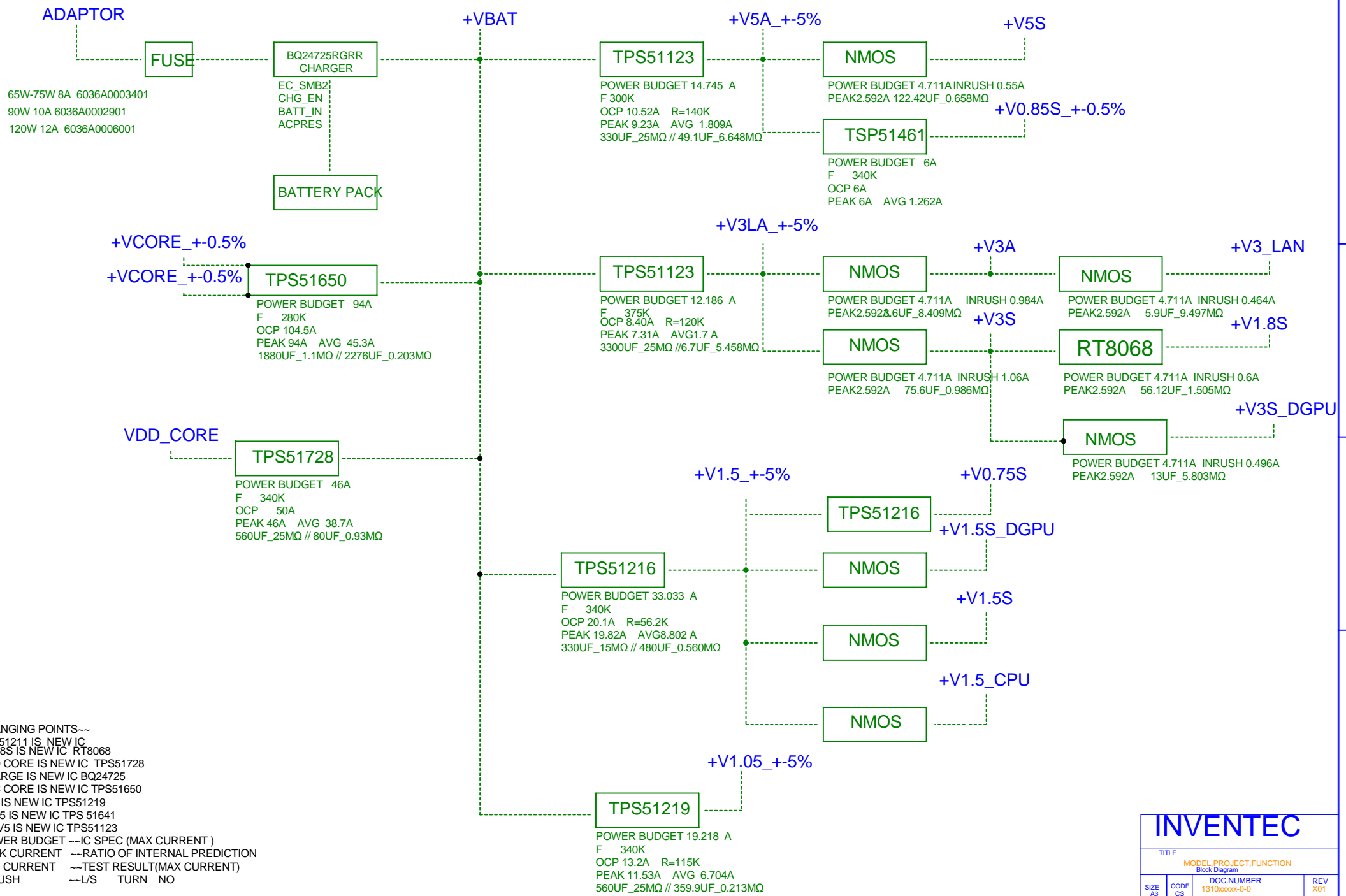
CHANGE by XXX

DATE 21-OCT-2002

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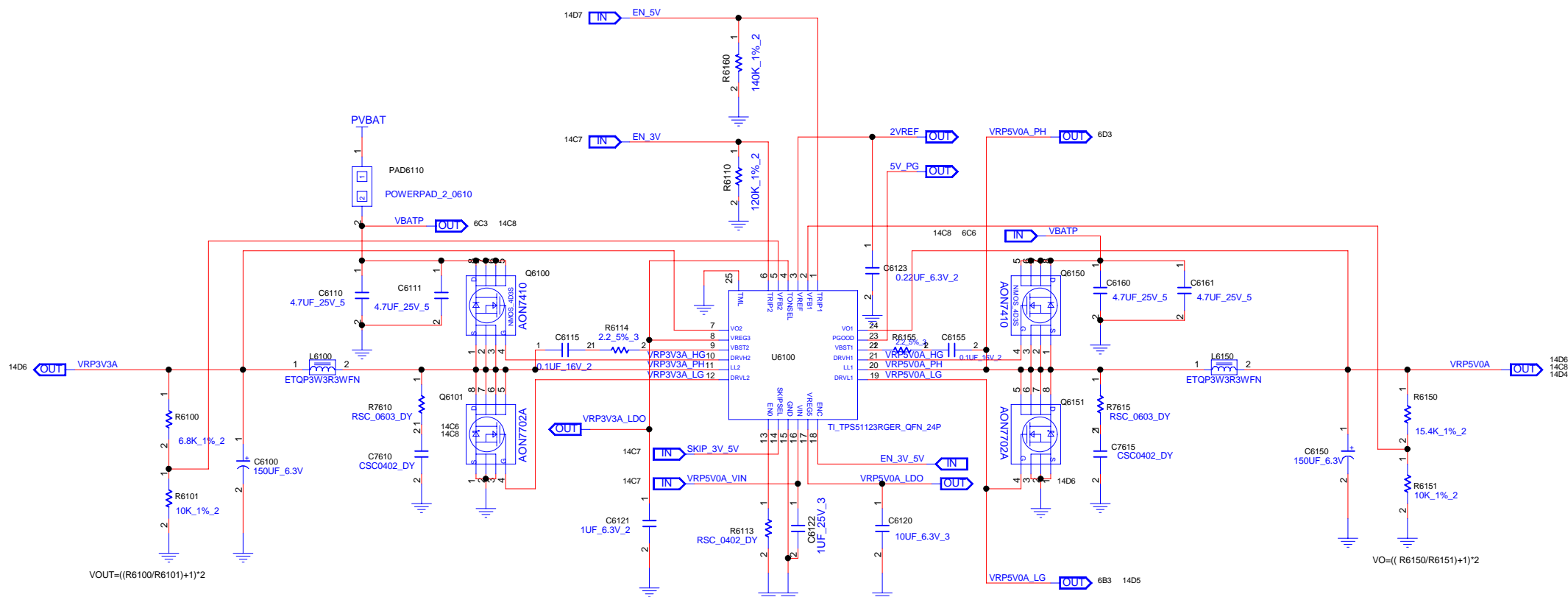


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CHANGING POINTS--
 TPS51211 IS NEW IC
 +V1.8S IS NEW IC RT8068
 VDD CORE IS NEW IC TPS51728
 CHARGE IS NEW IC BQ24725
 VCC CORE IS NEW IC TPS51650
 VTT IS NEW IC TPS51219
 V0.85 IS NEW IC TPS 51641
 V3_V5 IS NEW IC TPS51123
 POWER BUDGET --IC SPEC (MAX CURRENT)
 PEAK CURRENT --RATIO OF INTERNAL PREDICTION
 AVG CURRENT --TEST RESULT(MAX CURRENT)
 INRUSH --L/S TURN NO

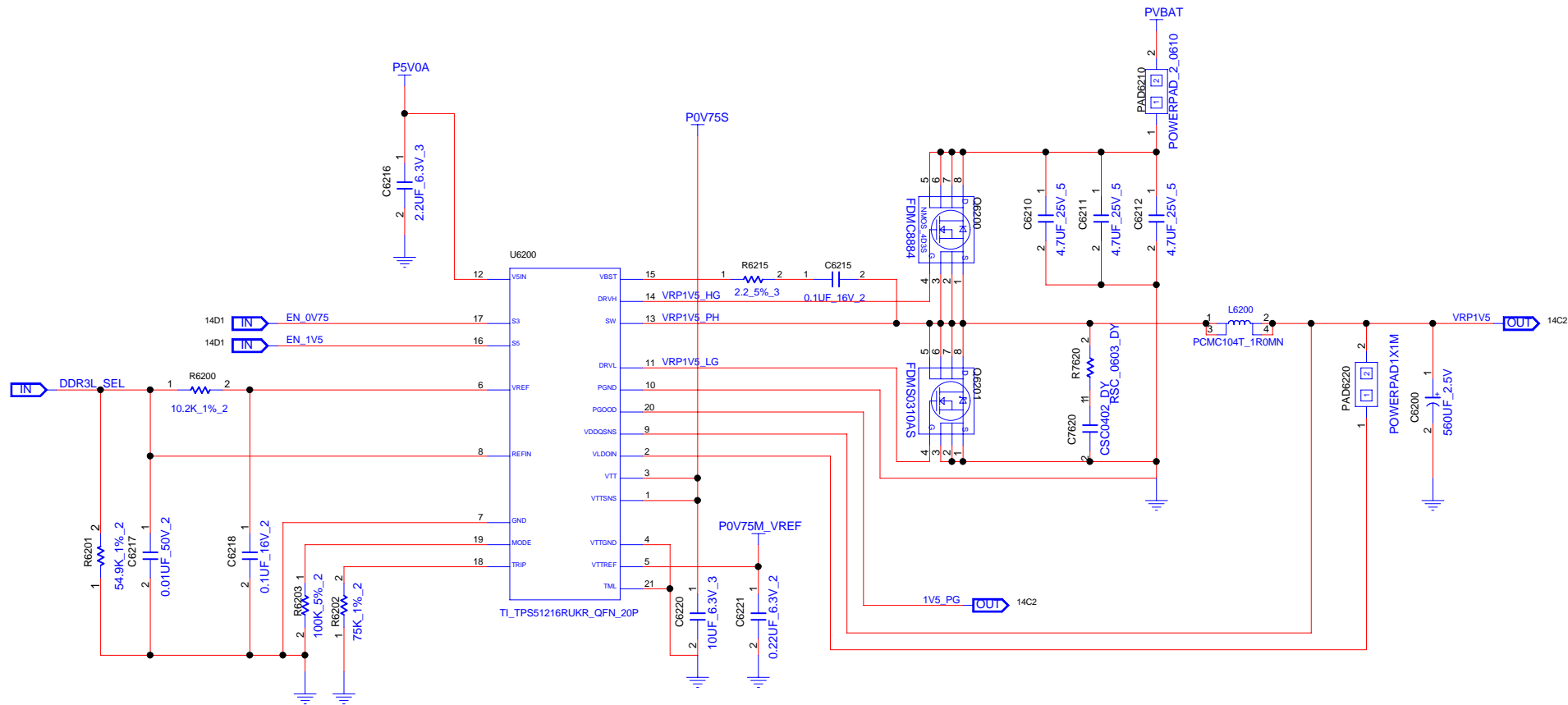
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$$V_{OUT} = ((R6100/R6101)+1) \cdot 2$$

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$V_{OUT} = V_{REF} \cdot 1.8 \cdot \frac{R_{6201}}{R_{6201} + R_{6202}}$
 MODE=100KOHM:TRACKING DISCHARGE

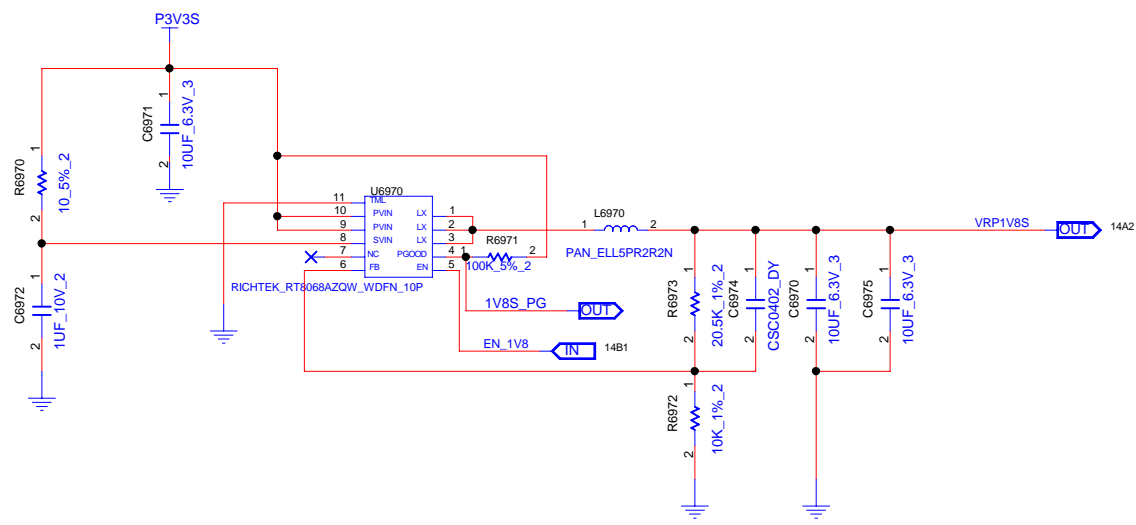
STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

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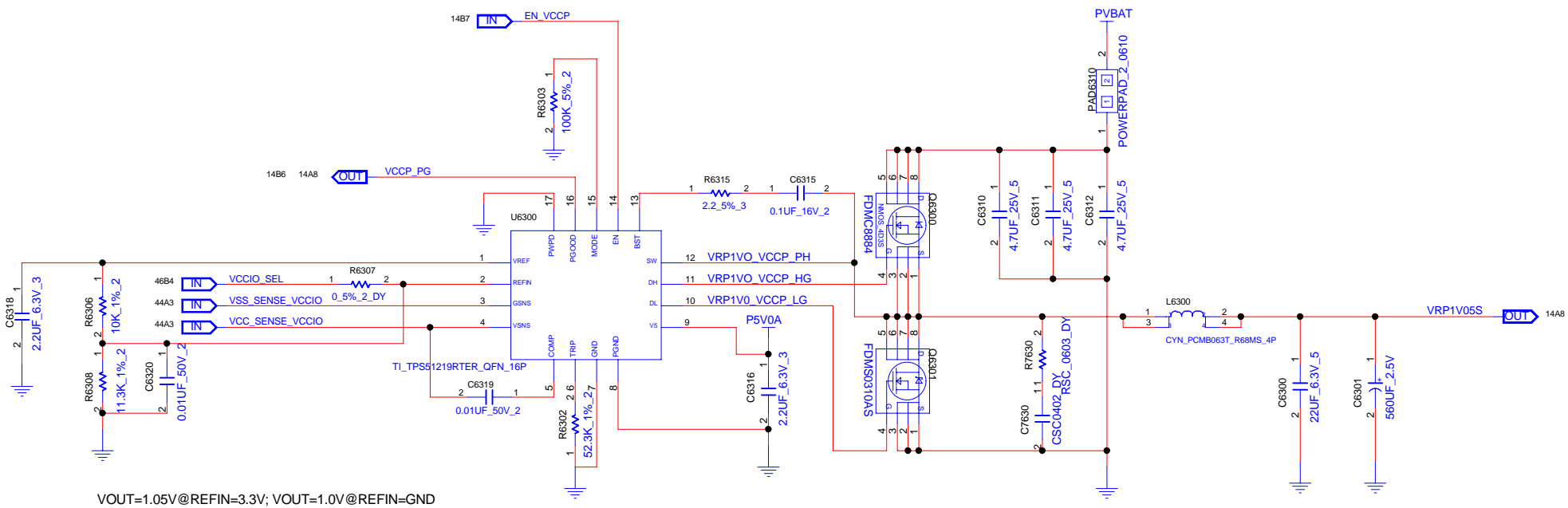
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Block Diagram

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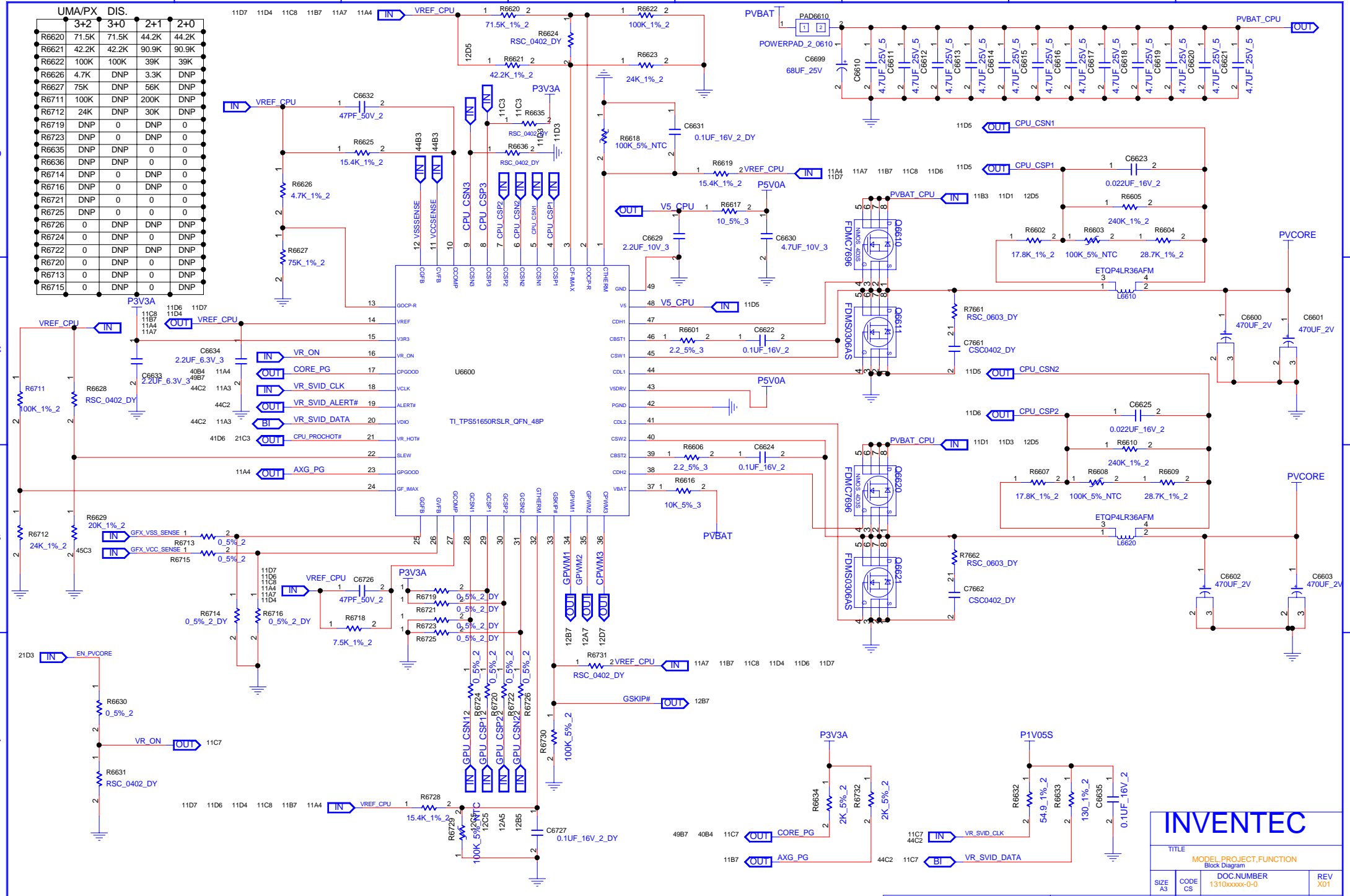
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UMA/PX DIS.	3+2	3+0	2+1	2+0
R6620	71.5K	71.5K	44.2K	44.2K
R6621	42.2K	42.2K	90.9K	90.9K
R6622	100K	100K	39K	39K
R6626	4.7K	DNP	3.3K	DNP
R6627	75K	DNP	56K	DNP
R6711	100K	DNP	200K	DNP
R6712	24K	DNP	30K	DNP
R6719	DNP	0	DNP	0
R6723	DNP	0	DNP	0
R6635	DNP	DNP	0	0
R6636	DNP	DNP	0	0
R6714	DNP	0	DNP	0
R6716	DNP	0	DNP	0
R6721	DNP	0	0	0
R6725	DNP	0	DNP	0
R6726	0	DNP	DNP	DNP
R6724	0	DNP	0	DNP
R6722	0	DNP	DNP	DNP
R6720	0	DNP	0	DNP
R6713	0	DNP	0	DNP
R6715	0	DNP	0	DNP

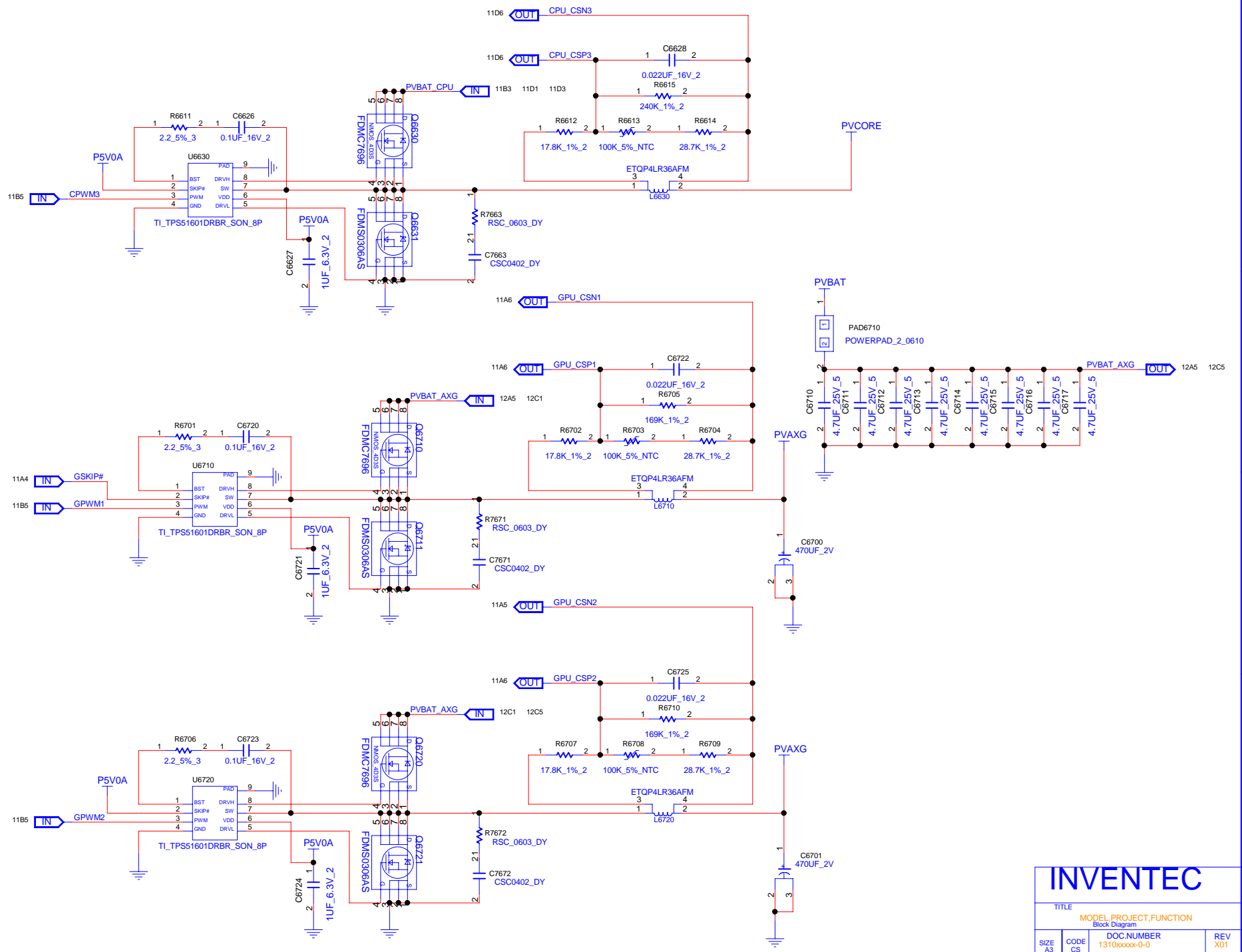


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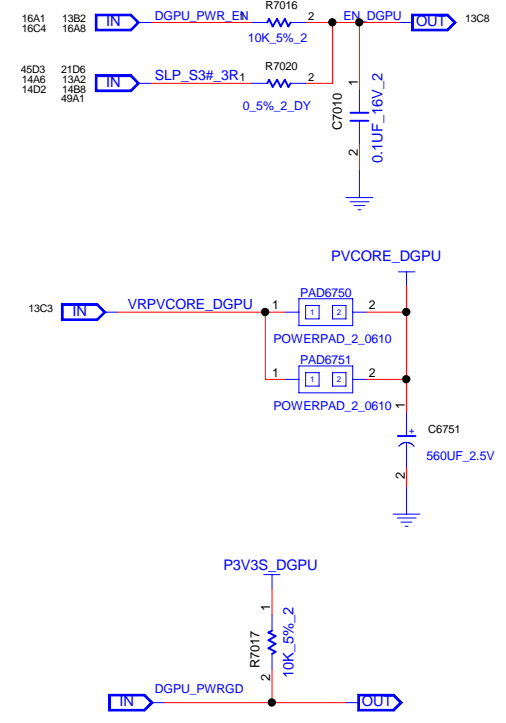
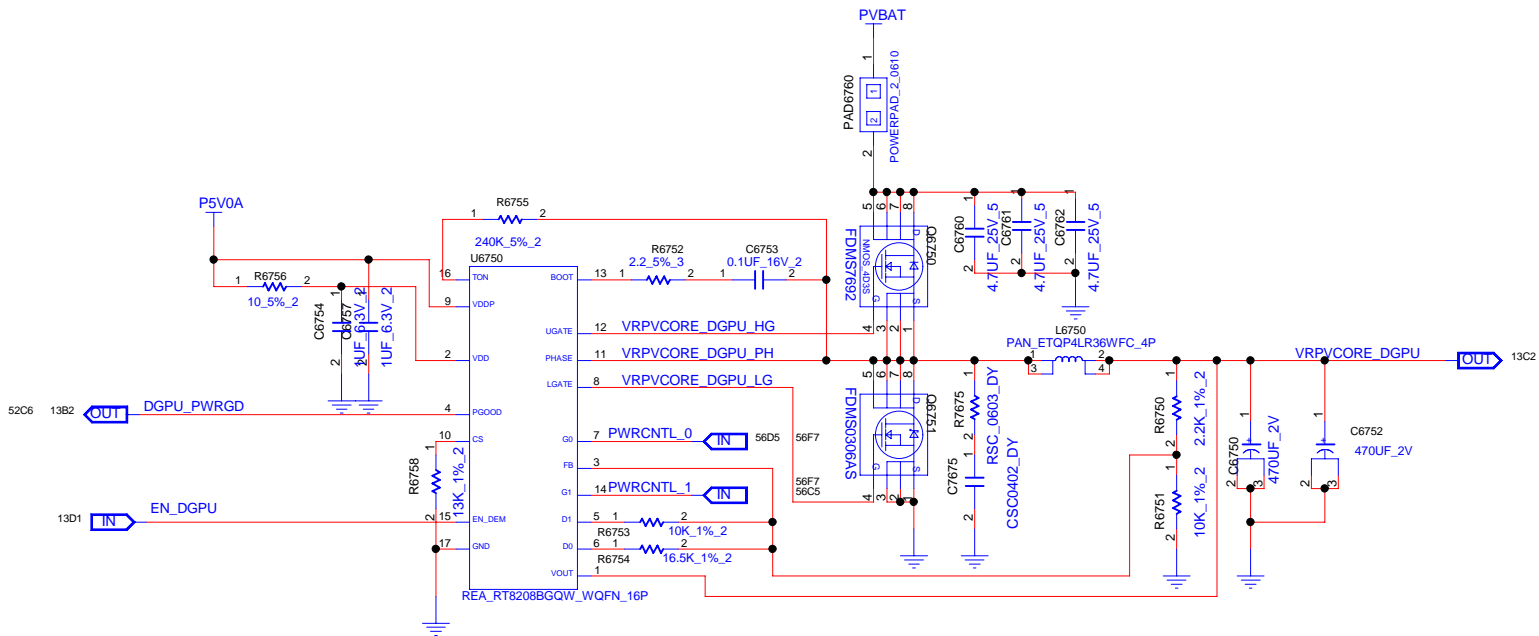
TITLE: MODEL PROJECT FUNCTION
Block Diagram

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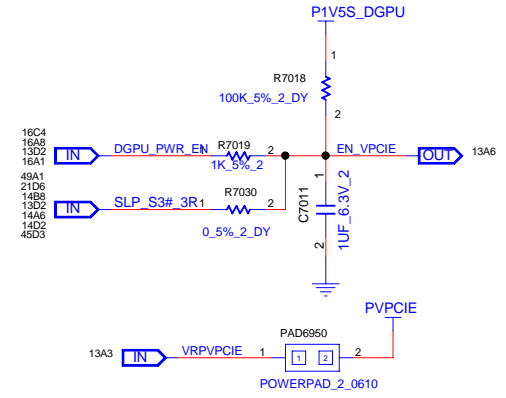
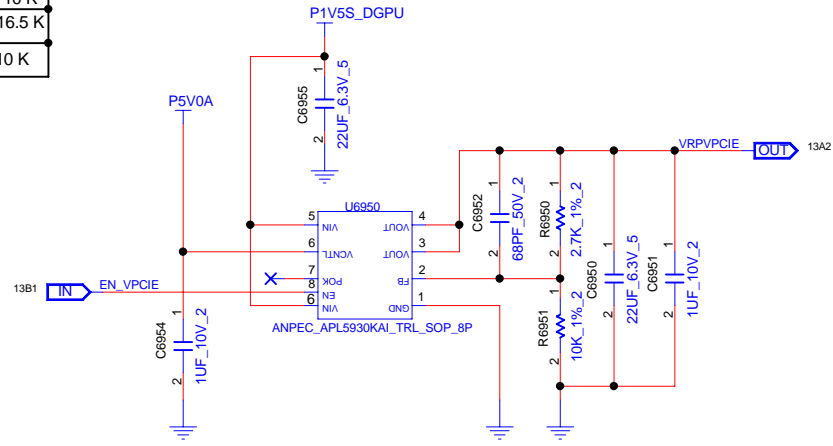
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P.S. R6750(R1)R6751(R2)R6753(R3)R6754(R4)

VGA TYPE :	SEYMOUR XTX	THAMES XT	THAMES LE		RESISTOR VALUE
G0	G1	VOUT	VOUT	VOUT	
0	0	1.15	N/A	N/A	R6750(R1) 2.2 K
0	1	1.05	N/A	N/A	R6751(R2) 10 K
1	0	1	1	1	R6754(R3) 16.5 K
1	1	0.9	0.9	0.9	R6753(R4) 10 K

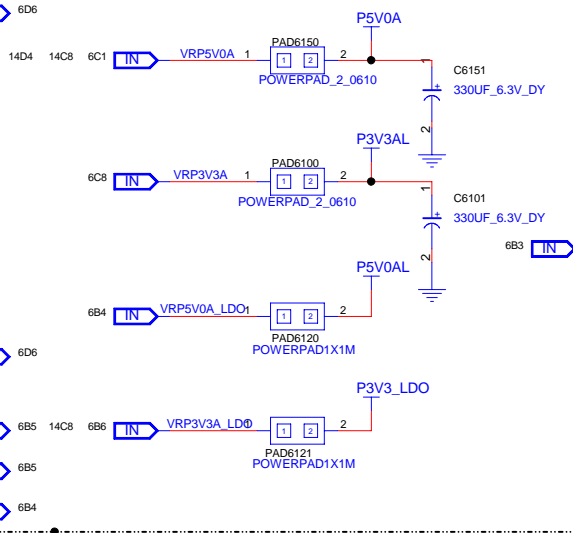
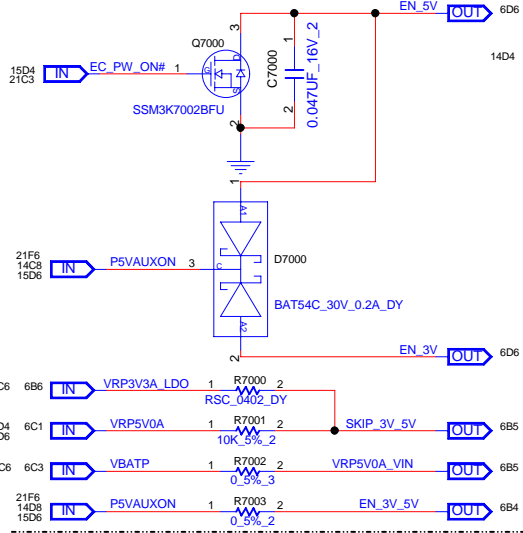
RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2/R3)}{(R2/R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2/R4)}{(R2/R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2/R3/R4)}{(R2/R3/R4)} \times 0.75$



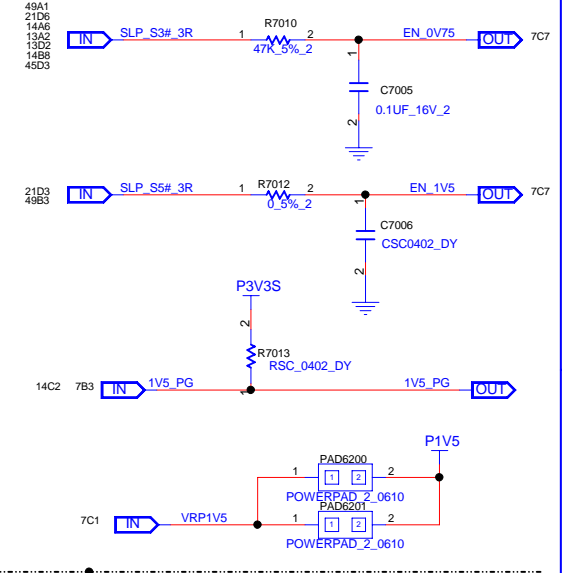
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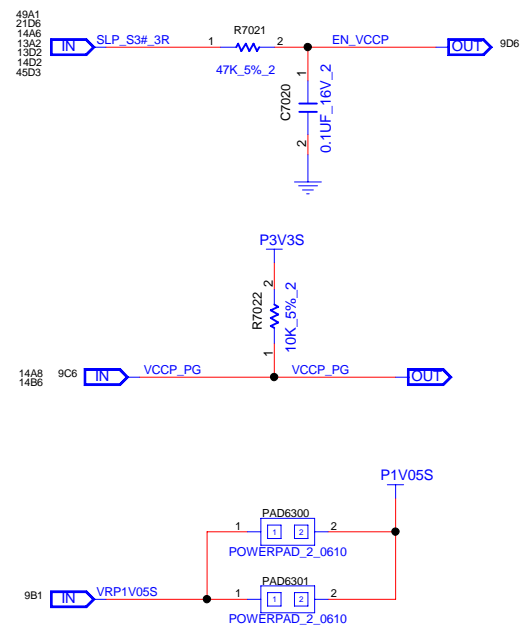
3V & 5V



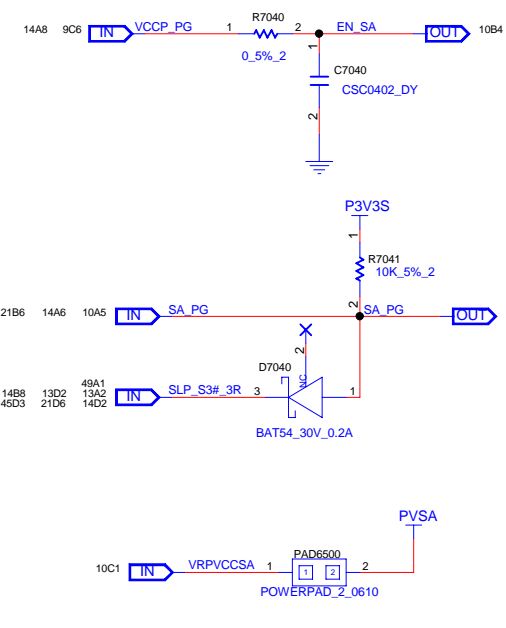
DDR_P1V5



VCCIO



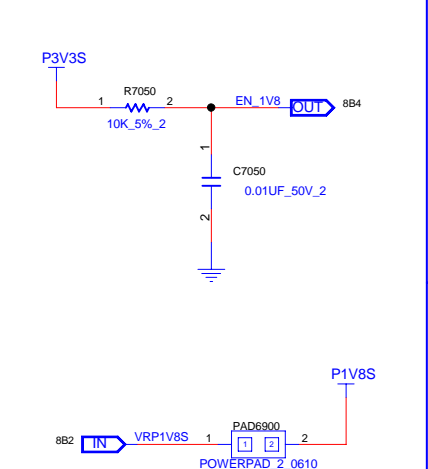
VCCSA



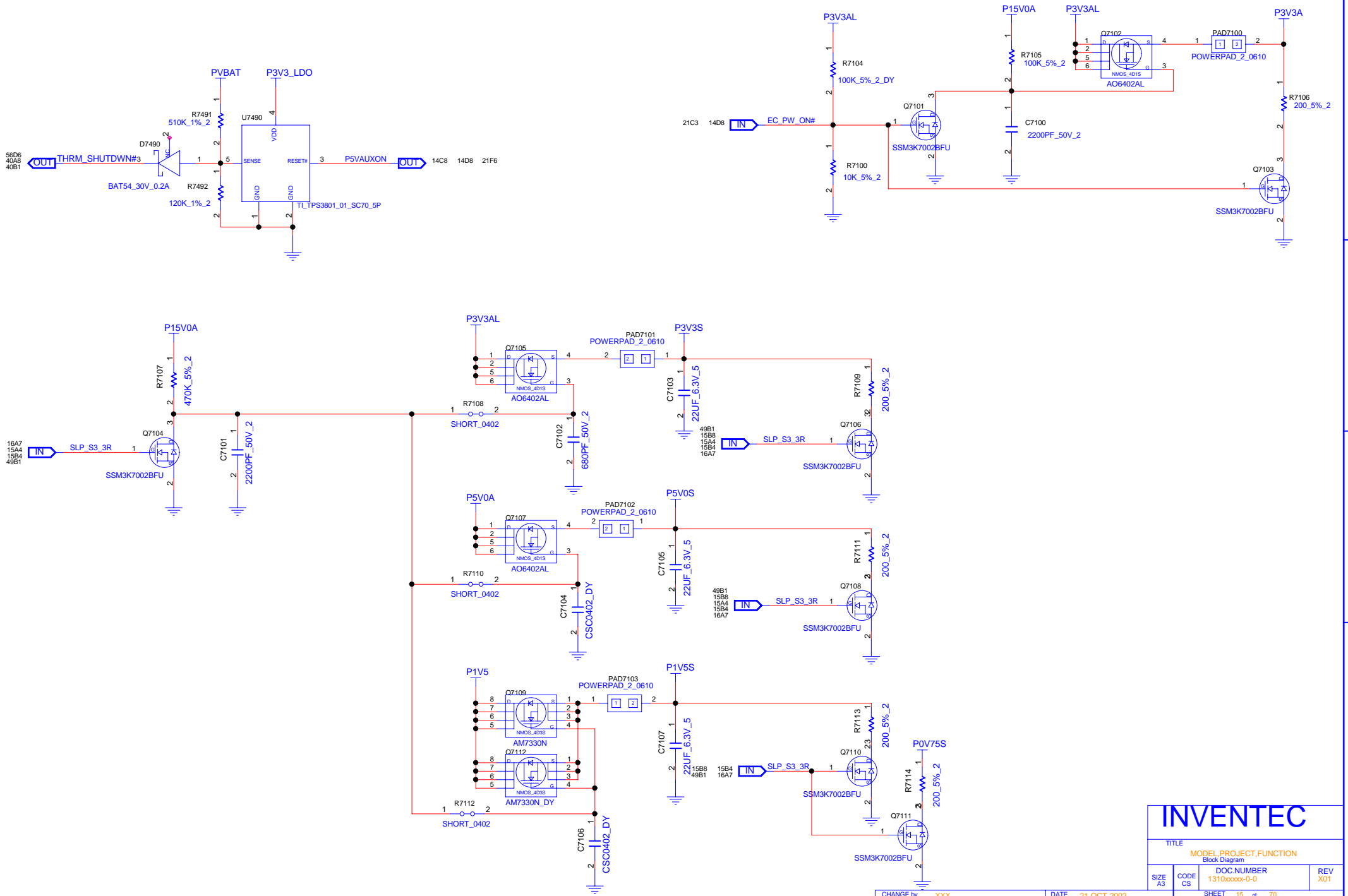
DGPU



P1V8S



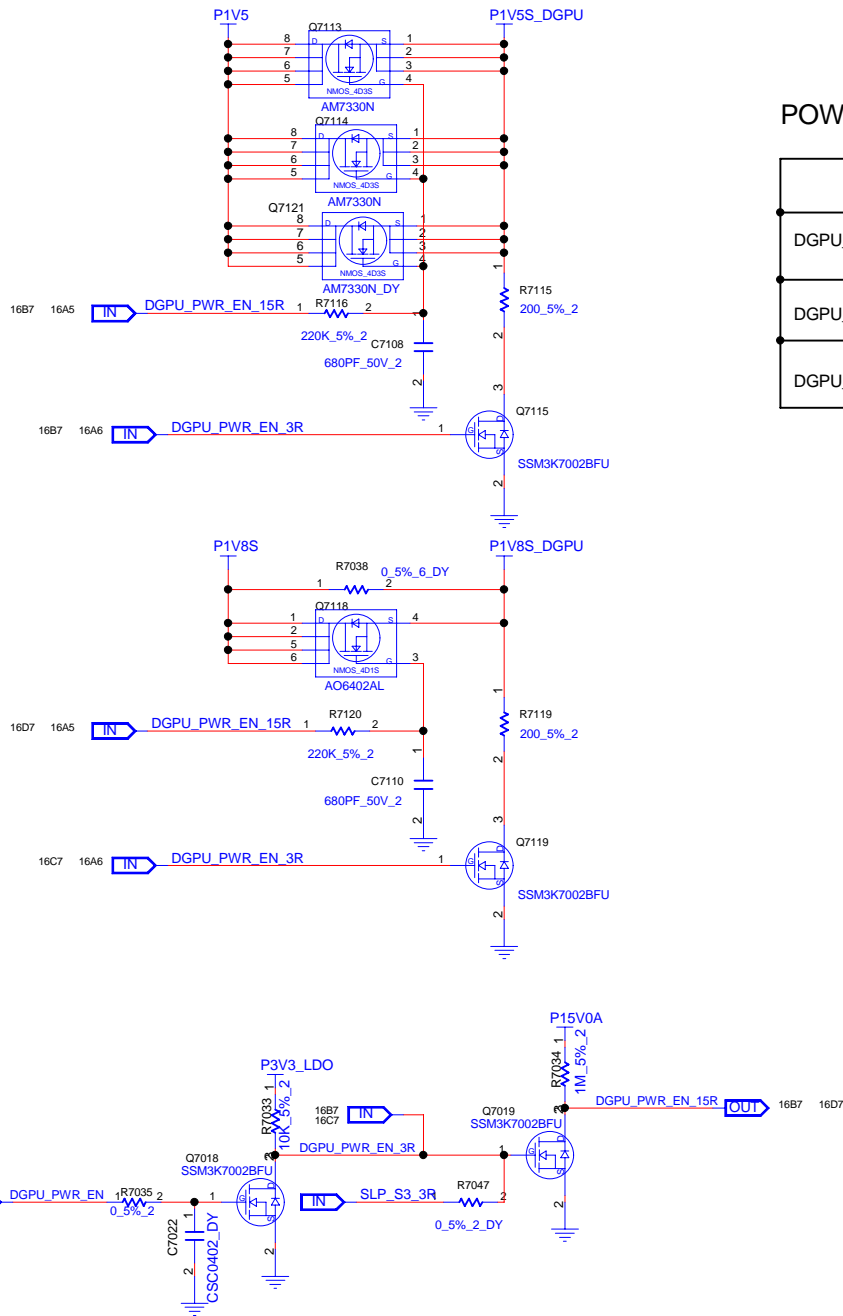
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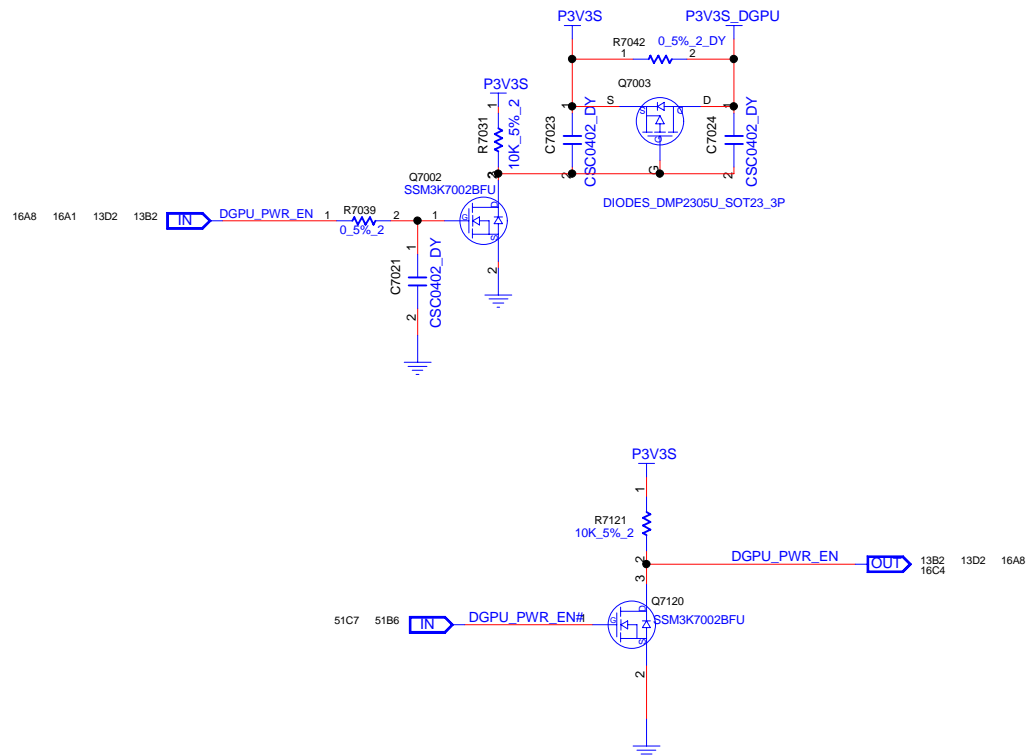
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POWER EXPRESS

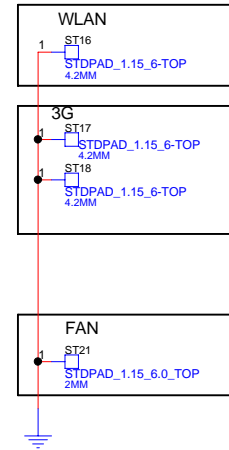
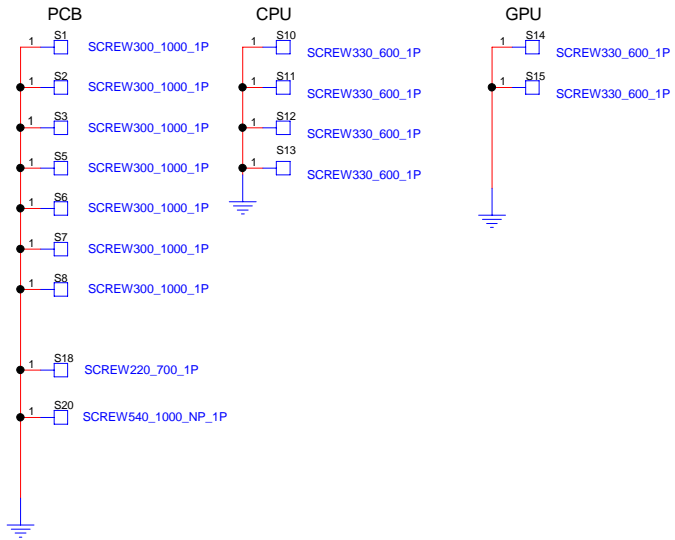
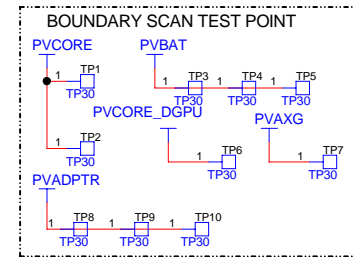
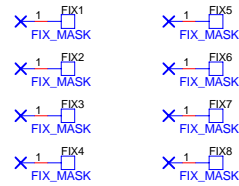
	DURING RESET	AFTER RESET	
DGPU_PWR_EN#	HIGH	HIGH	0 : DGPU POWER SWITCH TURNED ON 1 : POWER SWITCH TURNED OFF
DGPU_PWRGD			0 : DGPU POWER IS NOT STABLE 1 : DGPU POWER IS STABLE
DGPU_HOLD_RST#	LOW	LOW	0 : KEEP DGPU IN RESET 1 : RESET IS RELEASED



INVENTEC

TITLE			
MODEL PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
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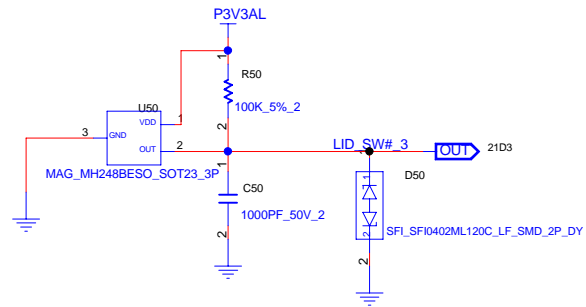
REFERENCE 0~49(PCB SCREW)



INVENTEC			
TITLE			
MODEL PROJECT FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01



REFERENCE 50-99(HALL SENSOR)

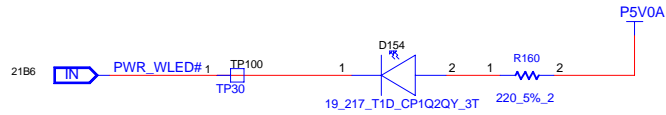


INVENTEC

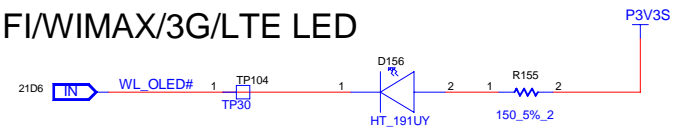
TITLE			
MODEL PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
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POWER ON LED

D154 BRIGHT WHEN SYSTEM IS POWER ON
 D154 BLINK WHEN SYSTEM GO TO SLEEP

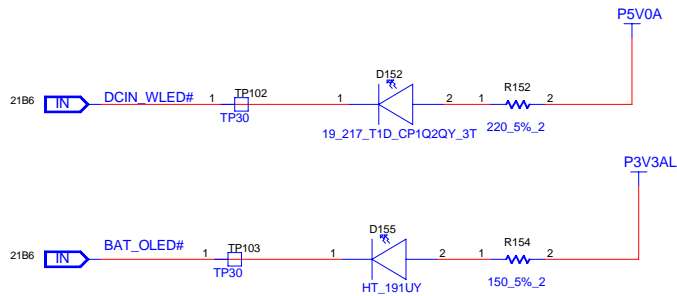


WIFI/WIMAX/3G/LTE LED



DC IN / BATTERY CHARGE LED

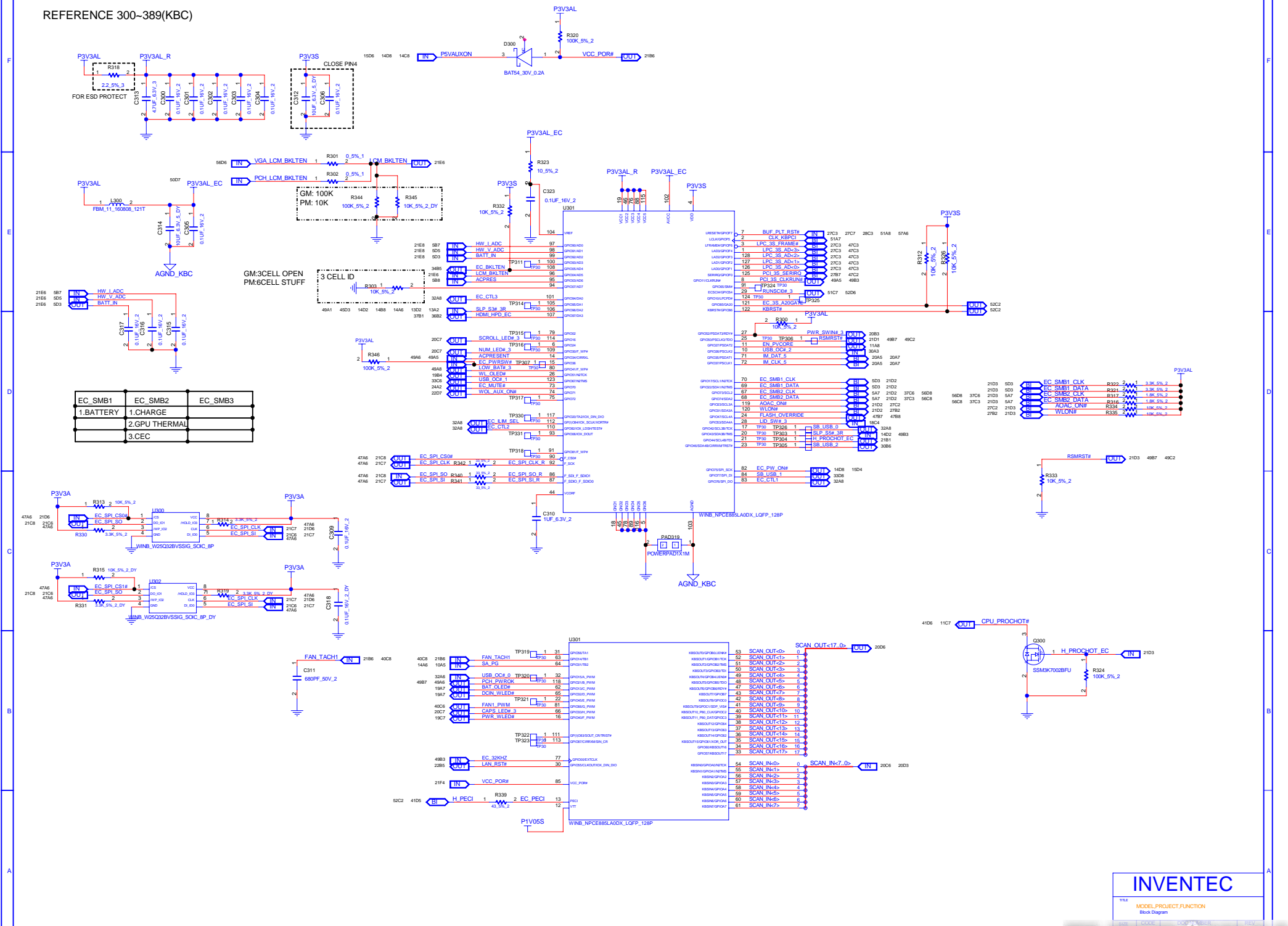
D152 BRIGHT: BOTH AC-ADAPTER IS PLUGGED IN AND BATTERY IS FULL CHARGED
 D155 BRIGHT: WHILE CHARGING BATTERY FROM AC-ADAPTER
 BLINK: LOW BATTERY



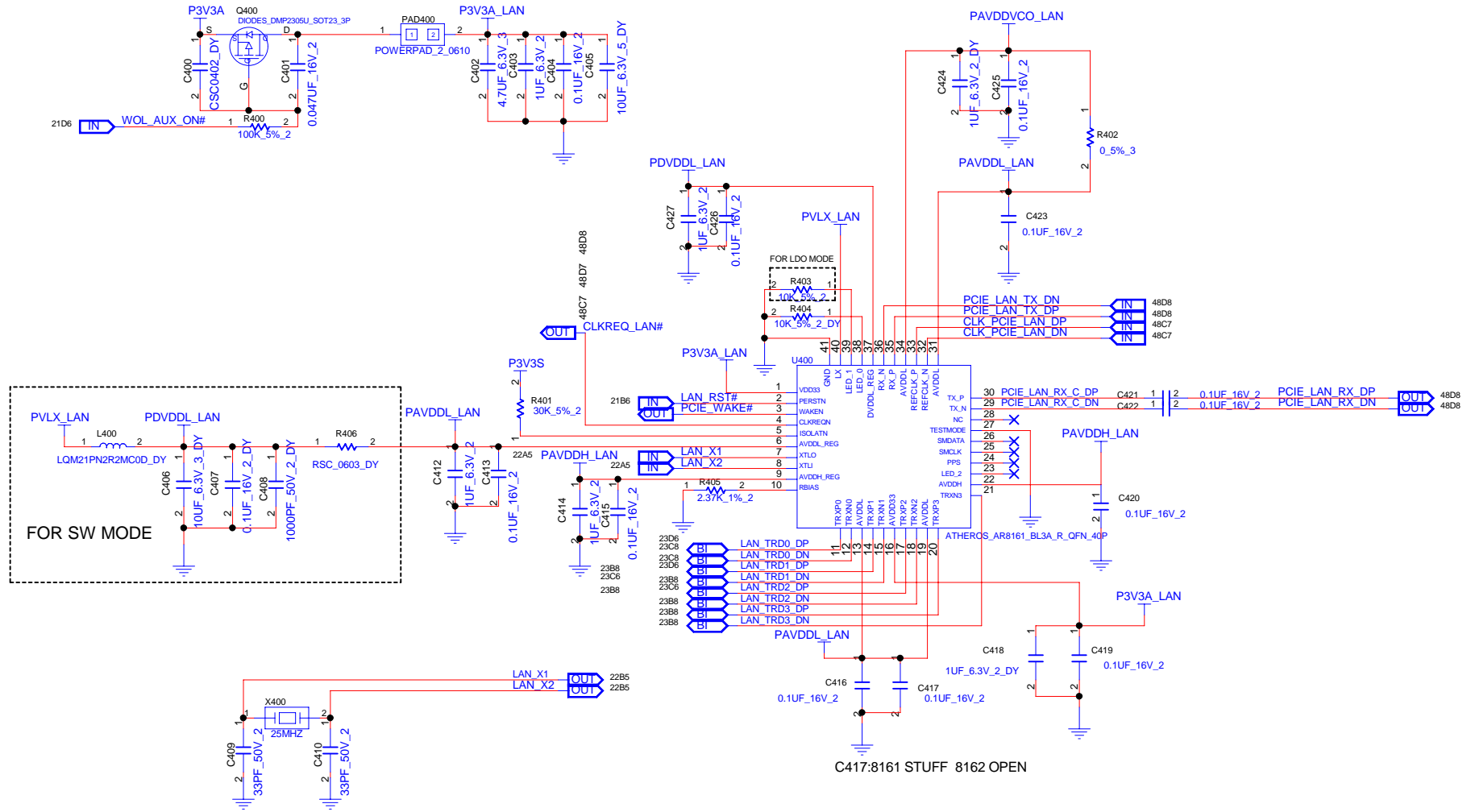
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TITLE			
MODEL PROJECT.FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01

REFERENCE 300-389(KBC)



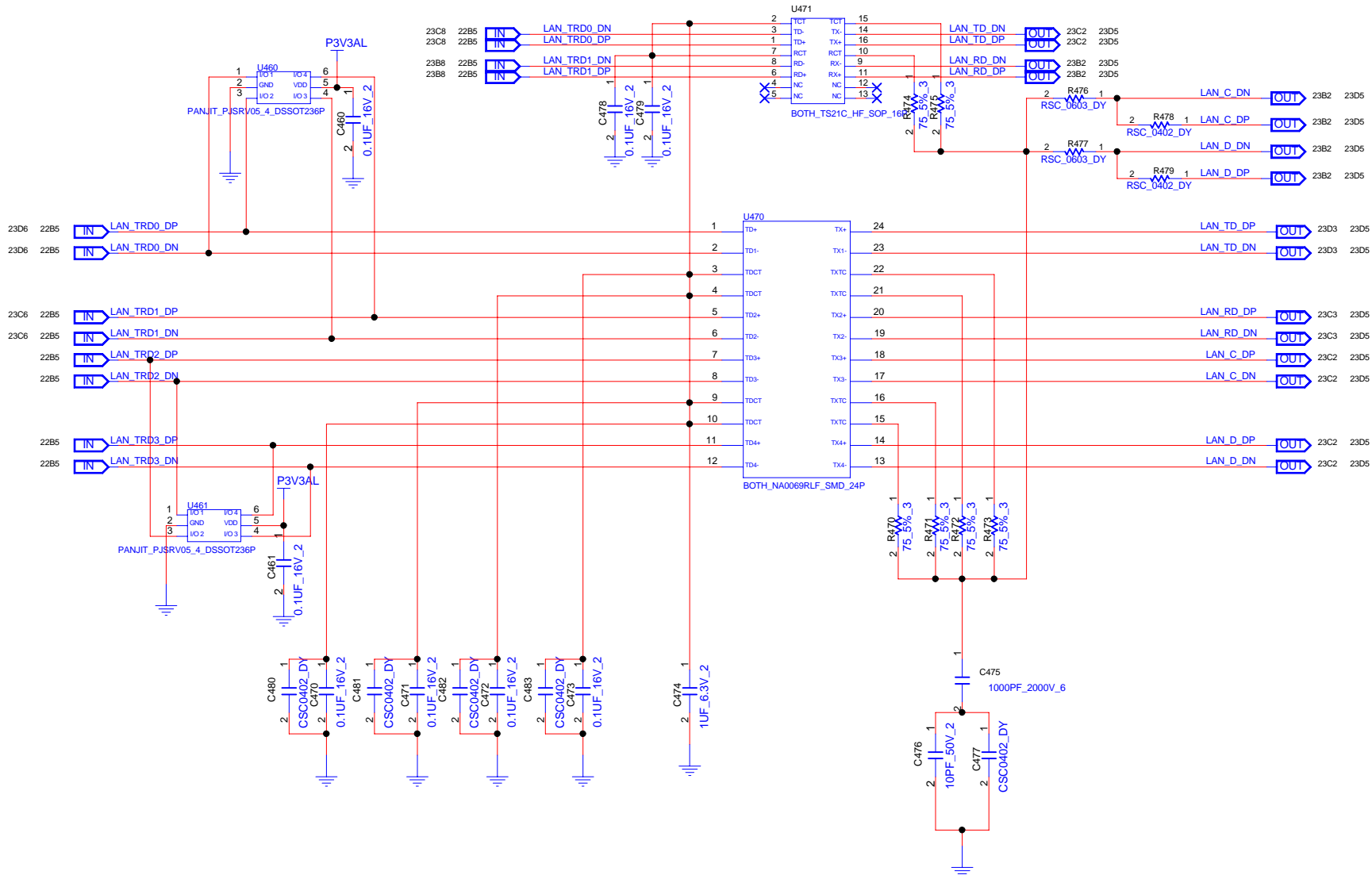
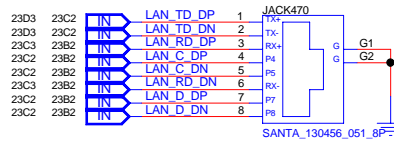
EC_SMB1	EC_SMB2	EC_SMB3
1.BATTERY	1.CHARGE	
	2.GPU THERMAL	
	3.CEC	



INVENTEC

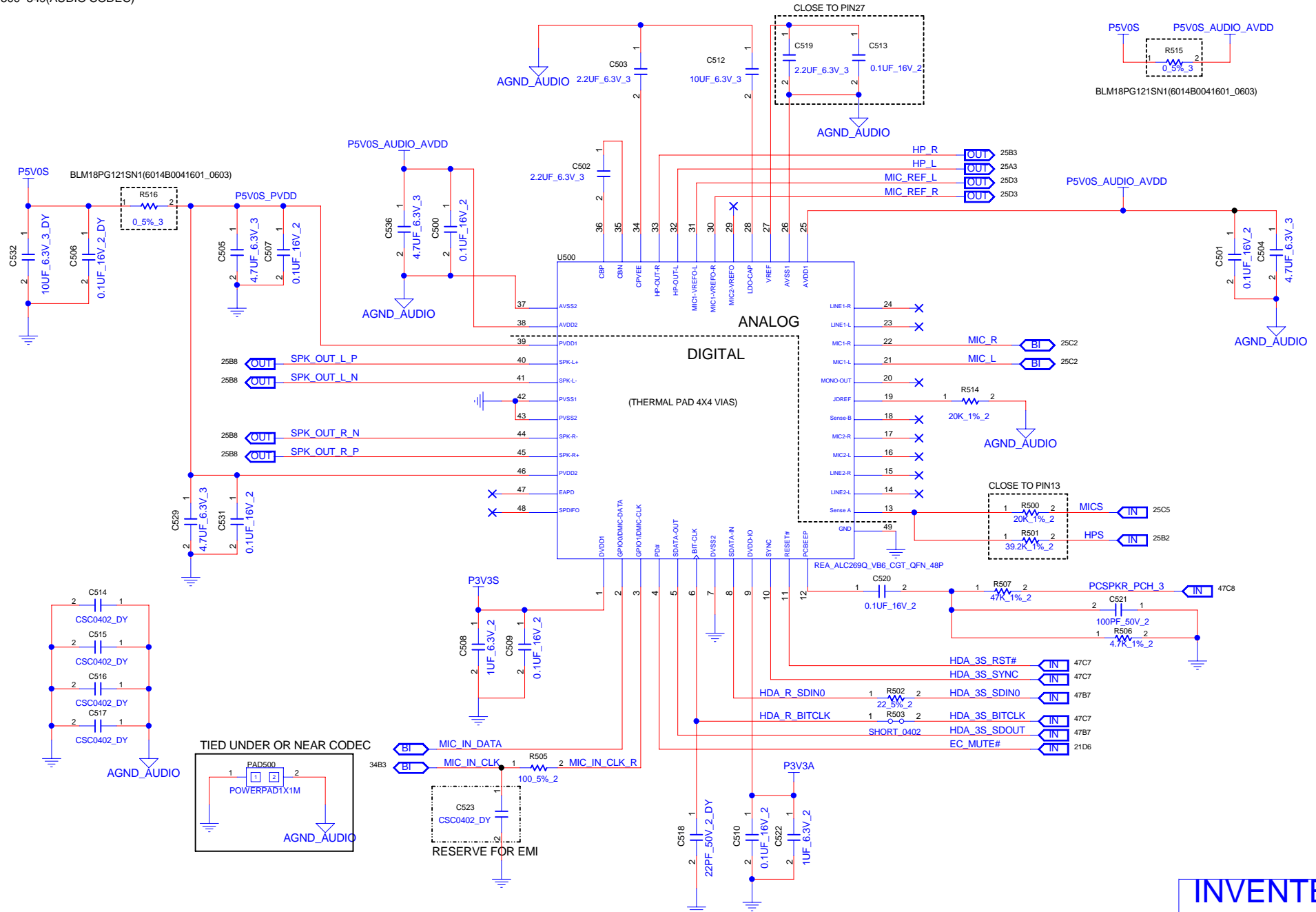
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REFERENCE 400-499(LAN)



INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
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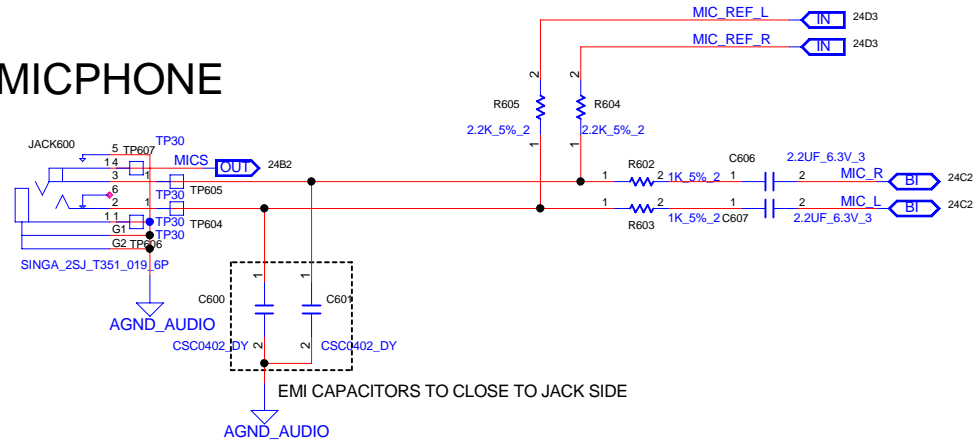




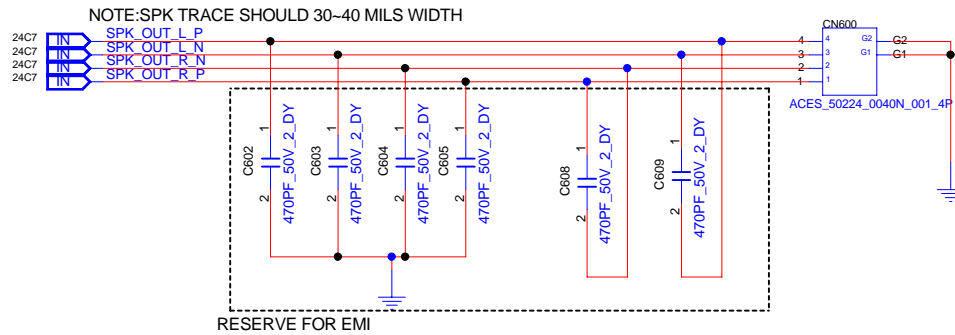
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AUDIO JACKS

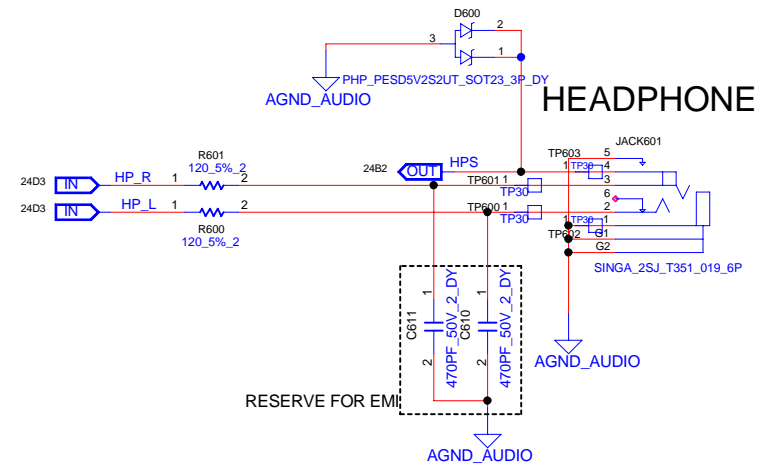
MICPHONE



INTERNAL SPEAKERS



HEADPHONE

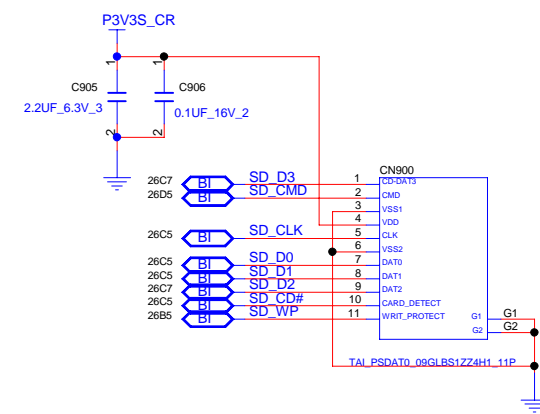
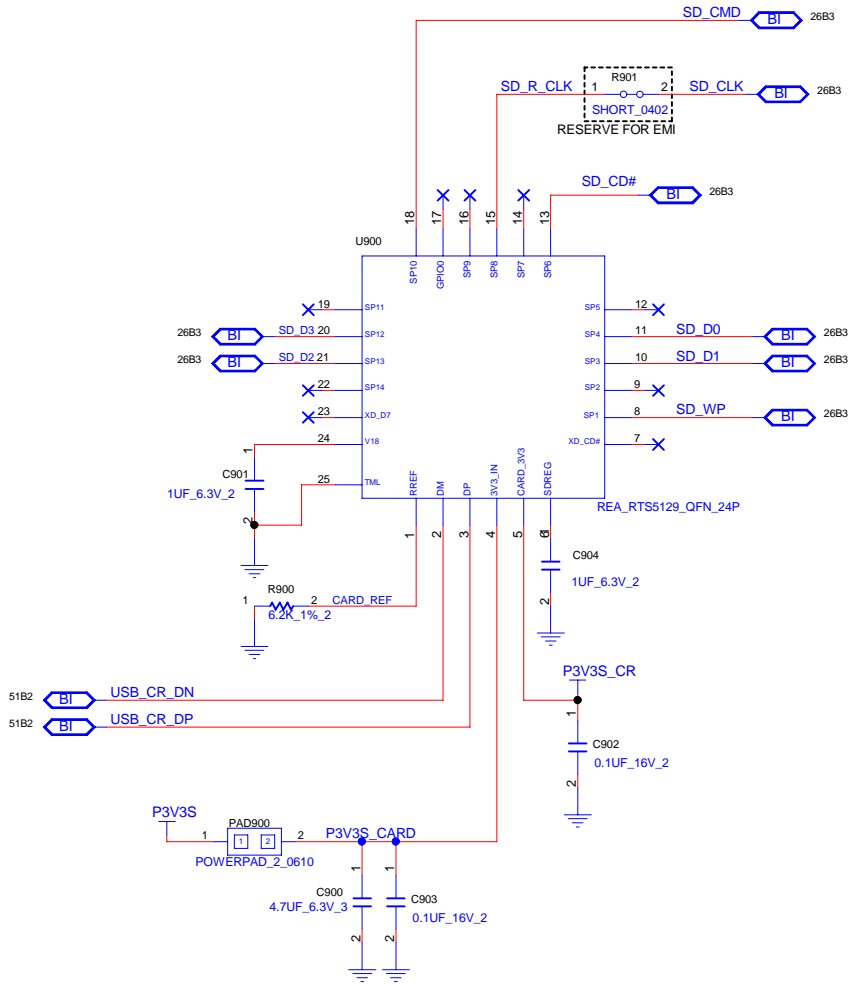


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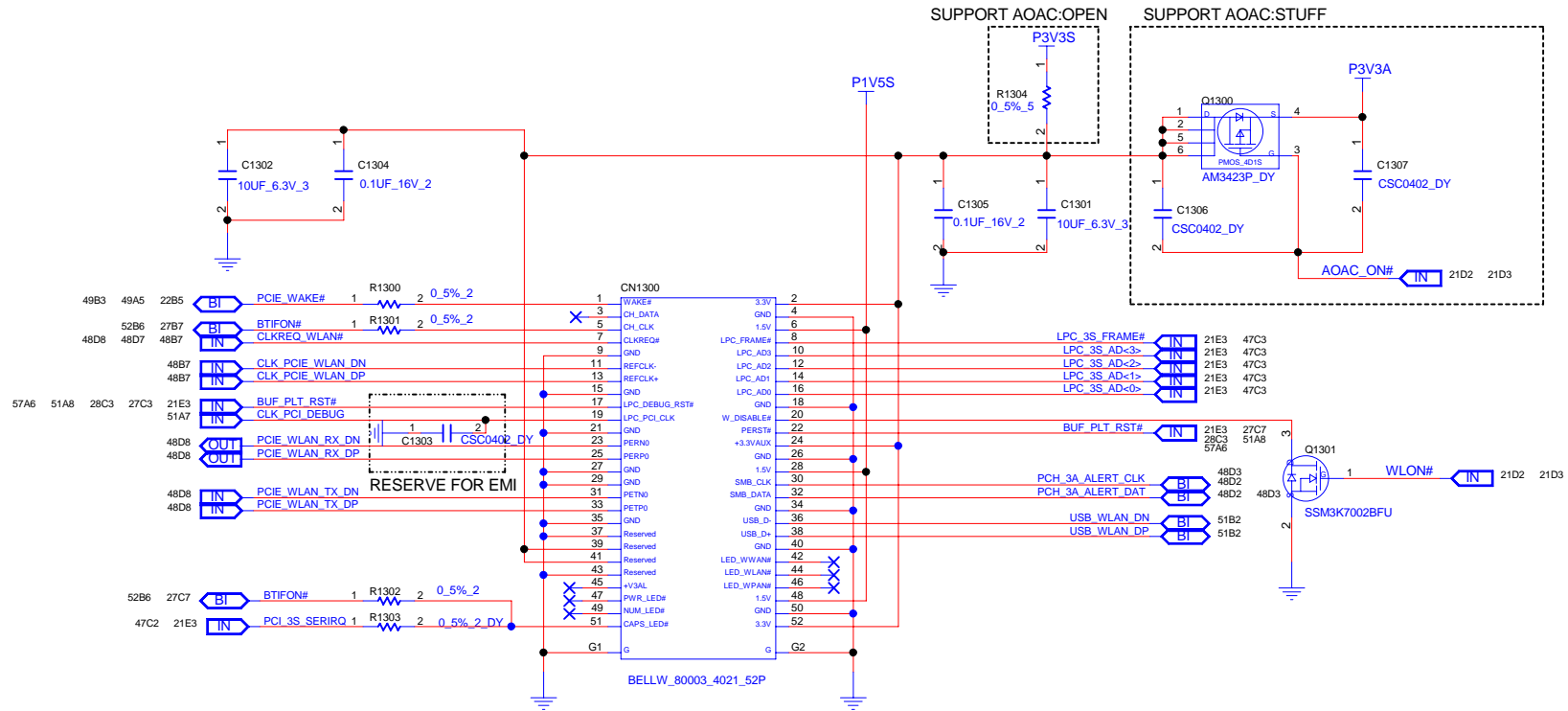
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MODEL PROJECT FUNCTION			
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REFERNCE 900~999(CARDREADER)



INVENTEC			
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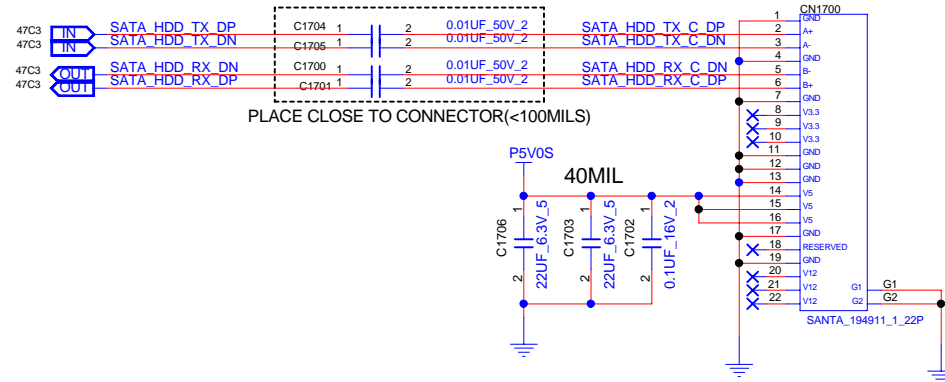
MINI CARD 1(WLAN)

INVENTEC			
TITLE			
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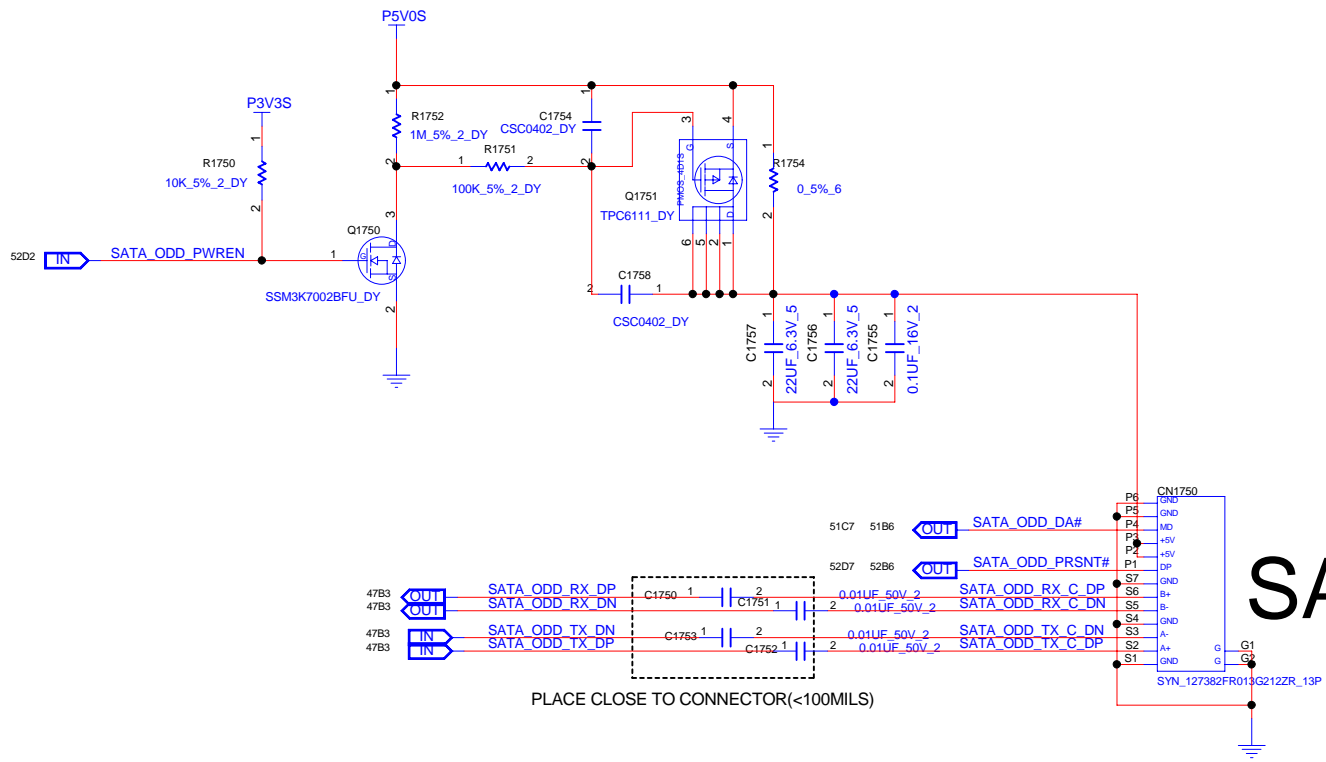


REFERENCE 1700~1749(HDD)
 REFERENCE 1750~1799(ODD)

SATA HDD



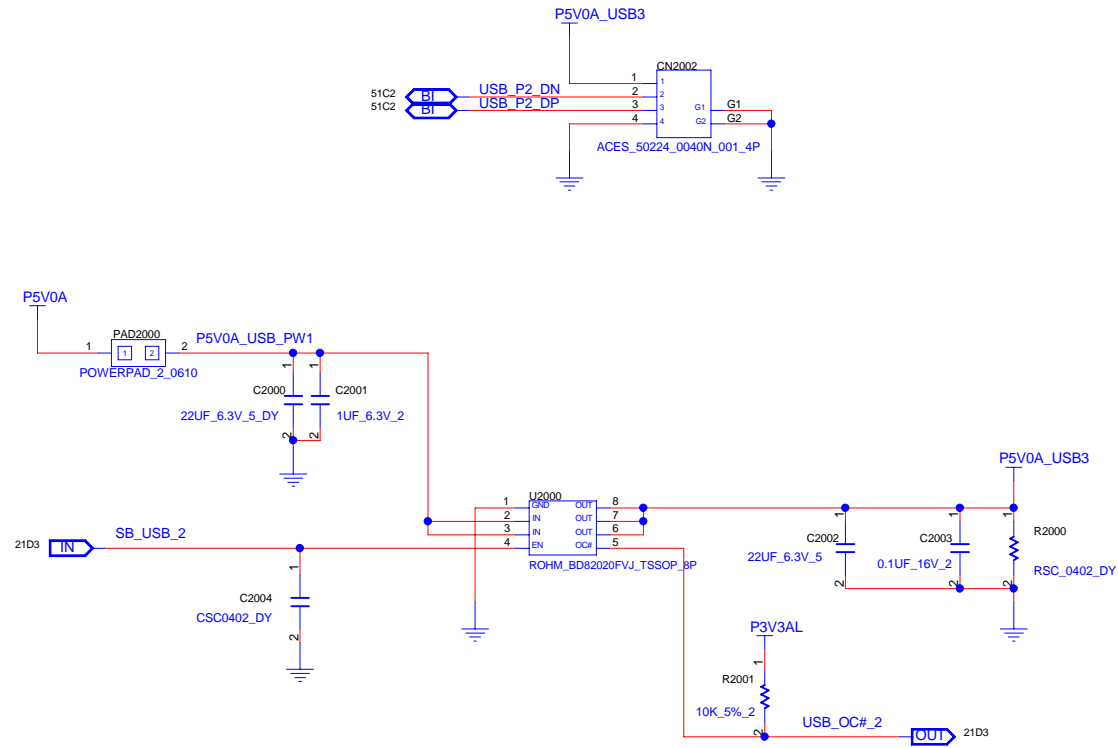
SATA ODD



INVENTEC			
TITLE Block Diagram			
MODEL,PROJECT,FUNCTION			
1310xxxx-0-0			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01



REFERENCE 2000~2099(USB)



INVENTEC

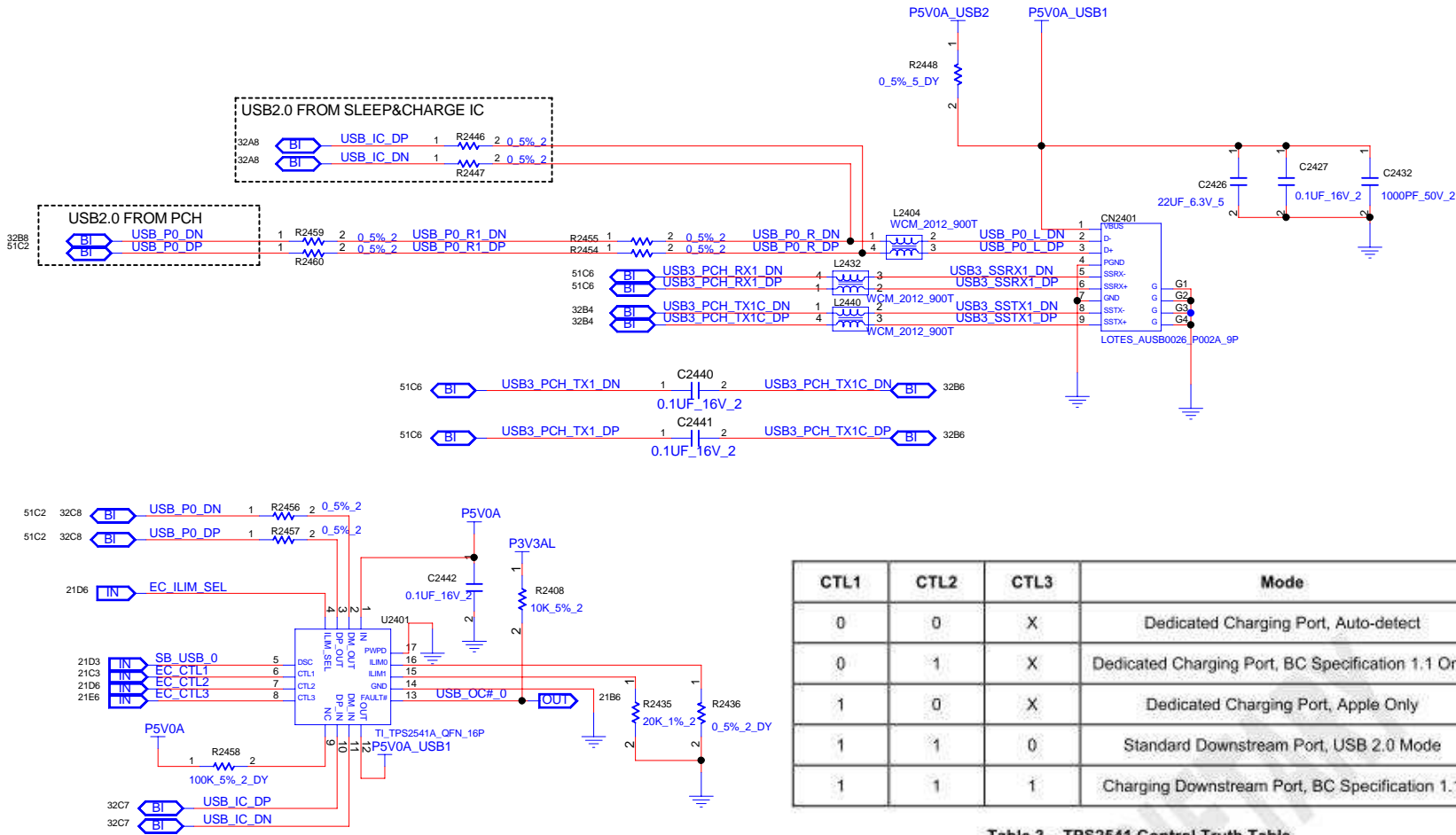
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MODEL PROJECT.FUNCTION Block Diagram			
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REFERENCE 2400~2499

REMOVE USB3.0 CONTROLLER IC

INVENTEC

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MODEL, PROJECT, FUNCTION Block Diagram			
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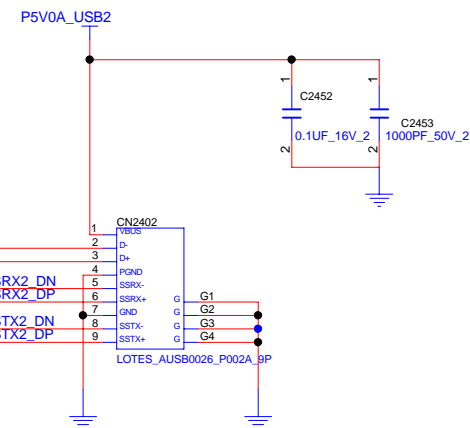
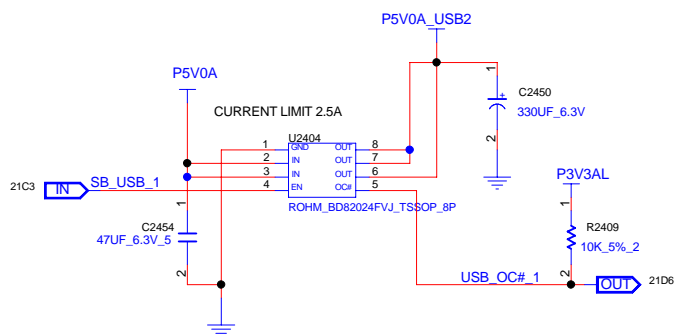
CTL1	CTL2	CTL3	Mode
0	0	X	Dedicated Charging Port, Auto-detect
0	1	X	Dedicated Charging Port, BC Specification 1.1 Only
1	0	X	Dedicated Charging Port, Apple Only
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

Table 3 – TPS2541 Control Truth Table

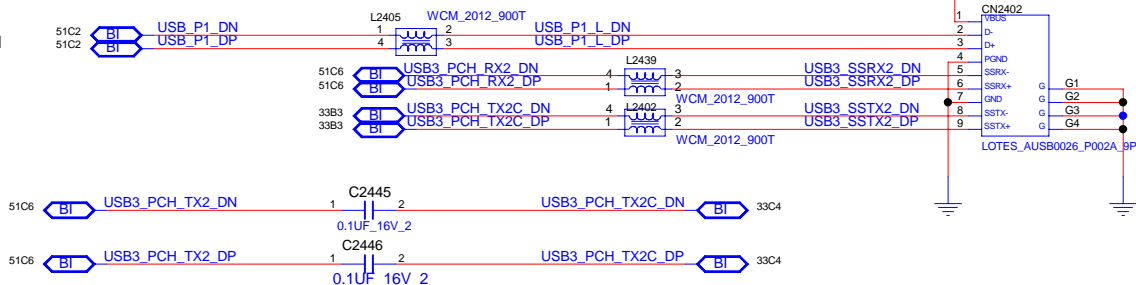
INVENTEC

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USB 3.0 CONNECTOR



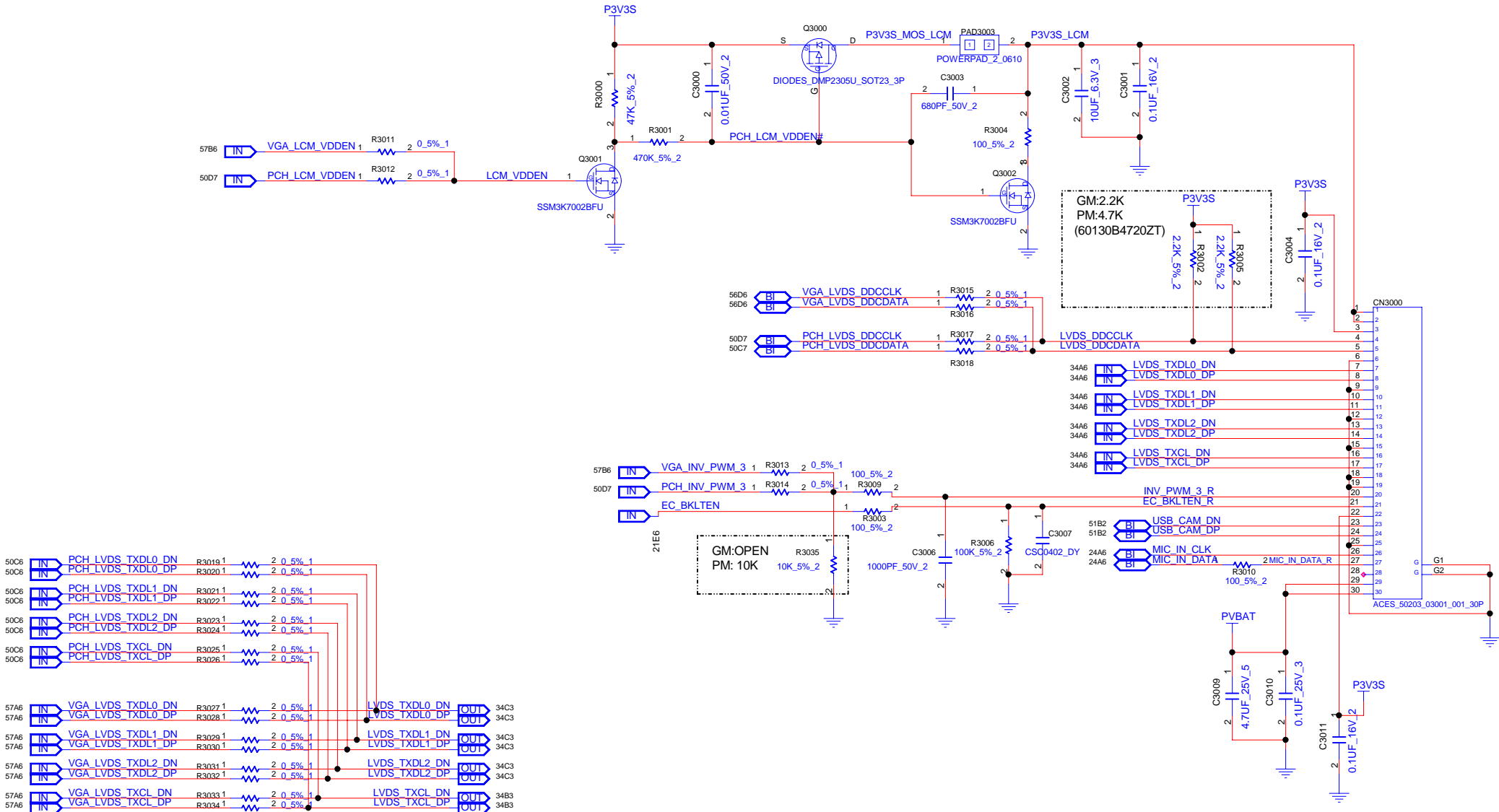
USB2.0 FROM PCH



INVENTEC			
TITLE			
MODEL PROJECT.FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01



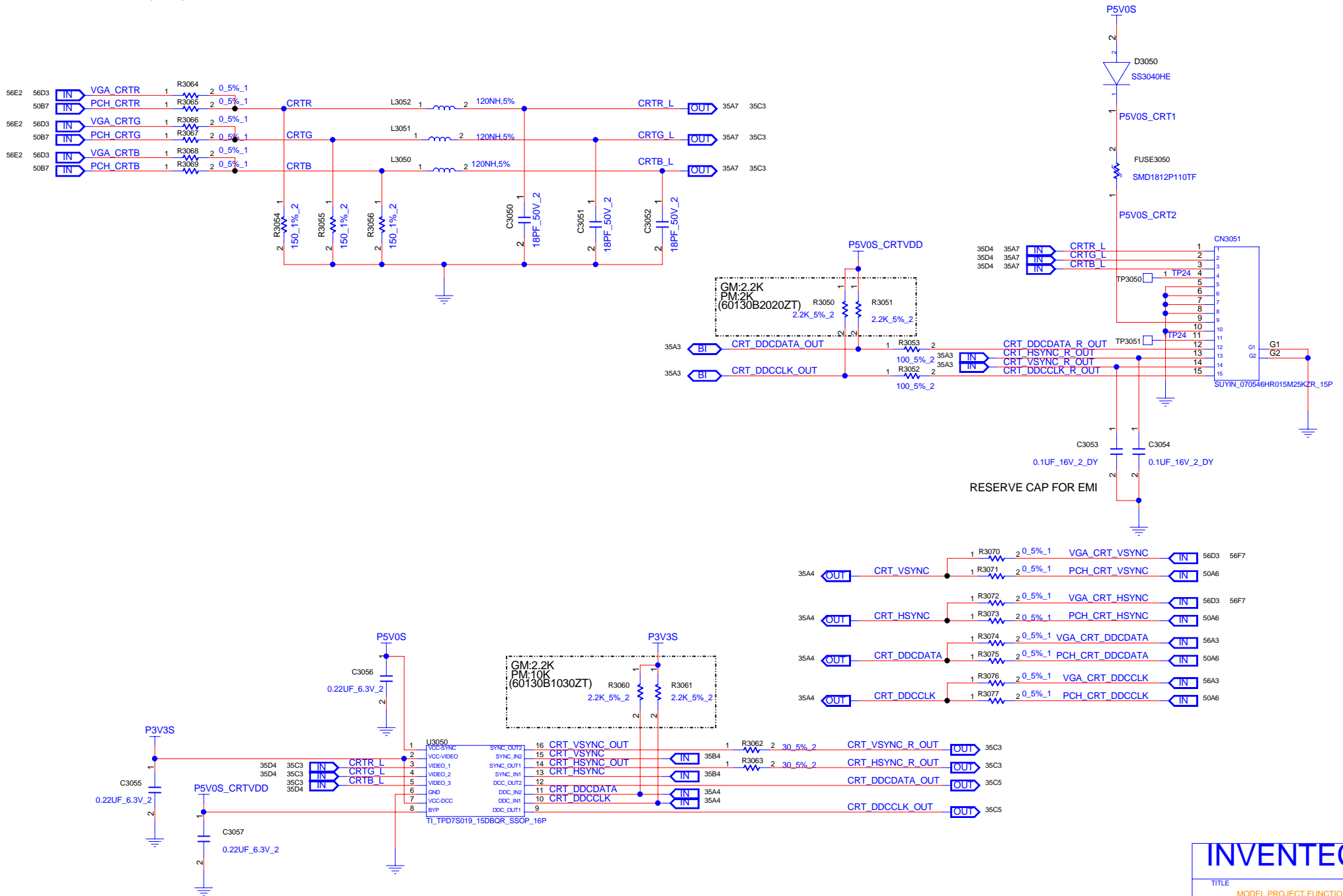
REFERENCE 3000~3049(LCM)



INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

REFERENCE 3050~3099(CRT)



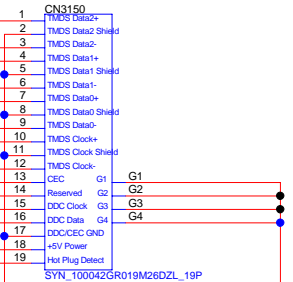
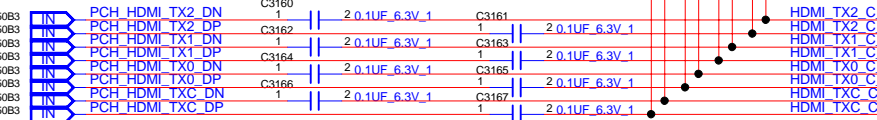
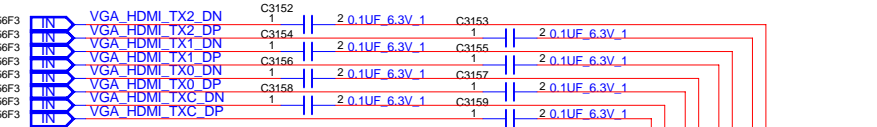
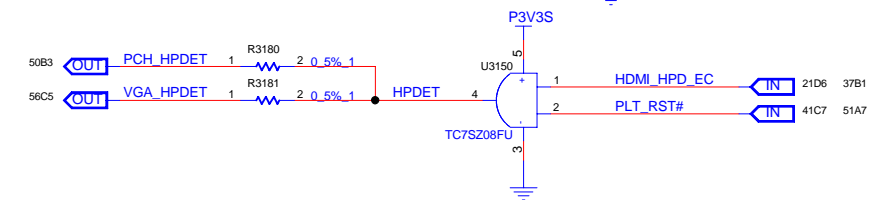
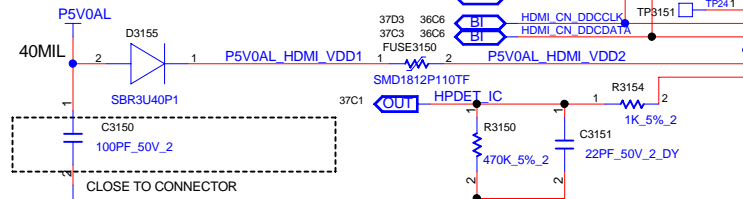
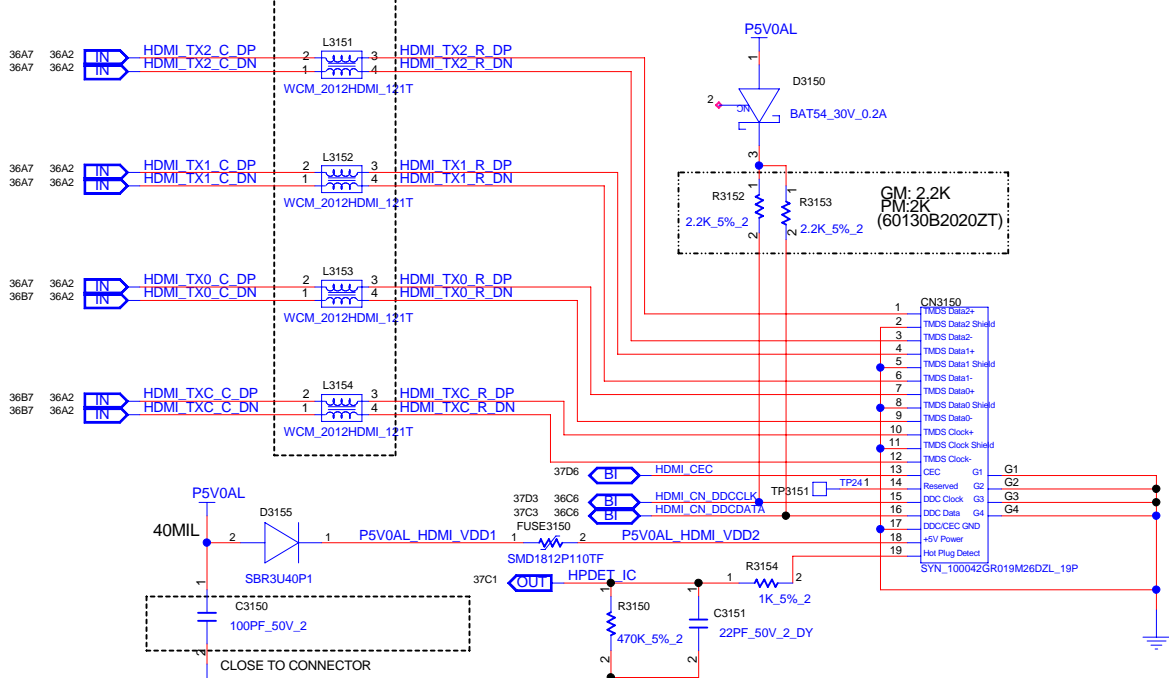
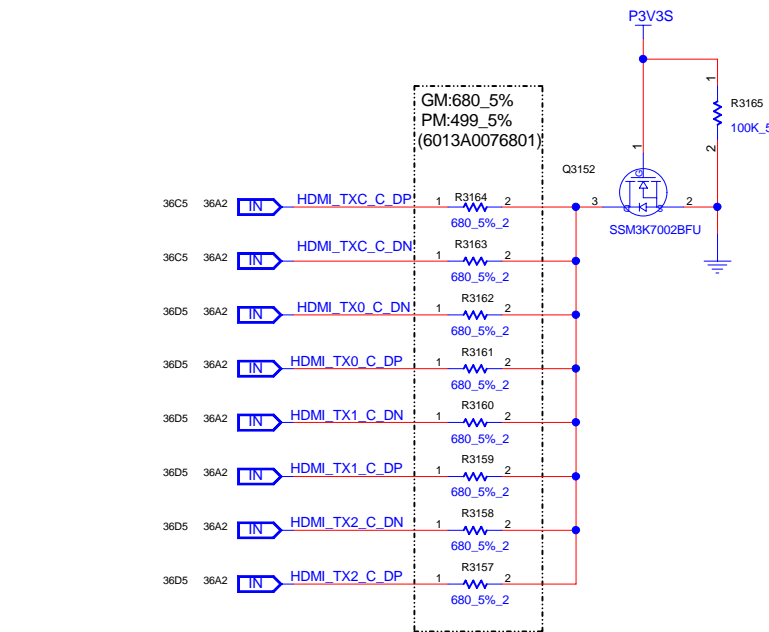
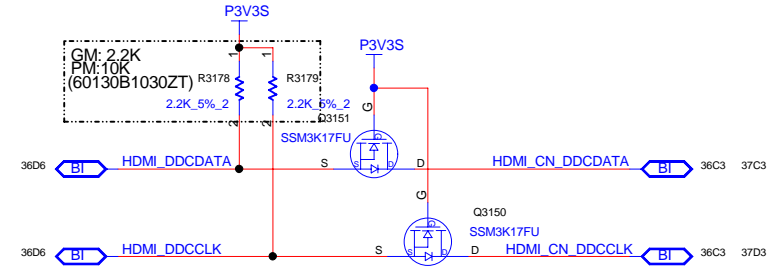
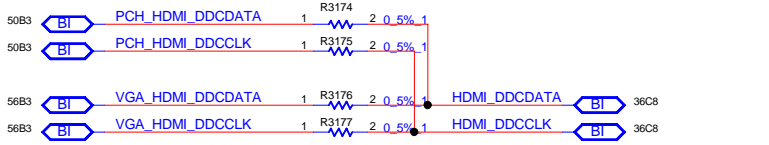
RESERVE CAP FOR EMI

INVENTEC

TITLE			
MODEL PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

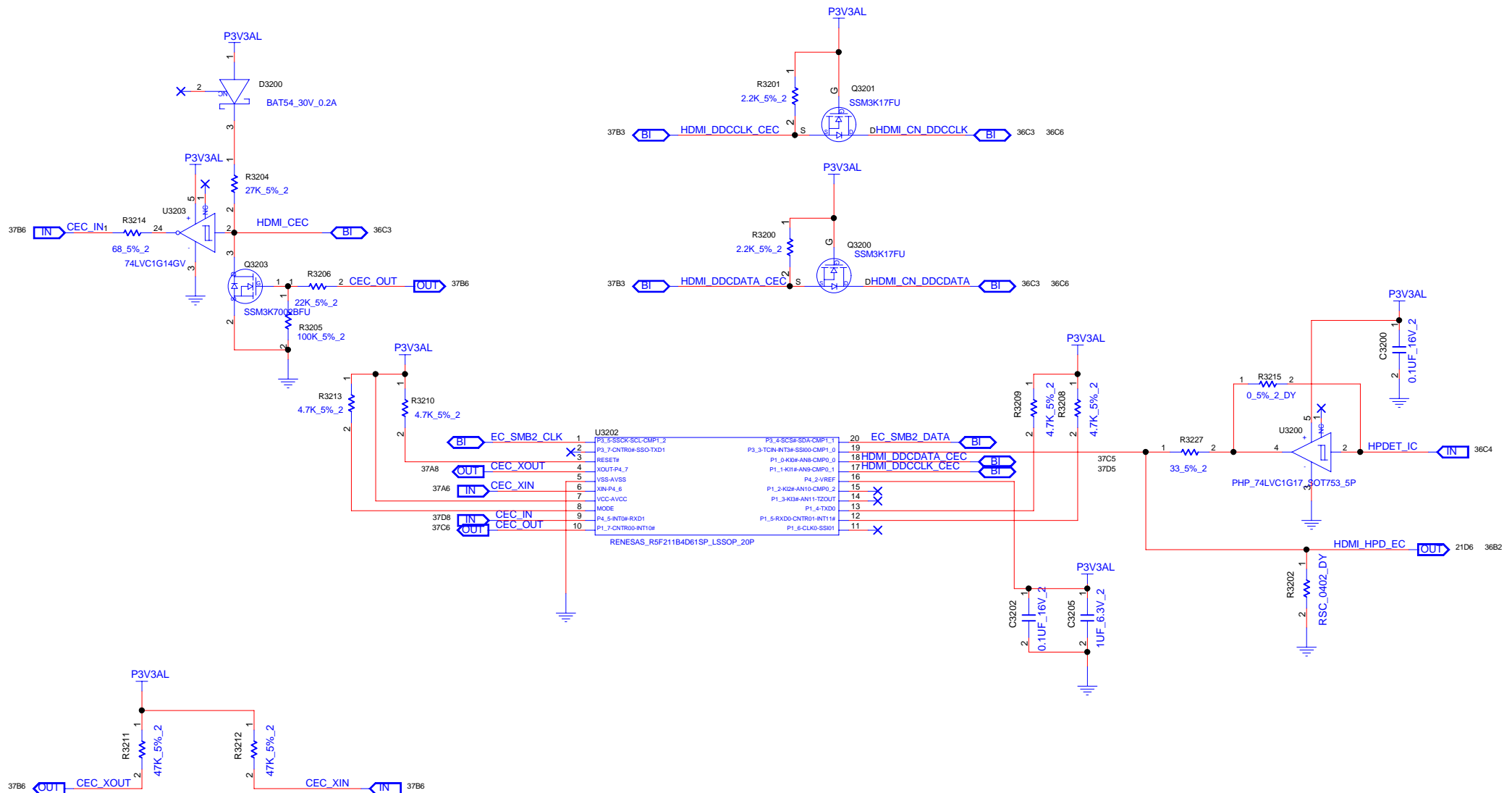
REFERENCE 3150~3199(HDMI)

PLACE CLOSE TO CONNECTOR



INVENTEC
 TITLE
 MODEL,PROJECT,FUNCTION
 Block Diagram

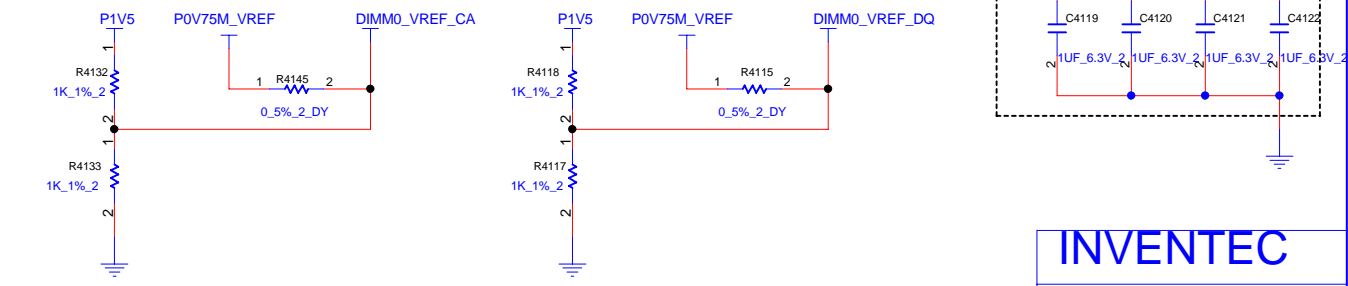
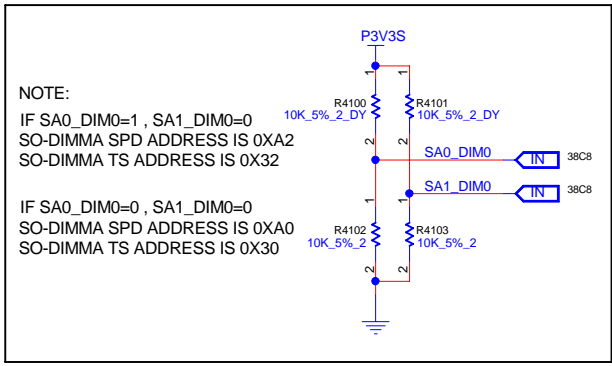
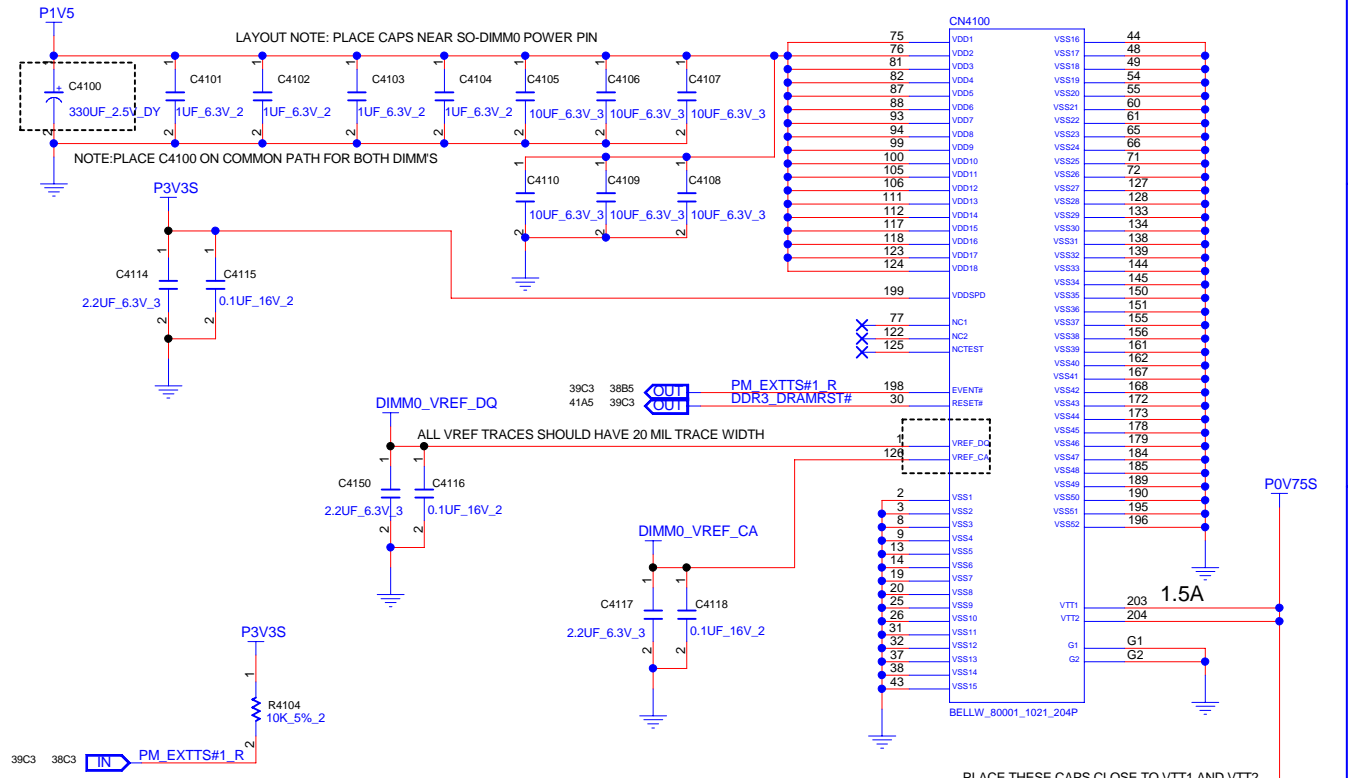
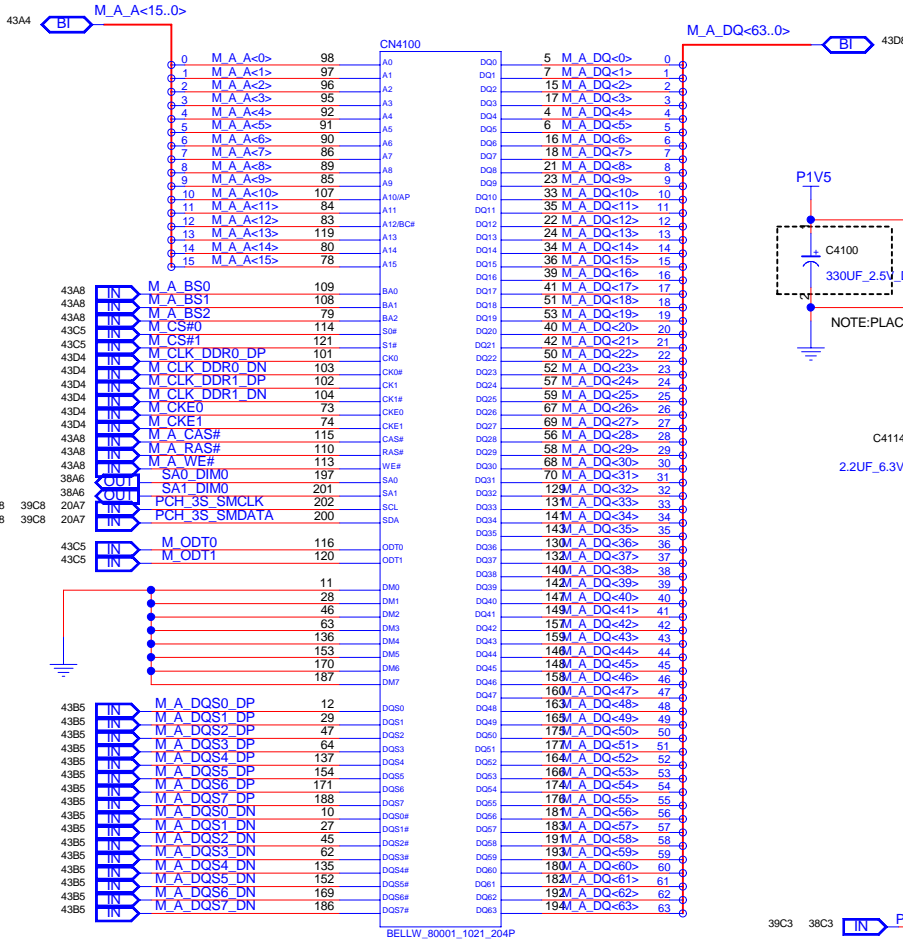
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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INVENTEC			
TITLE MODEL PROJECT FUNCTION Block Diagram			
SIZE A3		CODE CS	
DOC NUMBER 1310xxxxx-0-0		REV X01	

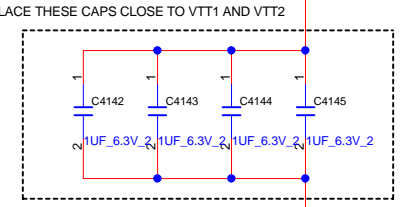
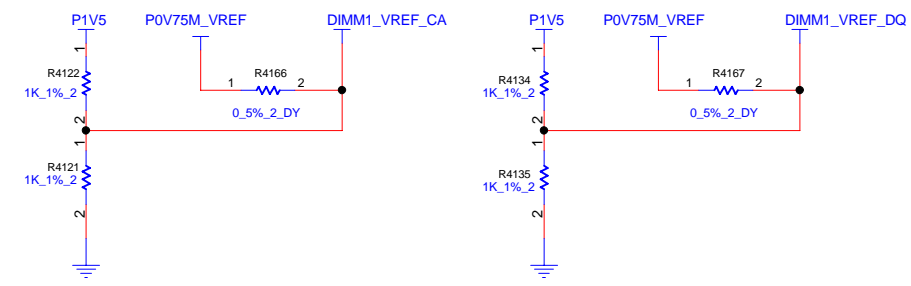
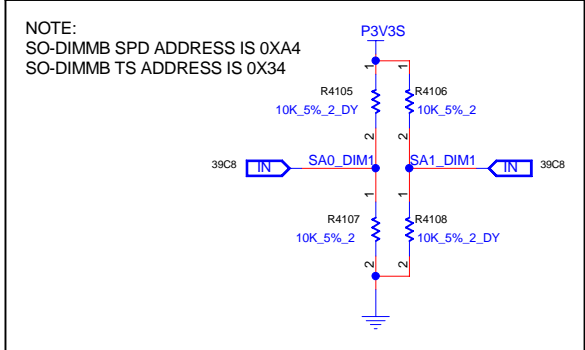
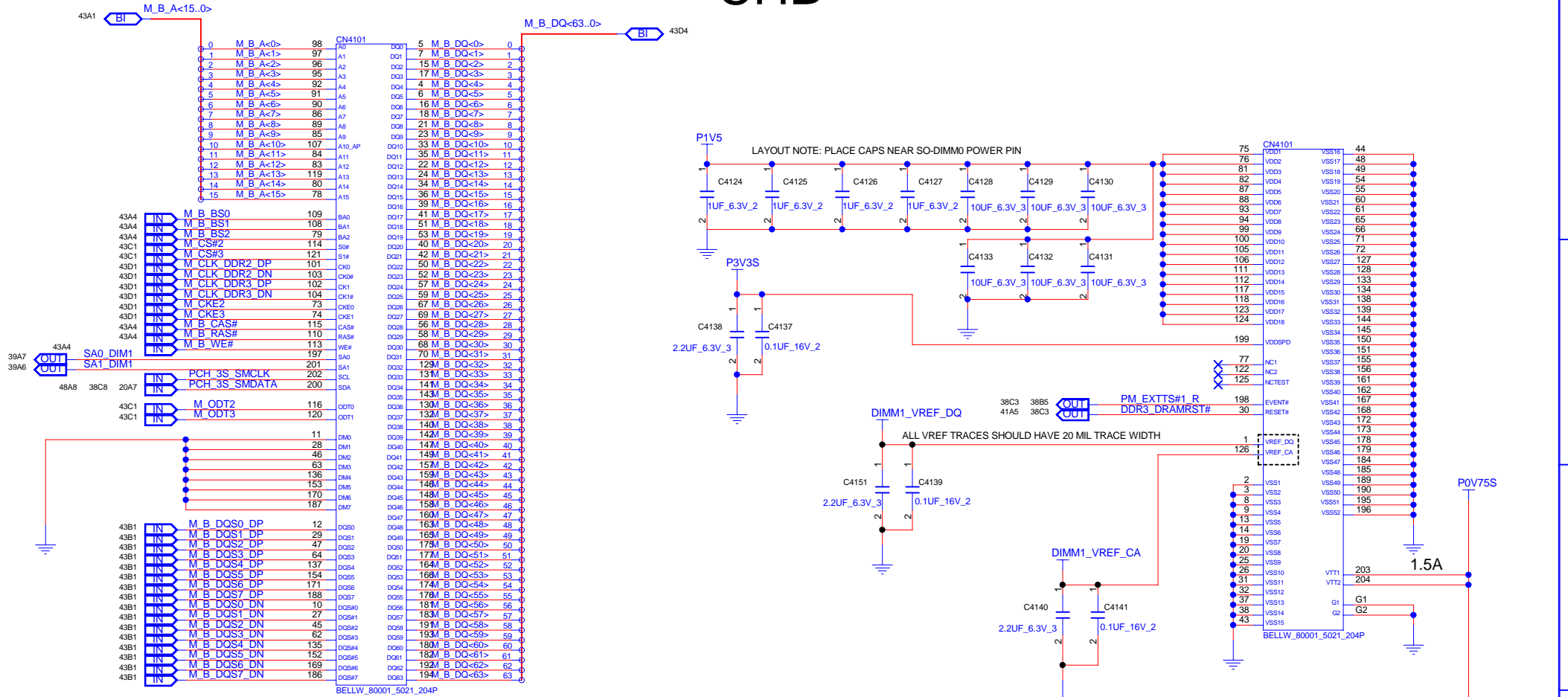


CHA



INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by XXX			
DATE 21-OCT-2002			
SHEET 38 of 70			

CHB

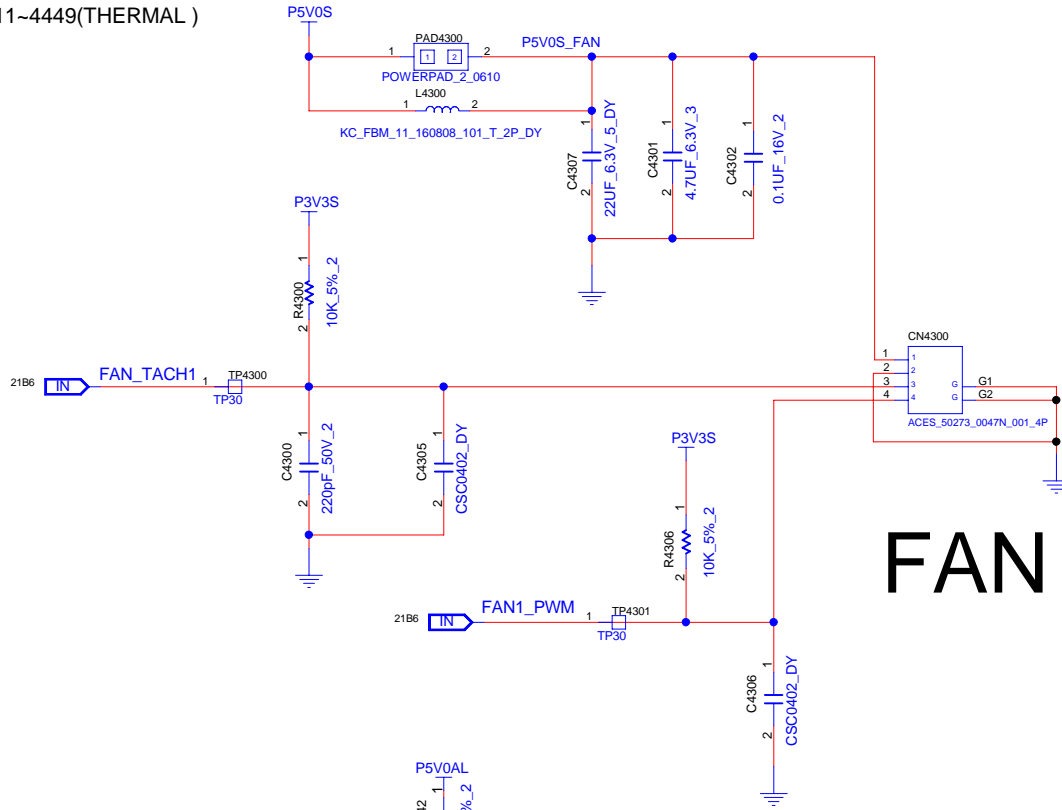


INVENTEC

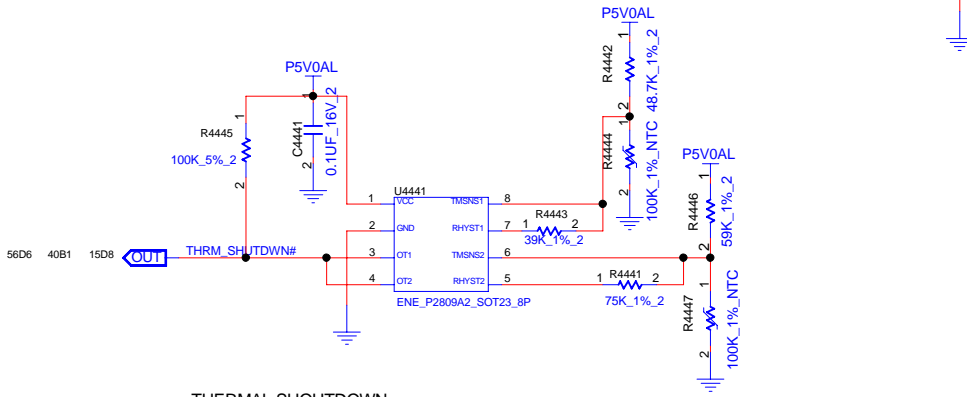
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01



REFERENCE 4300~4349(FAN)
 REFERENCE 4411~4449(THERMAL)



FAN CN

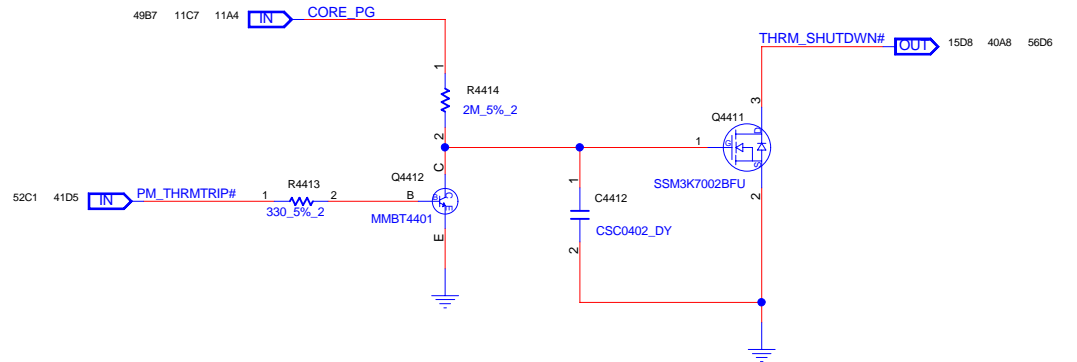


THERMAL SHUTDOWN

GM THERMAL SHUTDOWN CPU SIDE AT 68.6 C
 GM THERMAL SHUTDOWN VGA SIDE AT 63.4 C

PM THERMAL SHUTDOWN CPU SIDE AT 71.9 C
 PM THERMAL SHUTDOWN VGA SIDE AT 80.2 C

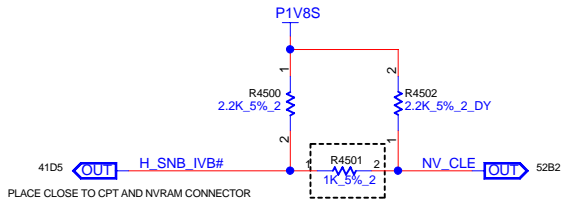
	10F	10FG
R4442	48.7K	43.2K
R4443	39K	30.1K
R4446	59K	32.4K
R4441	75K	18.2K



INVENTEC

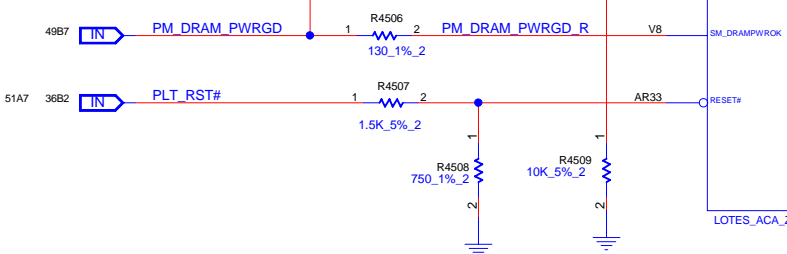
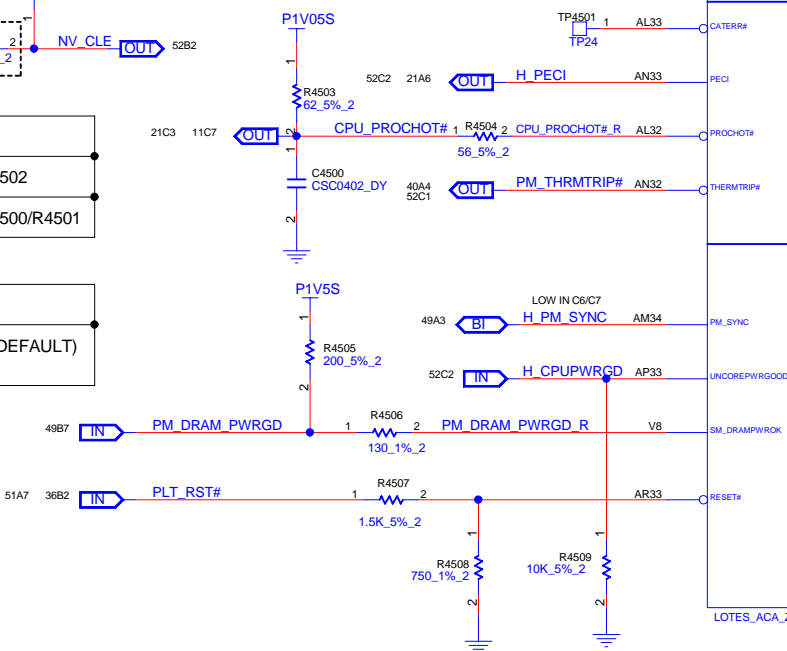
TITLE			
Block Diagram			
MODEL PROJECT.FUNCTION			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

REFERENCE 4500-4699(CPU)

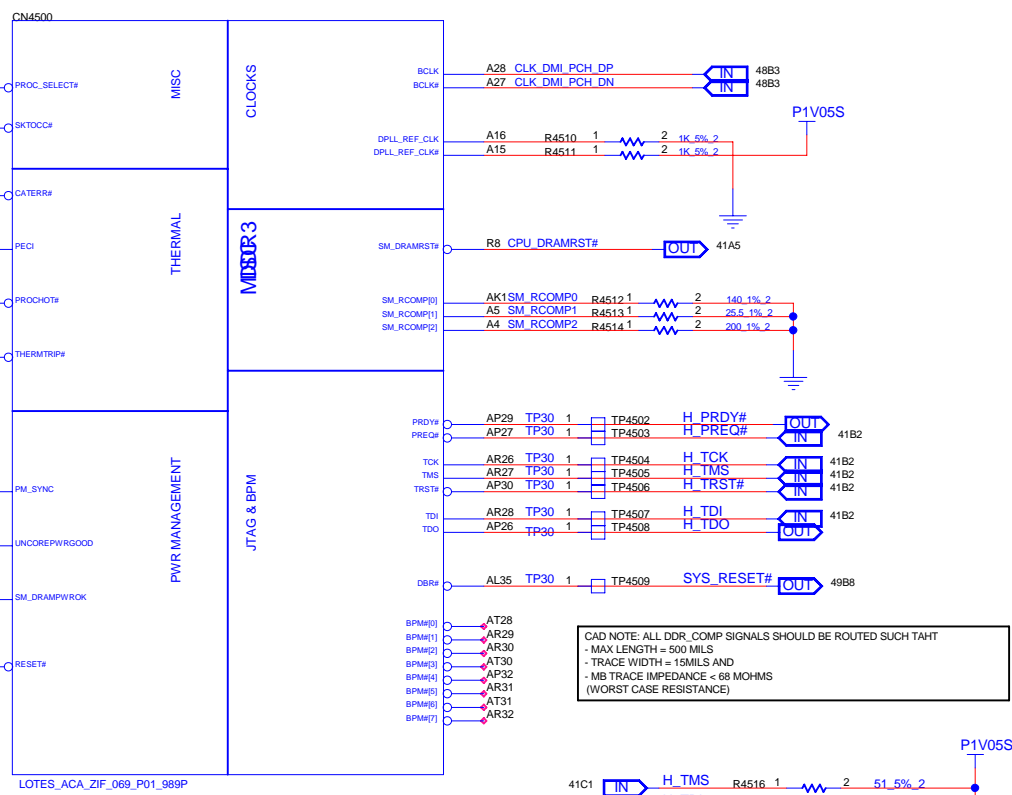
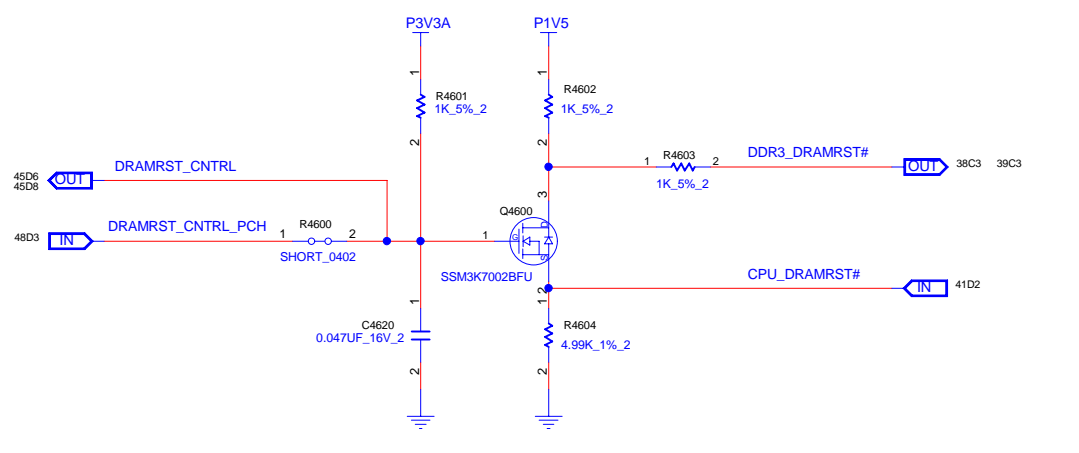


PROCESS STRAP SETTING	
SANDY BRIDGE ONLY	STUFF R4502
SANDY BRIDGE/IVY BRIDGE	STUFF R4500/R4501

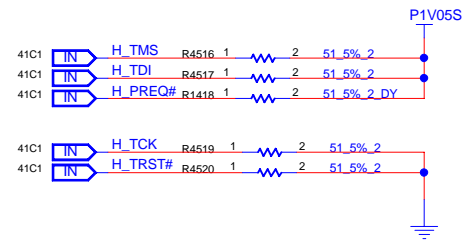
DMI&FDI TERMINATIONVOLTAGE	
NV_CLE	SET TOVSS WHEN LOW (DEFAULT) SET TOVCC WHEN HIGH



S3 CIRCUIT: DRAM_RST# TO MEMORY SHOULD BE HIGH DURING S3



CAD NOTE: ALL DDR_COMP SIGNALS SHOULD BE ROUTED SUCH THAT
 - MAX LENGTH = 500 MILS
 - TRACE WIDTH = 15MILS AND
 - MB TRACE IMPEDANCE = 68 MOHMS
 (WORST CASE RESISTANCE)



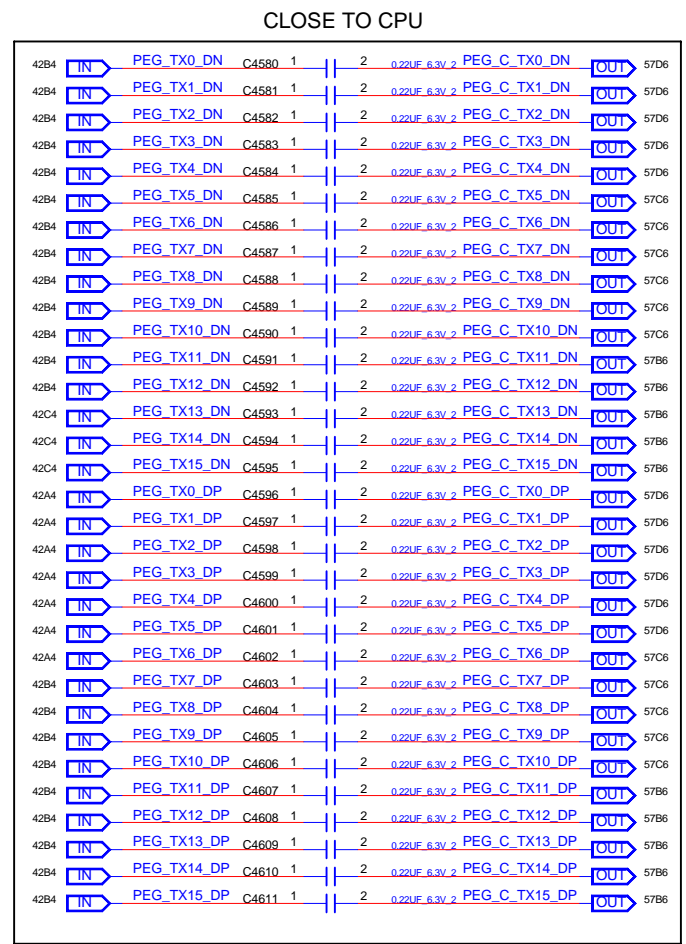
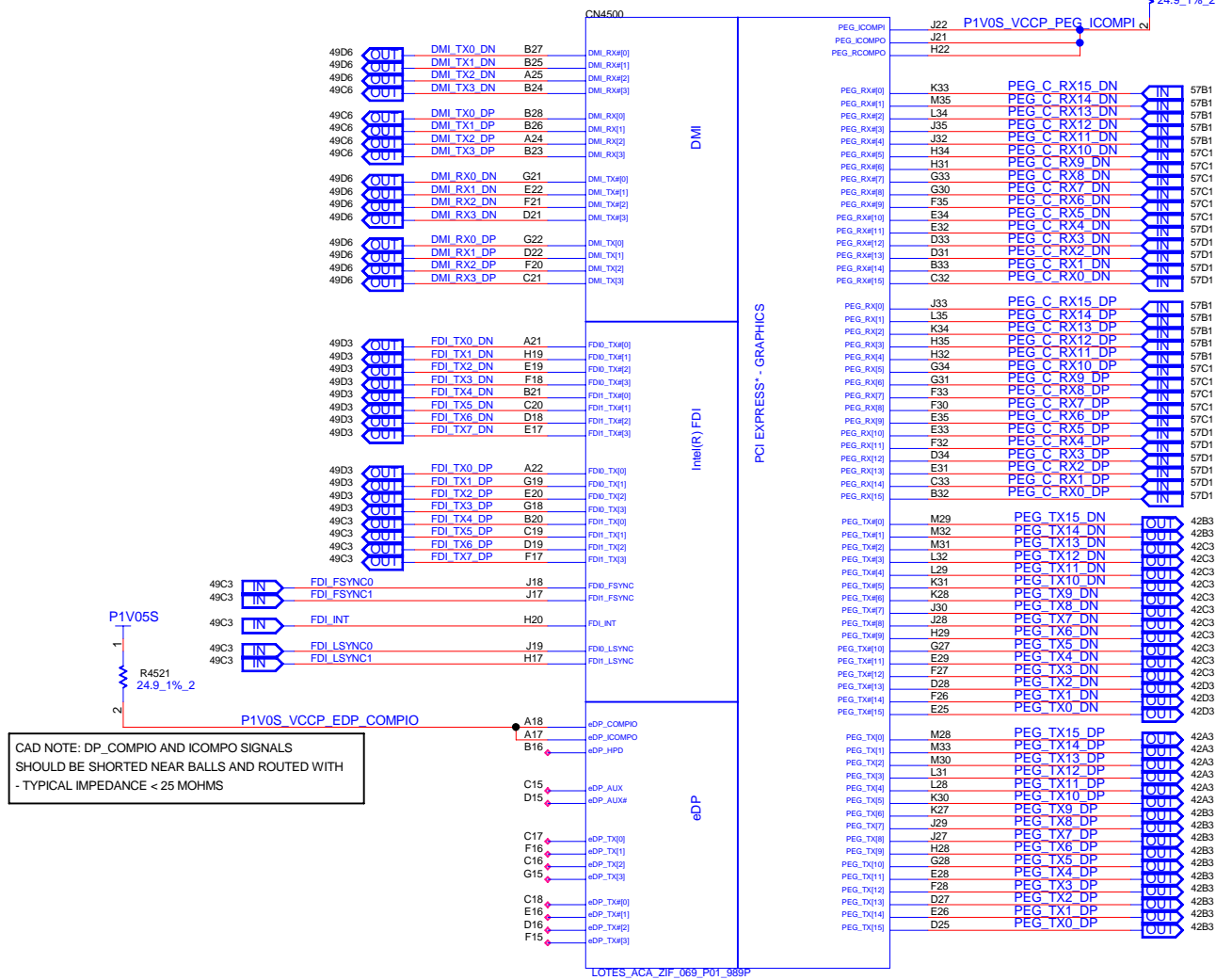
INVENTEC			
TITLE			
MODEL PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01



REFERENCE 4500~4699(CPU)

CAD NOTE: PEG_ICOMPI AND RCOMPO SIGNALS SHOULD BE SHORTED AND ROUTED WITH
 - MAX LENGTH = 500 MILS
 - TYPICAL IMPEDANCE = 43 MOHMS

PEG_ICOMPO SIGNALS SHOULD BE ROUTED WITH
 - MAX LENGTH = 500 MILS
 - TYPICAL IMPEDANCE = 14.5 MOHMS



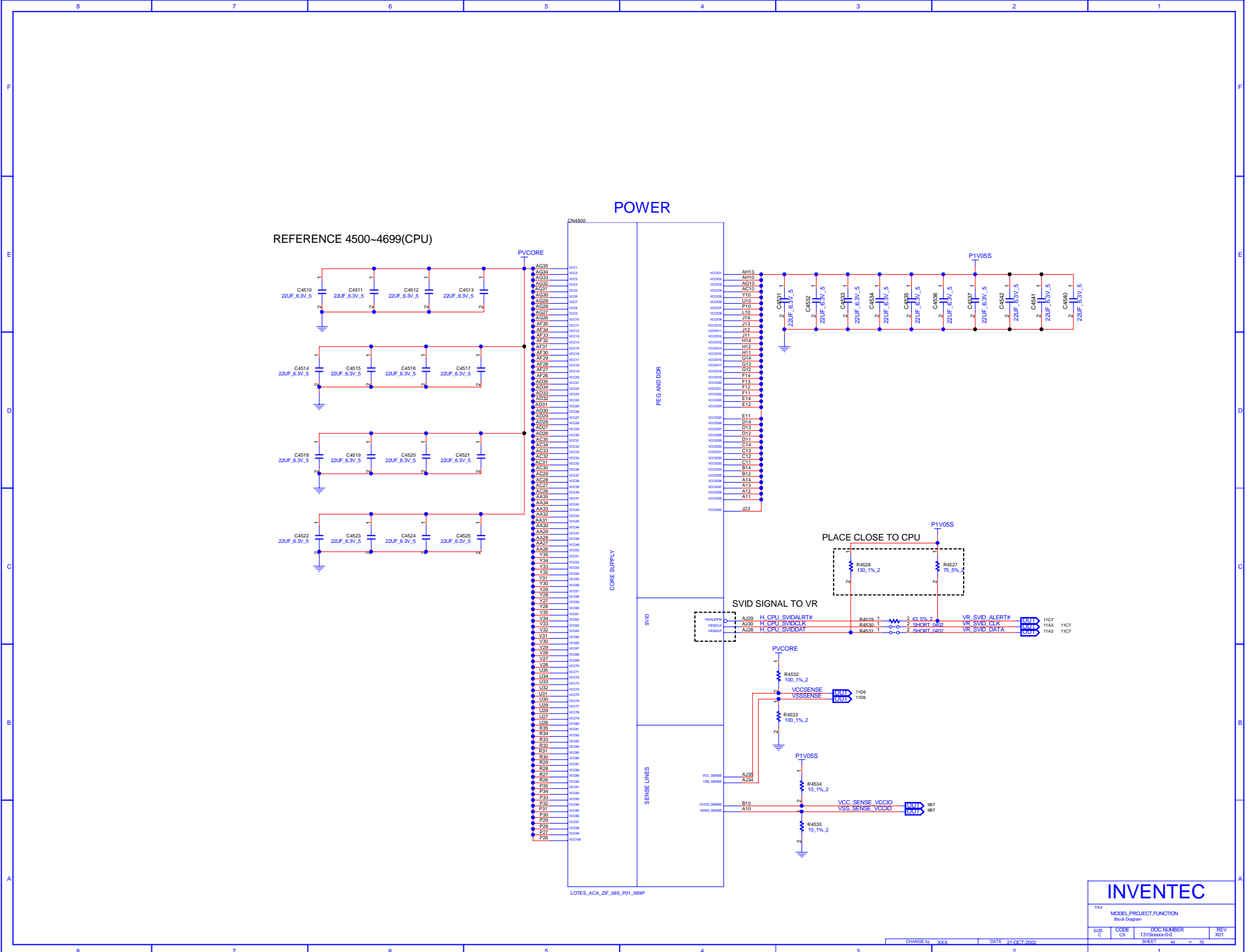
CAD NOTE: DP_COMPIO AND ICOMPO SIGNALS SHOULD BE SHORTED NEAR BALLS AND ROUTED WITH
 - TYPICAL IMPEDANCE < 25 MOHMS

INVENTEC

TITLE MODEL PROJECT FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002 SHEET 42 of 70



REFERENCE 4500-4699(CPU)

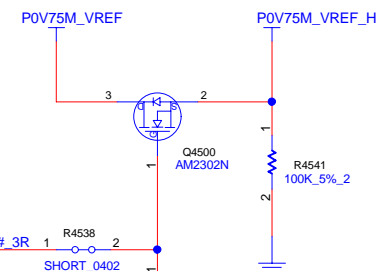
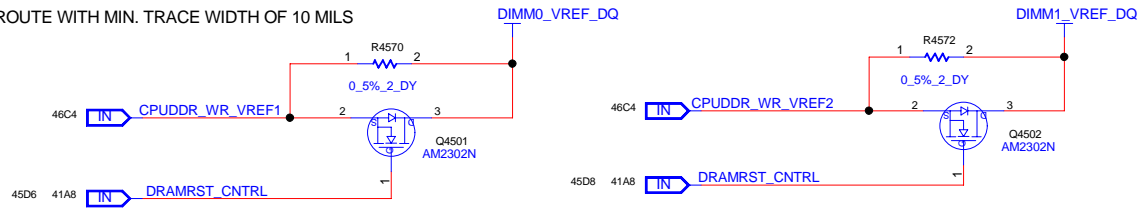
POWER

- AG35
- AG34
- AG33
- AG32
- AG31
- AG30
- AG29
- AG28
- AG27
- AG26
- AF35
- AF34
- AF33
- AF32
- AF31
- AF30
- AF29
- AF28
- AF27
- AF26
- AD35
- AD34
- AD33
- AD32
- AD31
- AD30
- AD29
- AD28
- AD27
- AC35
- AC34
- AC33
- AC32
- AC31
- AC30
- AC29
- AC28
- AC27
- AA35
- AA34
- AA33
- AA32
- AA31
- AA30
- AA29
- AA28
- AA27
- Y35
- Y34
- Y33
- Y32
- Y31
- Y30
- Y29
- Y28
- Y27
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- V35
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- P26

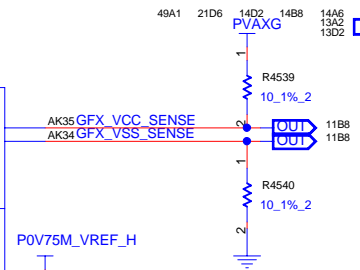
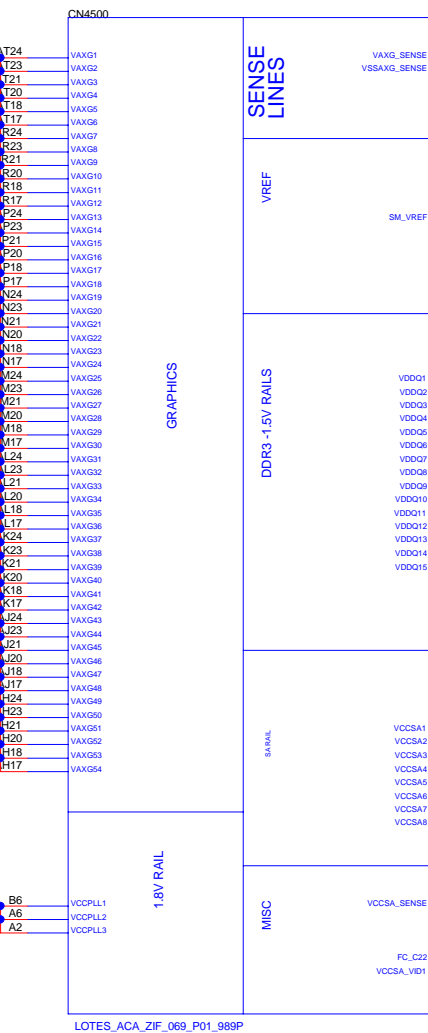
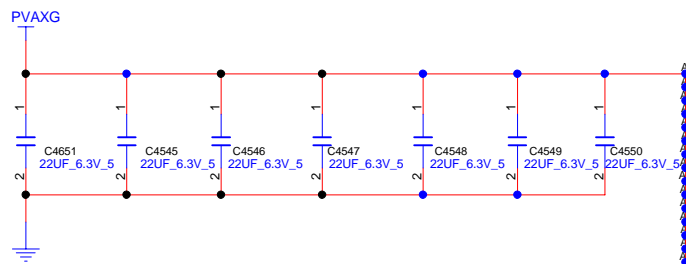
LOTES_ACA_ZIF_069_P01_989P

INVENTEC			
TITLE MODEL_PROJECT.FUNCTION Block Diagram			
SIZE C	CODE C3	DOC NUMBER 1310A0000000	REV X01
CHANGE BY XXX		DATE 21-OCT-2002	SHEET 44 of 50

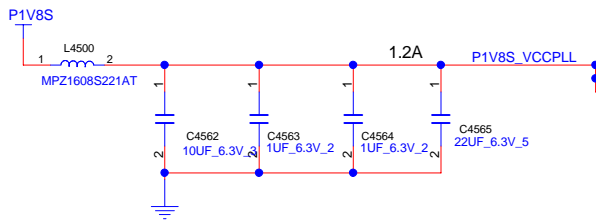
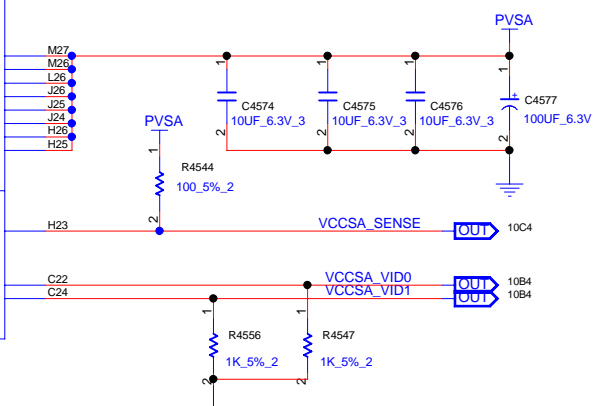
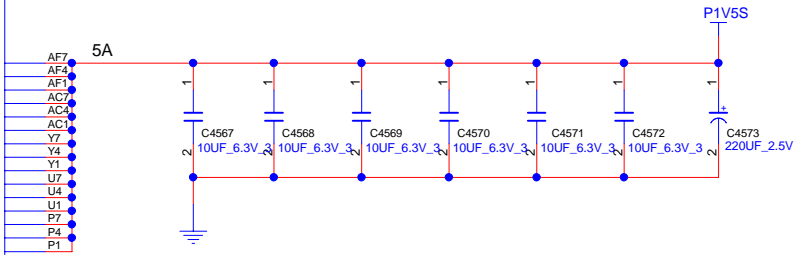
PROCESSOR DRIVEN VREF PATH WAS STUFFED BY DEFAULT:
ROUTE WITH MIN. TRACE WIDTH OF 10 MILS



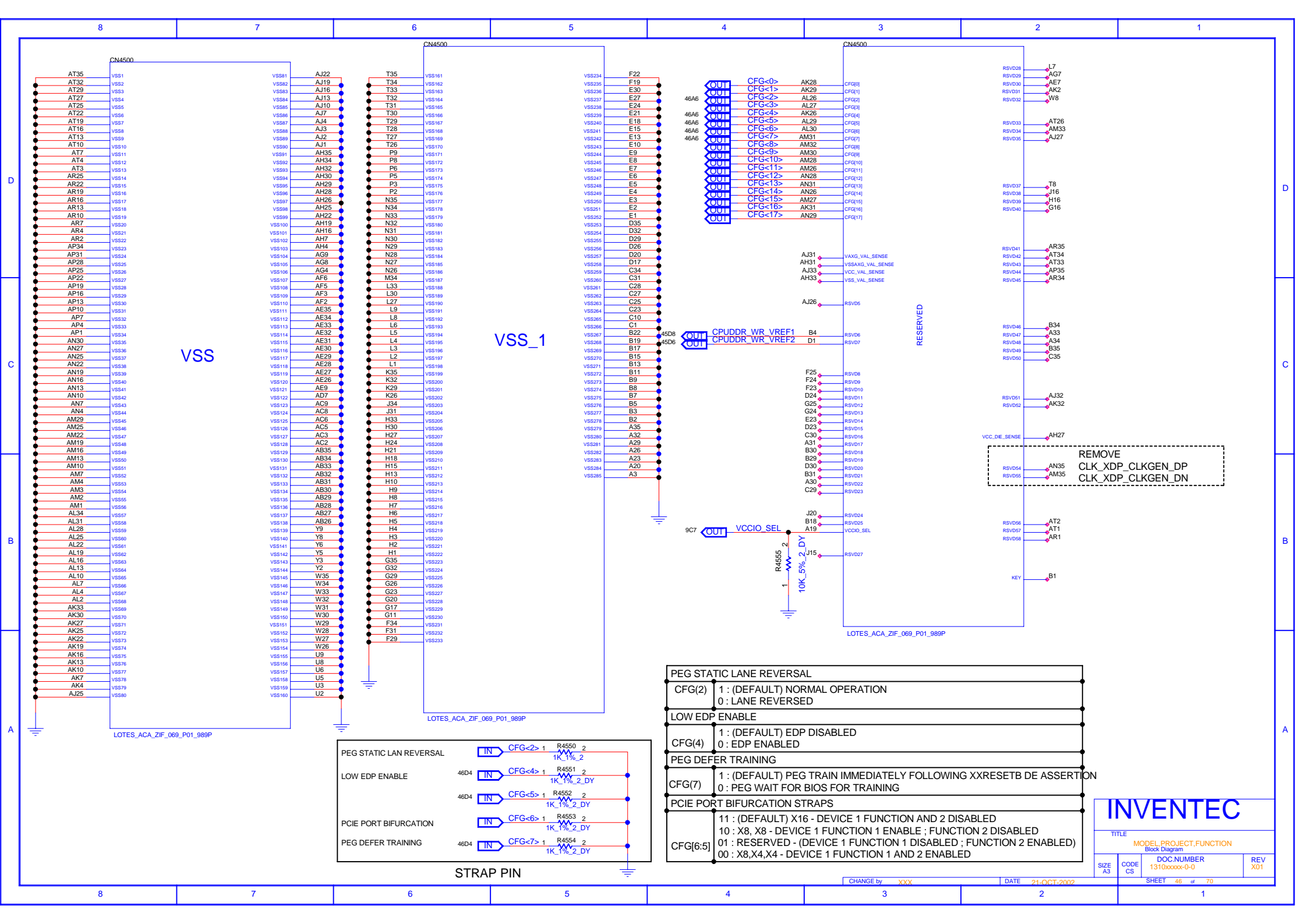
POWER



NOTE : DDR_WR_VREF SHOULD HAVE 20/20 MIL WHEREVER POSSIBLE



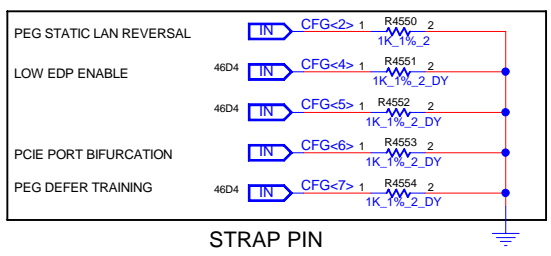
INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 45 of 70			



VSS

VSS_1

PEG STATIC LANE REVERSAL	
CFG(2)	1 : (DEFAULT) NORMAL OPERATION 0 : LANE REVERSED
LOW EDP ENABLE	
CFG(4)	1 : (DEFAULT) EDP DISABLED 0 : EDP ENABLED
PEG DEFER TRAINING	
CFG(7)	1 : (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB DE ASSERTION 0 : PEG WAIT FOR BIOS FOR TRAINING
PCIE PORT BIFURCATION STRAPS	
CFG[6:5]	11 : (DEFAULT) X16 - DEVICE 1 FUNCTION AND 2 DISABLED 10 : X8, X8 - DEVICE 1 FUNCTION 1 ENABLE ; FUNCTION 2 DISABLED 01 : RESERVED - (DEVICE 1 FUNCTION 1 DISABLED ; FUNCTION 2 ENABLED) 00 : X8,X4,X4 - DEVICE 1 FUNCTION 1 AND 2 ENABLED



REMOVE
CLK_XDP_CLKGEN_DP
CLK_XDP_CLKGEN_DN

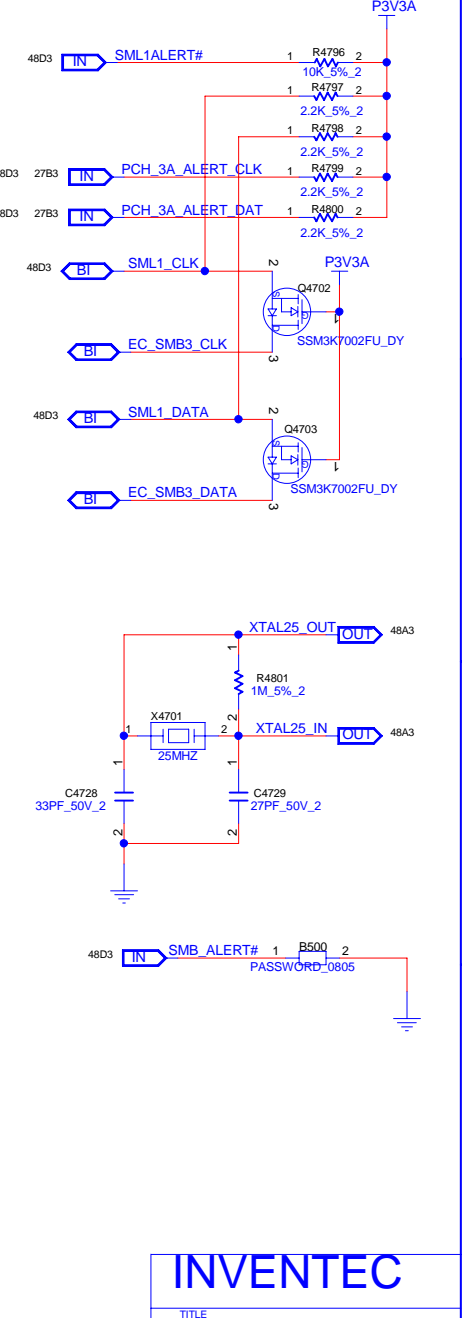
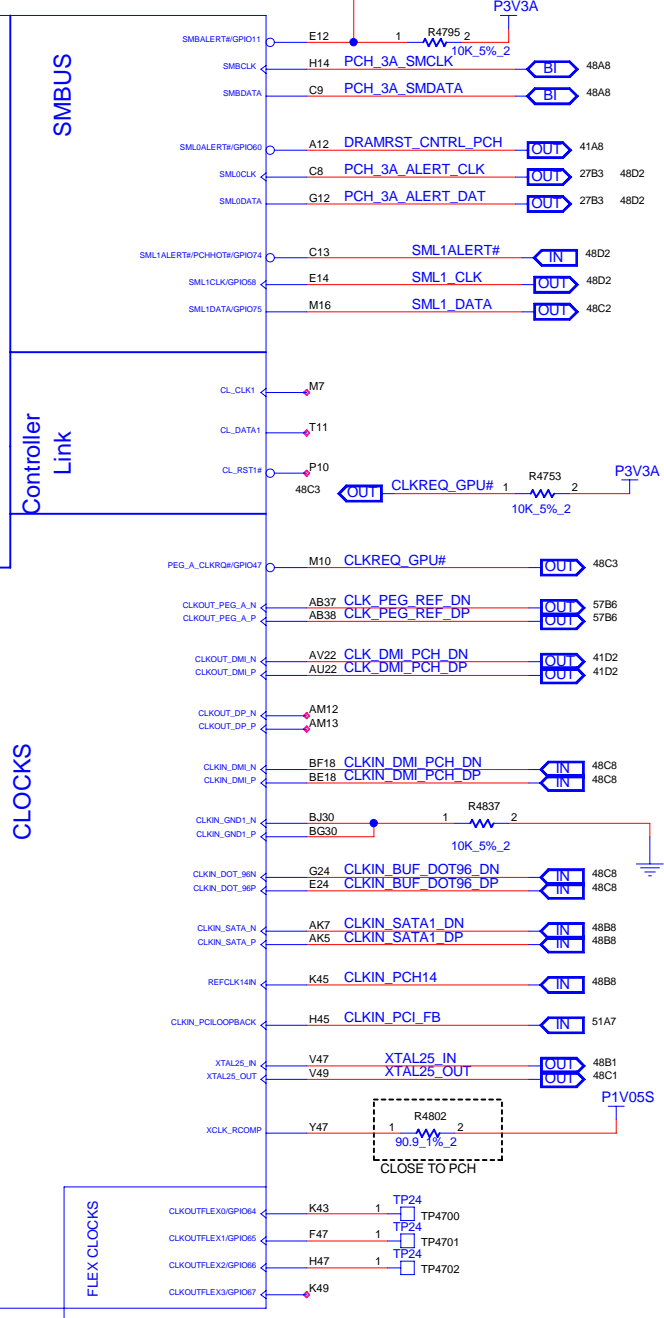
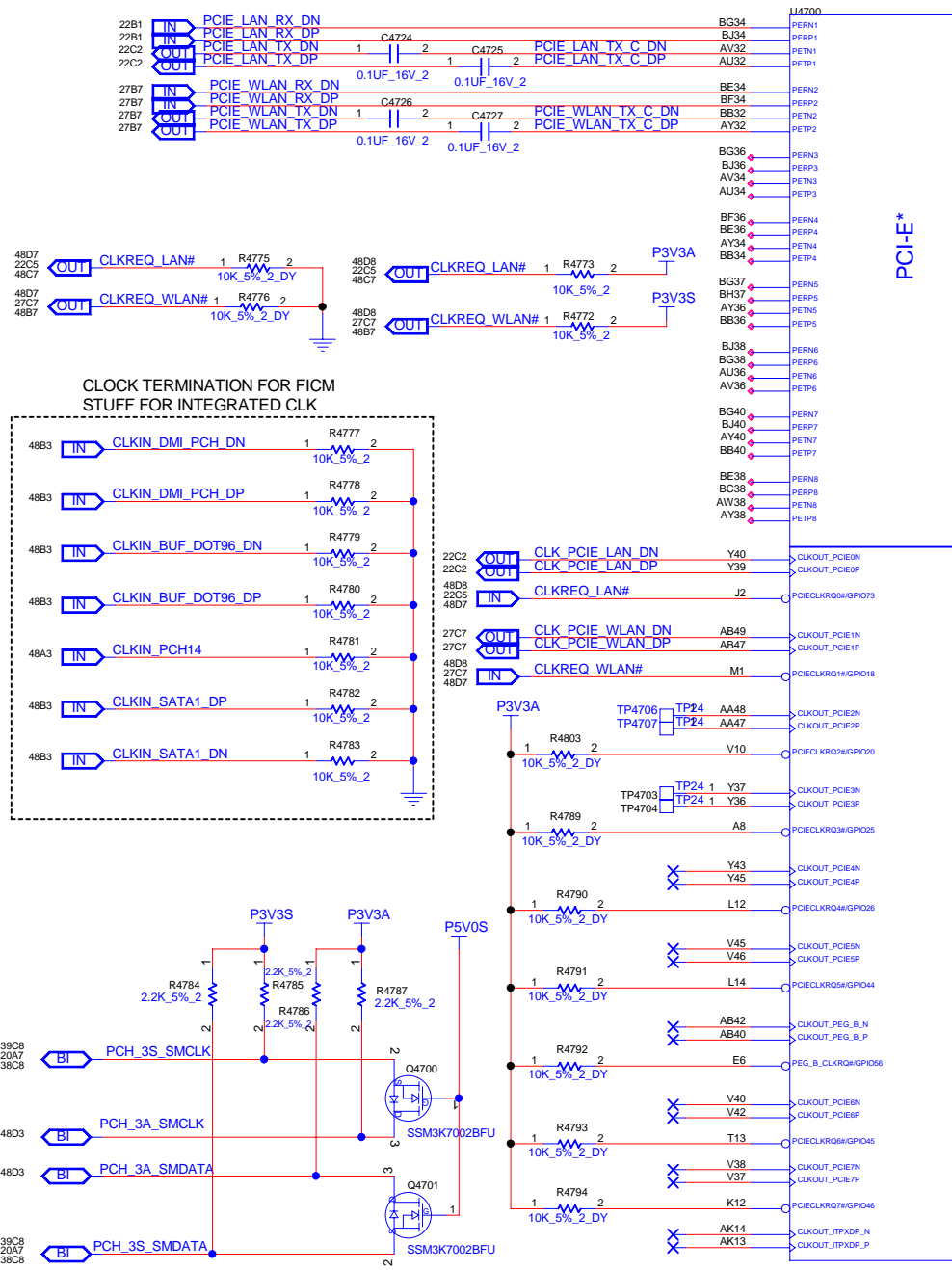
INVENTEC

TITLE
MODEL:PROJECT:FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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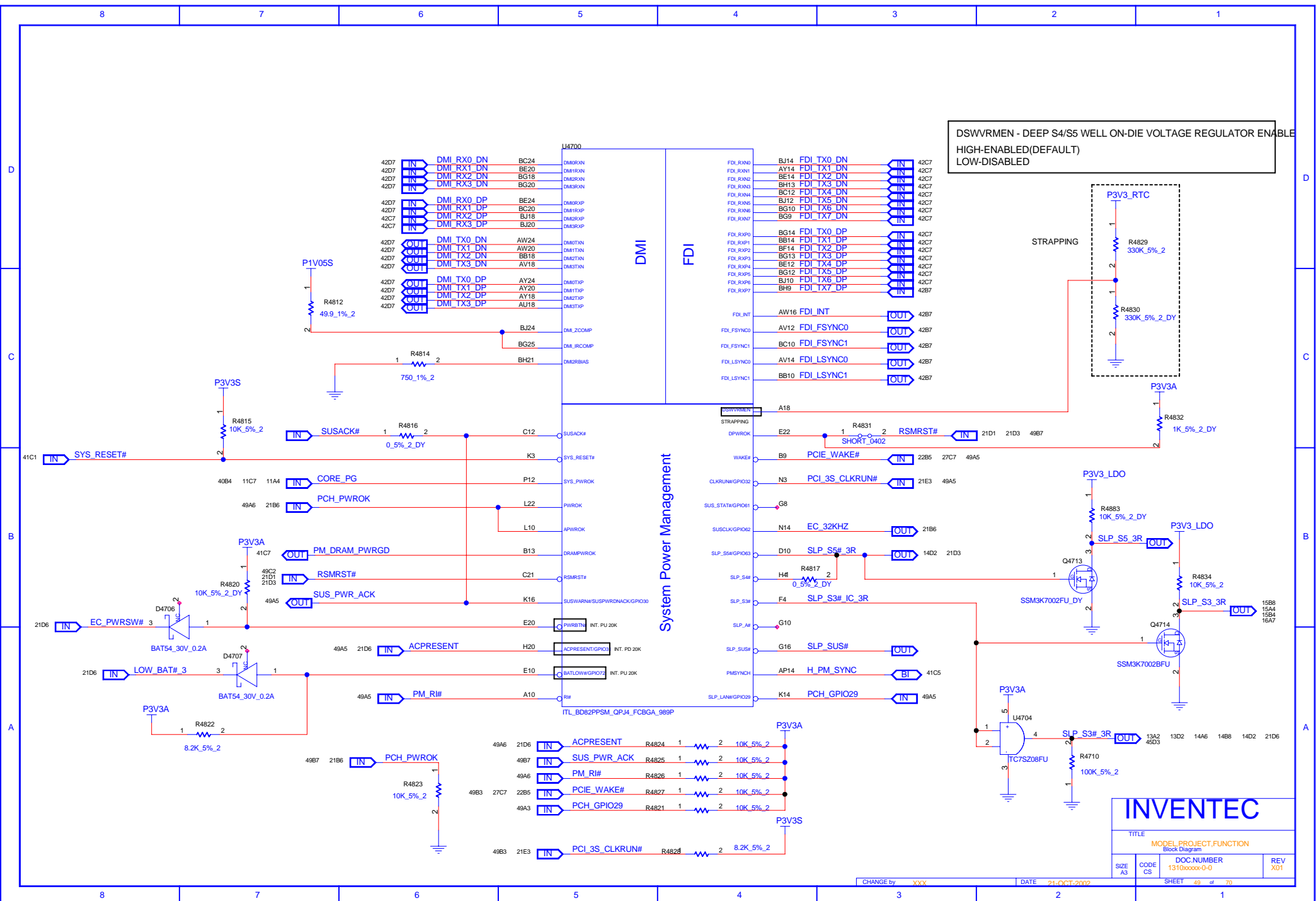
CHANGE by XXX DATE 21-OCT-2002 SHEET 46 of 70

REFERENCE 4700~4949(PCH)



ITL_BD82PPSM_OPJ4_FCBGA_989P

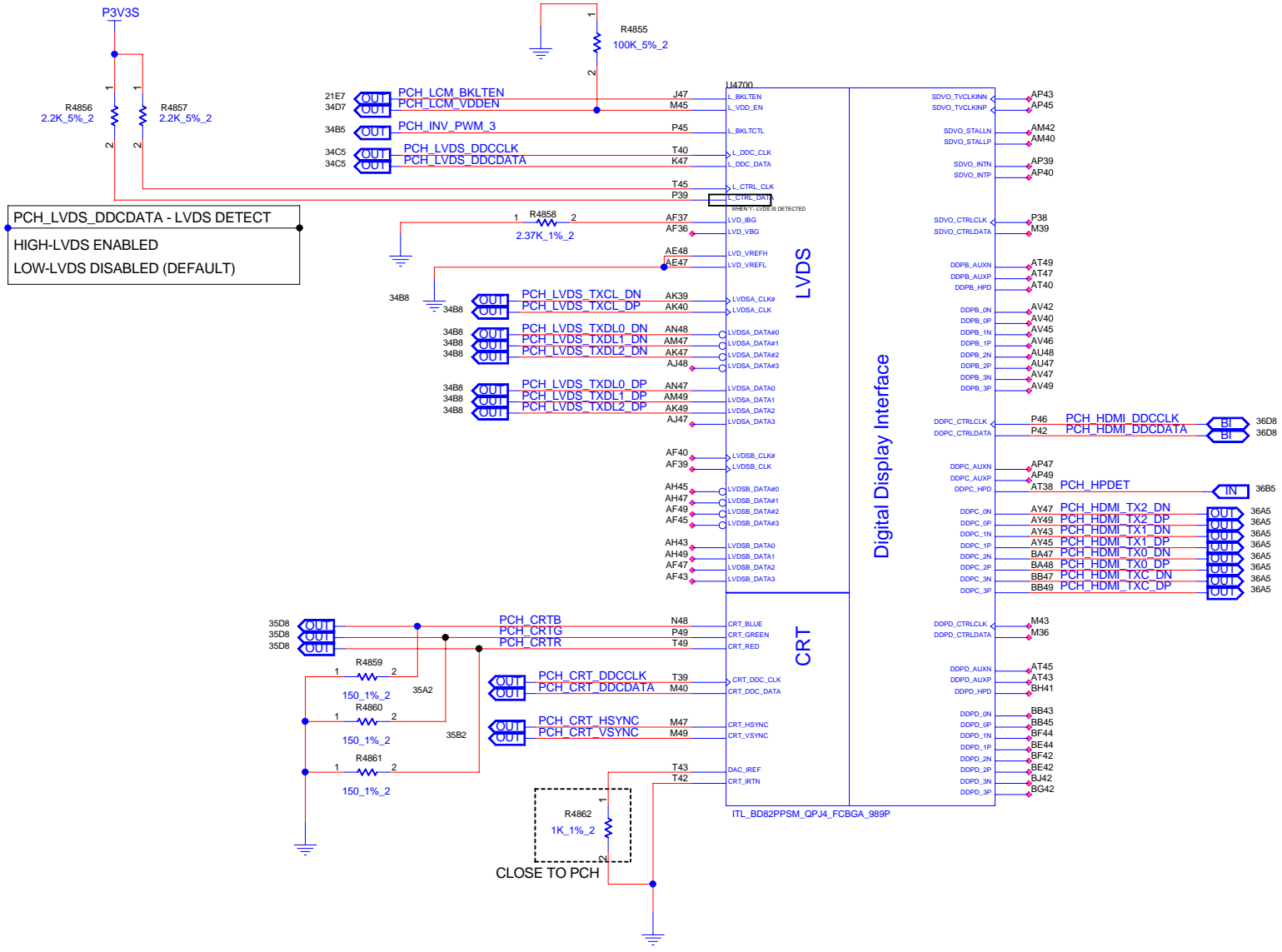
INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
DOC NUMBER			
1310xxxxx-0-0			
SIZE	CODE	REV	
A3	CS	X01	



DSWVRMEN - DEEP S4/S5 WELL ON-DIE VOLTAGE REGULATOR ENABLE
HIGH-ENABLED(DEFAULT)
LOW-DISABLED

System Power Management

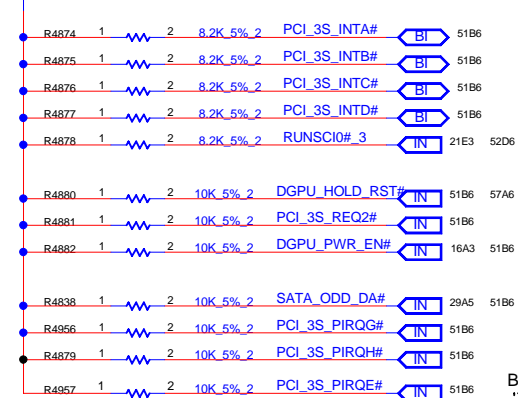
INVENTEC			
TITLE			
MODEL PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-U-0	X01
CHANGE by XXX		DATE 21-OCT-2002	
SHEET 49		of 70	



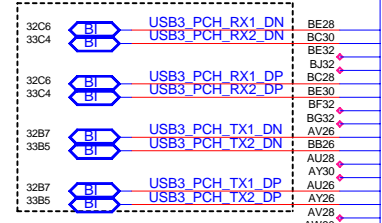
INVENTEC			
TITLE			
MODEL PROJECT FUNCTION Block Diagram			
SIZE A3		CODE CS	
DOC NUMBER 1310xxxxx-0-0		REV X01	
CHANGE by XXX		DATE 21-OCT-2002	
SHEET 50 of 70			

GPIO51 BBS_BIT1	GPIO19 BBS_BIT0	BOOT BIOS DESTINATION
0	1	RESERVED(NAND)
1	0	-----
1	1	SPI (DEFAULT)
0	0	LPC

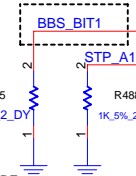
P3V3S



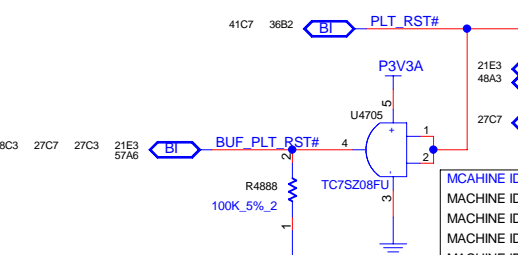
ROUTE WITH 90 OHMS IMPEDANCE
TOTAL LENGTH NO LONGER THAN 11 INCHES



BBS STRAPING



LOW=A16 SWAP OVERRIDE
STP_A160VR
TOP-BLOCK SWAP OVERRIDE
HIGH=DEFAULT



MACHINE ID 0: USB ID0
MACHINE ID 1: POWER EXPRESS (YES:1 NO:0)
MACHINE ID 2: UMA:1 / DIS:0
MACHINE ID 3: MAINSTREAM:1 / ENTRY:0
MACHINE ID 4: HDMI:1 / NO HDMI:0
MACHINE ID 5: SLEEP&CHARGE&DOLBY:(YES1 / NO 0)
MACHINE ID 6: USB ID1
MACHINE ID 1_DB : 35W CPU ONLY :1 / 35W&45W CPU:0

USB ID0	USB ID1	USB3.0 X2 / 2.0 X1	USB3.0 X1 / 2.0 X2	USB2.0 X3
1	1	1	1	0
1	0	1	0	1

NOTE:10K_5%(60130B1030ZT)

- BG26 TP1
- BJ26 TP2
- BH25 TP3
- BJ16 TP4
- BG16 TP5
- AH38 TP6
- AH37 TP7
- AK43 TP8
- AK45 TP9
- C18 TP10
- N30 TP11
- H3 TP12
- AH12 TP13
- AM4 TP14
- AM5 TP15
- Y13 TP16
- K24 TP17
- L24 TP18
- AB46 TP19
- AB45 TP20

RSVD

NVRAM

PCI

USB

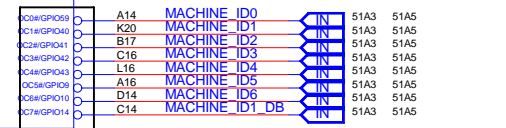
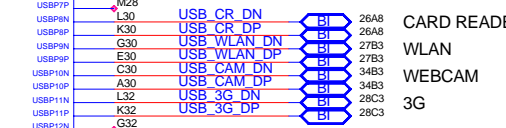
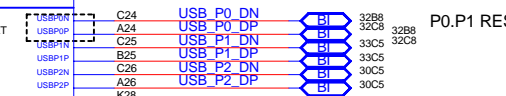
DEBUG PORT

P3V3A

51A5

- RSVD1 AY7
- RSVD2 AV7
- RSVD3 AU3
- RSVD4 BG4
- RSVD5 AT10
- RSVD6 BC8
- RSVD7 AU2
- RSVD8 AT4
- RSVD9 AT3
- RSVD10 AT1
- RSVD11 AY3
- RSVD12 AT5
- RSVD13 AV3
- RSVD14 AV1
- RSVD15 BB1
- RSVD16 BA3
- RSVD17 BB5
- RSVD18 BB3
- RSVD19 BB7
- RSVD20 BE8
- RSVD21 BD4
- RSVD22 BF6
- RSVD23 AV5
- RSVD24 AV10
- RSVD25 AT8
- RSVD26 AY5
- RSVD27 BA2
- RSVD28 AT12
- RSVD29 BF3

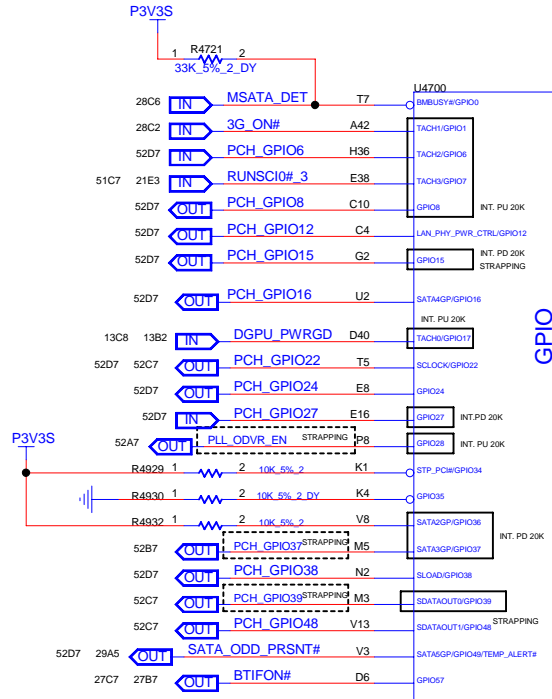
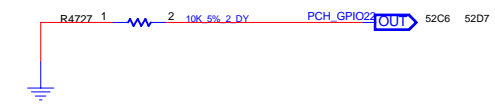
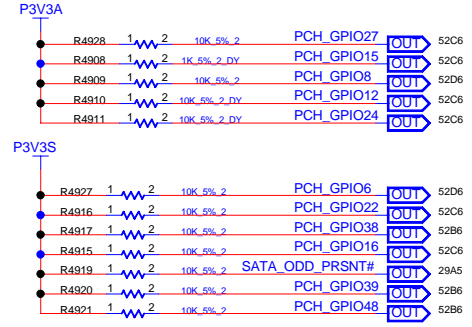
NOTE:
USB2.0/3.0 COMBO-USB2.0 PORT 0,1 MAPPED USB3.0 PORT 1,2



NOTE:10K_5%(60130B1030ZT)

INVENTEC

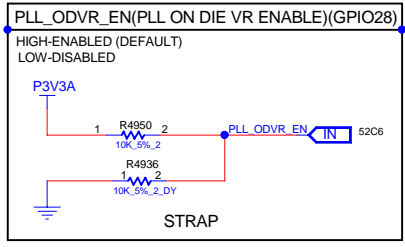
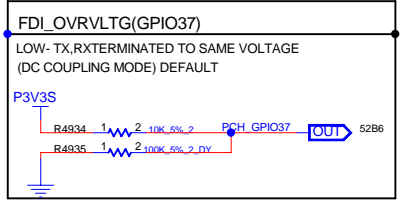
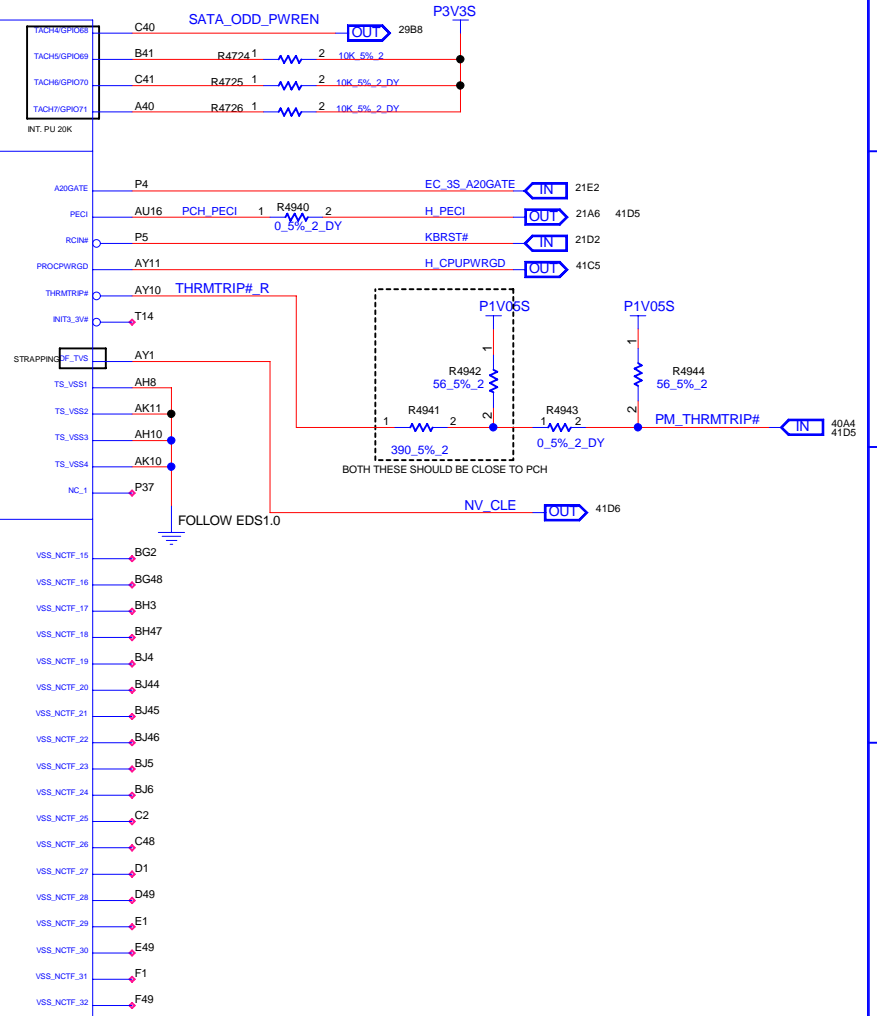
TITLE	MODEL_PROJECT.FUNCTION	REV
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0
SHEET 51 of 70		REV X01



GPIO

NCTF

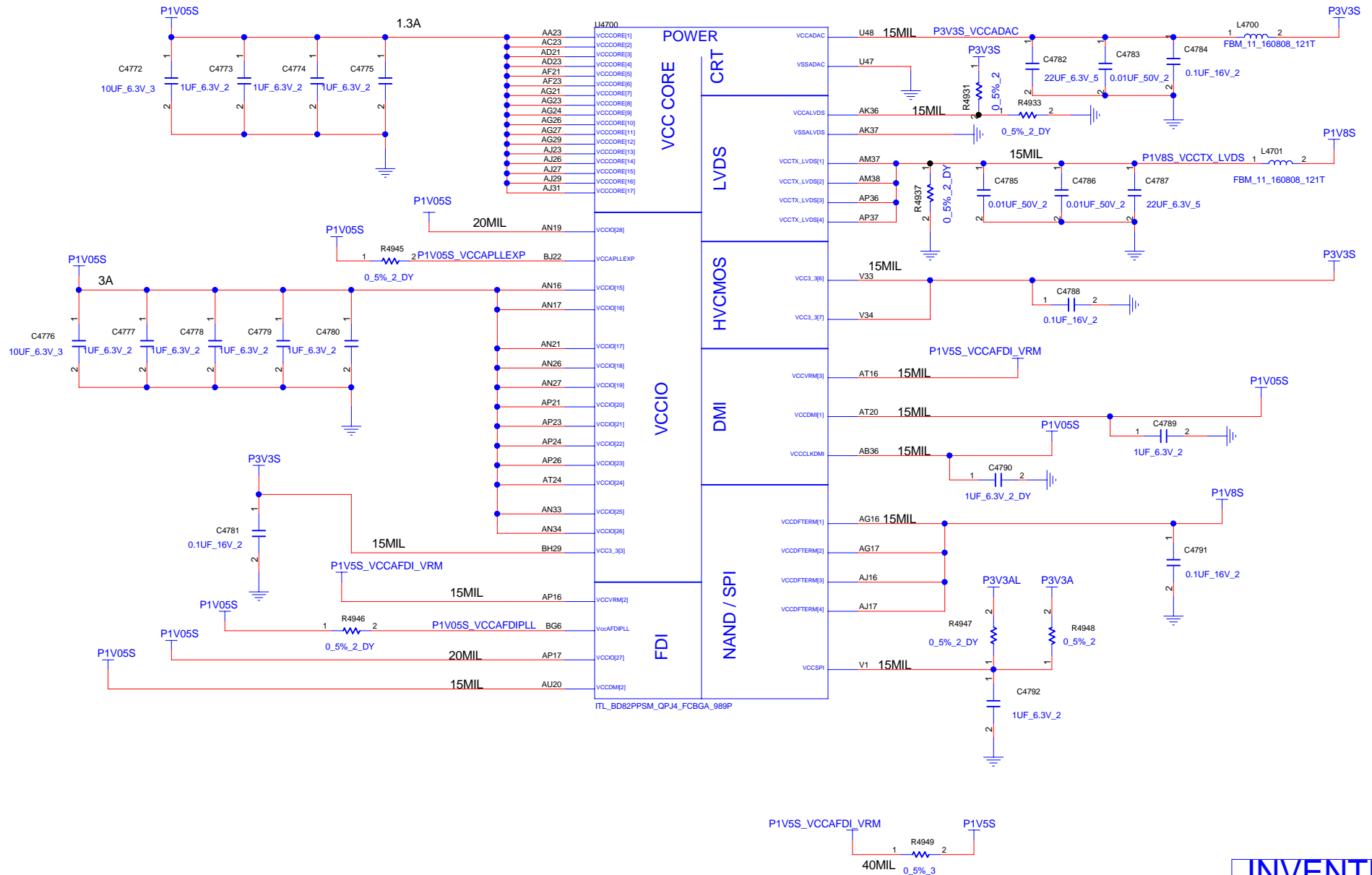
CPU/MISC



INVENTEC

TITLE			
MODEL PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

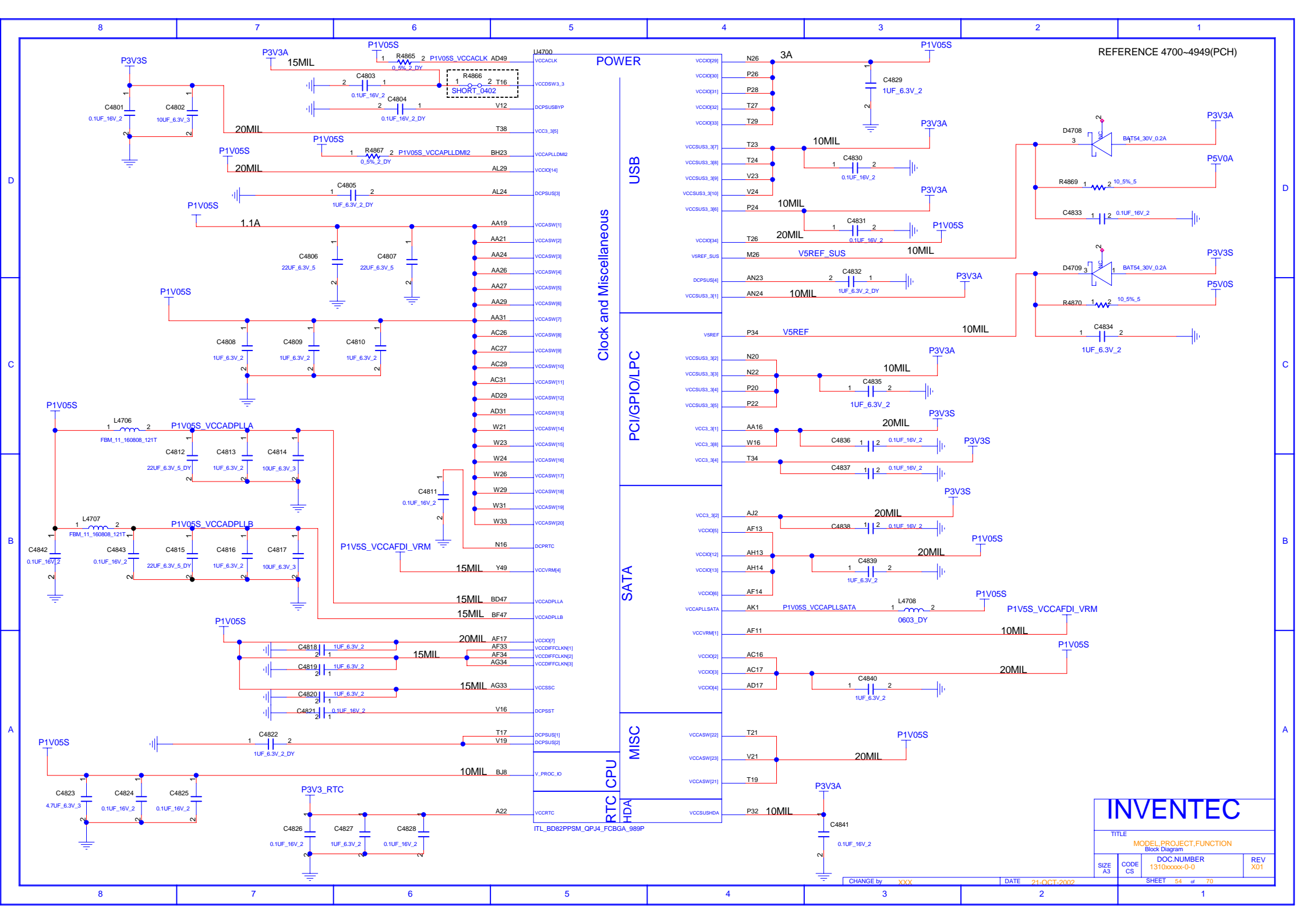
REFERENCE 4700~4949(PCH)



INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01





REFERENCE 4700-4949(PCH)

POWER

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

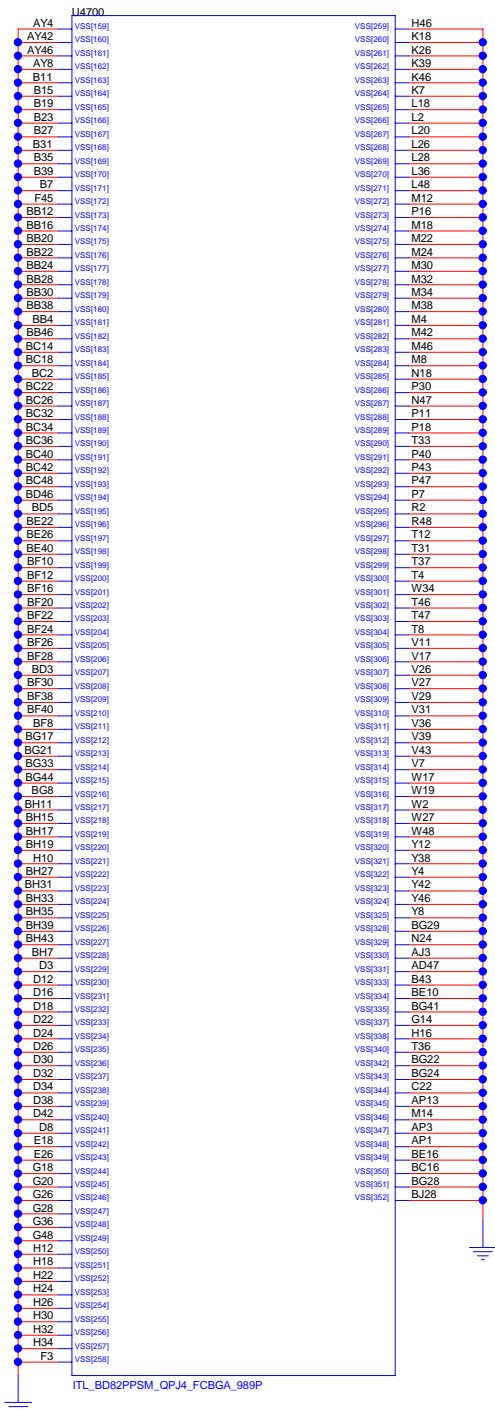
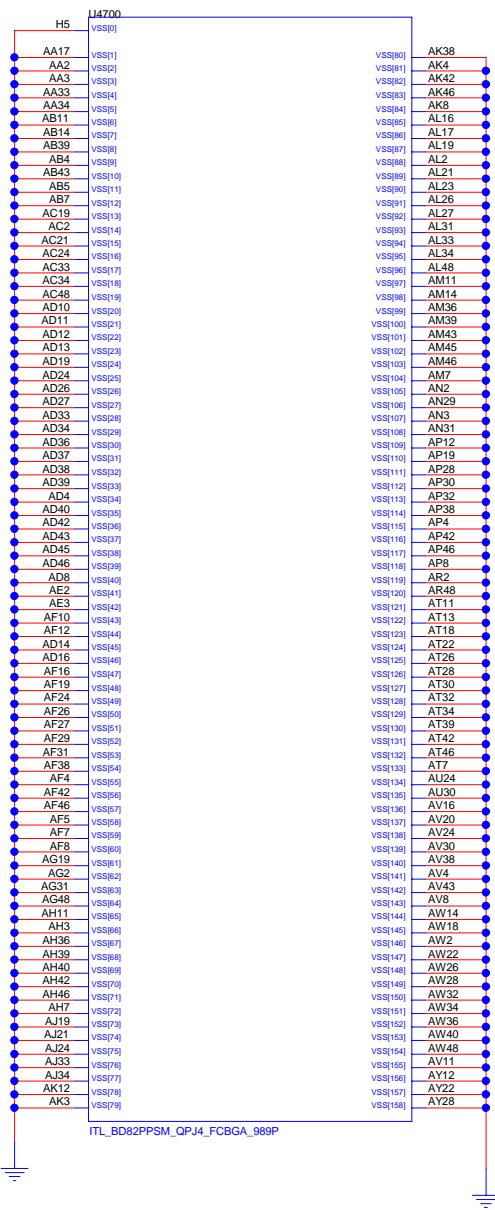
RTC CPU

HDA

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE		DOC NUMBER	
A3	CS	1310xxxx-0-0	REV X01

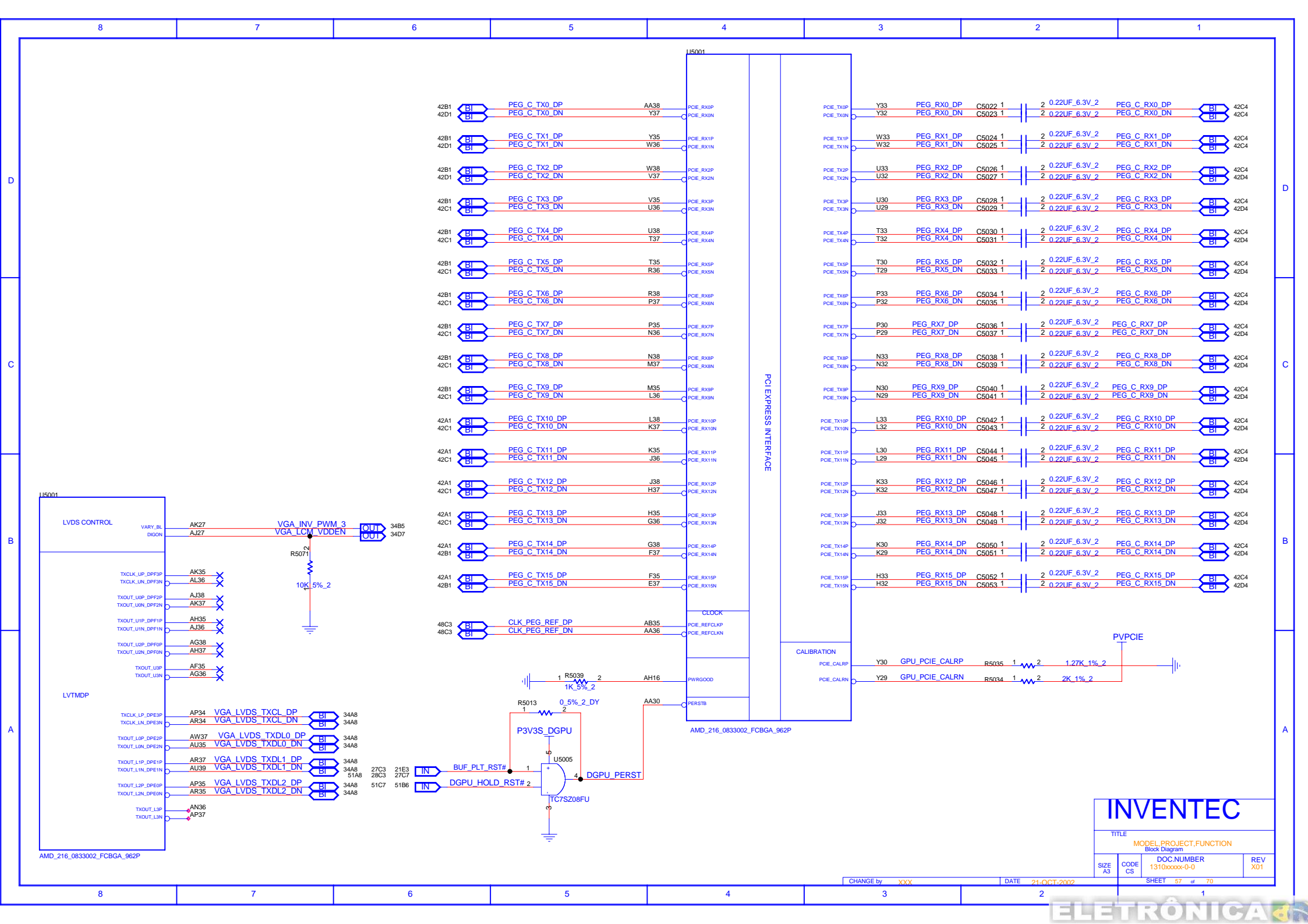
REFERENCE 4700-4949(PCH)



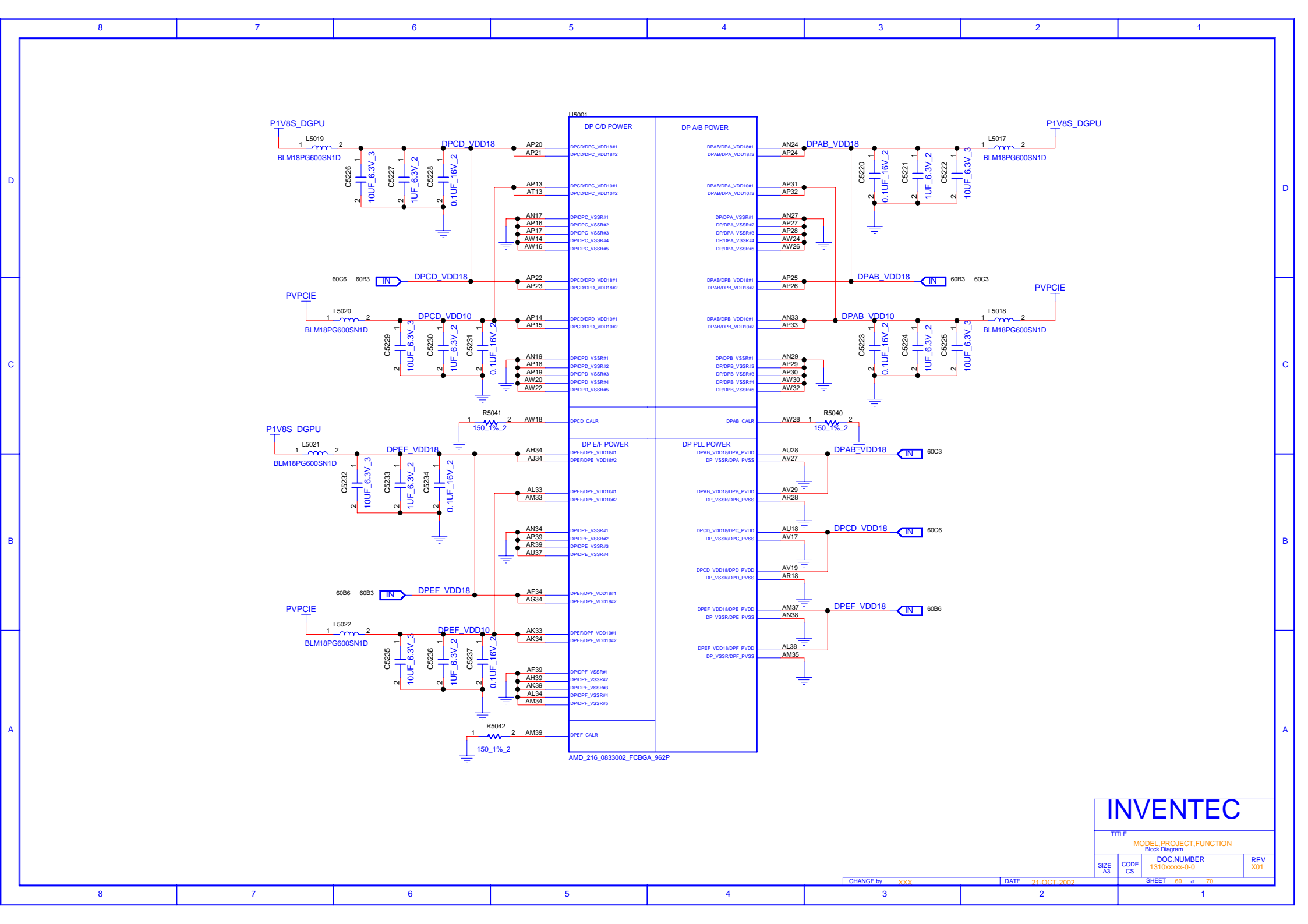
INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01



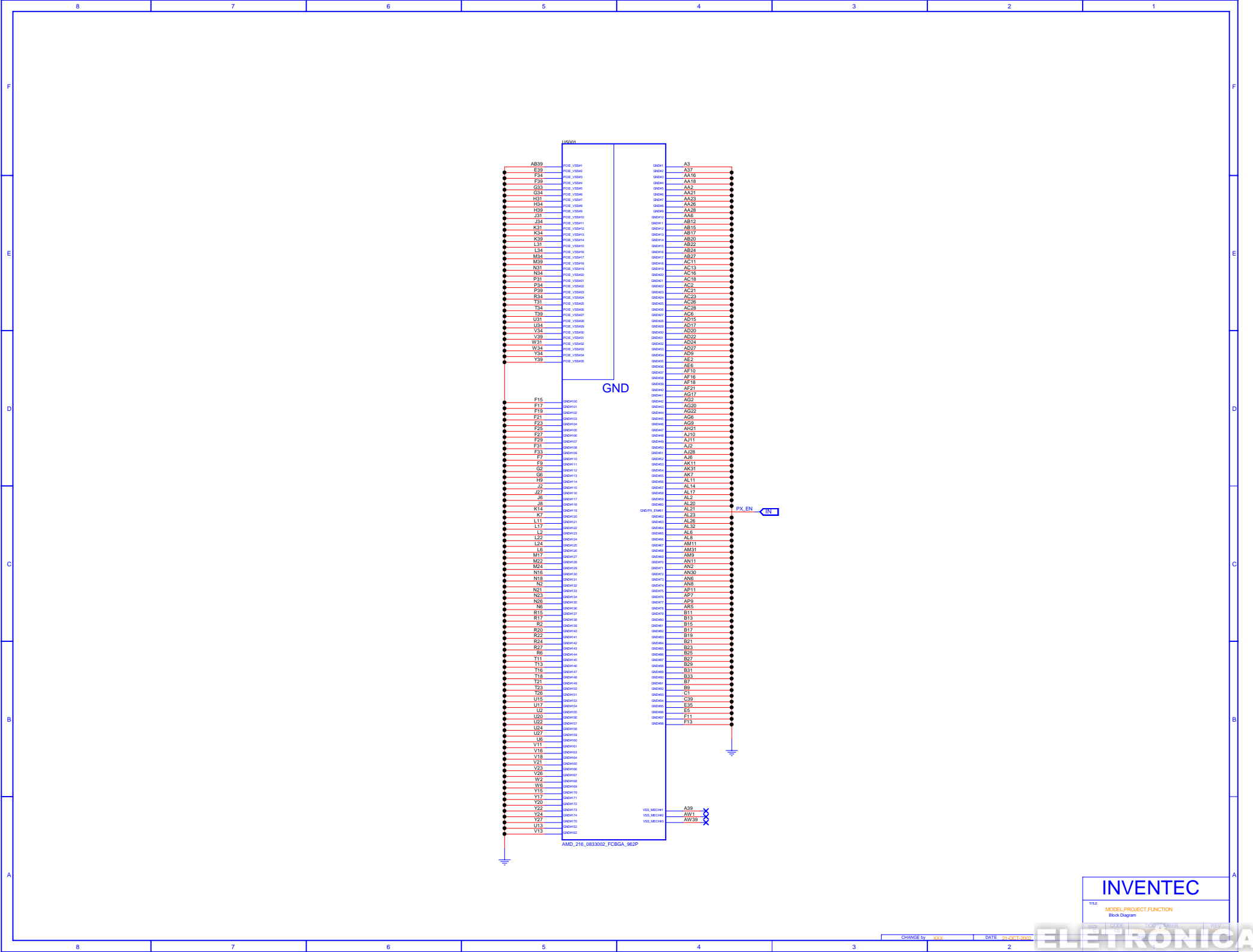


INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 57 of 70



INVENTEC

TITLE			
MODEL PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01



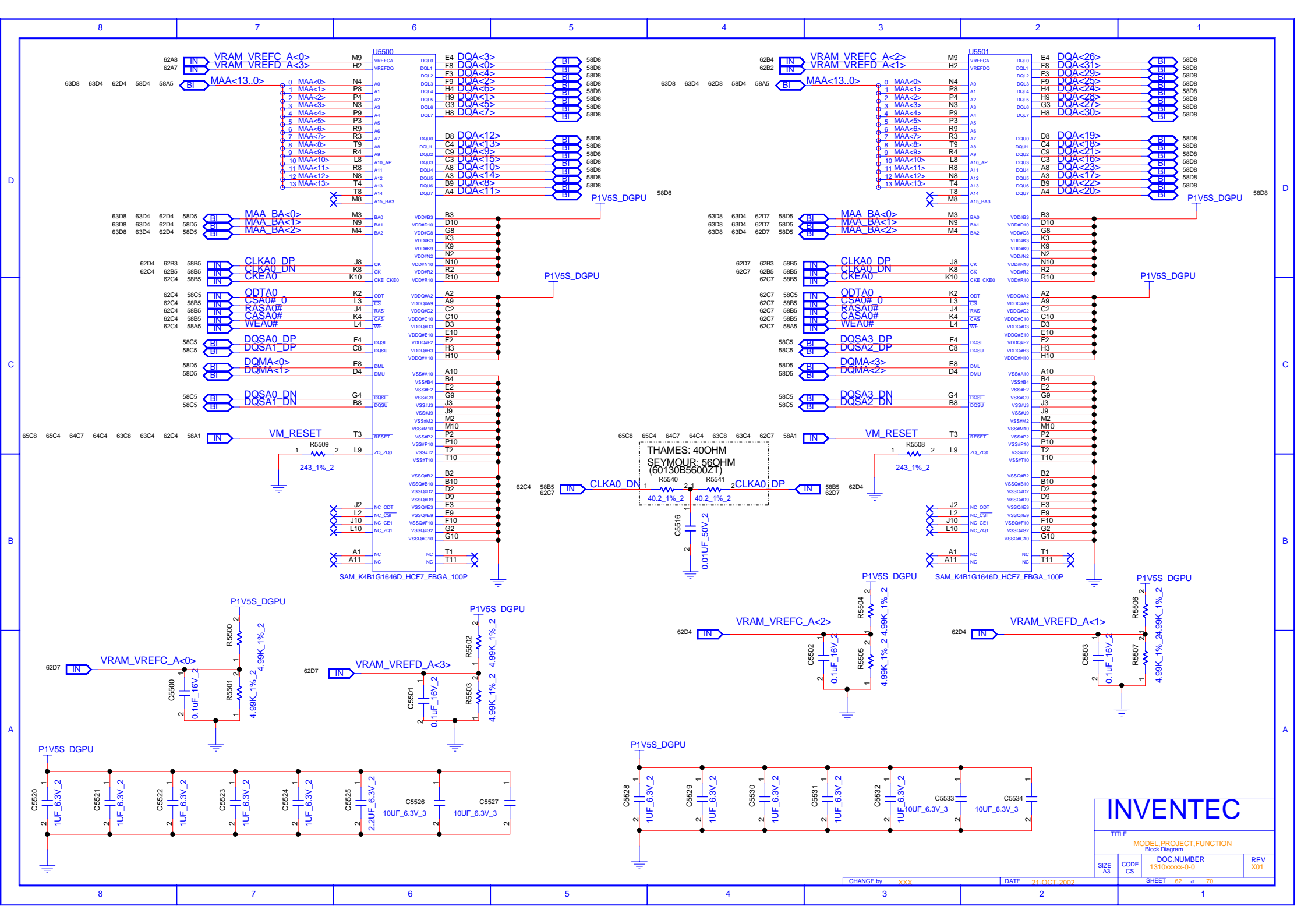
AMD_216_0833002_FCBGA_962P

INVENTEC

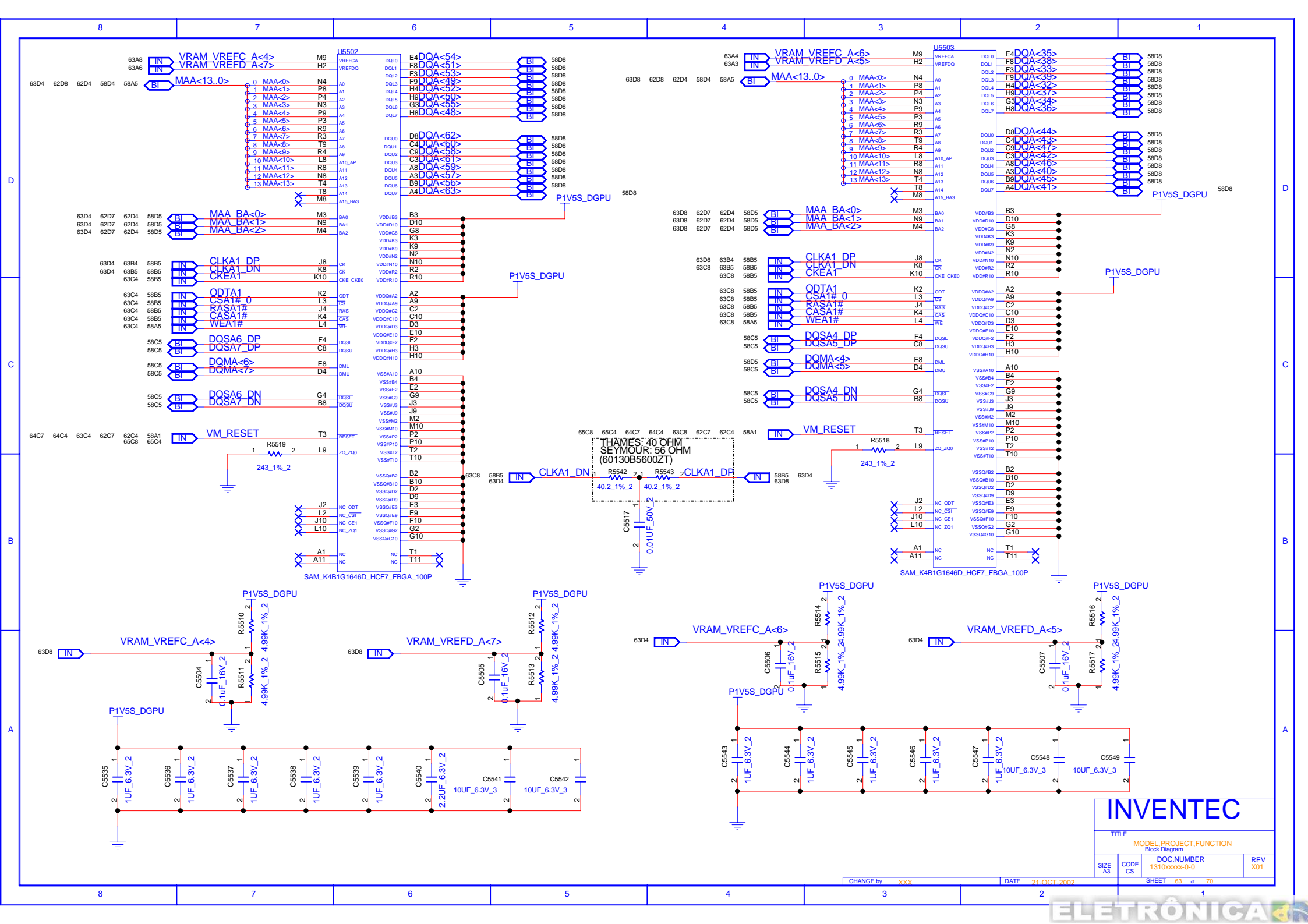
TITLE
MODEL_PROJECT_FUNCTION
Block Diagram

DATE: 21-04-2020



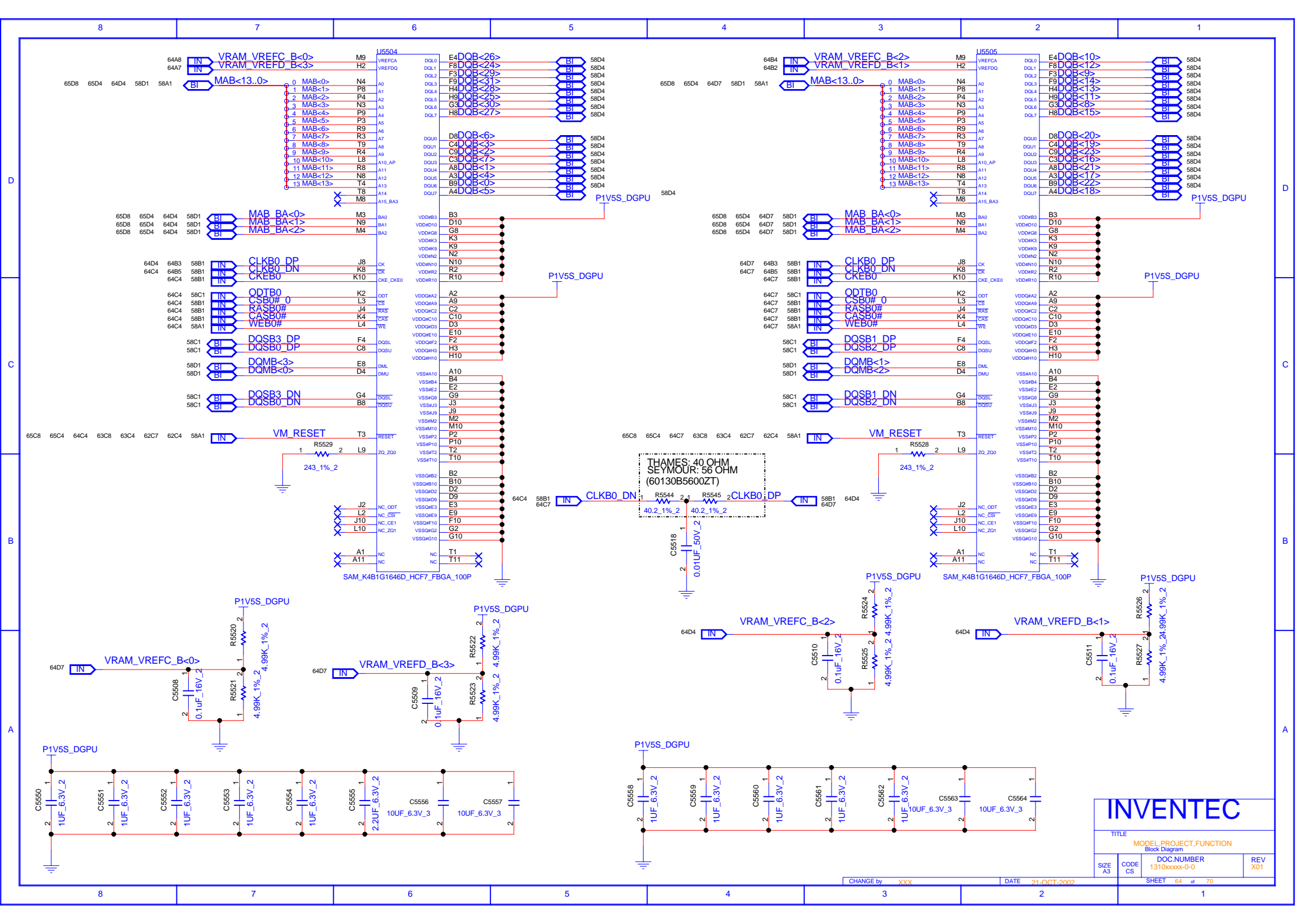


INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 62 of 70

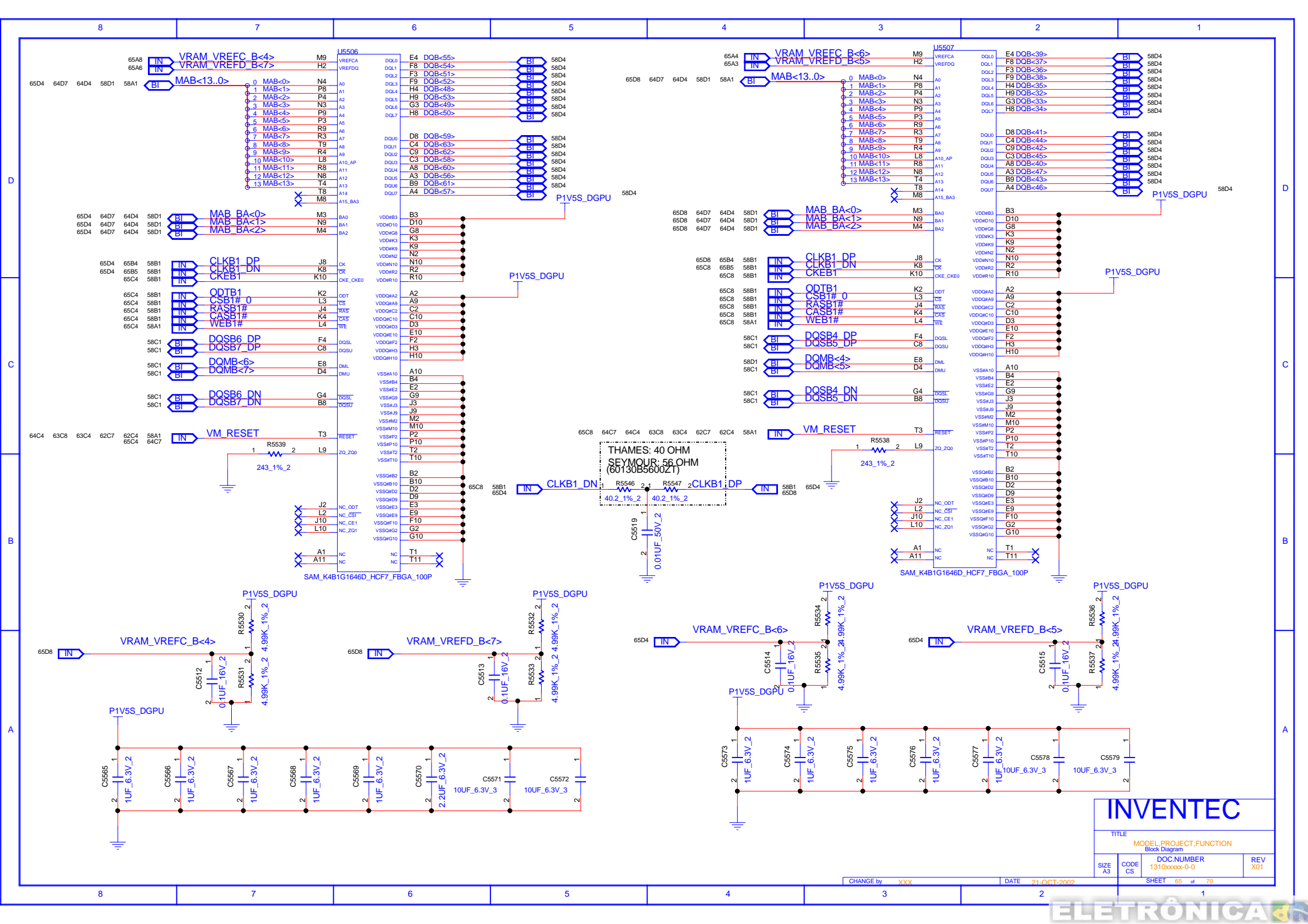


INVENTEC

TITLE			
MODEL PROJECT FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 63 of 70

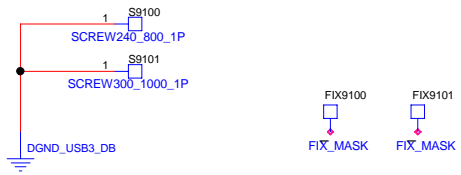
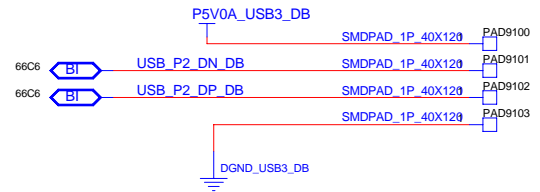
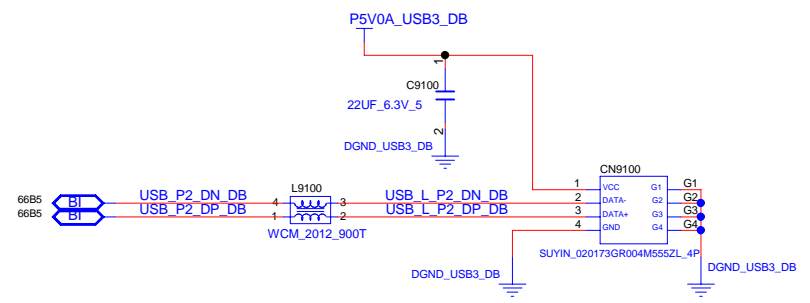


INVENTEC			
TITLE MODEL PROJECT FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 64 of 70



INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	SHEET
XXX		21-OCT-2002	65 of 70

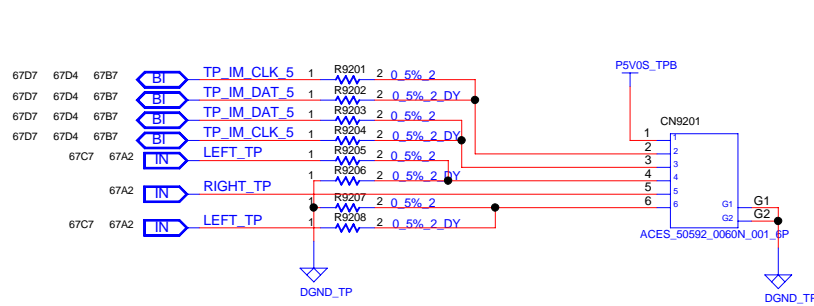
USB BOARD



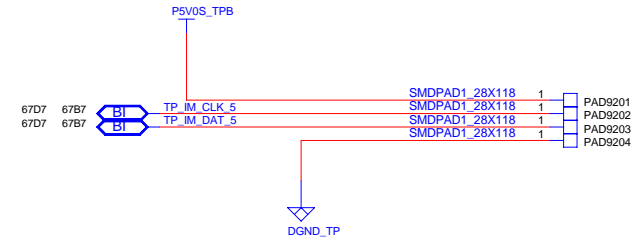
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01

TOUCH PAD BOARD 4 PIN

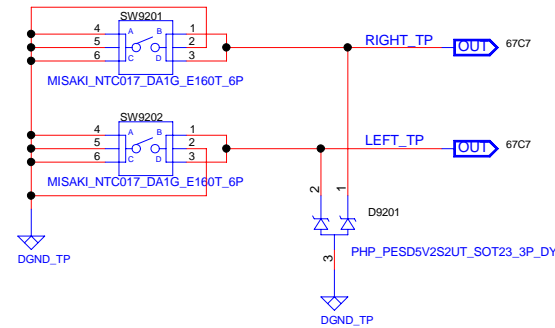
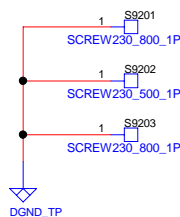
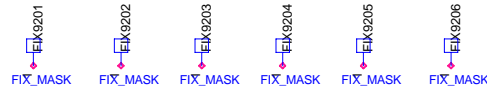
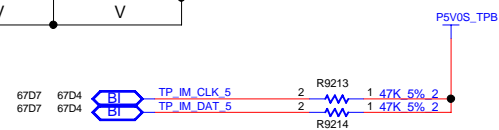
TOUCHPAD TO MODULE CONN



TOUCHPAD TO MB CONN



4PIN	IMR/METAL	TEXTURE
R9201		V
R9202	V	
R9203		V
R9204	V	
R9205		V
R9206	V	
R9207		V
R9208	V	
R9213	V	V
R9214	V	V



INVENTEC

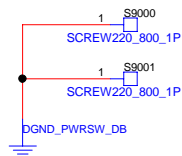
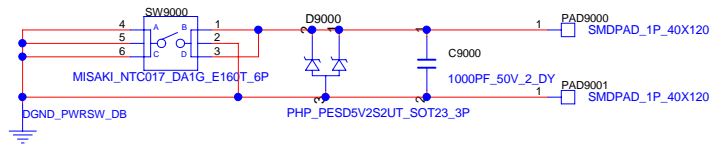
TITLE: MODEL PROJECT.FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002 SHEET 67 of 70

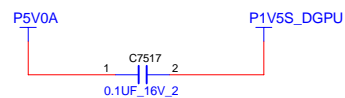
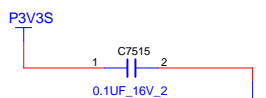
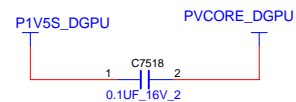
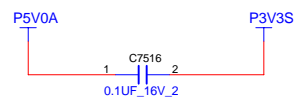
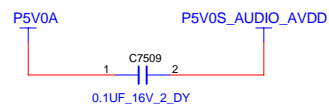
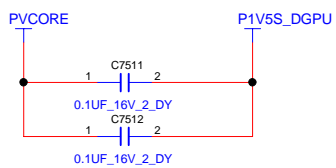
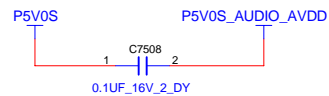
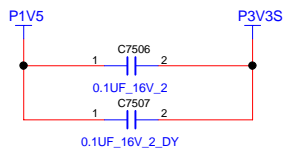
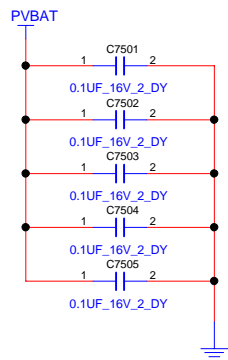
REFERENCE 9000~9999(SMALL BOARD)

POWER BUTTON



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

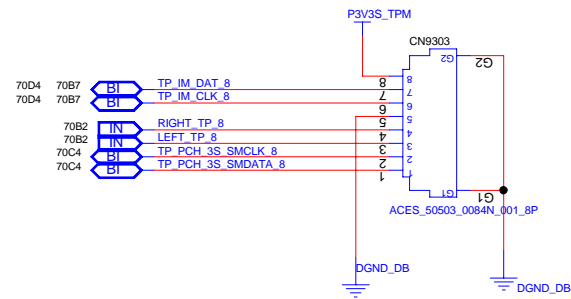


INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01

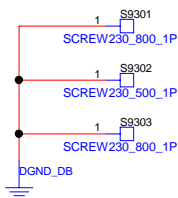
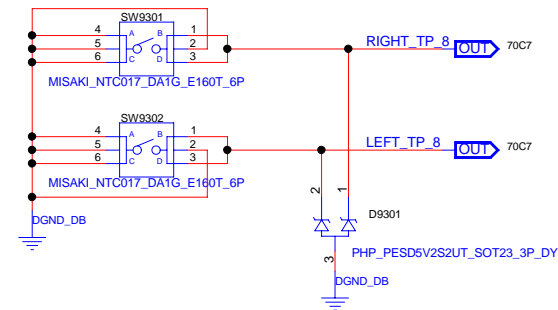
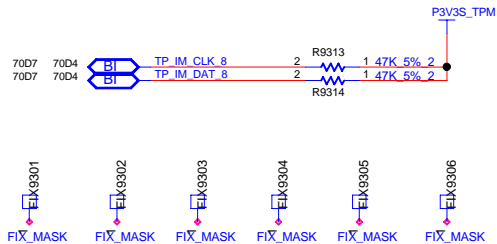
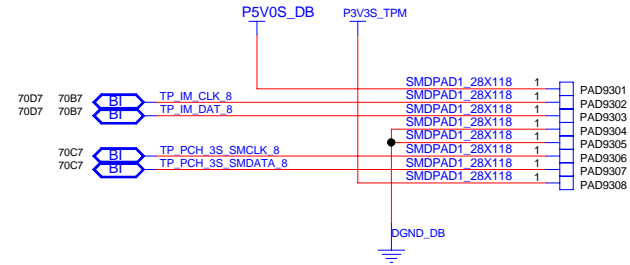


TOUCH PAD BOARD 8 PIN

TOUCHPAD TO MODULE CONN



TOUCHPAD TO MB CONN



INVENTEC

TITLE			
MODEL PROJECT FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01