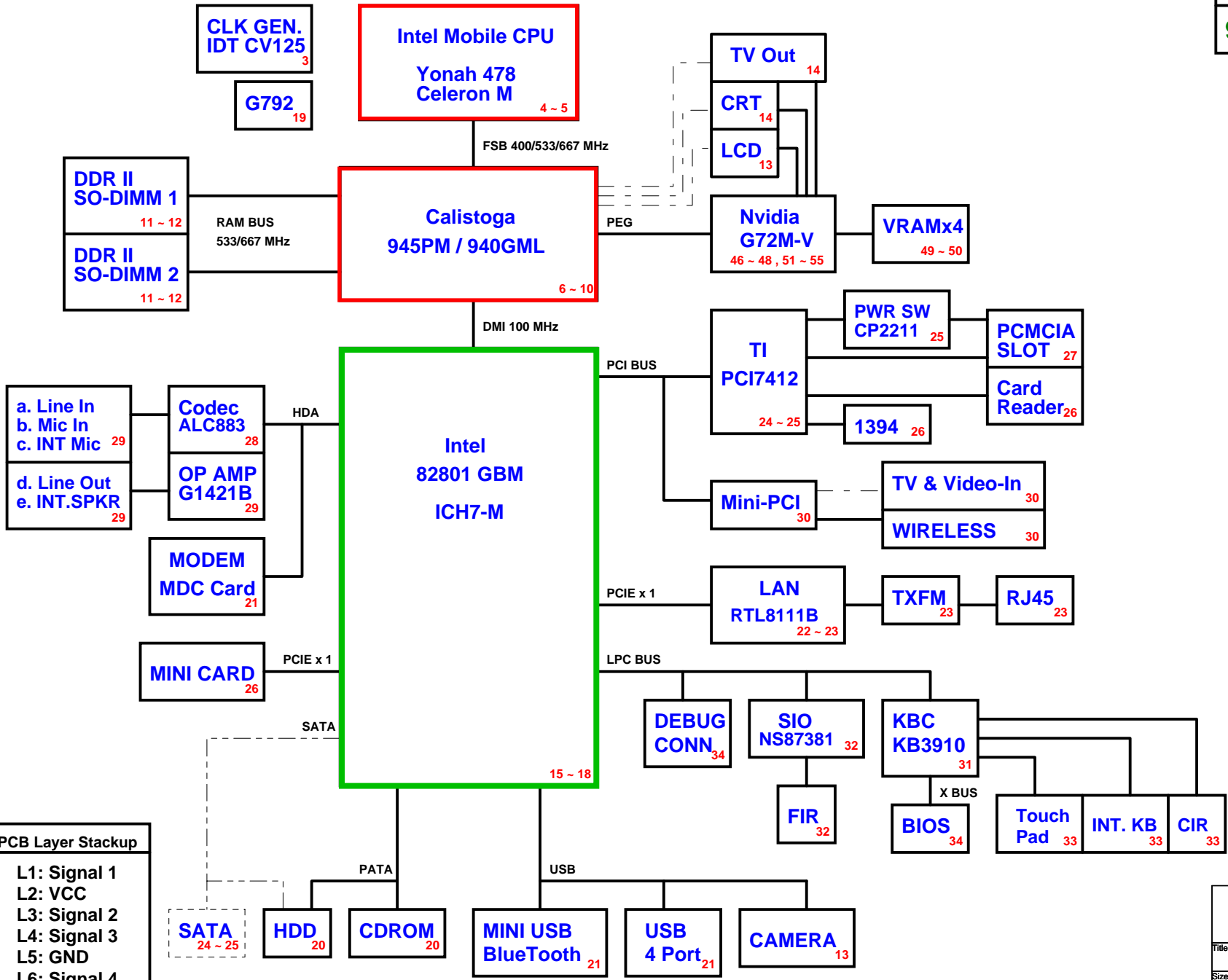


MYALL2 Block Diagram

Project Code	PCB
91.4G901.001	06203-MP



CPU DC/DC ISL6262 37 ~ 38	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

SYSTEM DC/DC MAX8744 35	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

APL5331-KAC APL5912-KAC APL5308-25AC 40	
INPUTS	OUTPUTS
1D5V_S5	1D05V_S0
1D8V_S3	1D5V_S0
3D3V_S5	1D5V_S5
3D3V_S0	2D5V_S0

APW7057-KC TPS51100DGQ APL5331-KAC 41	
INPUTS	OUTPUTS
5V_S5	3D3V_S5
5V_S5	1D8V_S3
5V_S5	0D9V
1D8V_S0	1D2V_S0

CHARGER ISL6255 42	
INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

PCB Layer Stackup	
L1:	Signal 1
L2:	VCC
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	Signal 4

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Title: BLOCK DIAGRAM

Size: Document Number MYALL2 Rev: MP

Date: Tuesday, April 11, 2006 Sheet 1 of 57

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GP017, PME#, LAD[3:0]#/FW[3:0]#, LAN_RXD[2:0]	ICH7 internal 20K pull-ups
LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/GPIO17#, GNT4#/GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+0.25 Center
1	0	0	1	+0.5 Center
1	0	1	0	+0.75 Center
1	0	1	1	+1.0 Center
1	1	0	0	+0.25 Center
1	1	0	1	+0.5 Center
1	1	1	0	+0.75 Center
1	1	1	1	+1.0 Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
7412	22	A->G, B->B, C->F, D->G'	0
MiniPCI	21	A/C B/D -> E E	1

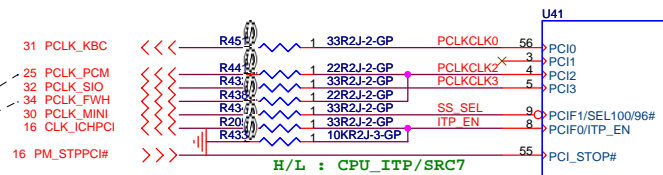
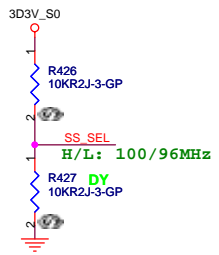
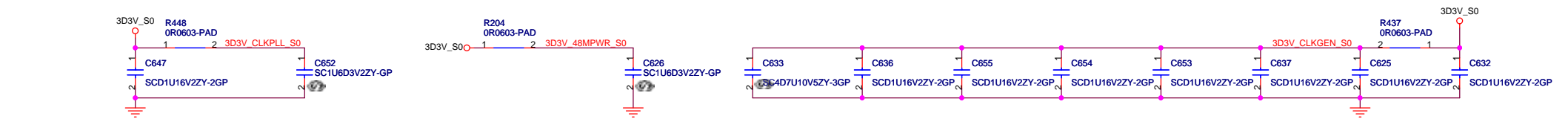
Calistoga Strapping Signals and Configuration

EDS 17050 0.71 page 7

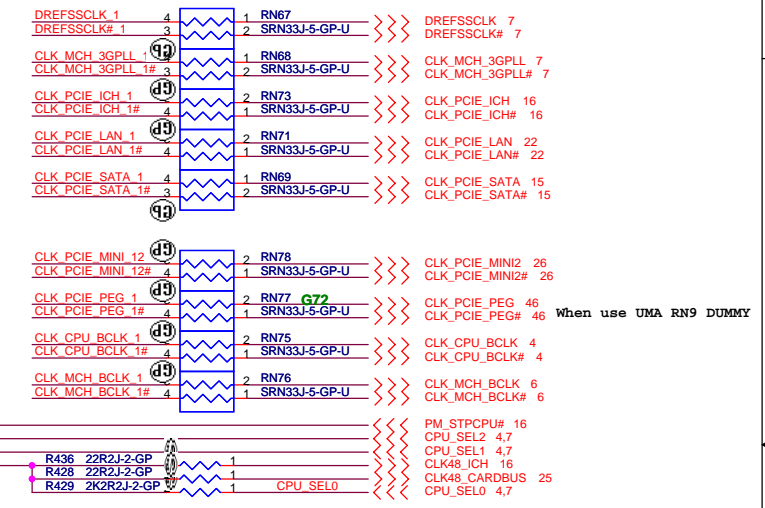
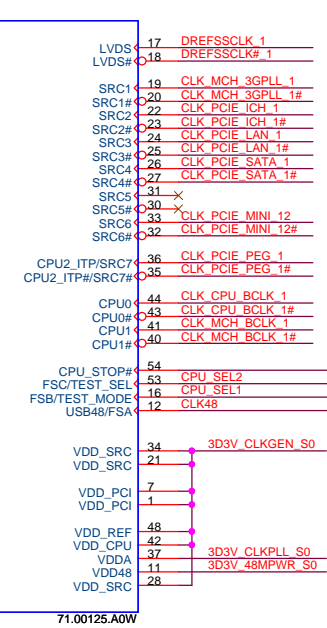
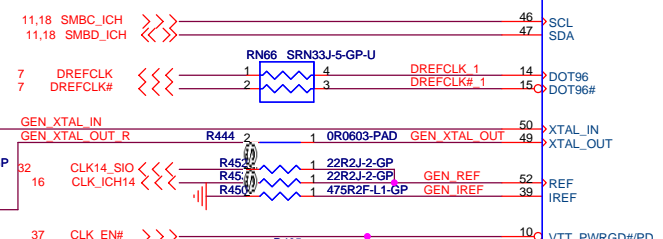
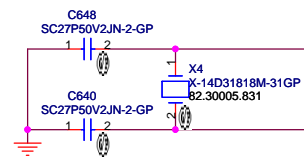
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes, 15->0, 14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane, 4->0, 3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWROK in signal.

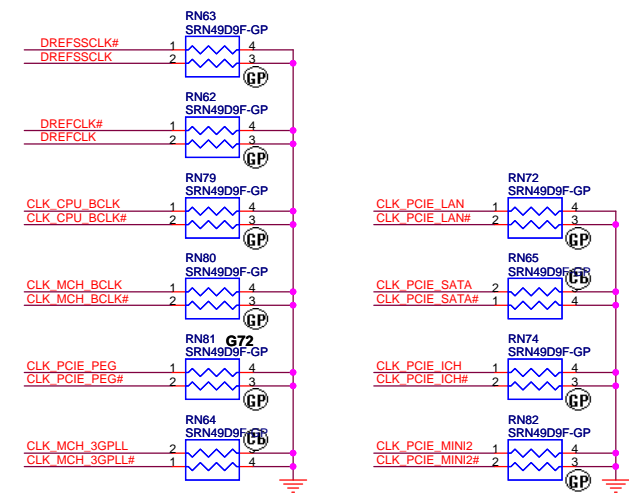
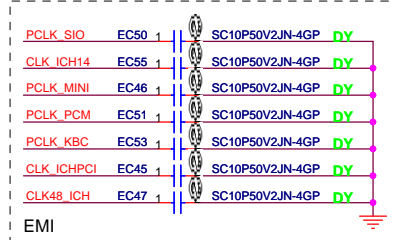
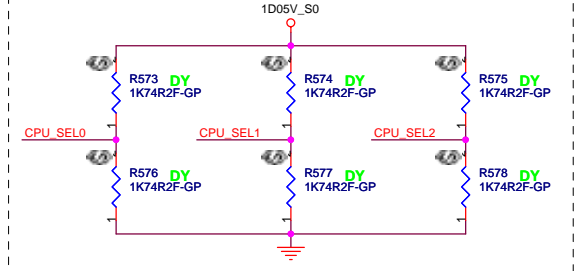
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Reference			
Title	Document Number		Rev
	MYALL2		MP
Date:	Friday, March 24, 2006	Sheet 2 of	57



PClk_FWH & PClk_PCM need equal length



FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	1.33M	533M
0	1	0	200M	X
0	1	1	1.66M	667M
1	0	0	333M	X
1	0	1	1.00M	X
1	1	0	400M	X
1	1	1	Reserved	X

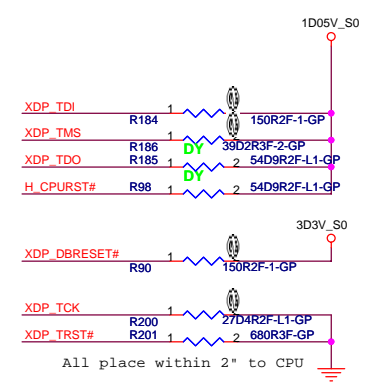
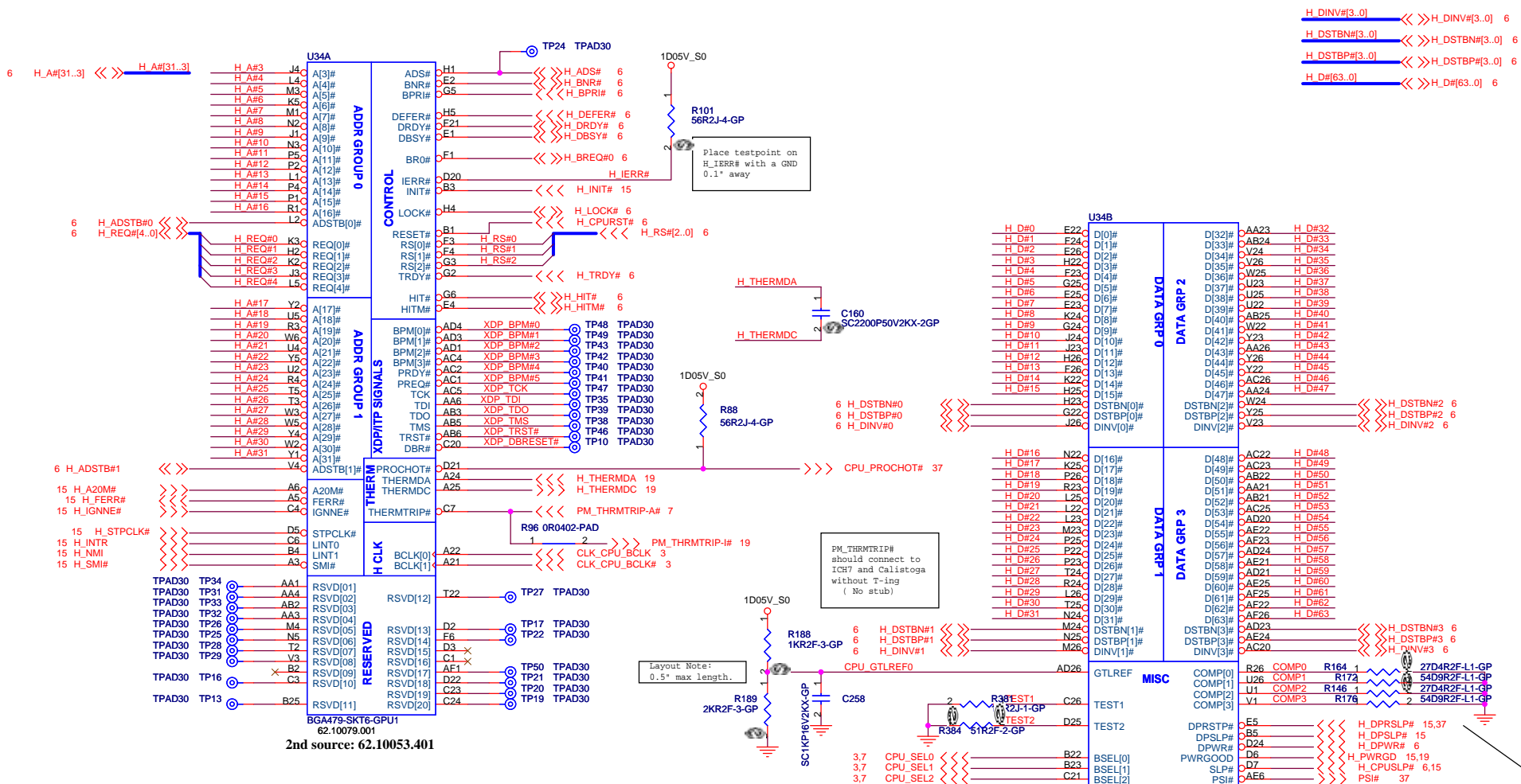


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Title: **Clock Generator ICS954805D**

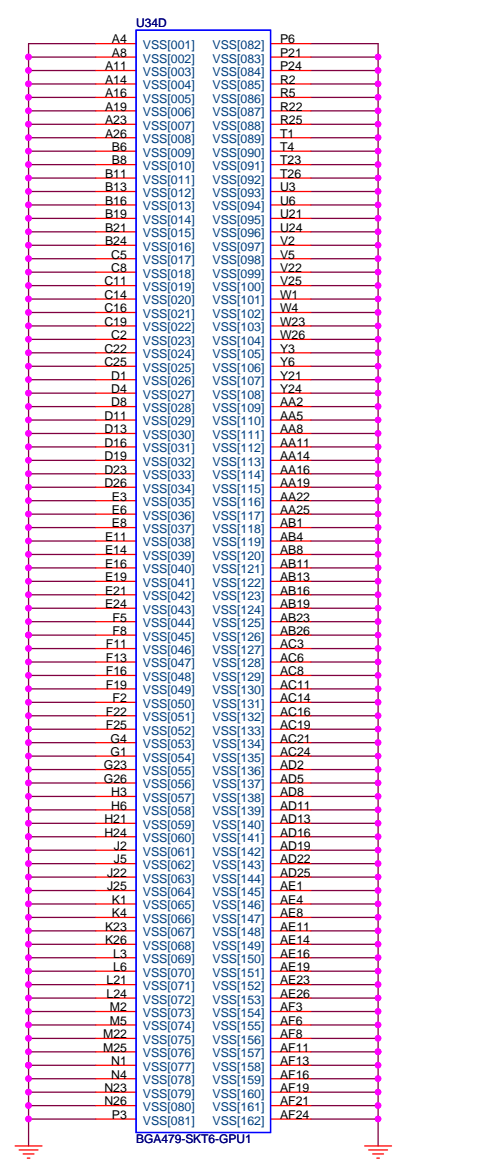
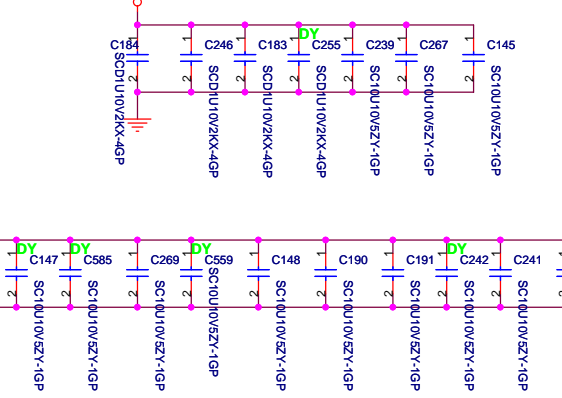
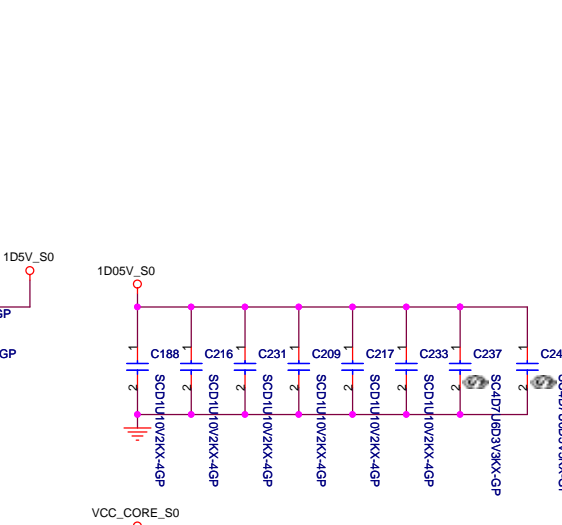
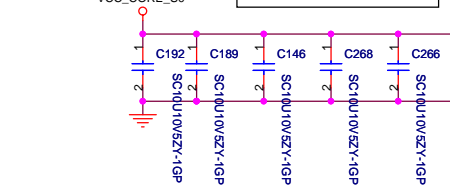
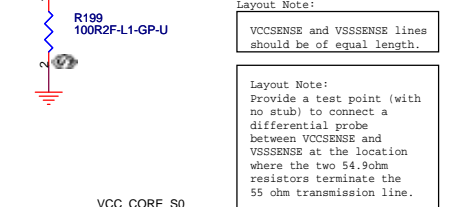
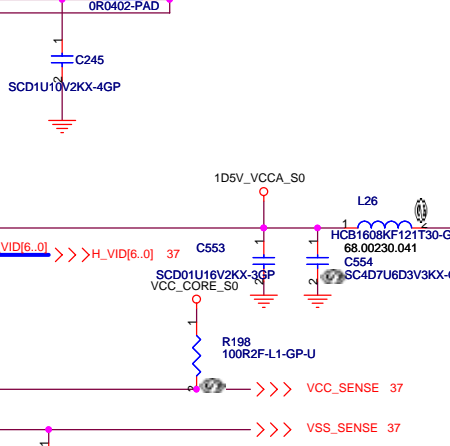
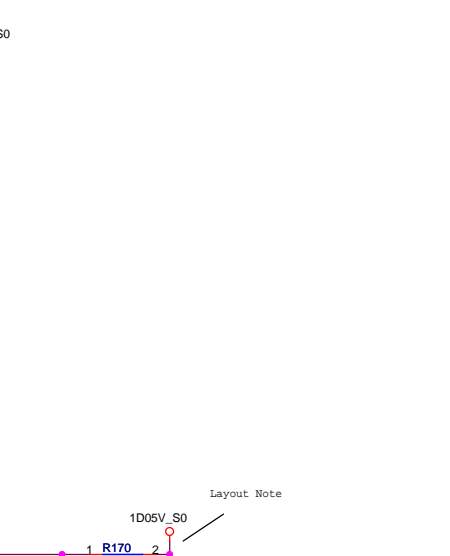
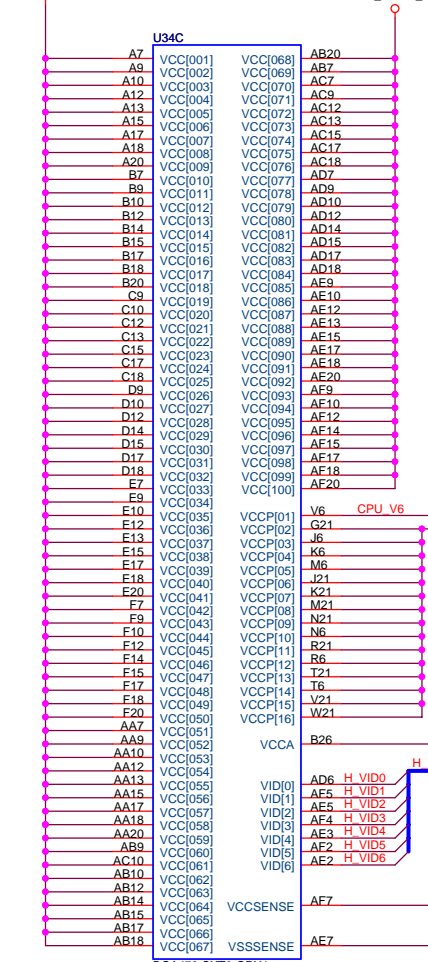
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Date: Thursday, March 30, 2006 Sheet 3 of 57



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VCC_CORE_S0



Layout Note

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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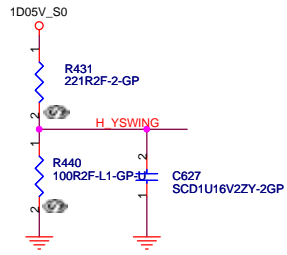
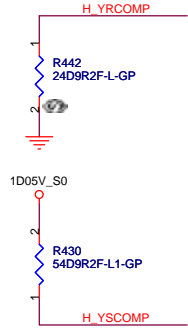
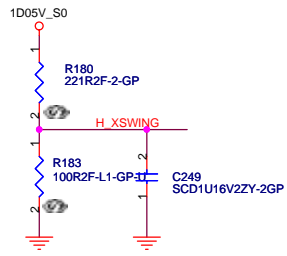
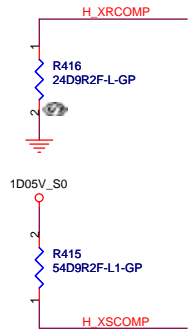
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Sheet 5 of 57



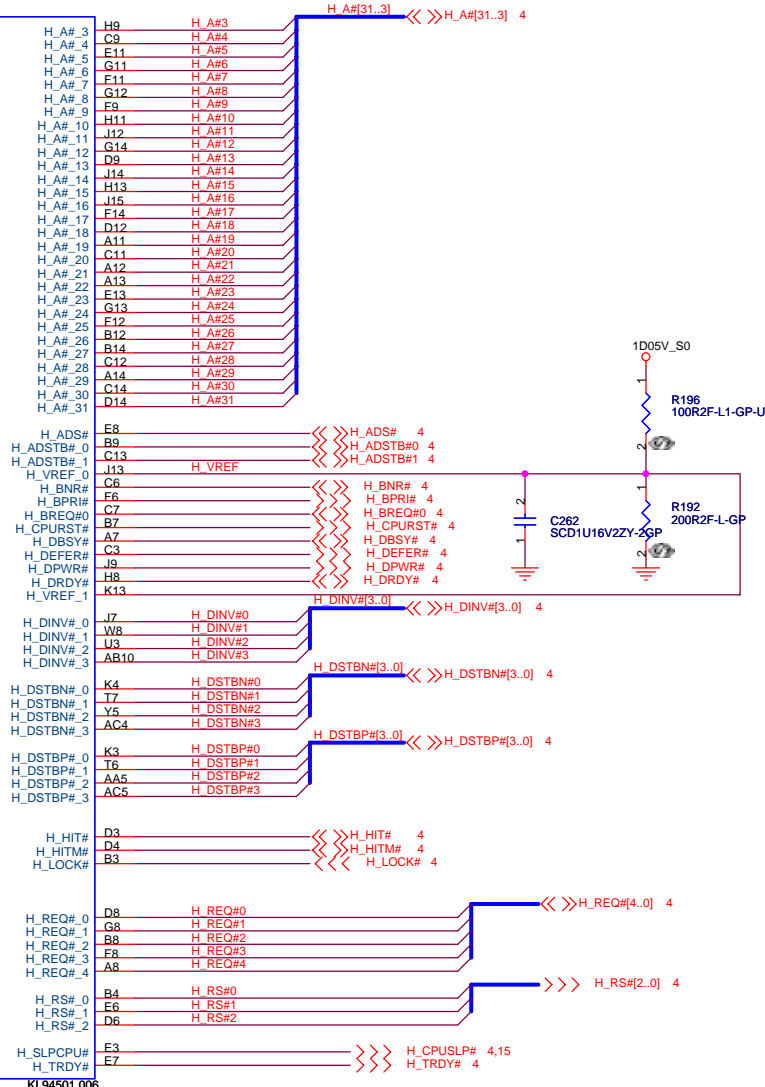
Place them near to the chip (< 0.5")

3 CLK_MCH_BCLK
3 CLK_MCH_BCLK#

H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G1	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	K7	H_D#_10
H_D#11	J8	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	J3	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W9	H_D#_23
H_D#24	T1	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T5	H_D#_31
H_D#32	AB7	H_D#_32
H_D#33	AA9	H_D#_33
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H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	Y10	H_D#_39
H_D#40	AB8	H_D#_40
H_D#41	W2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA7	H_D#_43
H_D#44	AA2	H_D#_44
H_D#45	AA6	H_D#_45
H_D#46	AA10	H_D#_46
H_D#47	Y8	H_D#_47
H_D#48	AA1	H_D#_48
H_D#49	AB4	H_D#_49
H_D#50	AC9	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC6	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63
H_XRCOMP	E1	H_XRCOMP
H_XSCOMP	E2	H_XSCOMP
H_XSWING	E4	H_XSWING
H_YRCOMP	Y1	H_YRCOMP
H_YSCOMP	U1	H_YSCOMP
H_YSWING	W1	H_YSWING
H_CLKIN	AG2	H_CLKIN
H_CLKIN#	AG1	H_CLKIN#

U39A
CALISTOGA
KI.94501.006

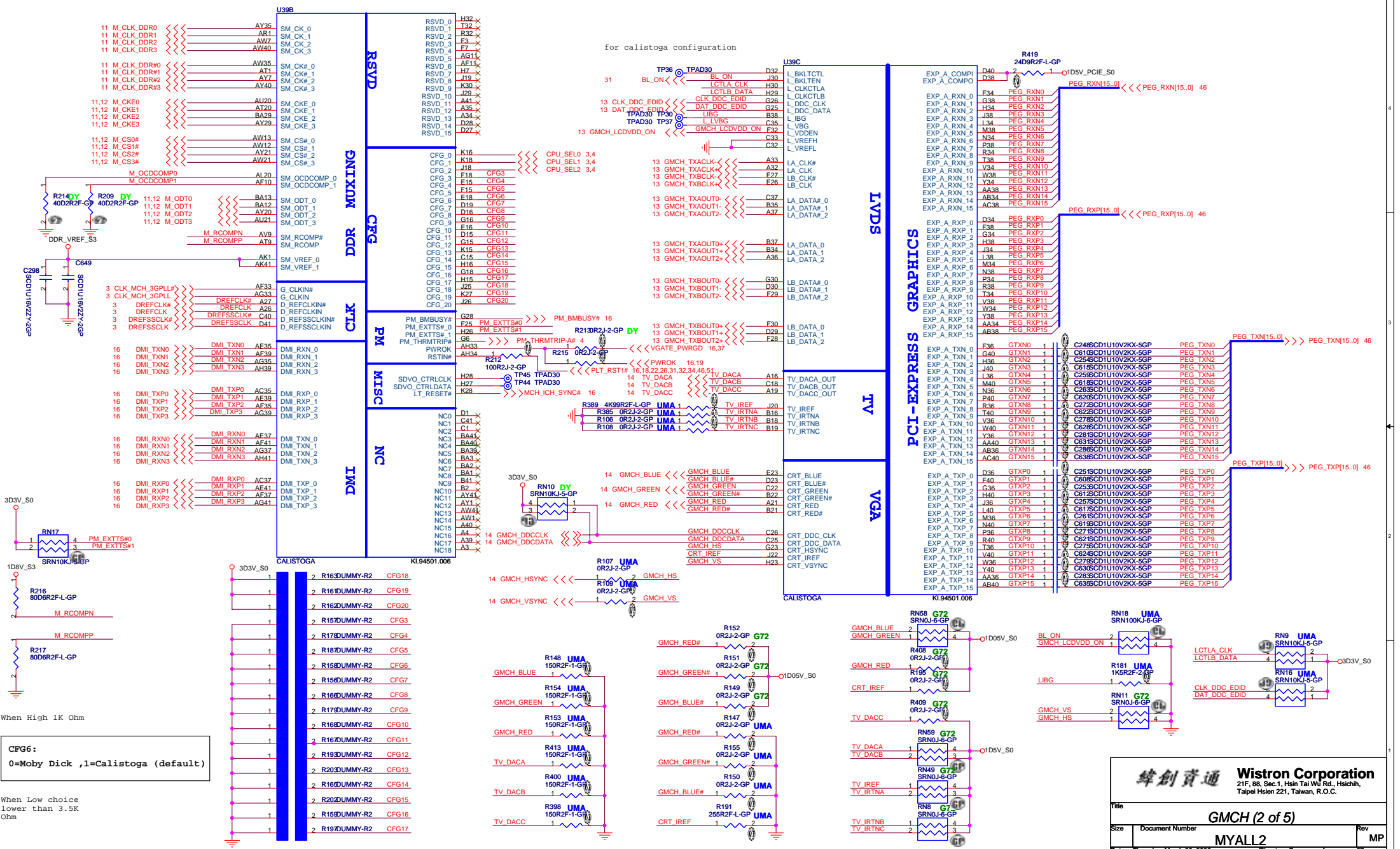
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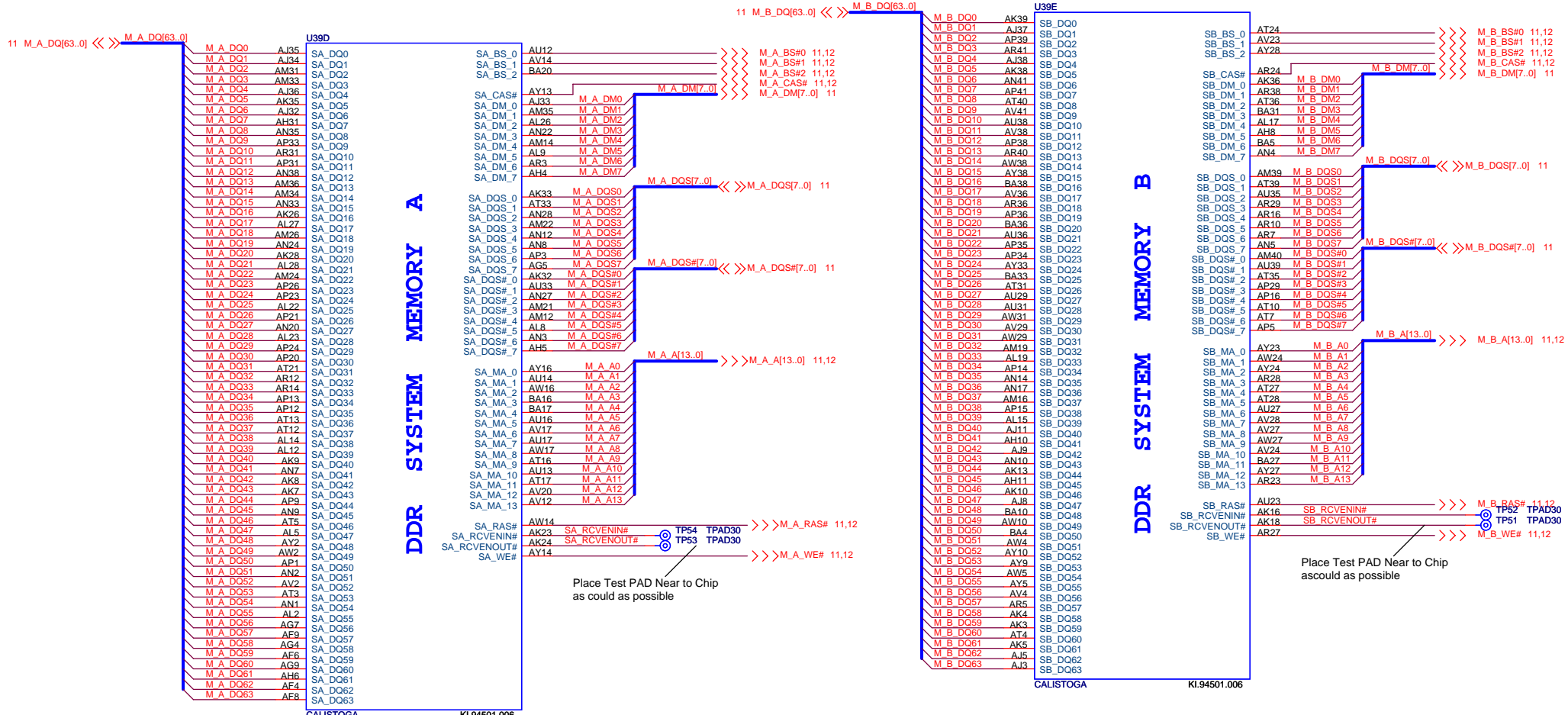
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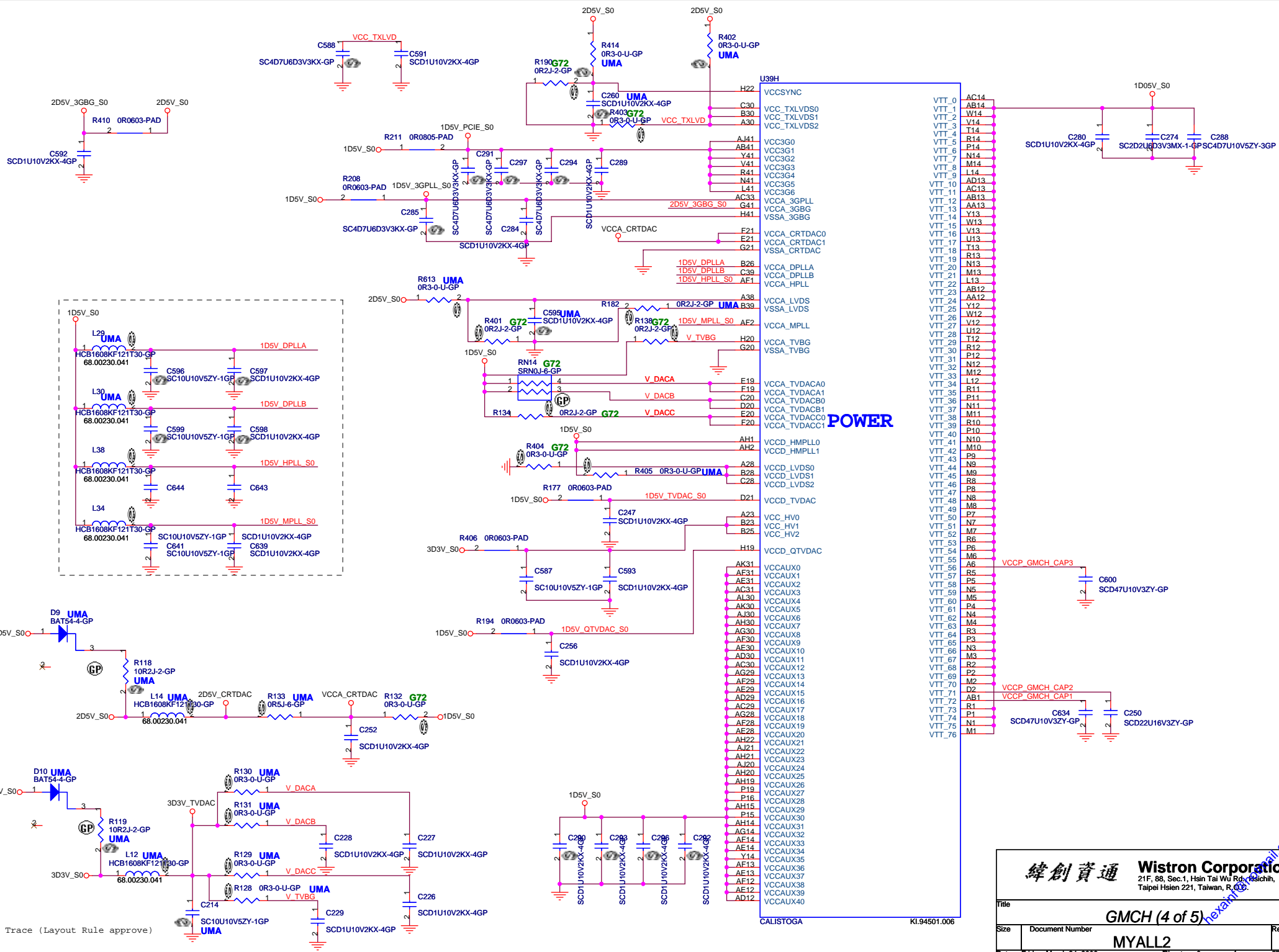


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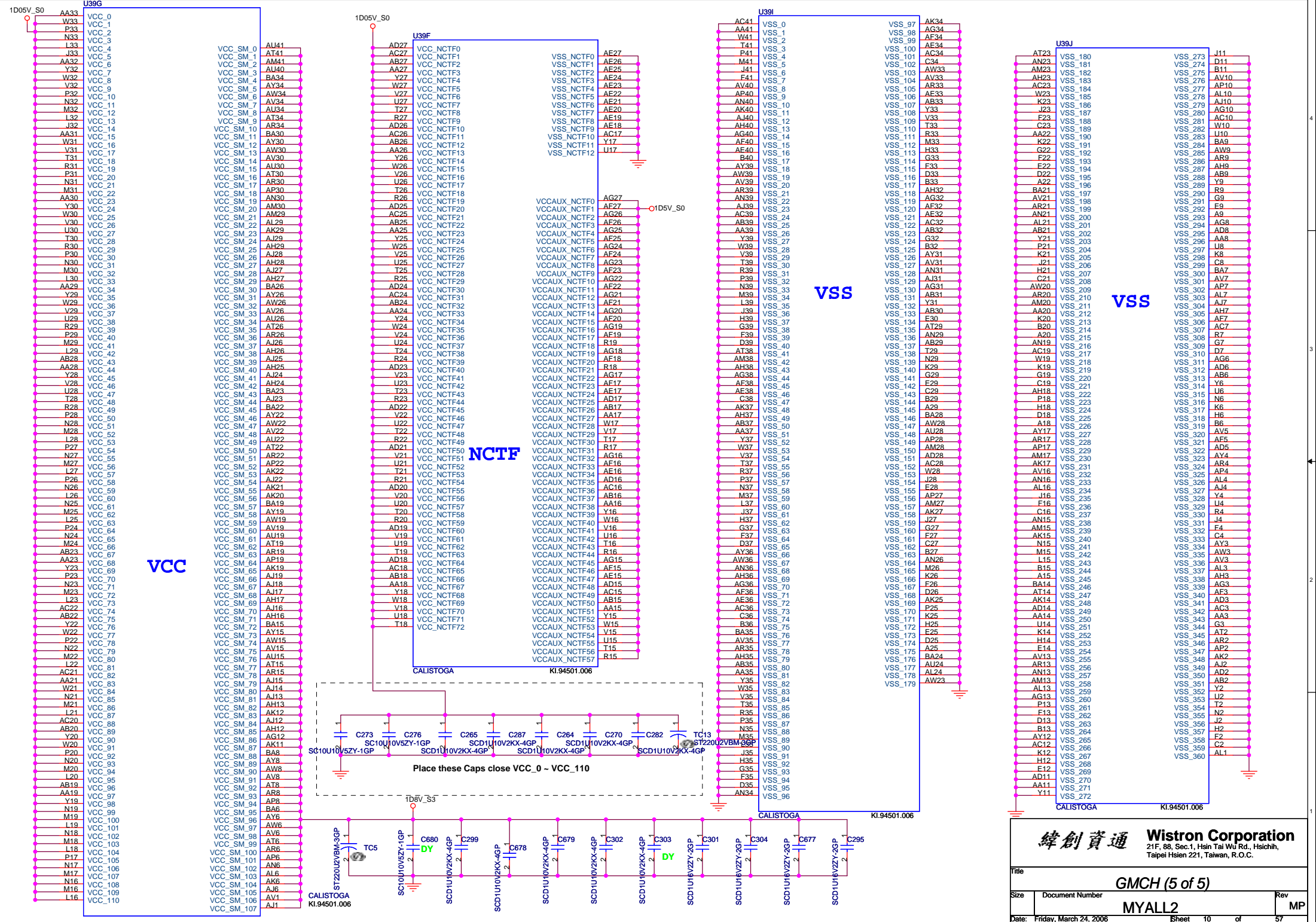


POWER

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Divide by Trace (Layout Rule approve)



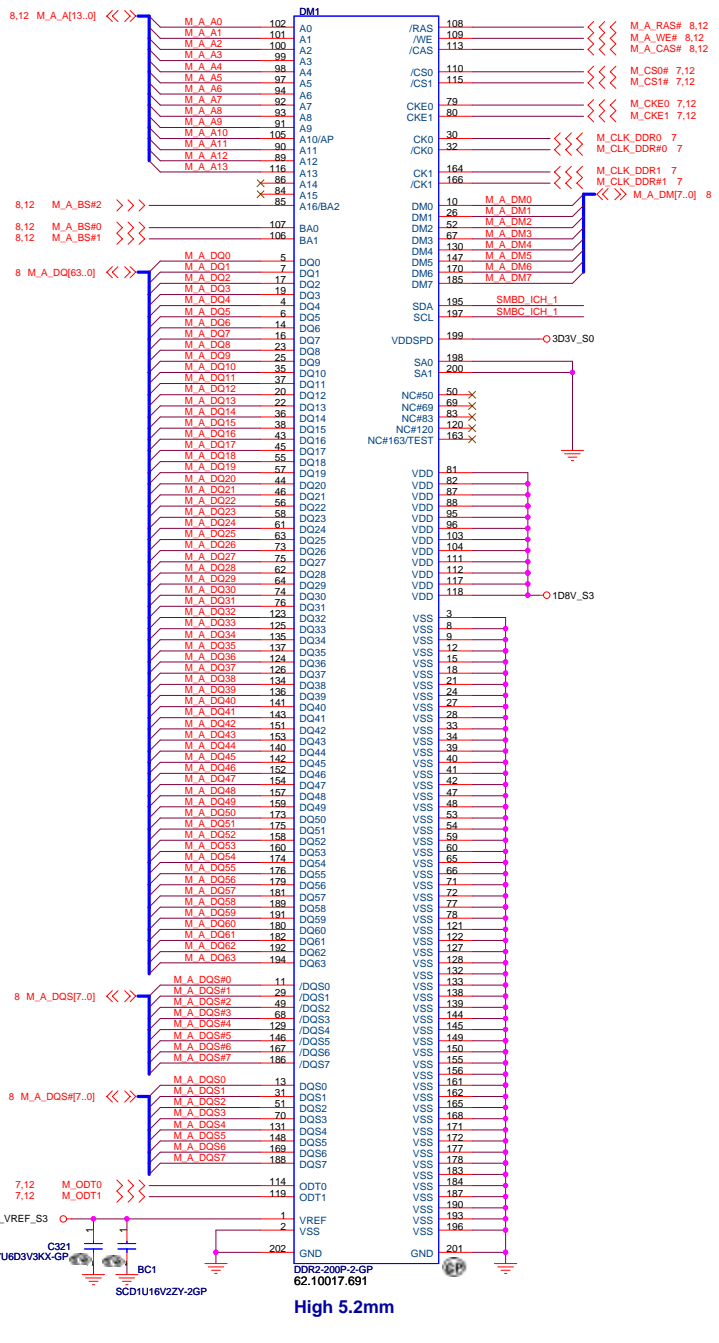
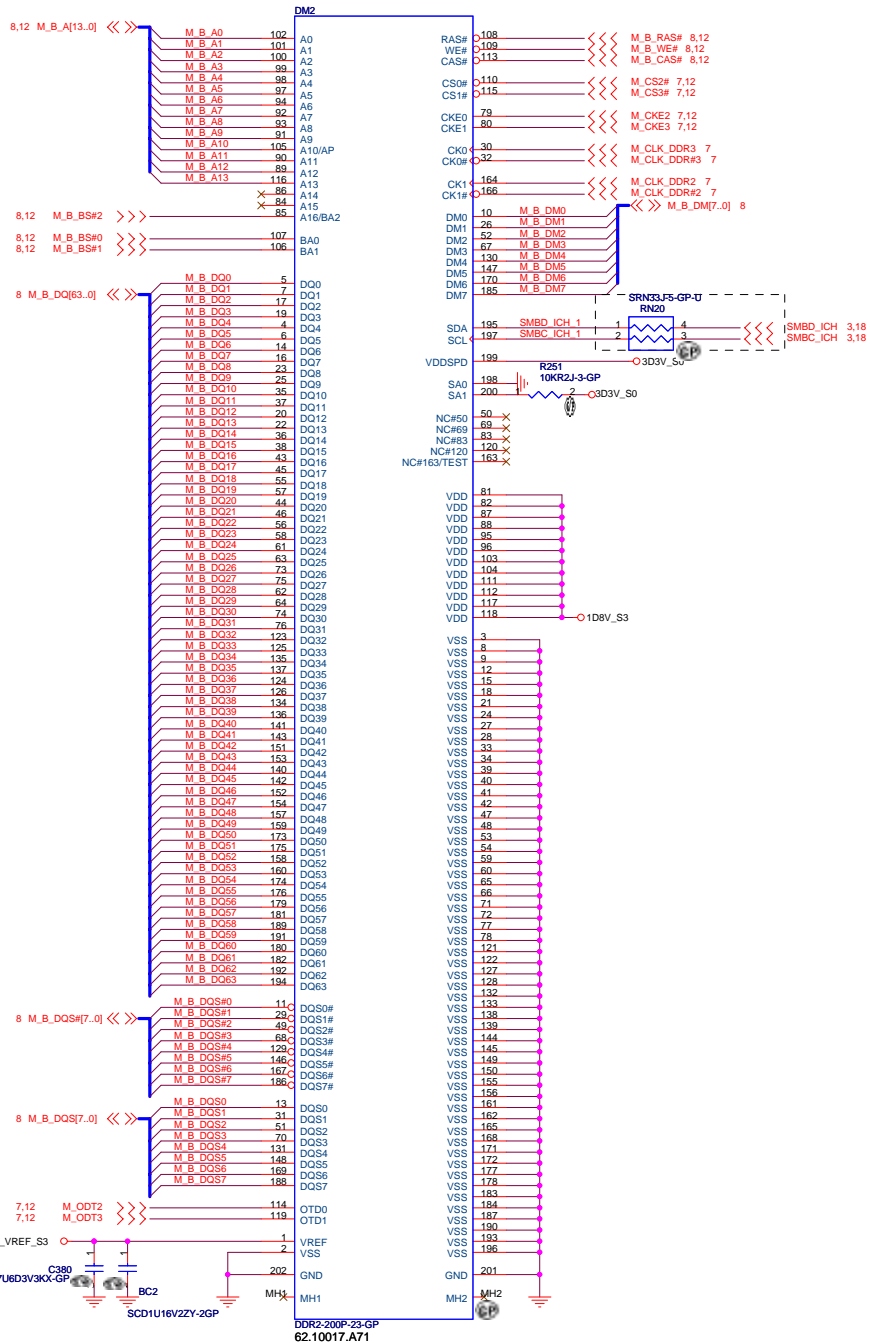
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GMCH (5 of 5)

MYALL2

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Title	Rev
Size	MP
Document Number	

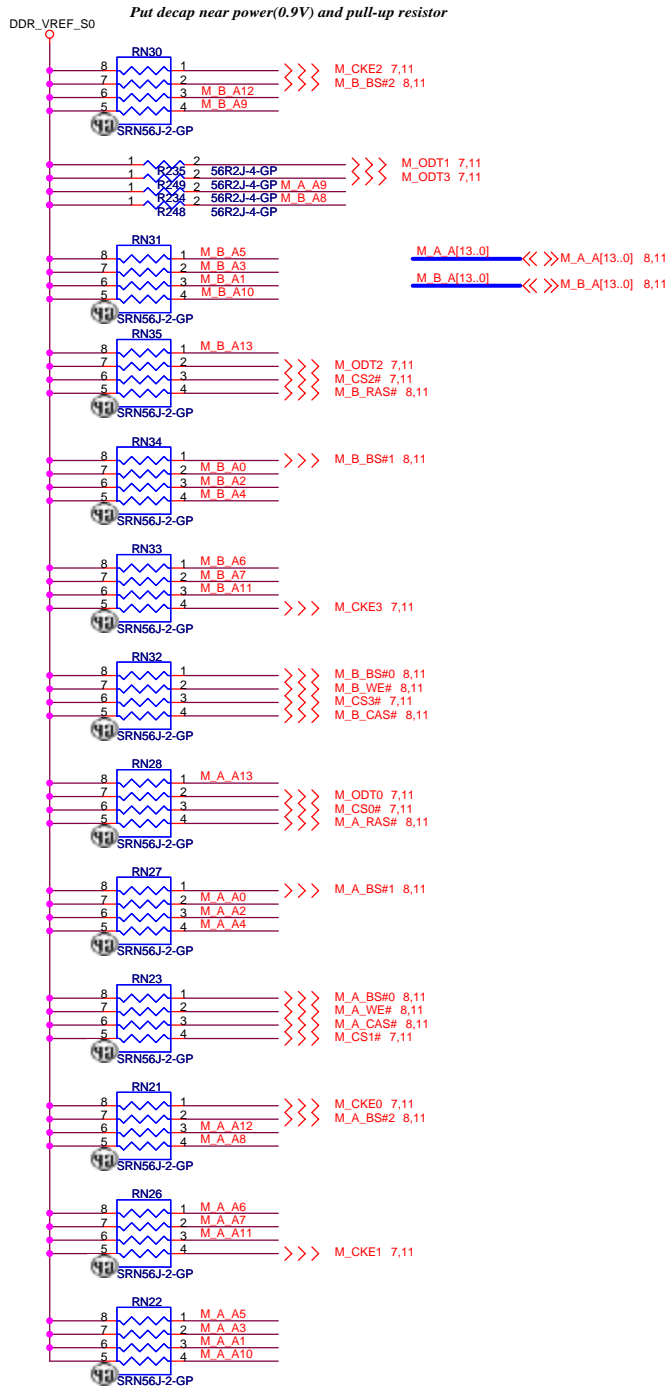


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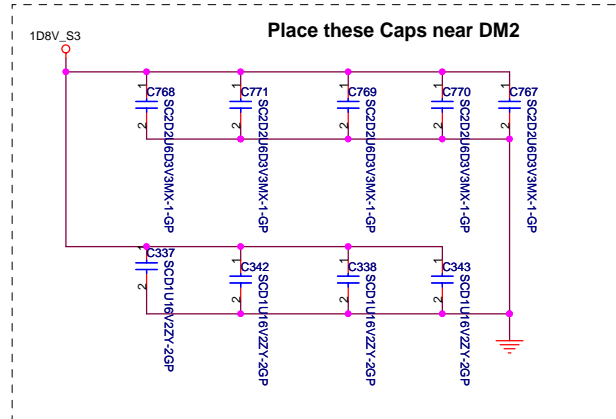
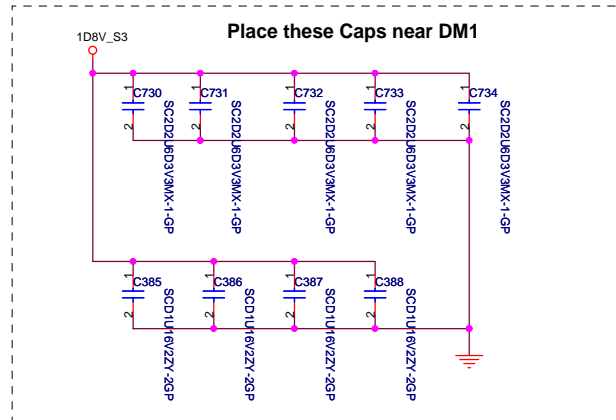
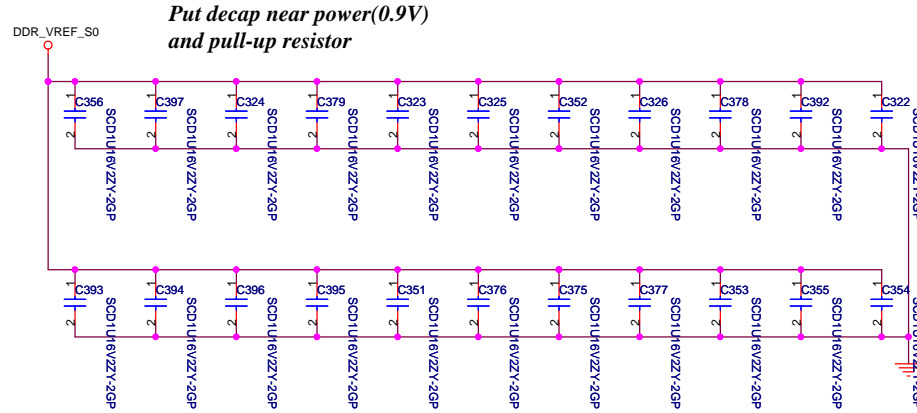
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DDR2 Socket		MP	
Size	Document Number	Rev	
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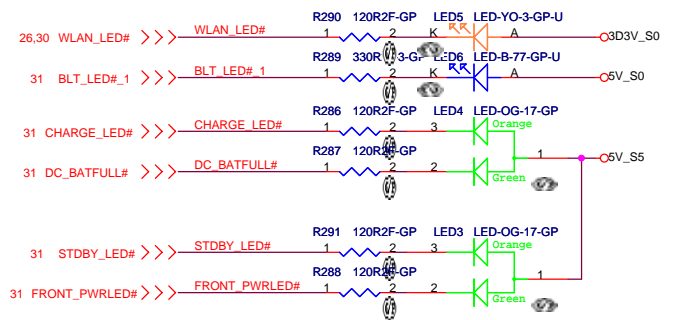
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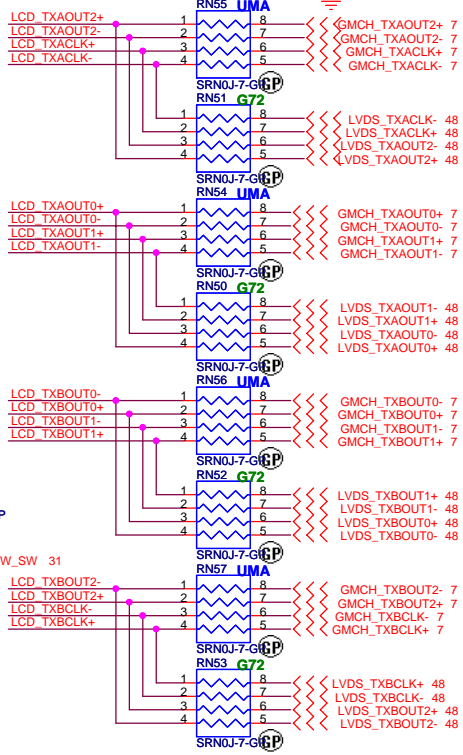
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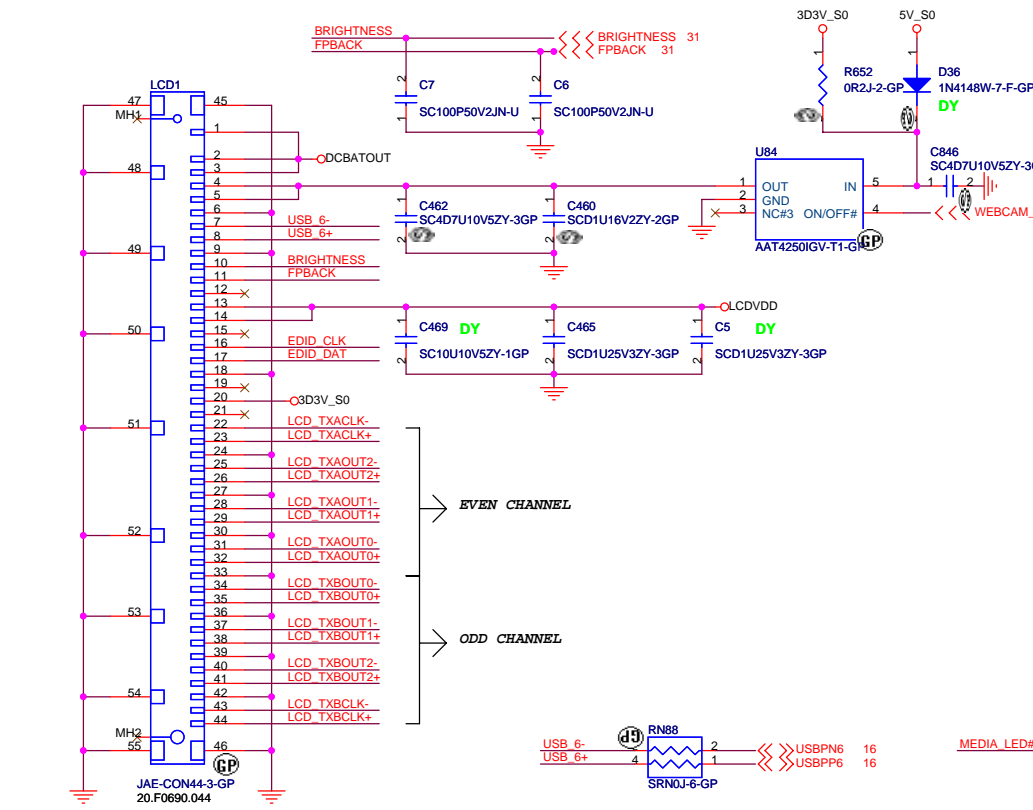
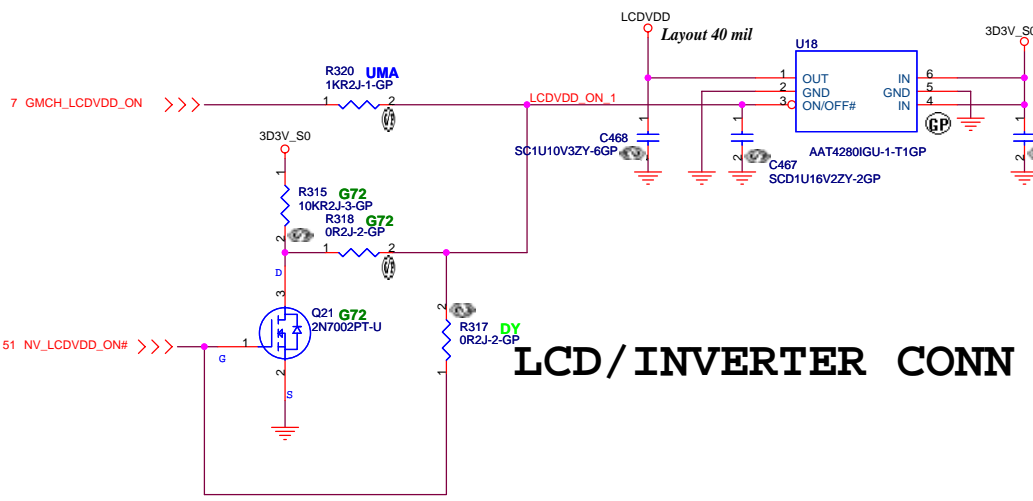
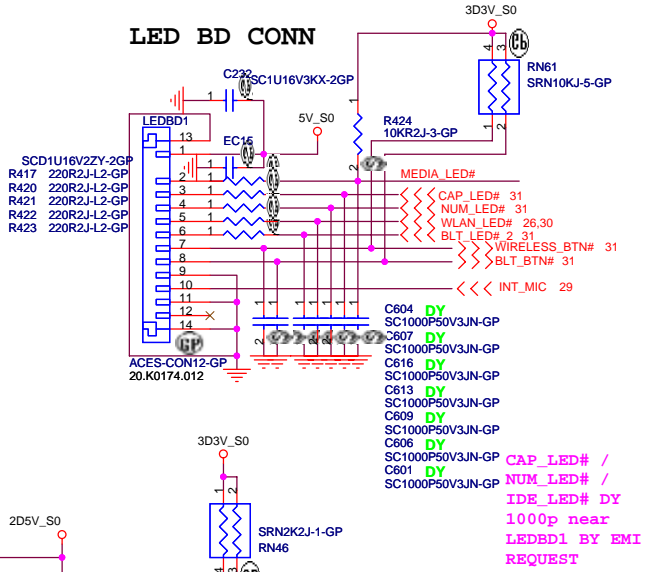
LED



LCD/INVERTER CONN



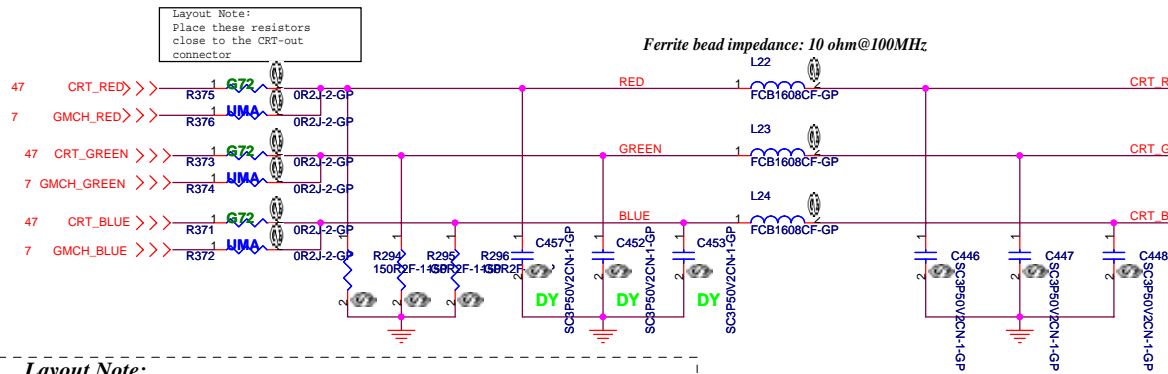
LED BD CONN



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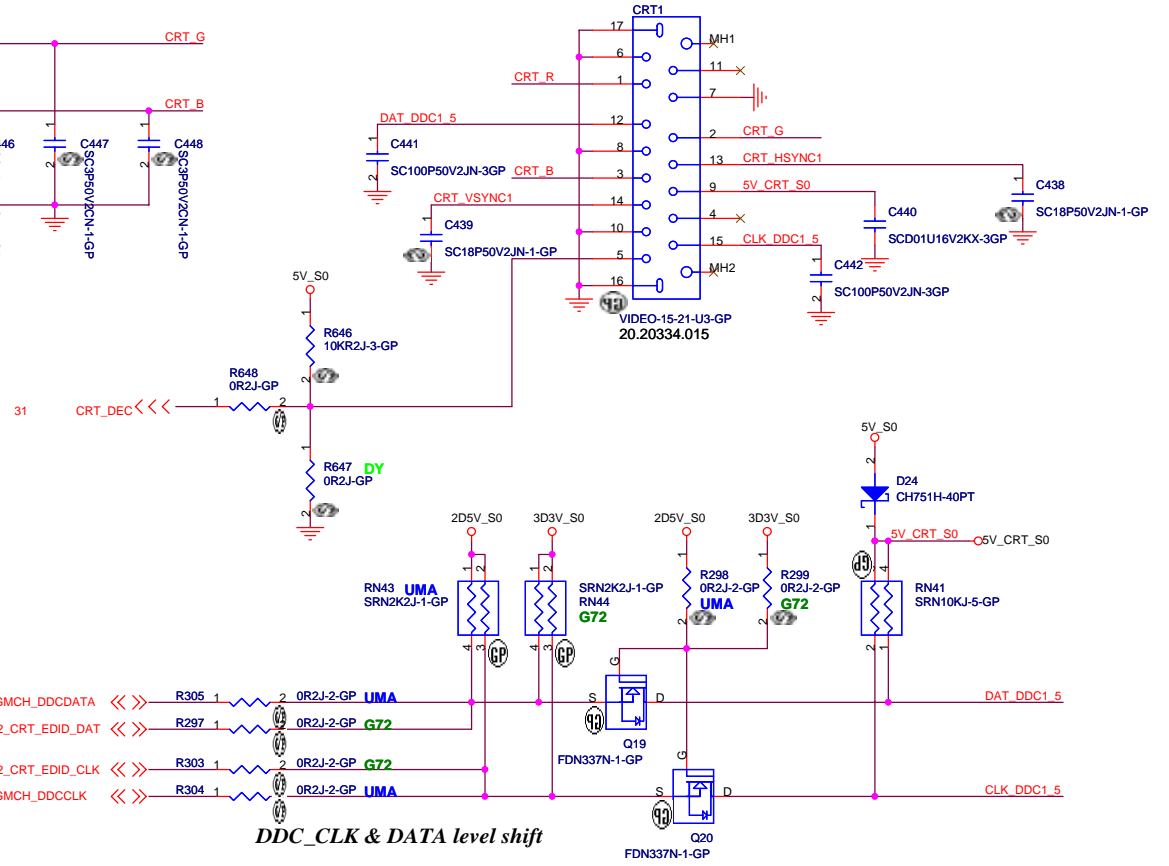
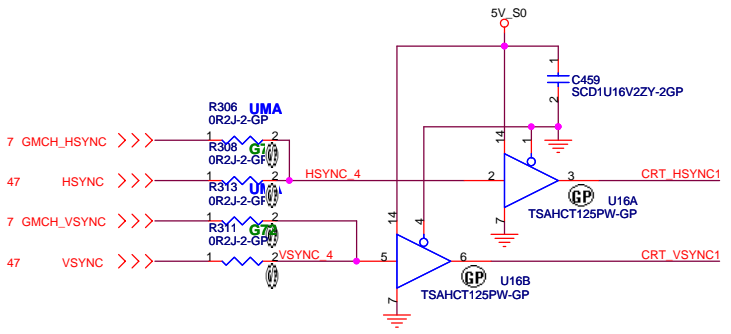
File			
LCD CONN & LED			
Size	Document Number	Rev	MP
	MYALL2		
Date: Tuesday, April 11, 2006	Sheet 13 of		57

CRT I/F & CONNECTOR

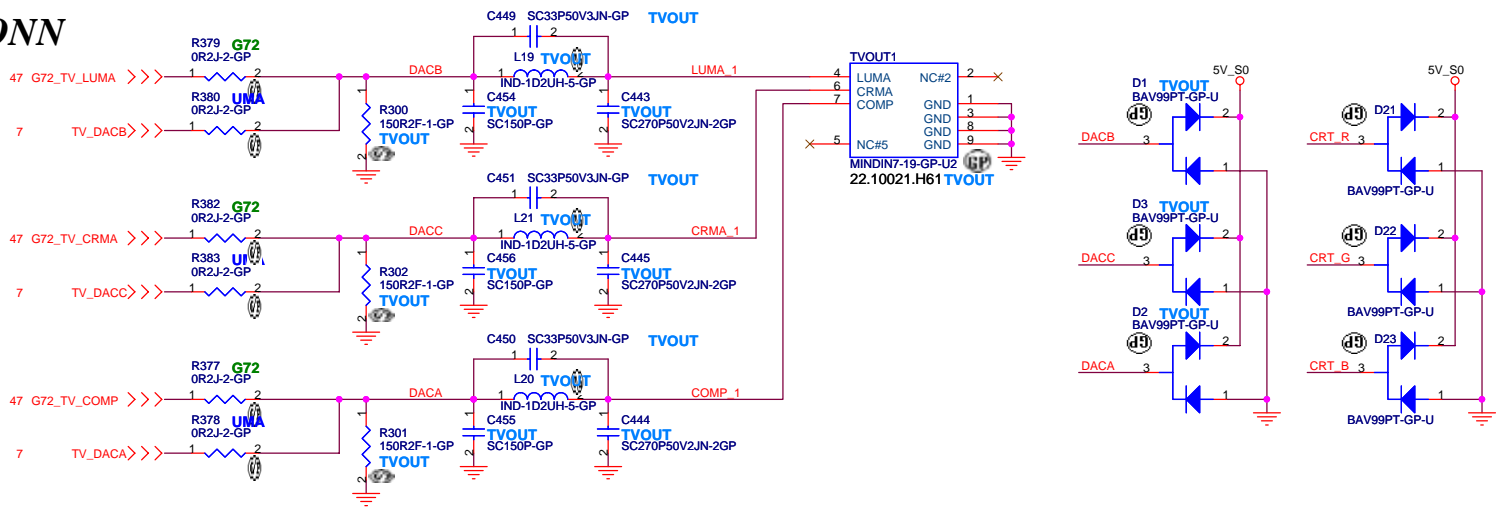


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



TV CONN

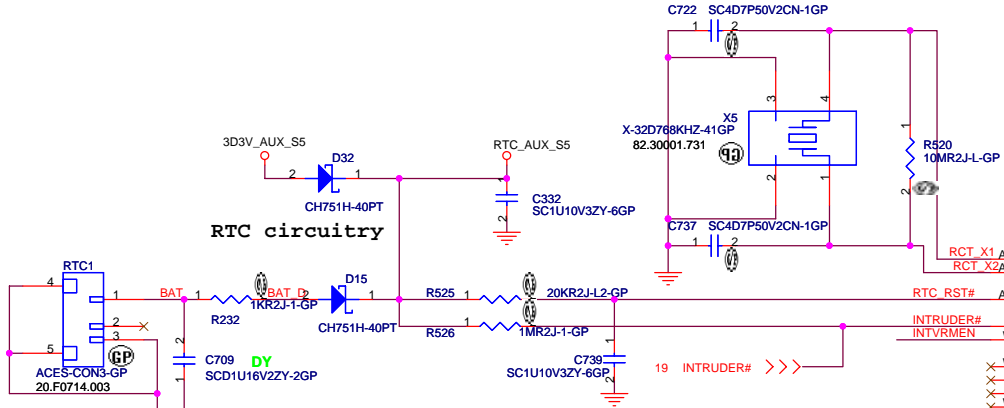


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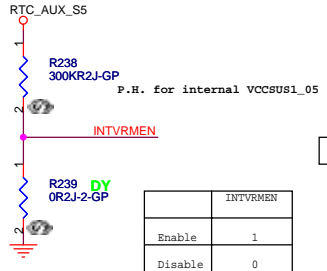
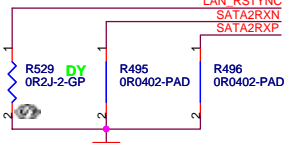
Title: CRT/TV Connector
Size: Document Number: MYALL2
Date: Thursday, March 30, 2006

Rev: MP
Sheet 14 of 57

RTC circuitry



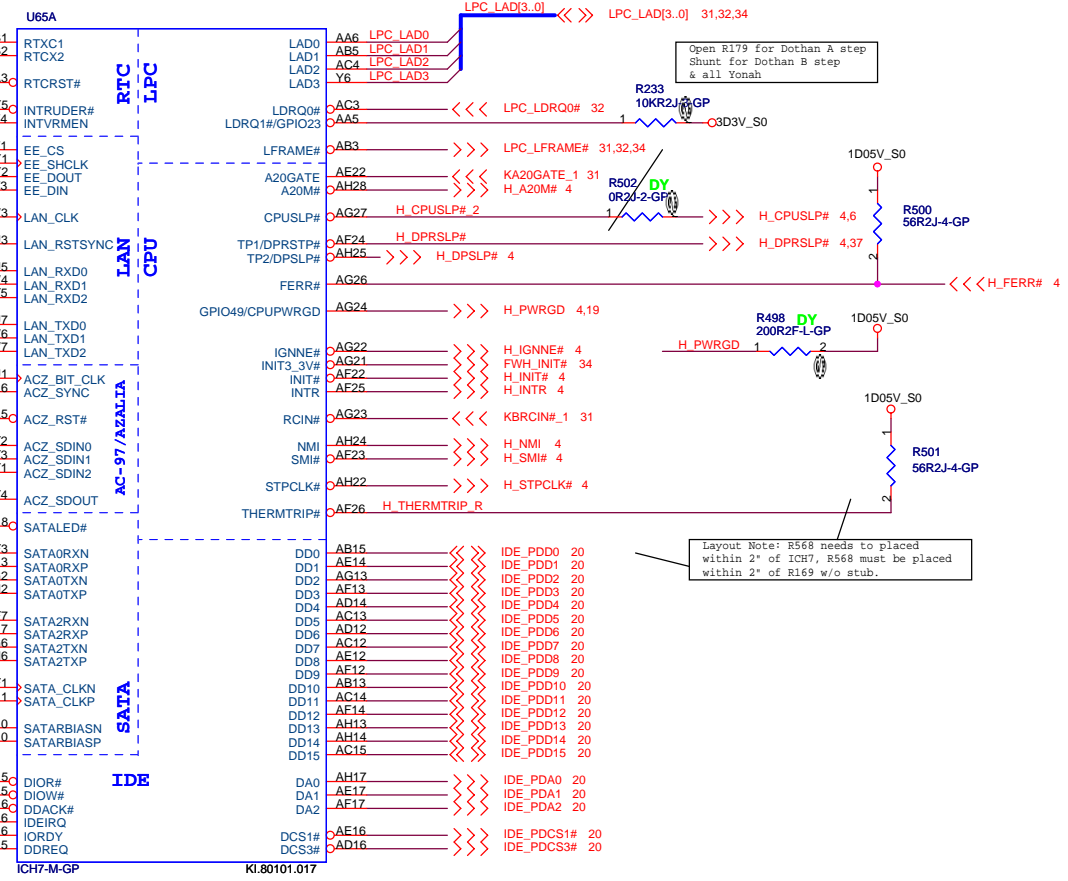
2nd source: 20.D0198.103



Placement Note:
Distance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.

Place within 500 mils of ICH7ball

Change to 24.9 1% ohm when use SATA HD



Open R179 for Dothan A step
Shunt for Dothan B step
& all Ionah

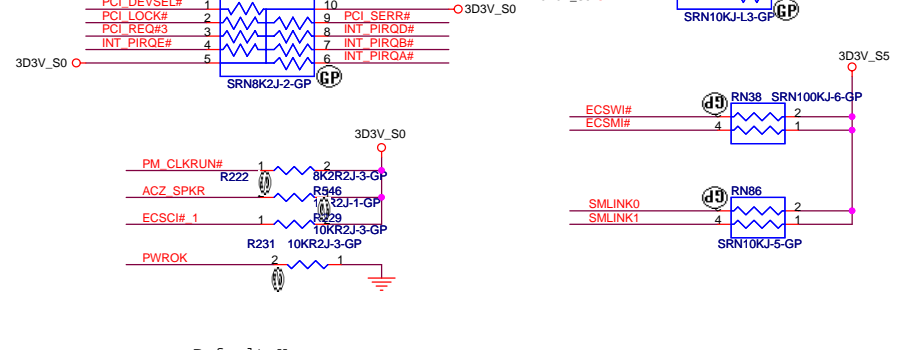
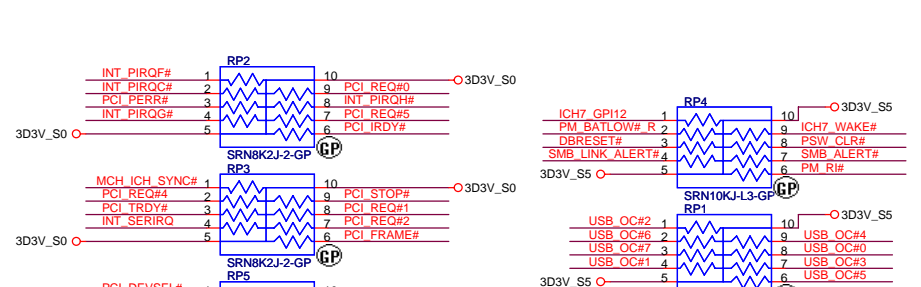
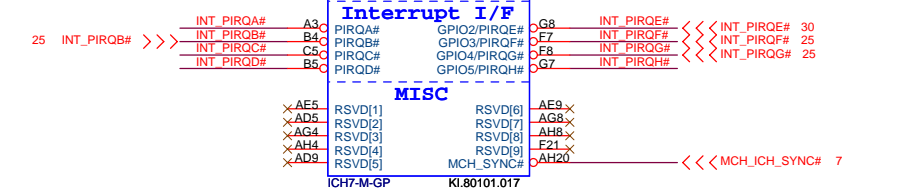
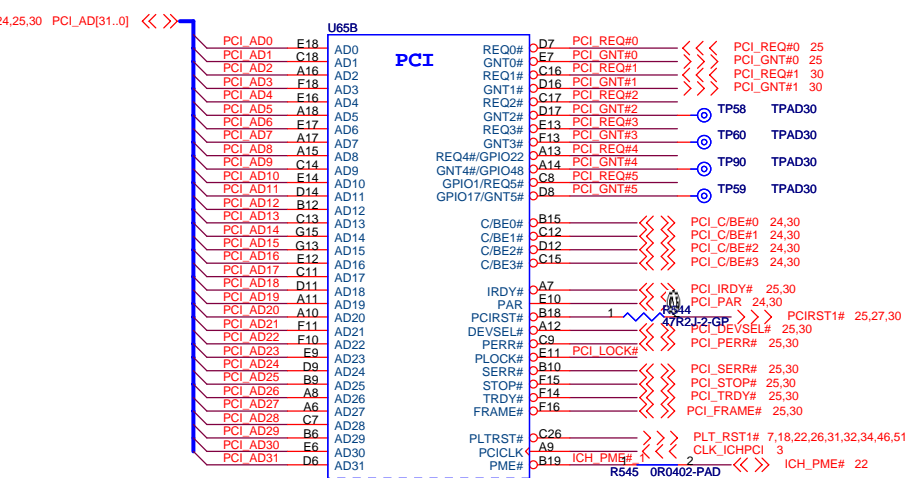
Layout Note: R568 needs to be placed within 2" of ICH7, R568 must be placed within 2" of R169 w/o stub.

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Title: ICH7-M (1 of 4)

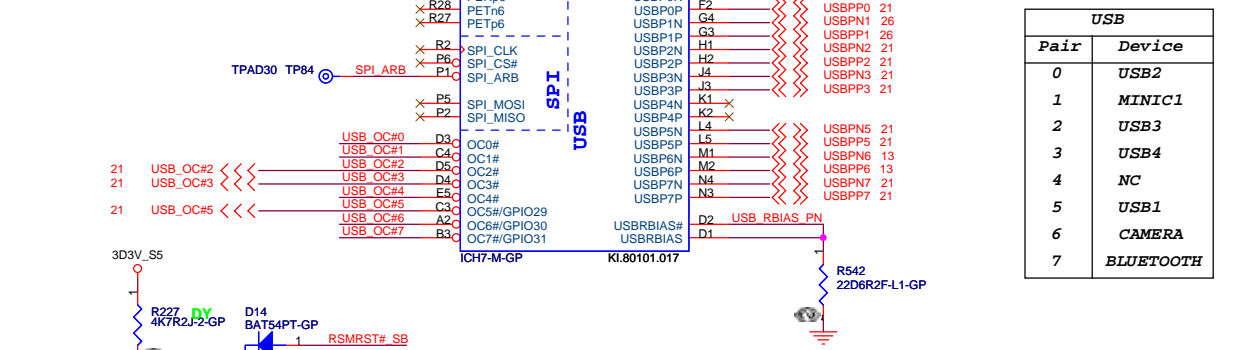
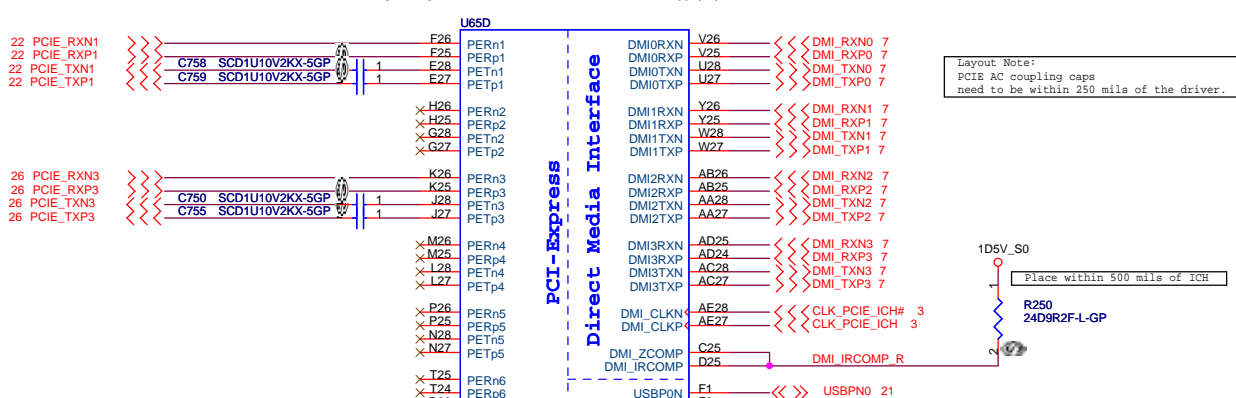
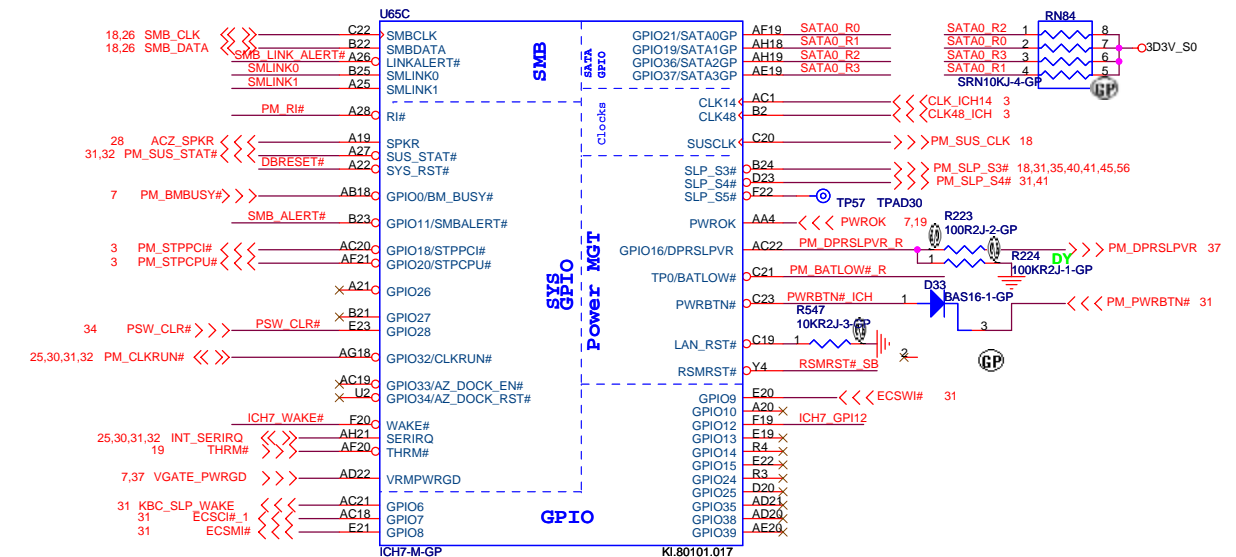
Size: Document Number: MYALL2 Rev: MP

Date: Thursday, March 30, 2006 Sheet 15 of 57



Default :H

	GNT5#	GNT4#
LPC	H	H
PCI	H	L
SPI	L	H



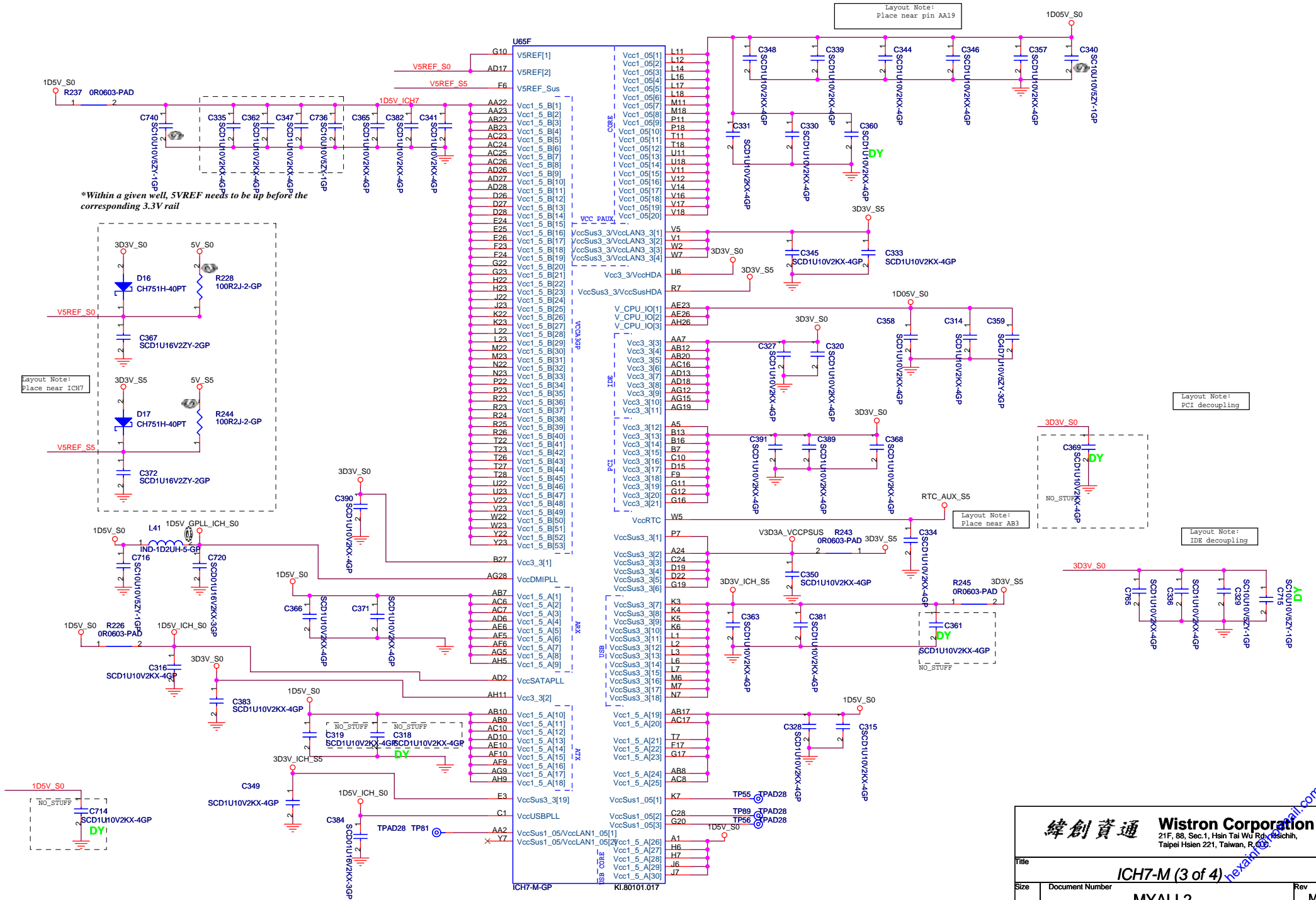
Layout Note:
 PCB AC coupling caps
 need to be within 250 mils of the driver.

Place within 500 mils of ICH
 R250 24D9R2F-L-GP

USB

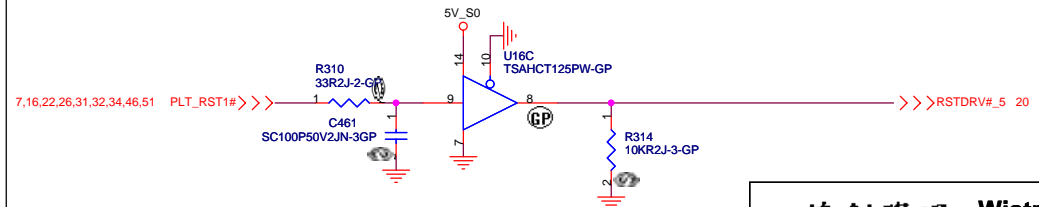
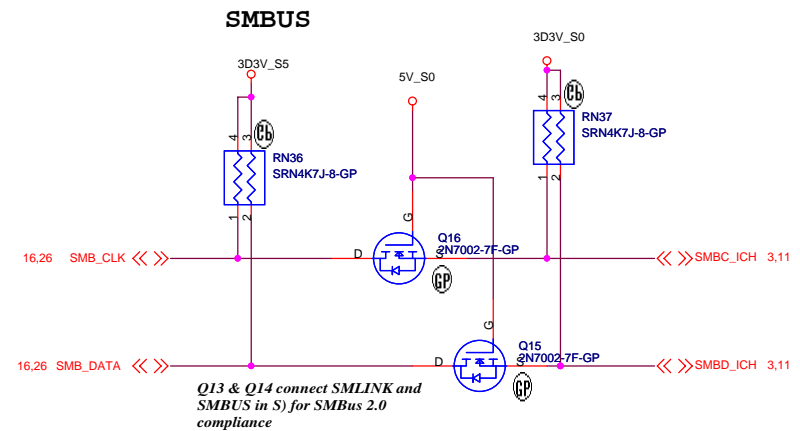
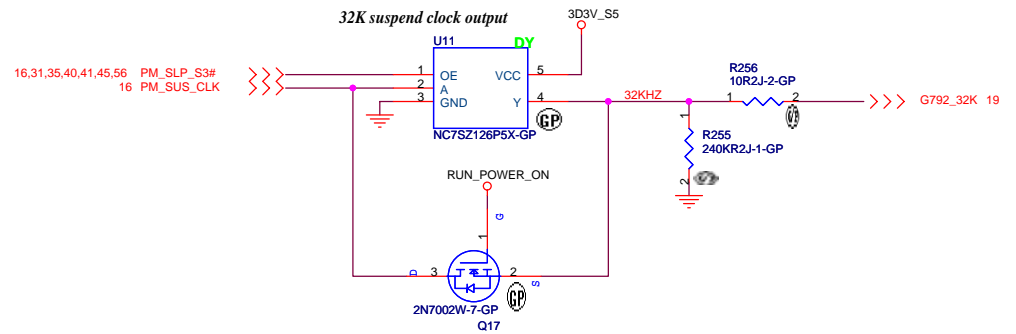
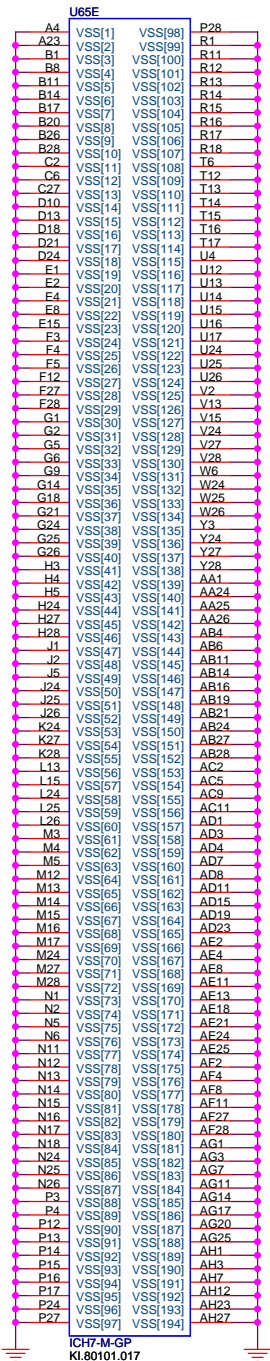
Pair	Device
0	USB2
1	MINIC1
2	USB3
3	USB4
4	NC
5	USB1
6	CAMERA
7	BLUETOOTH

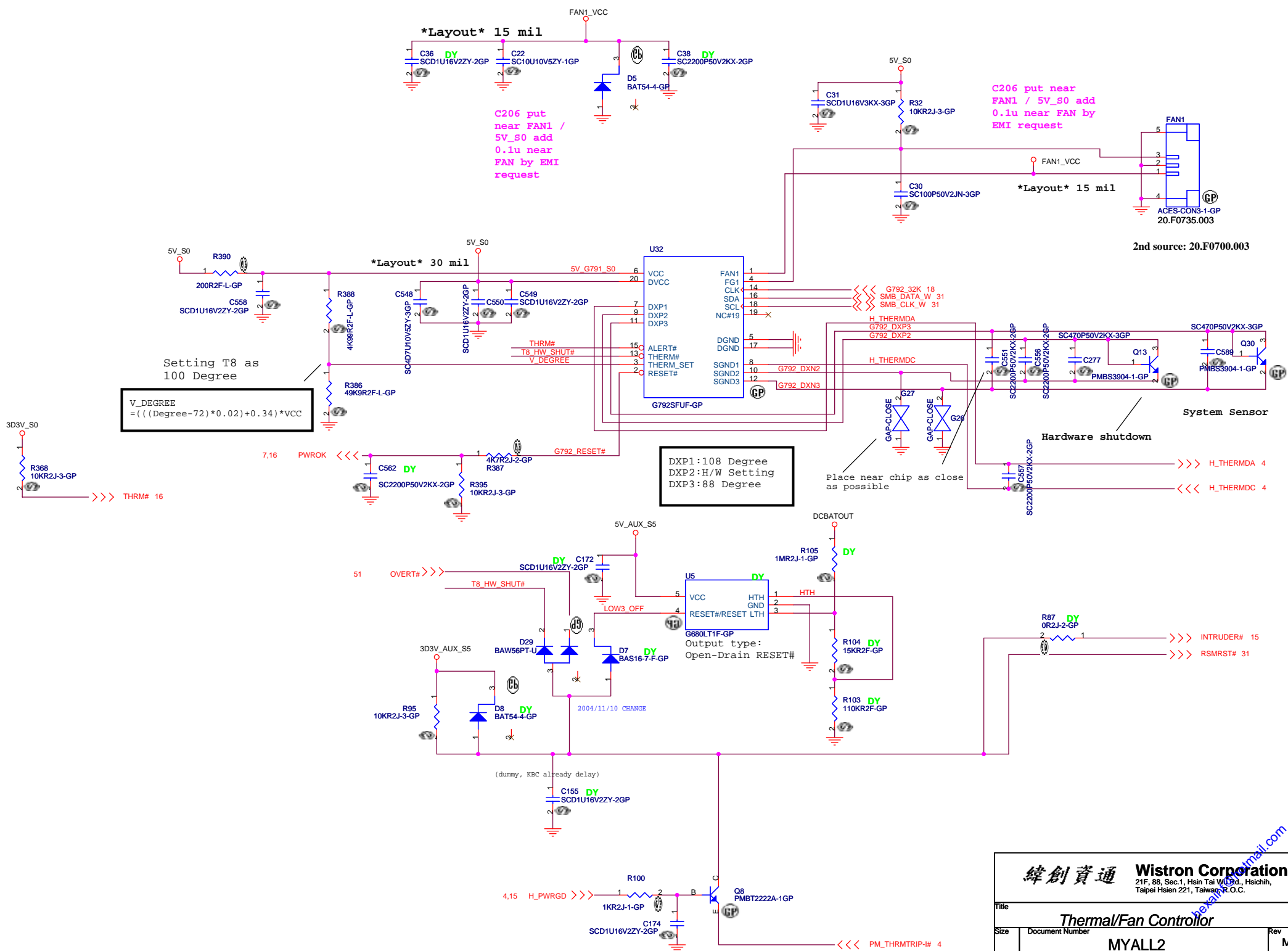
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.



 緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Neihu, Taipei Hsien 221, Taiwan, R.O.C.	
ICH7-M (3 of 4)	
Title MYALL2	Rev MP
Size Document Number	Rev MP
Date: Friday, March 24, 2006 Sheet 17 of 57	

hexamail.com





C206 put near FAN1 / 5V_S0 add 0.1u near FAN by EMI request

C206 put near FAN1 / 5V_S0 add 0.1u near FAN by EMI request

Layout 30 mil

Setting T8 as 100 Degree

$$V_DEGREE = (((Degree-72) * 0.02) + 0.34) * VCC$$

DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

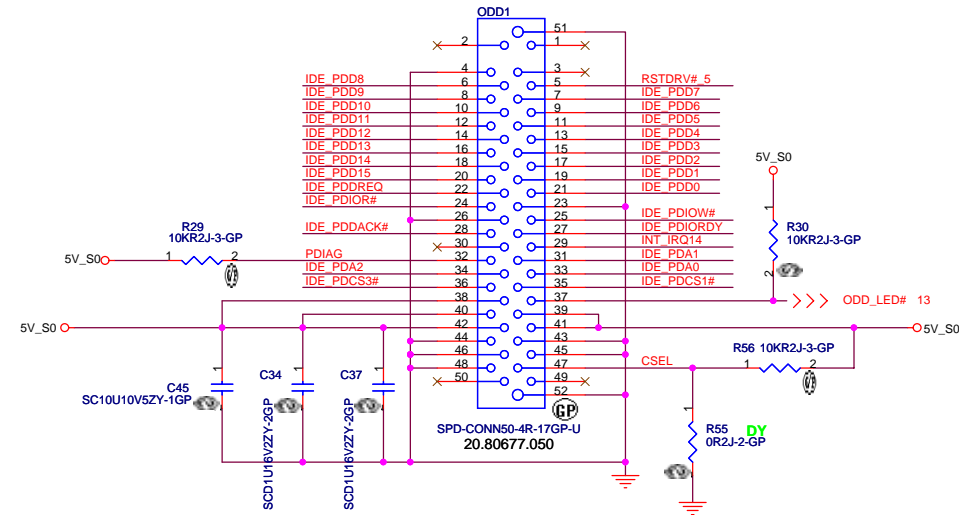
Place near chip as close as possible

2nd source: 20.F0700.003

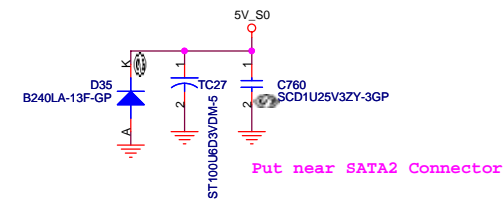
System Sensor

Hardware shutdown

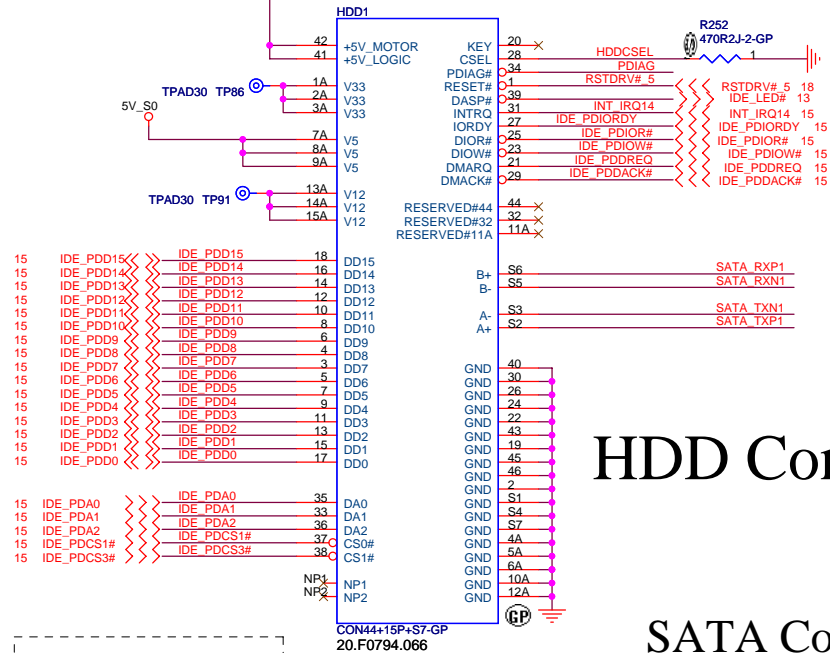
CD-ROM Connector



For HDD & SATA both

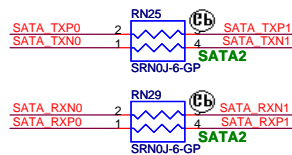
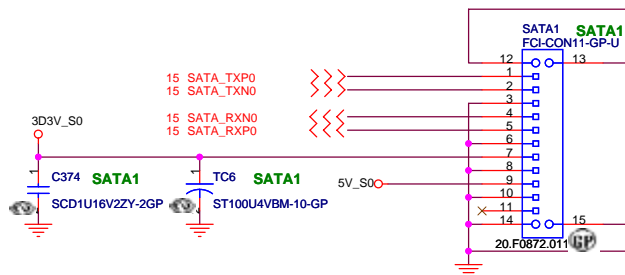


HDD Connector



SATA PN : 20.F0794.066
PATA PN : 20.E0021.222

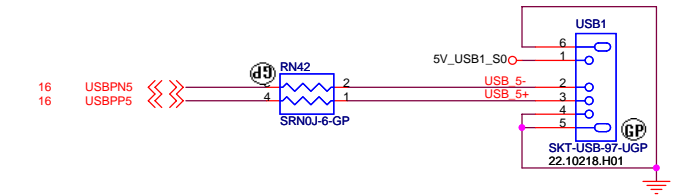
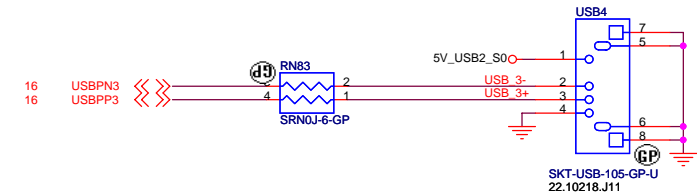
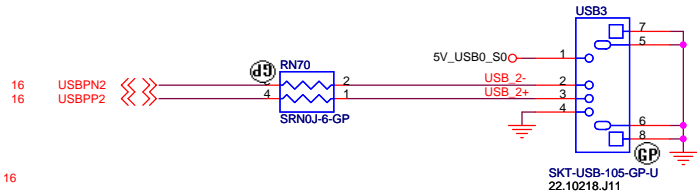
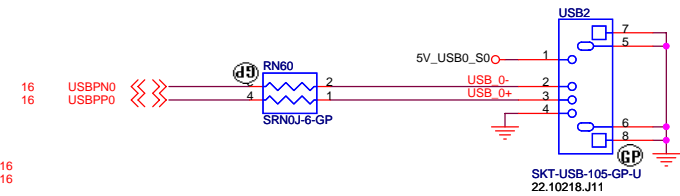
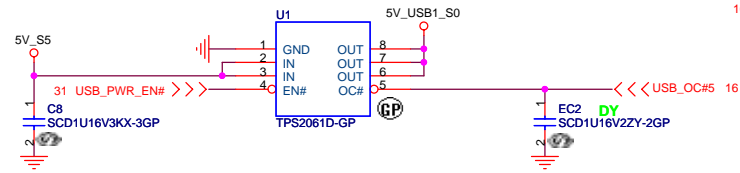
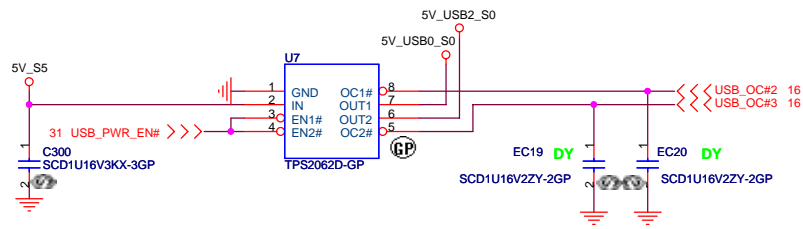
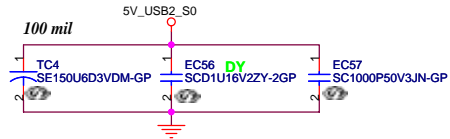
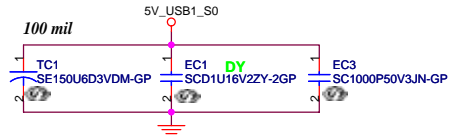
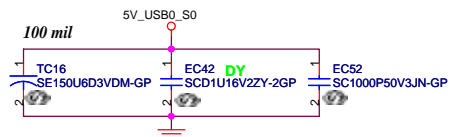
SATA Connector



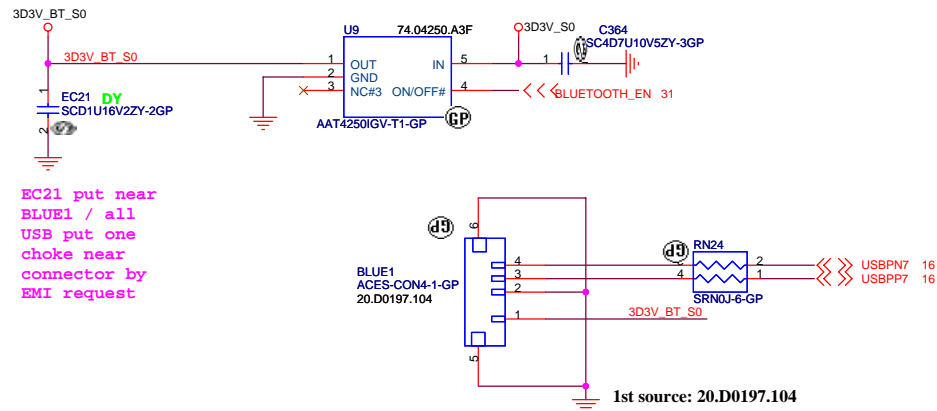
? 0 Ohms close to SATA2 Connector

Dummy when use IDE

ME : 20.F0777.022



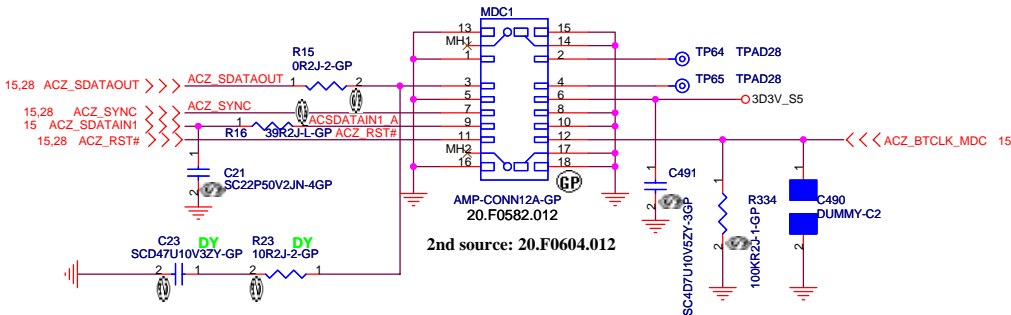
BLUETOOTH MODULE

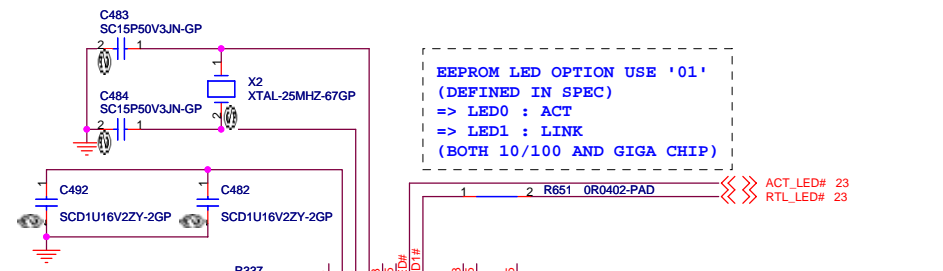
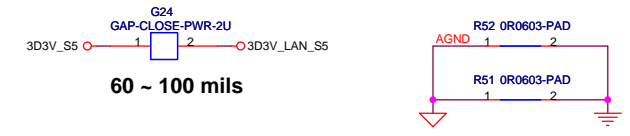
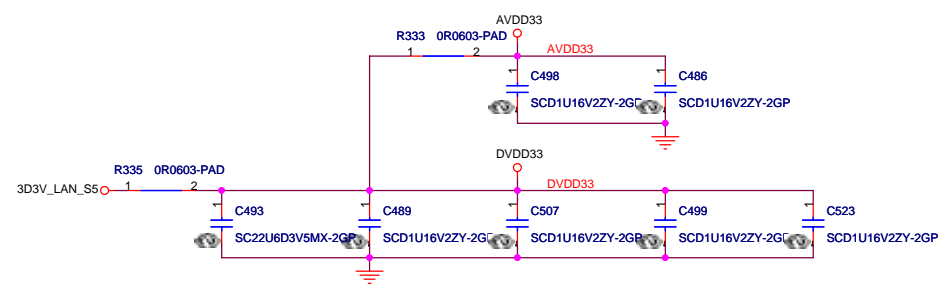
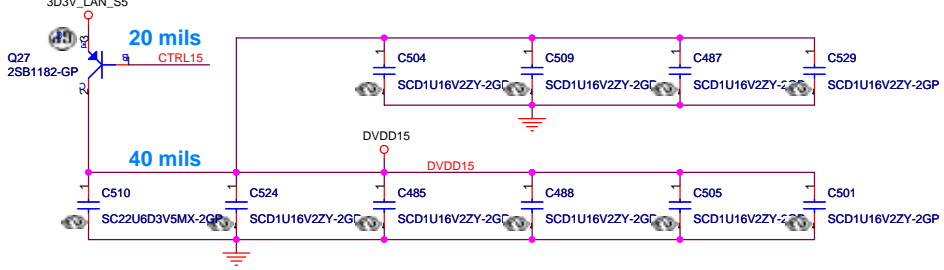
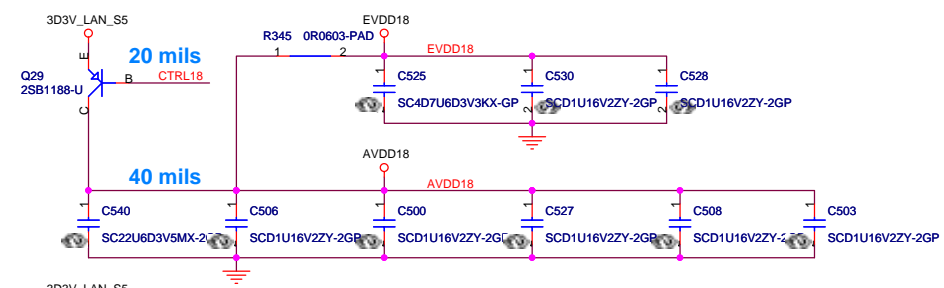


EC21 put near BLUE1 / all USB put one choke near connector by EMI request

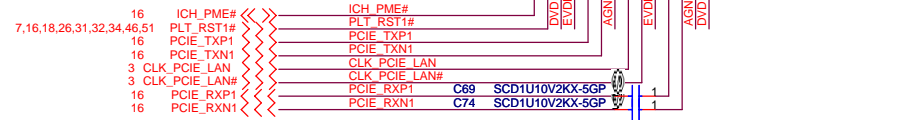
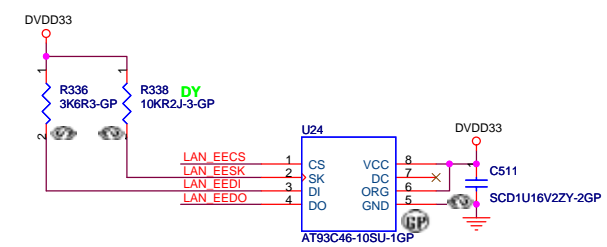
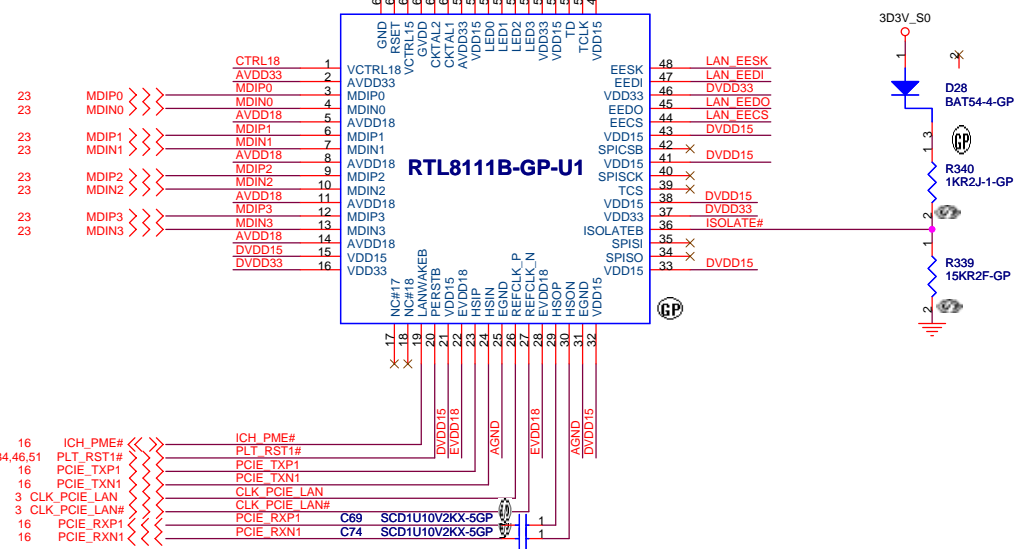
MDC 1.5 CONNECTOR

CHANGE TO AZ





EEPROM LED OPTION USE '01'
 (DEFINED IN SPEC)
 => LED0 : ACT
 => LED1 : LINK
 (BOTH 10/100 AND GIGA CHIP)

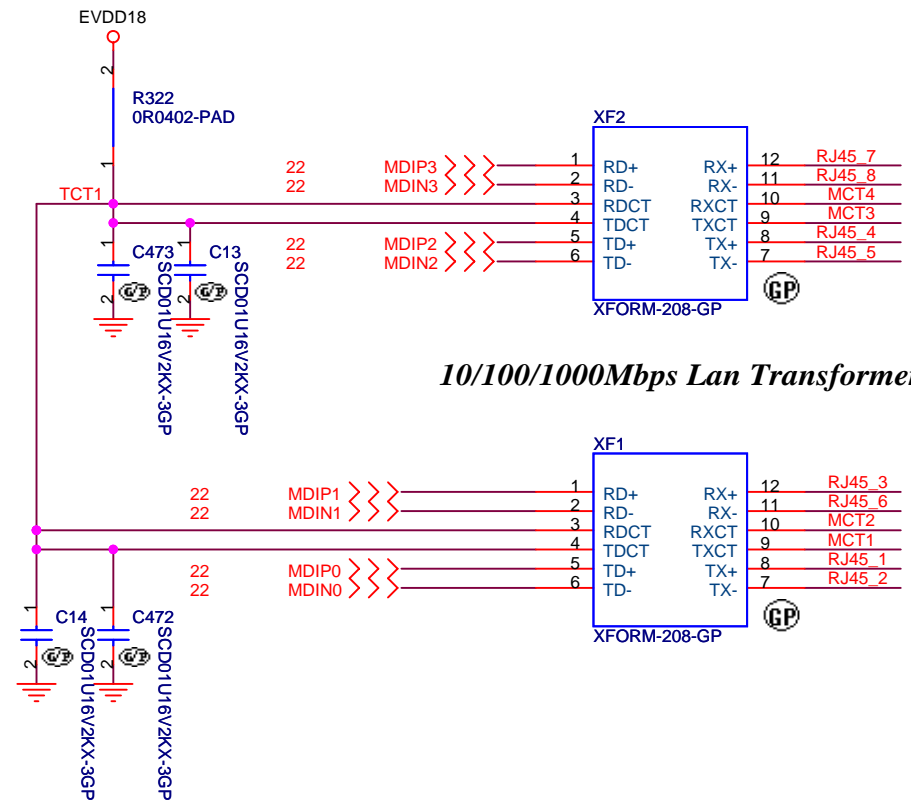


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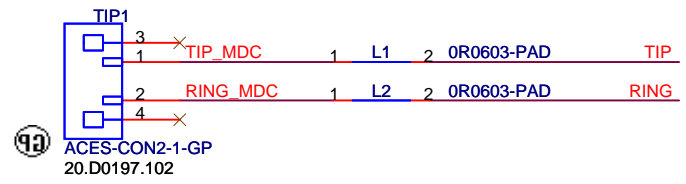
Title: **RTL8111B**

Size: Document Number: **MYALL2** Rev: **MP**

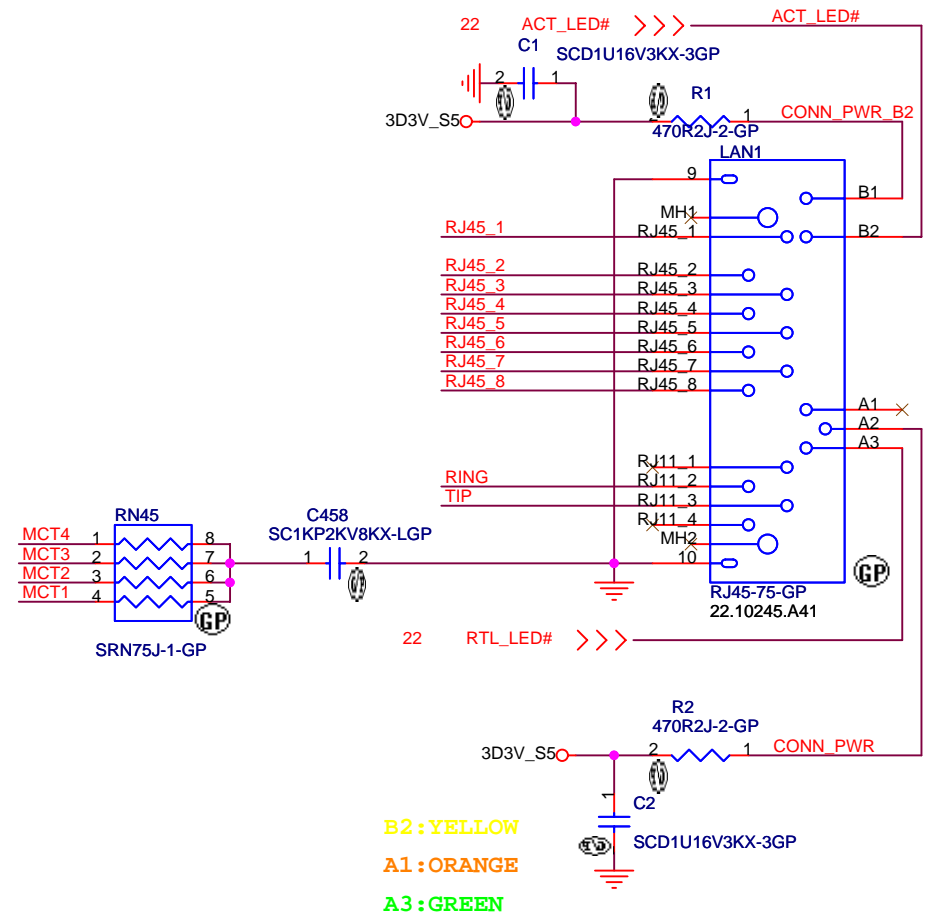
Date: Thursday, March 30, 2006 Sheet 22 of 57



10/100/1000Mbps Lan Transformer

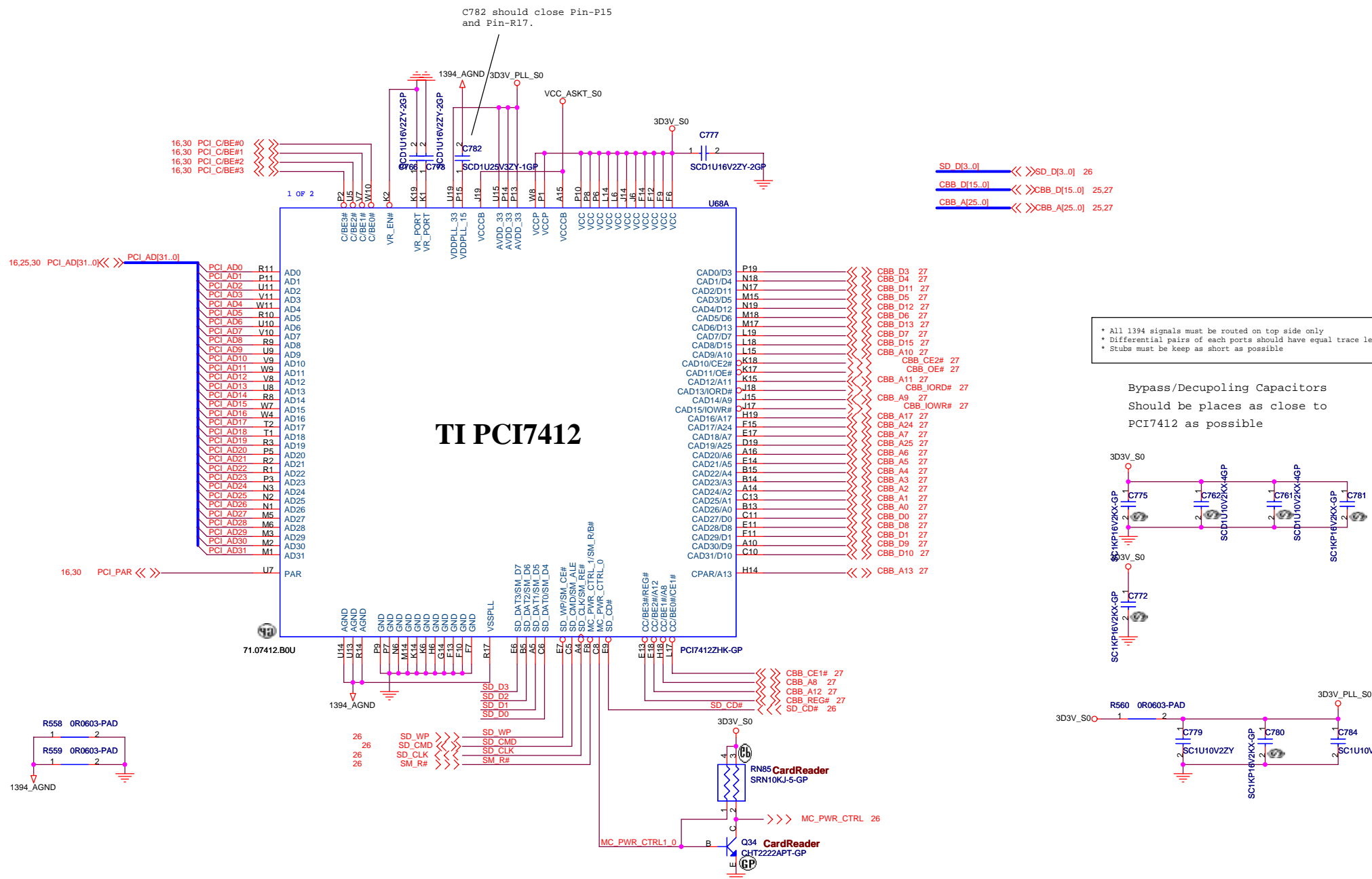


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



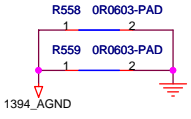
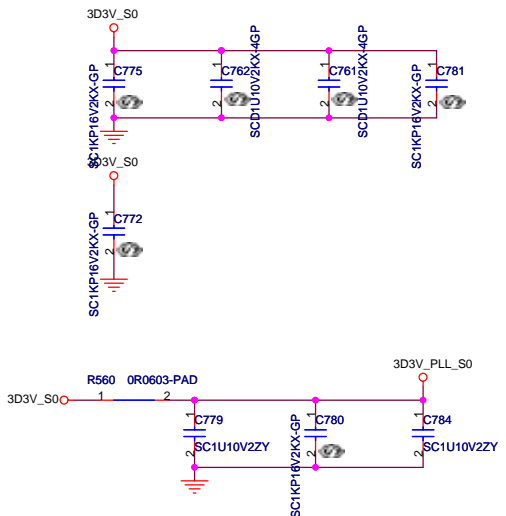
3D3V_S5 add 0.1u near LAN1 by EMI request

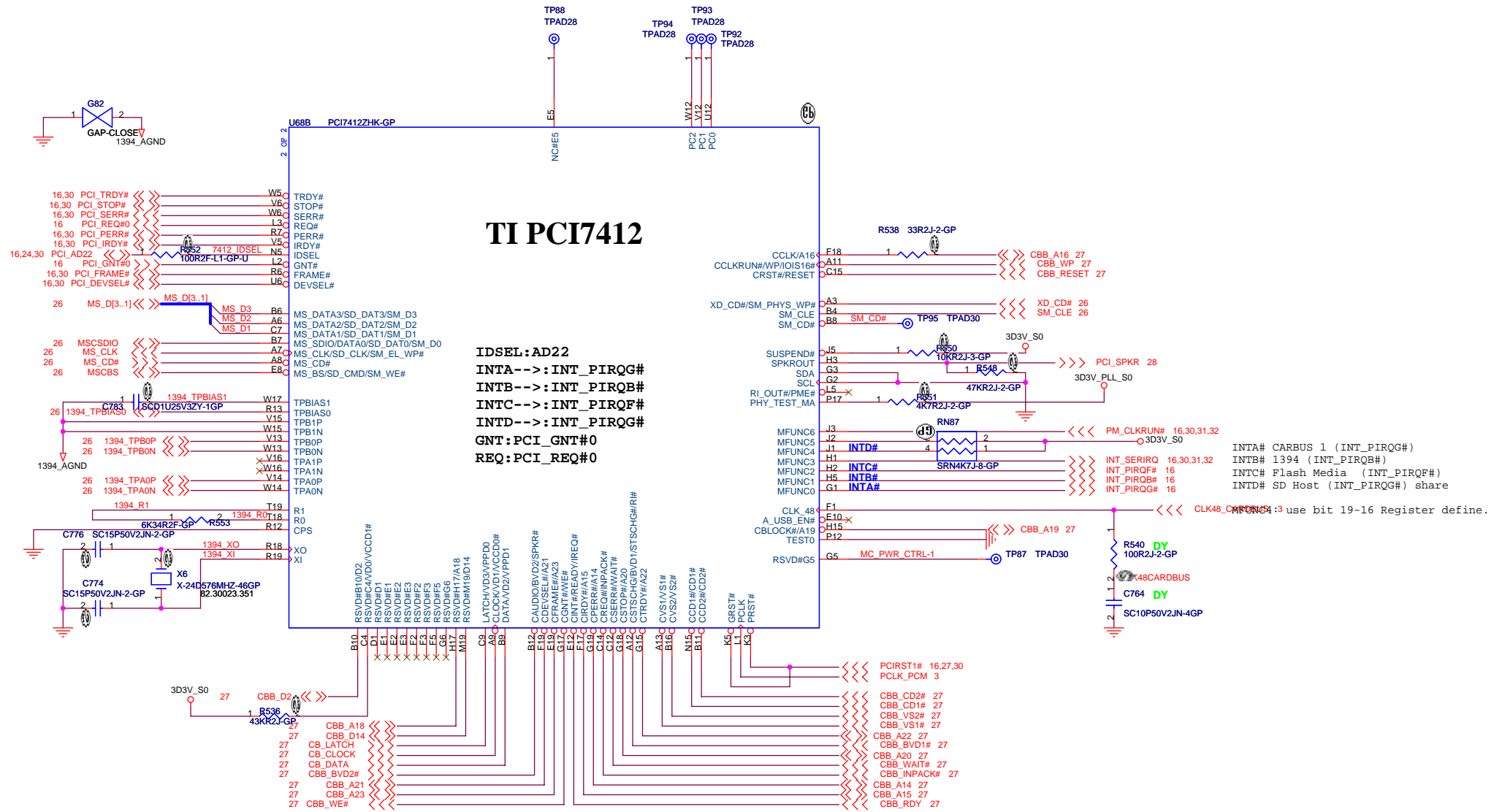
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title LAN CONN			
Size	Document Number	Rev	MP
MYALL2			
Date: Thursday, March 30, 2006	Sheet 23	of	57



* All 1394 signals must be routed on top side only
 * Differential pairs of each ports should have equal trace length
 * Stubs must be keep as short as possible

Bypass/Decoupling Capacitors
 Should be places as close to
 PCI7412 as possible





TI PCI7412

IDSEL: AD22
INTA-->: INT_PIRQ#
INTB-->: INT_PIRQ#
INTC-->: INT_PIRQ#
INTD-->: INT_PIRQ#
GNT: PCI_GNT#0
REQ: PCI_REQ#0

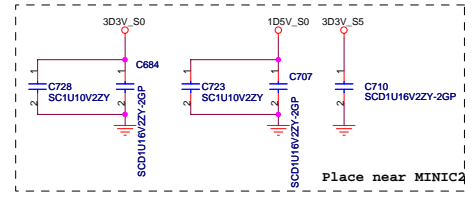
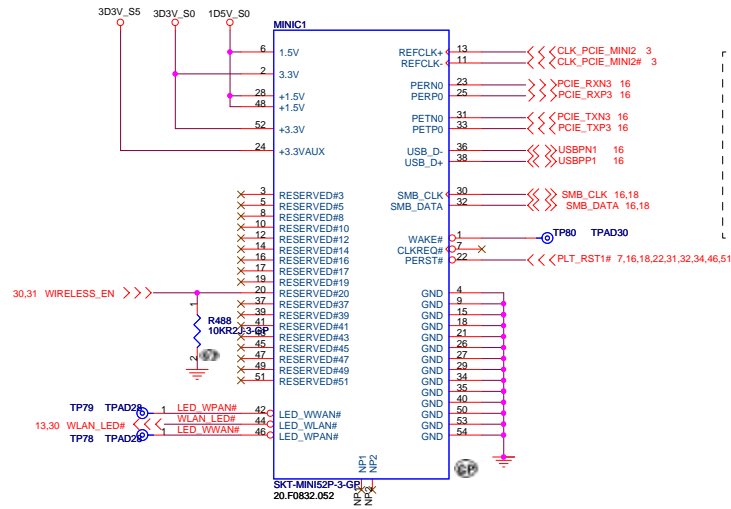
INTA# CARBUS 1 (INT_PIRQ#)
 INTB# 1394 (INT_PIRQ#)
 INTC# Flash Media (INT_PIRQ#)
 INTD# SD Host (INT_PIRQ#) share

CLK48_CMRUN#3 use bit 19-16 Register define.

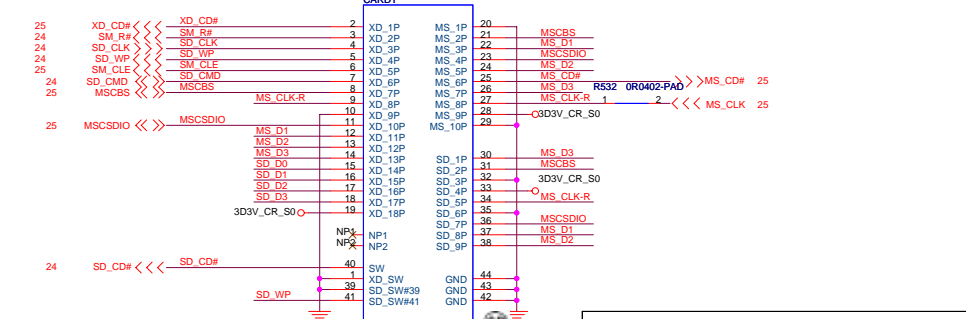
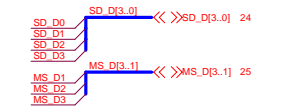
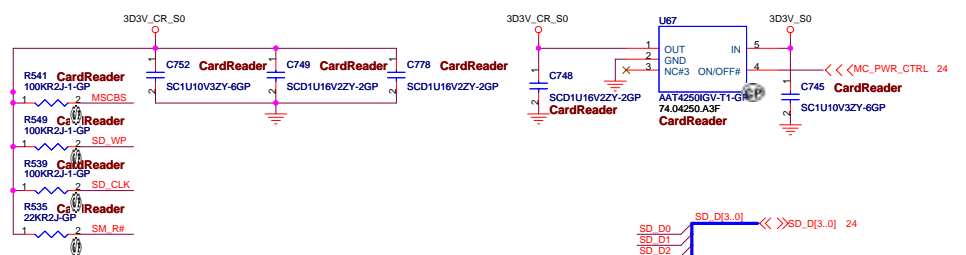
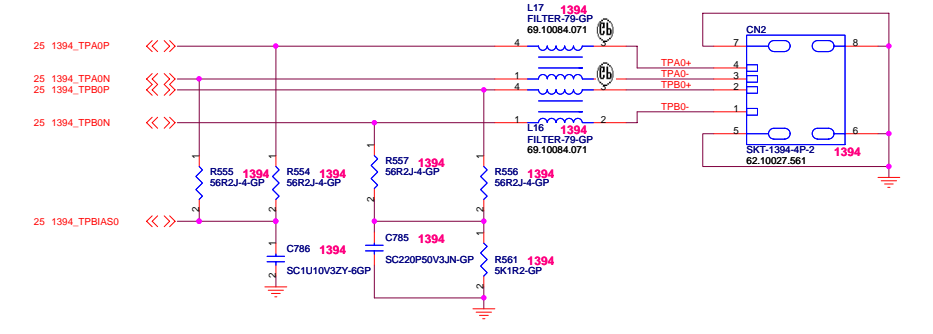
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title		Rev	
TI PCI7412 (2 of 2)		MP	
Size	Document Number	Date	
	MYALL2	Thursday, March 30, 2006	

Mini Card Connector



1394 Connector



**XD
MS / MS PRO
SD / SD IO / MMC**

CARD-PUSH-41P-GP-U
20.10036.001
CardReader

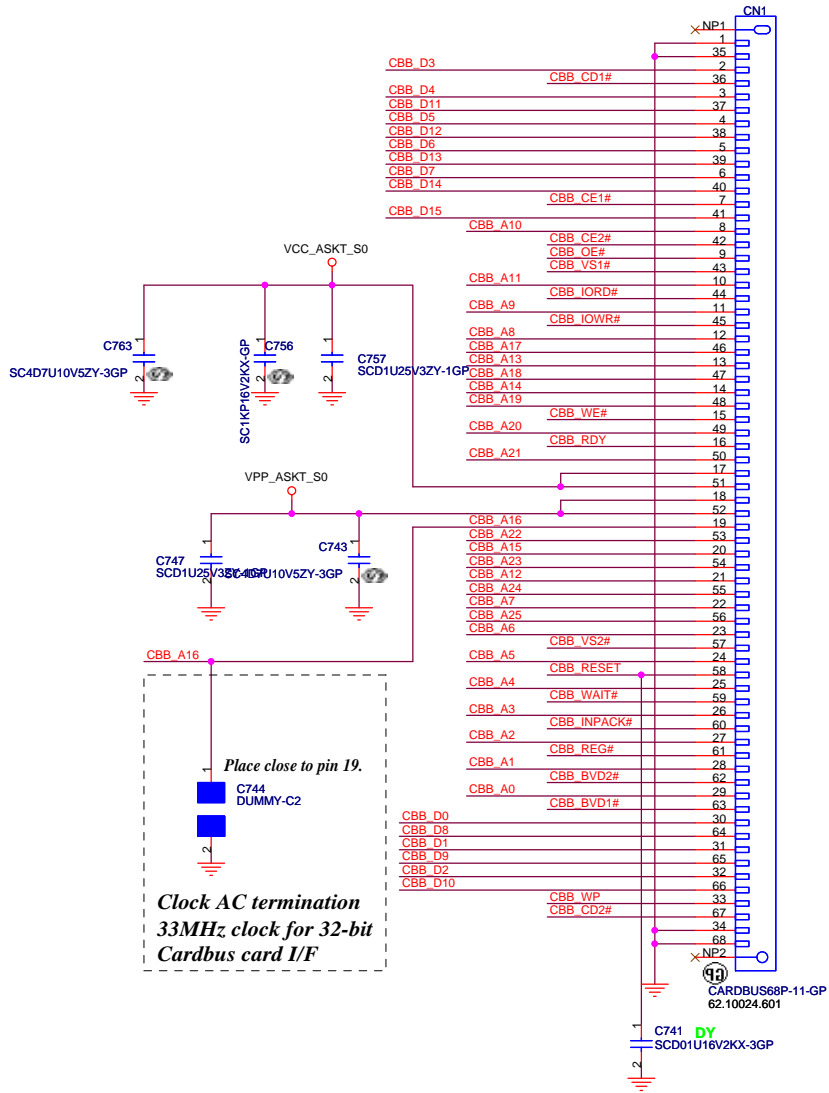
緯創資通 **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai WJ Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD / 1394 / CARD READER**

Size: **MYALL2** Rev: **MP**

Date: Friday, March 31, 2006 Sheet 26 of 57

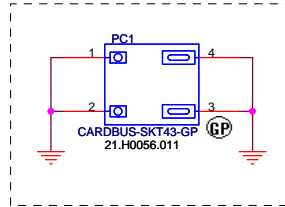
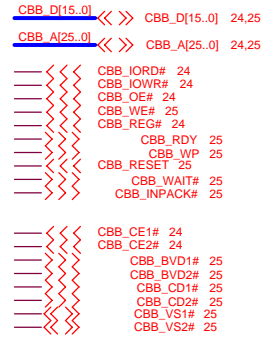
PCMCIA Socket



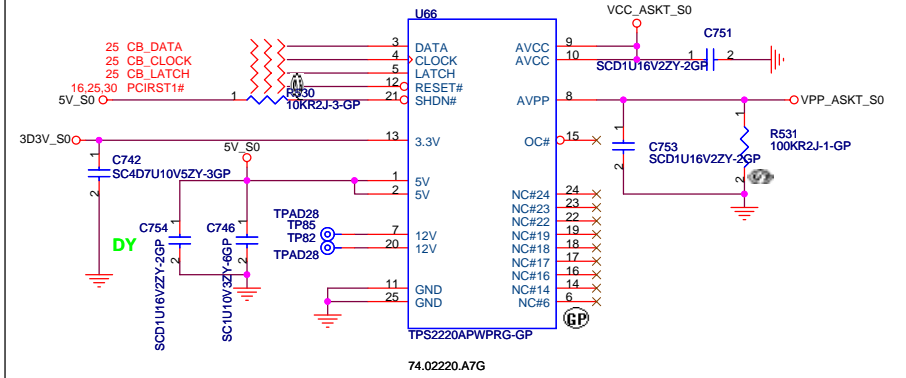
Place close to pin 19.

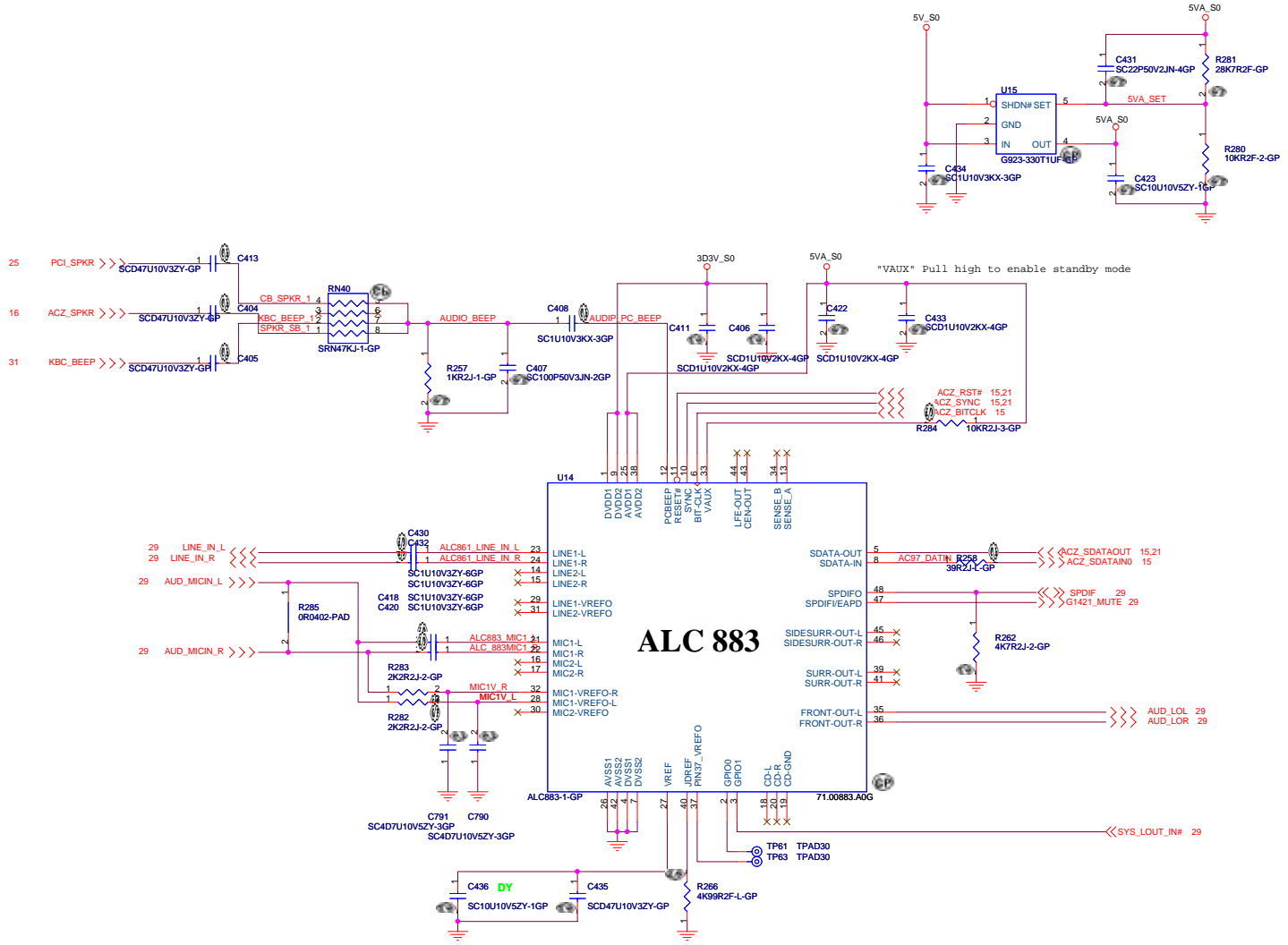
Clock AC termination
33MHz clock for 32-bit
Cardbus card I/F

Cardbus I/F

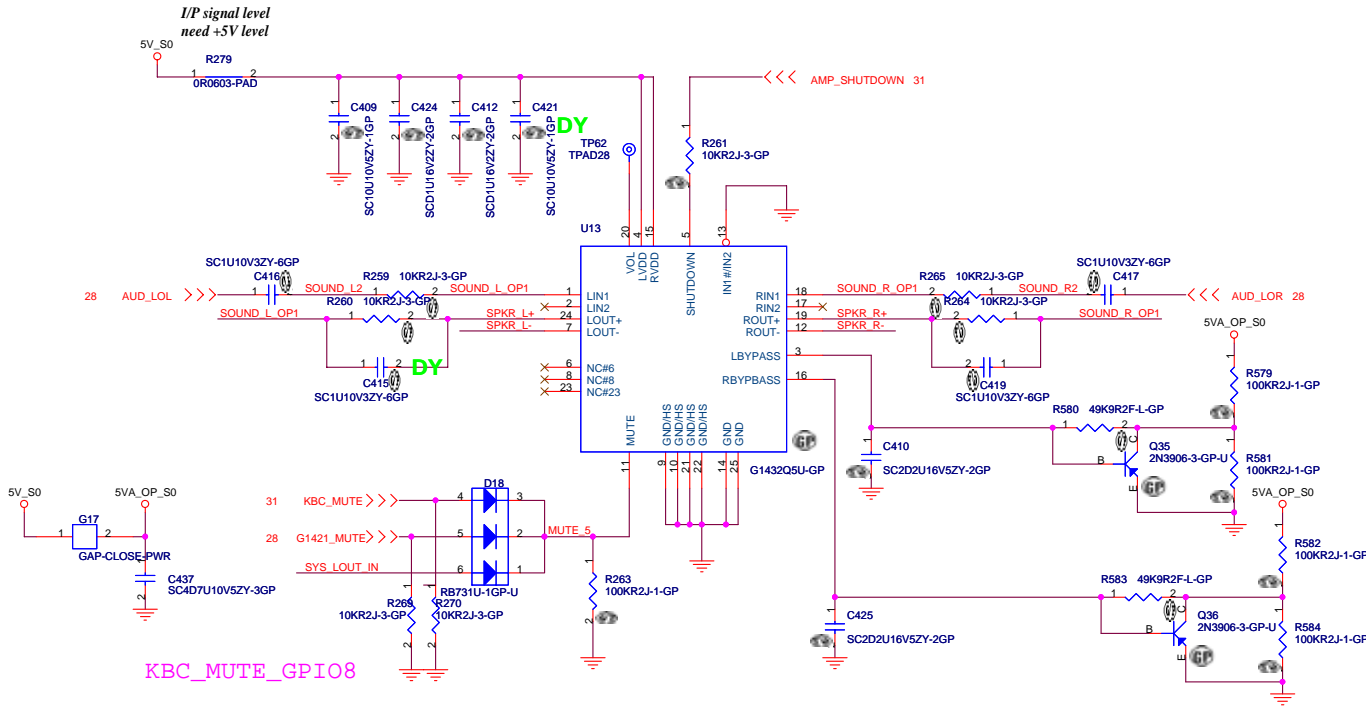


Power switch

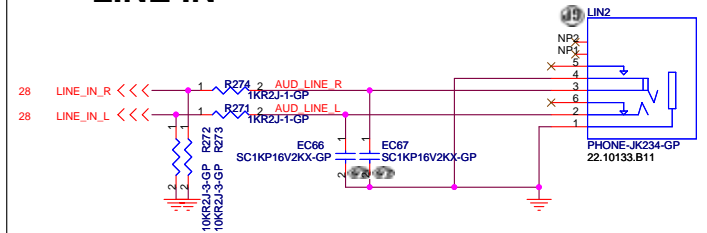




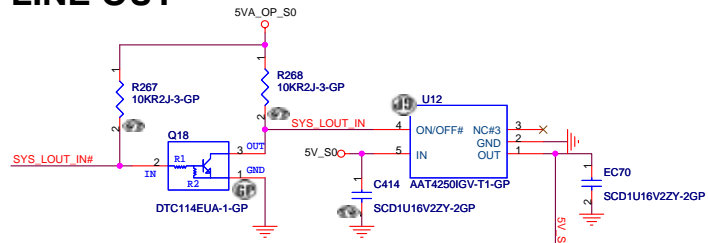
AUDIO OP AMPLIFIER



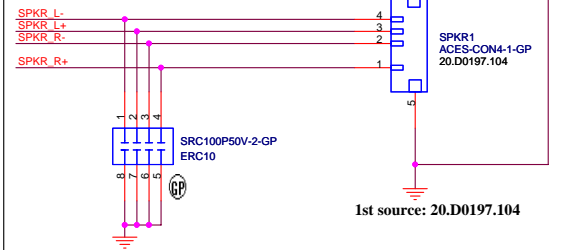
LINE IN



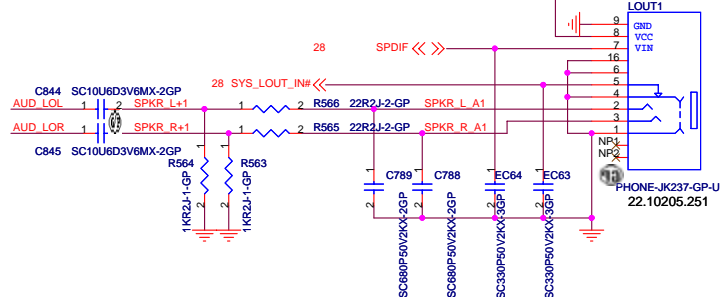
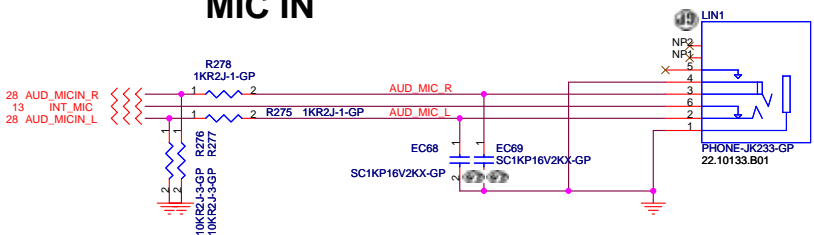
LINE OUT



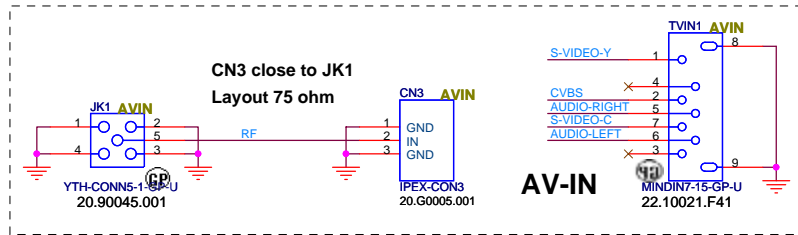
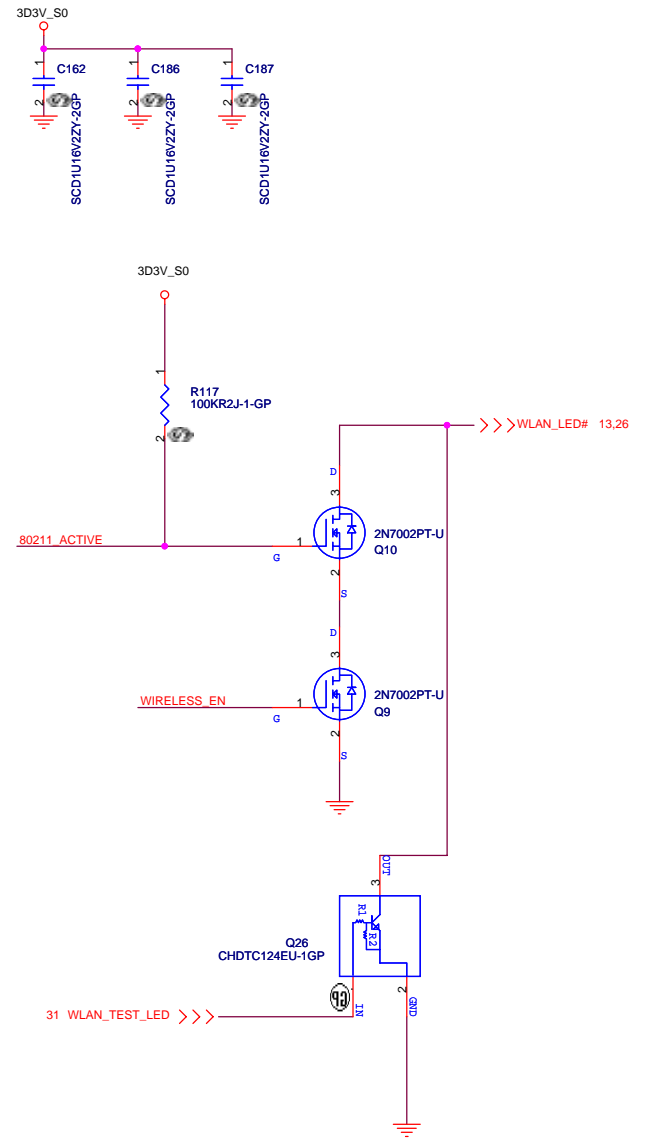
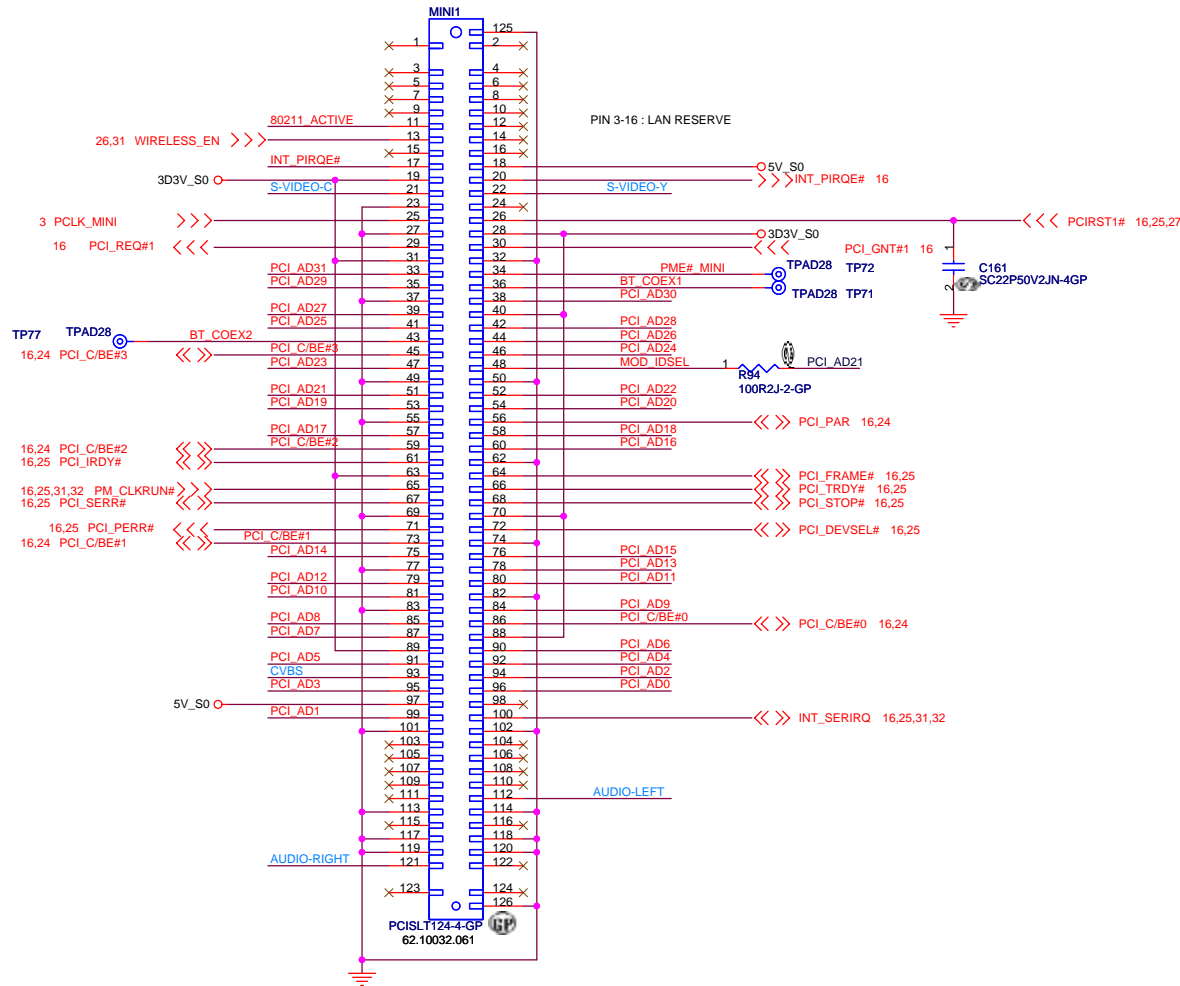
Internal Speaker

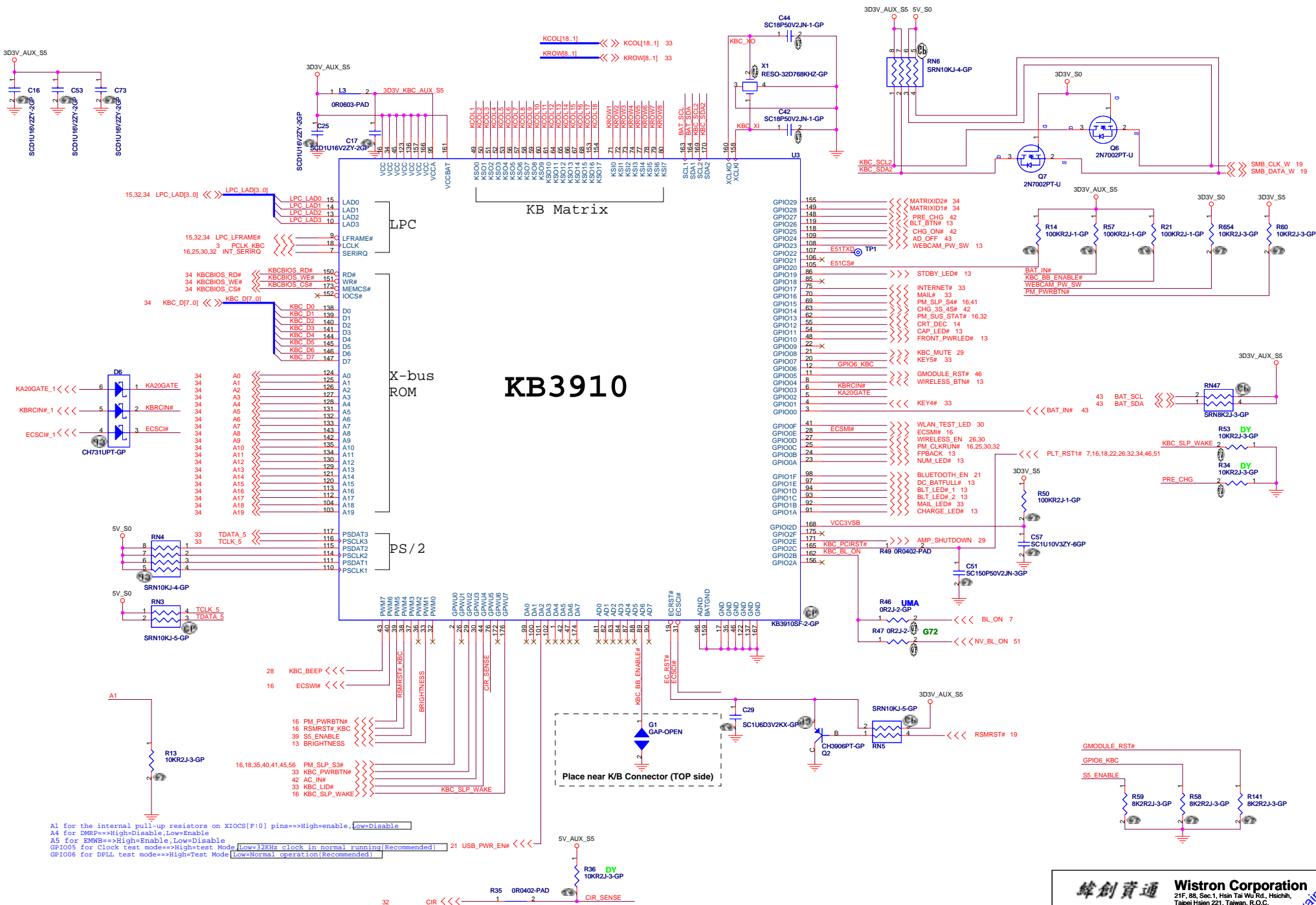


MIC IN



16,24,25 PCI_AD[31..0] <<< PCI_AD[31..0]

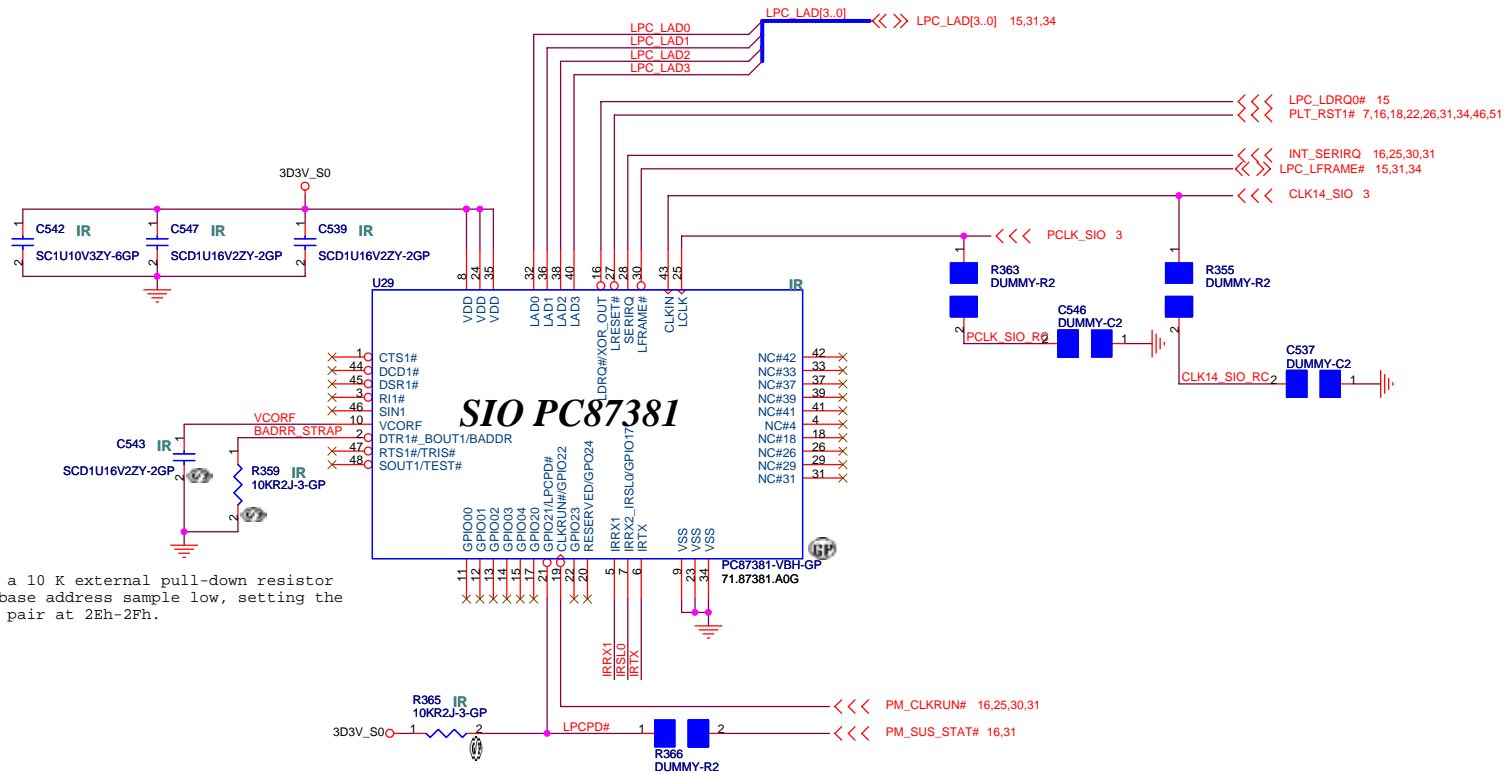




A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable, Low=Disable
 A4 for DMRF==>High=Disable, Low=Enable
 A5 for EMWB==>High=Enable, Low=Disable
 GPIO05 for Clock test mode==>High=test Mode [Low=32KHz clock in normal running Recommended]
 GPIO06 for DPLL test mode==>High=test Mode [Low=Normal operation Recommended]

Place near K/B Connector (TOP side)

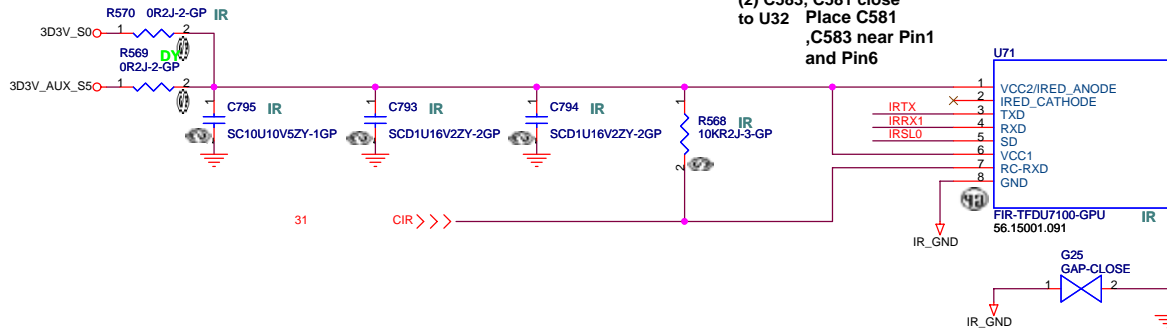
hexainf@hotmail.com



Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.

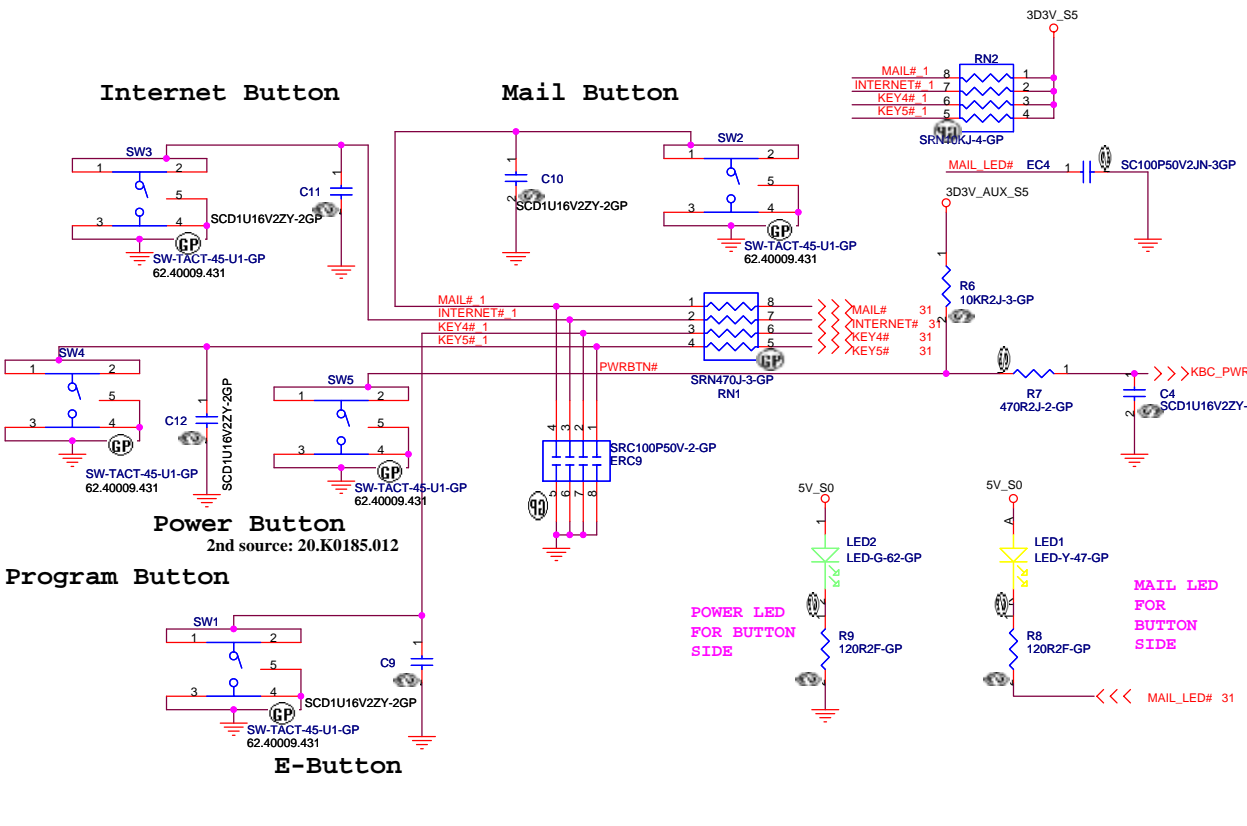
VISHAY FIR/CIR Module

- Layout Guide:
 (1) FIR_3D3V : 30 mils,
 (2) C583, C581 close
 to U32 Place C581
 , C583 near Pin1
 and Pin6

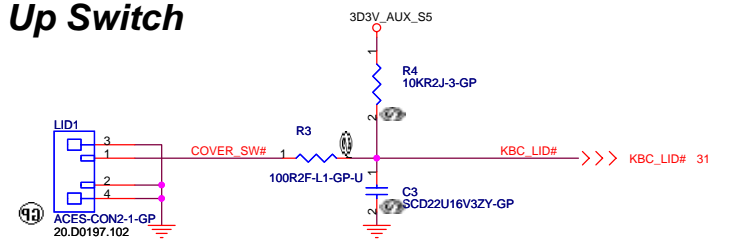


緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

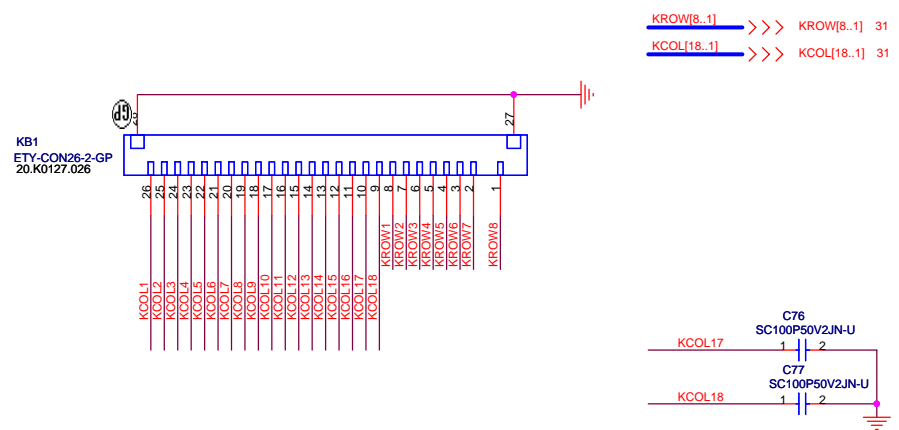
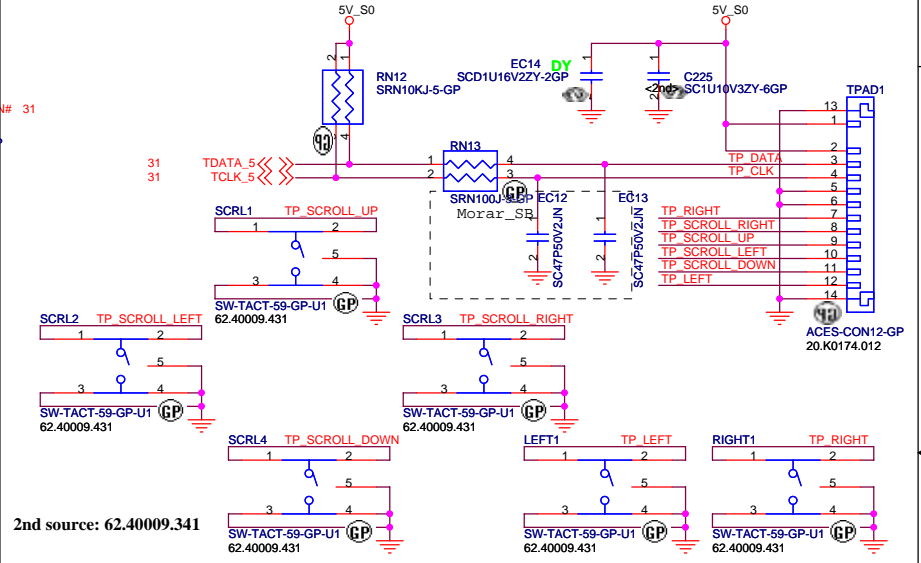
Title		
SIO 87381 / IR		
Size	Document Number	Rev
		MP
Date	Thursday, March 30, 2006	Sheet 32 of 57



Cover Up Switch



TOUCH PAD

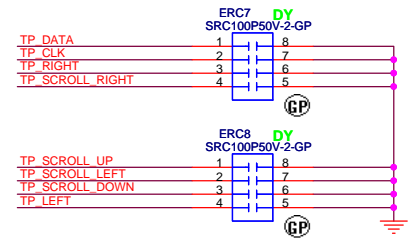
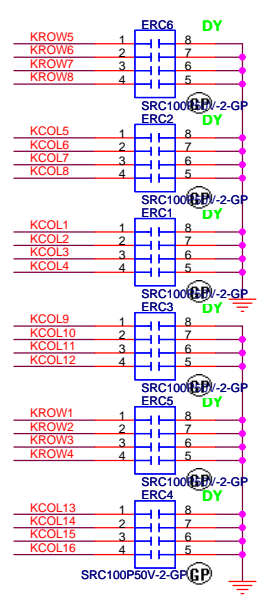


Internal KeyBoard CONN



CHECK KB SPEC. AND PIN DEFINE

EMI Bypass cap.

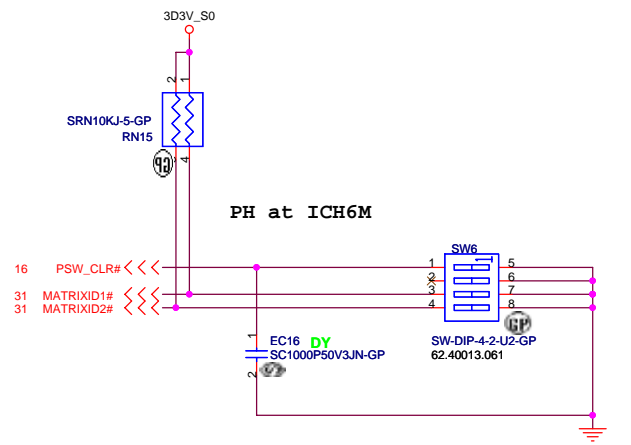
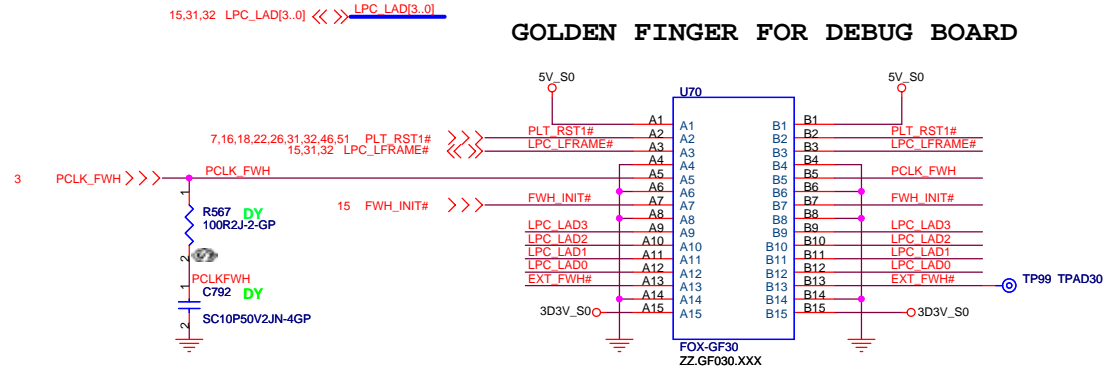
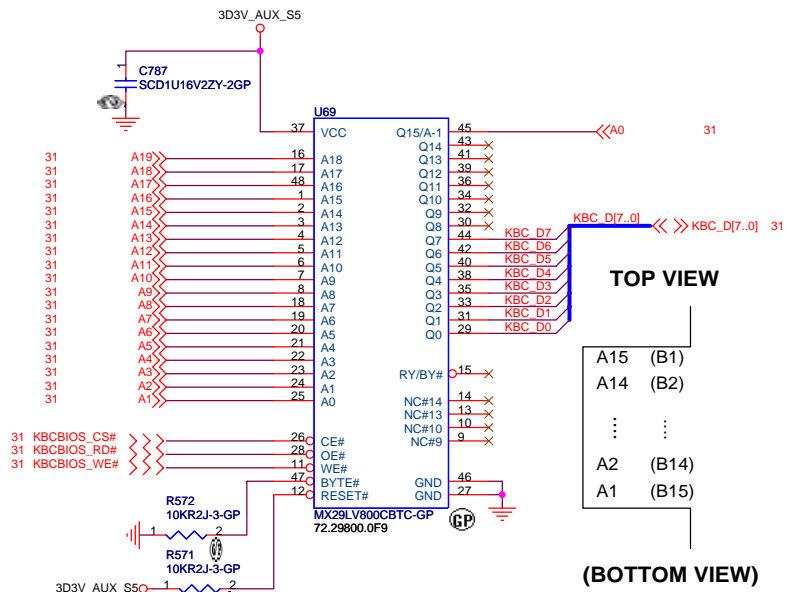


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BUTTONS / KB / TOUCHPAD**

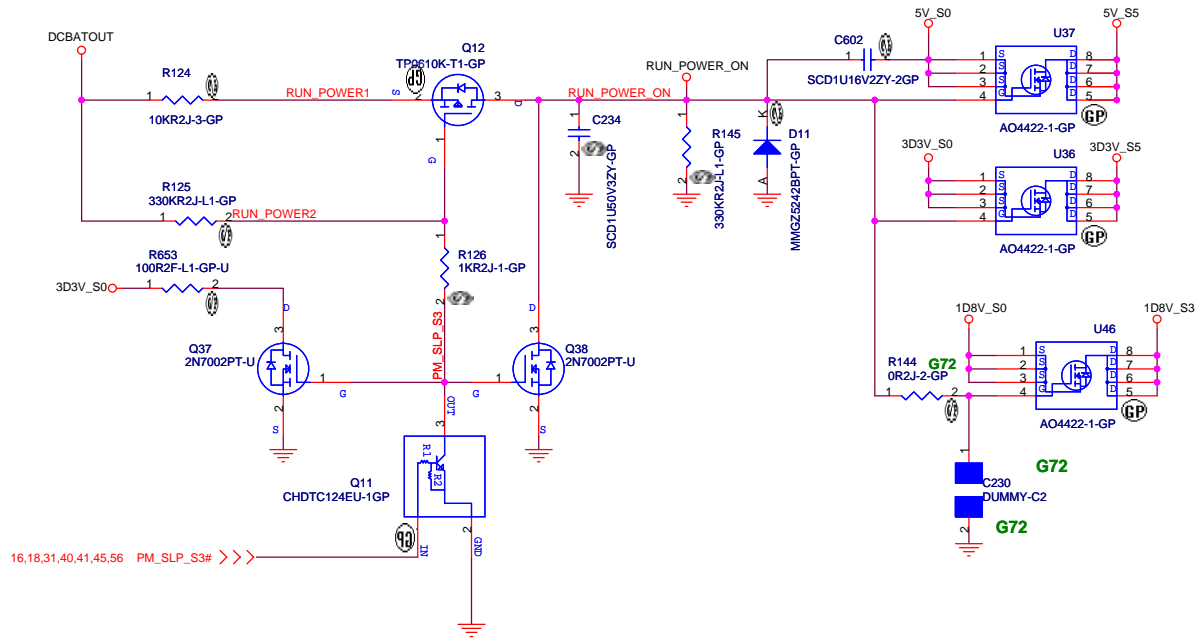
Size: Document Number: **MYALL2** Rev: **MP**

Date: Thursday, March 30, 2006 Sheet 33 of 57



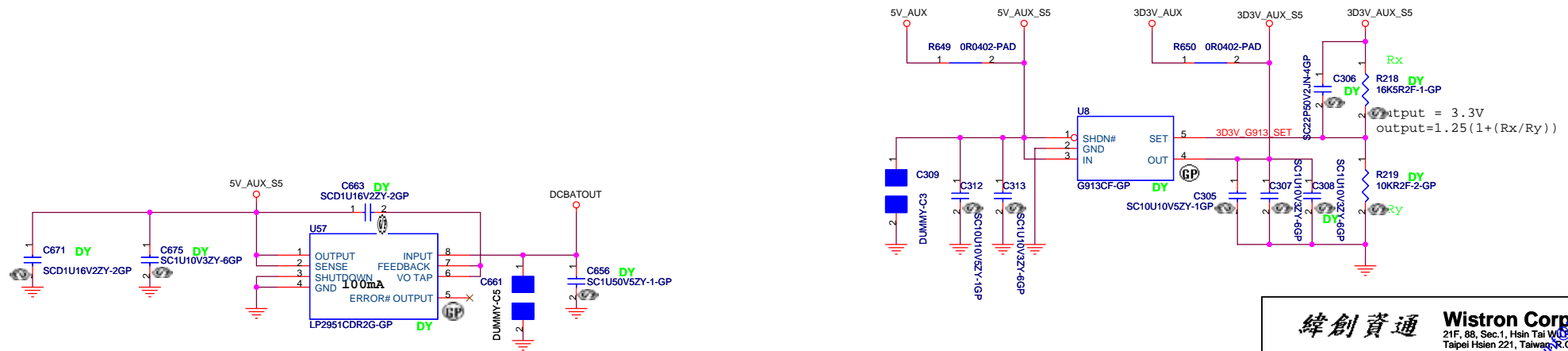
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title BIOS	
Size	Document Number MYALL2 Rev MP
Date: Thursday, March 30, 2006	Sheet 34 of 57

Run Power



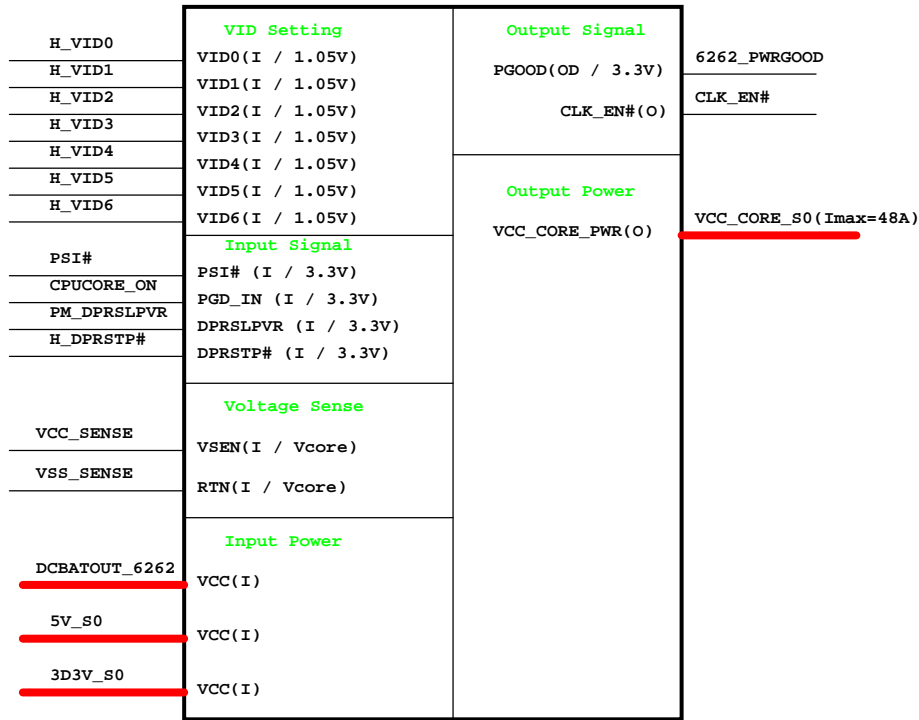
Aux Power

3D3V_AUX_S5

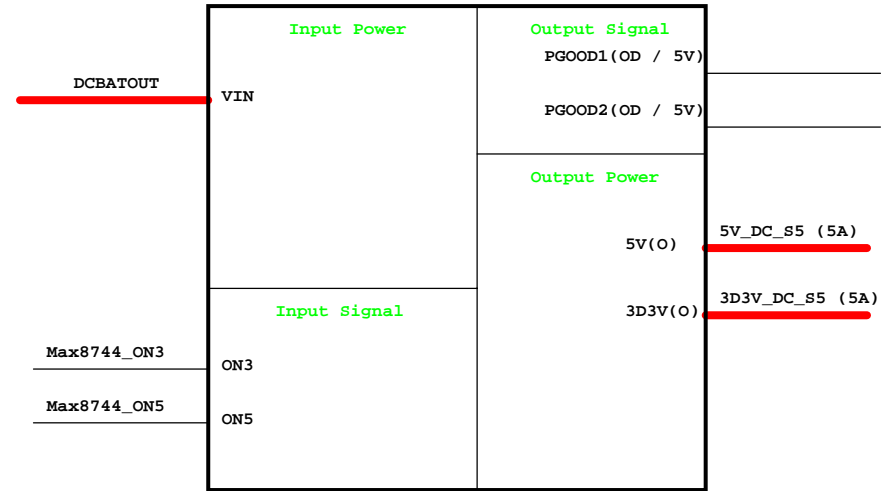


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RUN POWER and 3D3V_AUX_S5			
Size	Document Number		Rev
	MYALL2		MP
Date:	Thursday, March 30, 2006	Sheet	35 of 57

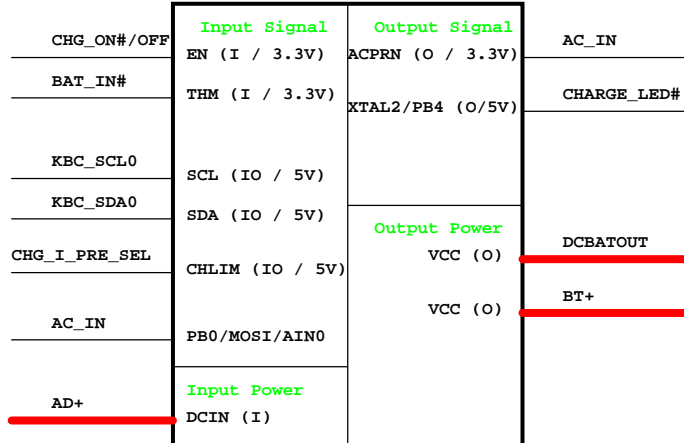
CPU_CORE
Intersil ISL6262



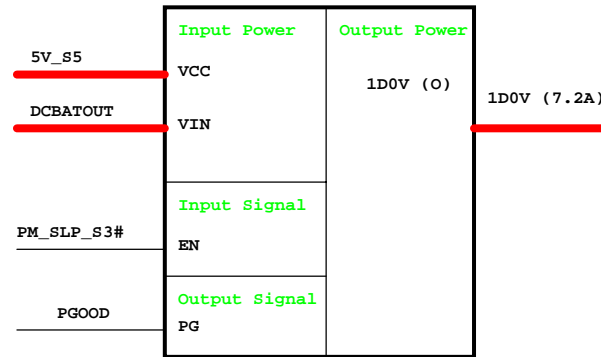
Max8744 3D3V/5V



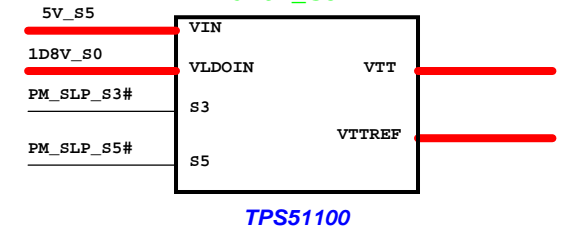
Charger_ISL6255



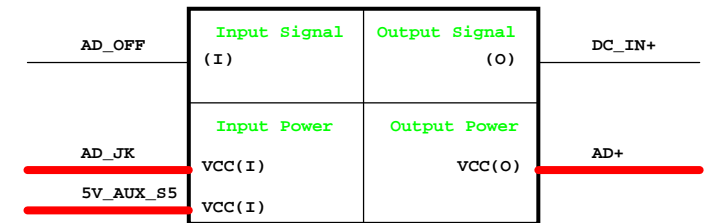
ISL6269_VGA_Core 1D0V



0D9V_S3

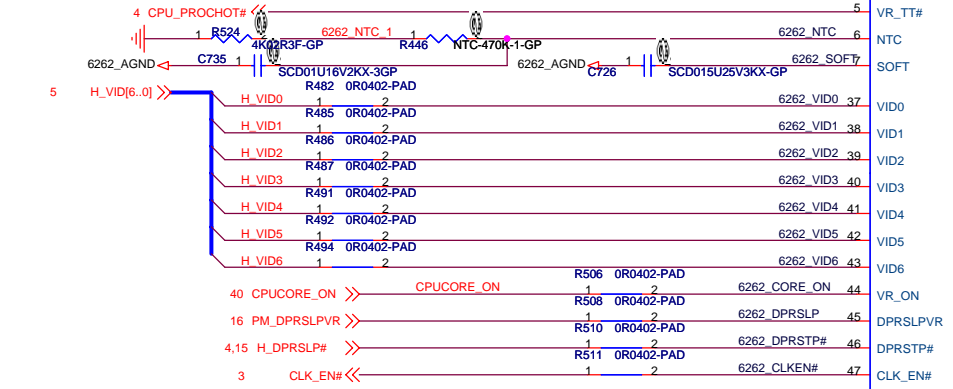


Adapter



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Place close to phase 1 choke



When test without cpu, change to 0 ohms

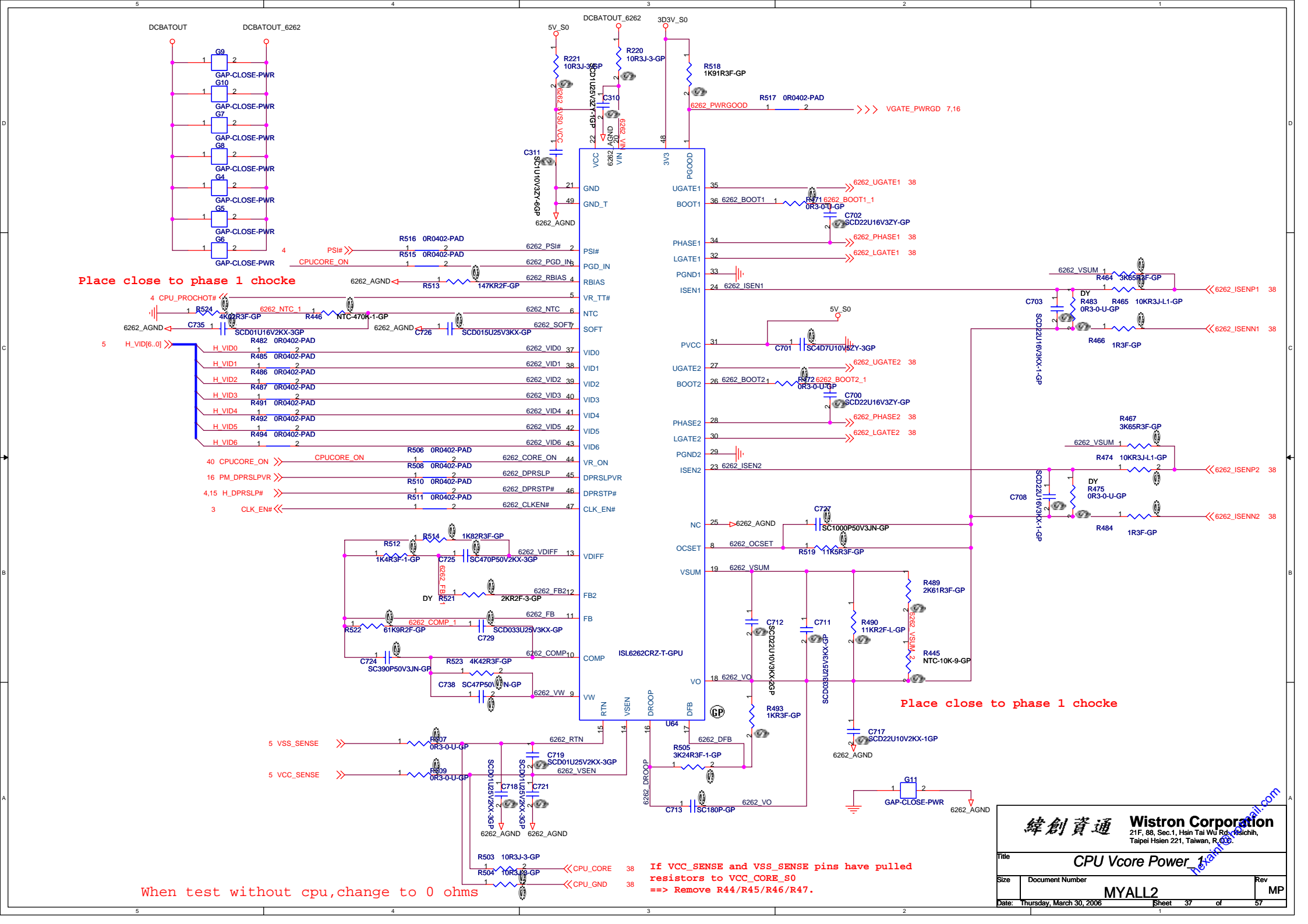
If VCC_SENSE and VSS_SENSE pins have pulled resistors to VCC_CORE_S0 ==> Remove R44/R45/R46/R47.

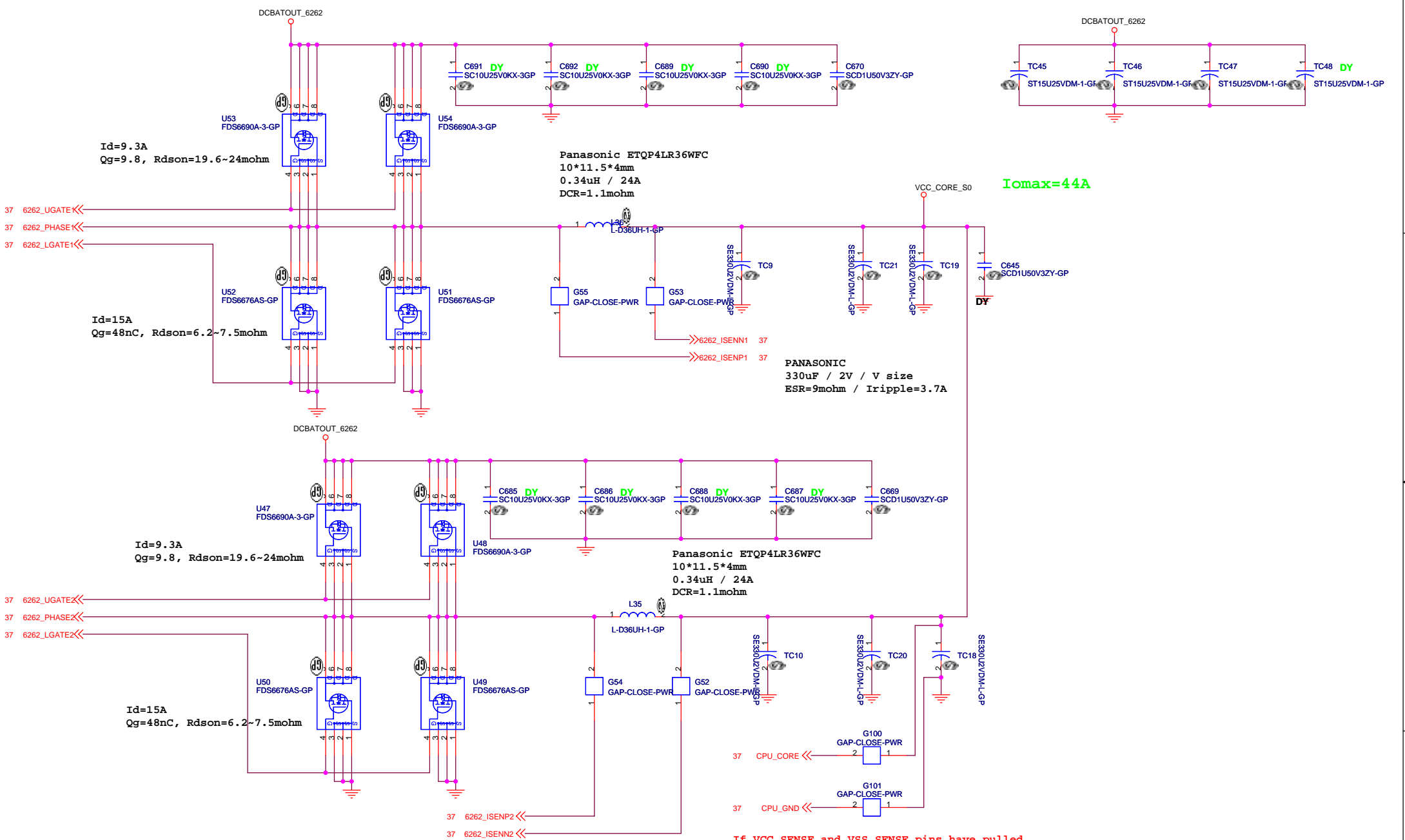
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU Vcore Power_1**

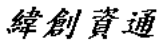
Size: Document Number: **MYALL2** Rev: **MP**

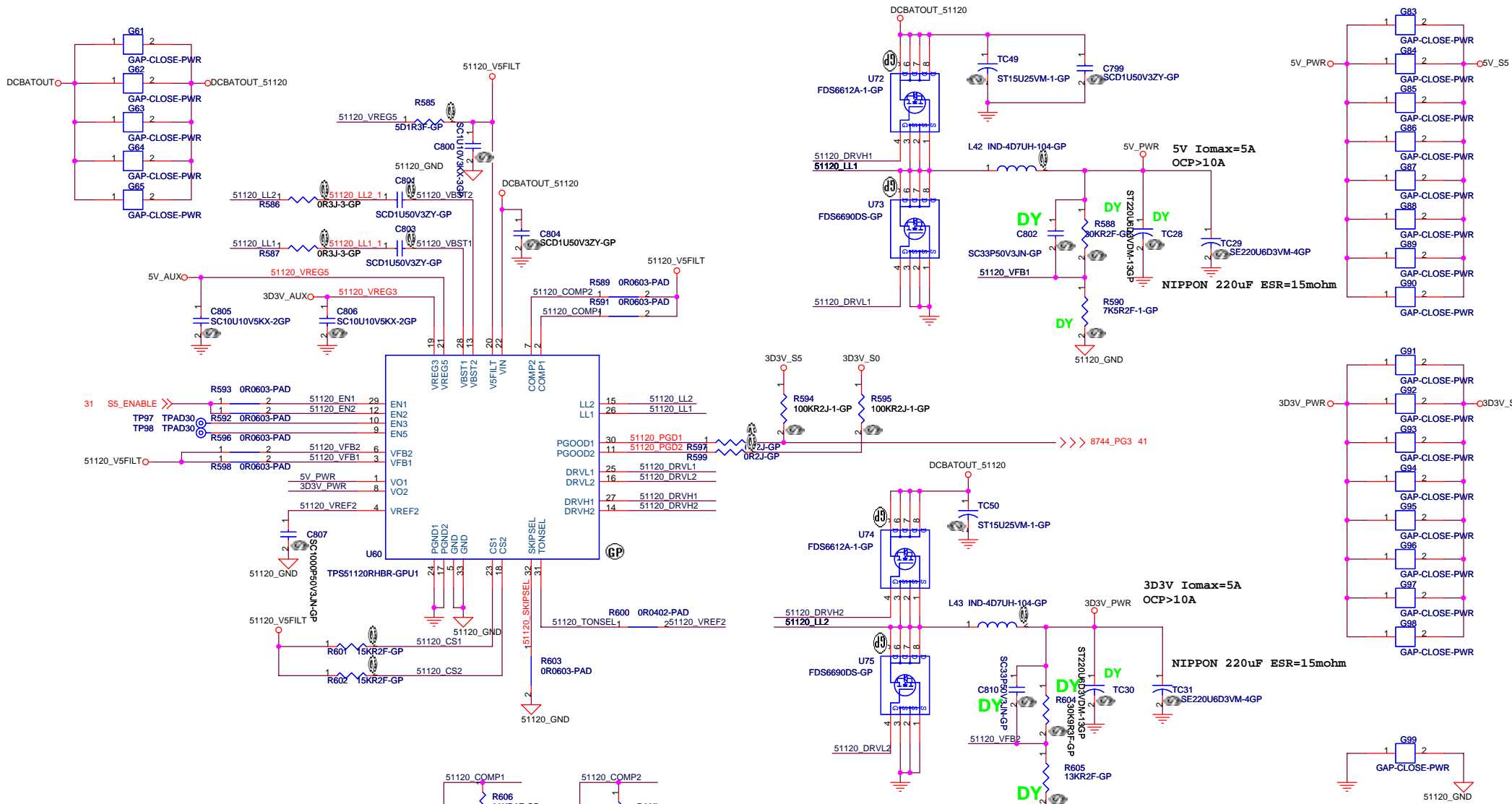
Date: Thursday, March 30, 2006 Sheet 37 of 57



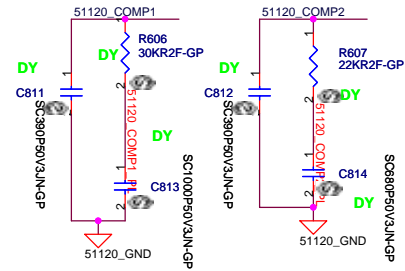


If VCC_SENSE and VSS_SENSE pins have pulled resistors to VCC_CORE_S0
 ==> Remove R44/R45/R46/R47.

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Title CPU Vcore Power_2	
Size Document Number MYALL2	Rev MP
Date: Thursday, March 30, 2006 Sheet 38 of 57	



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on



For TPS51120,
Vout=5V

- If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
- If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

- If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
- If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

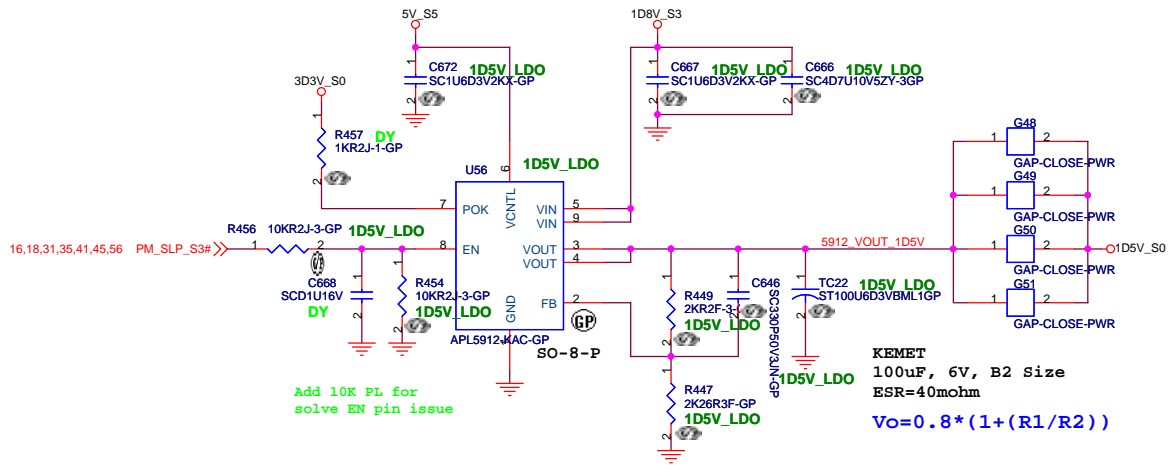
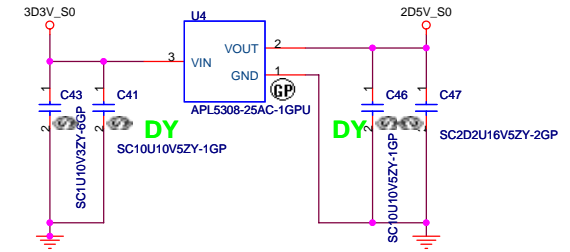
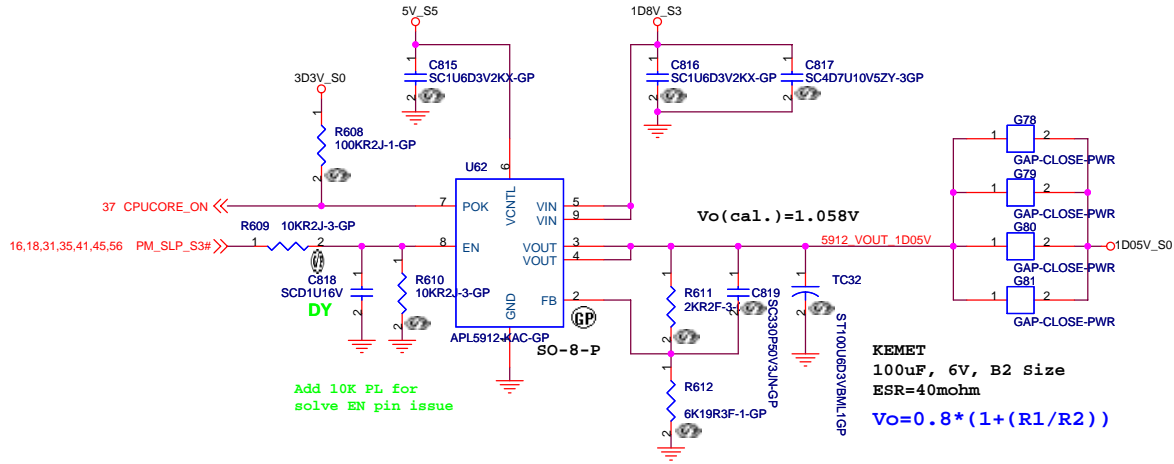
$$V_{out} = 1V \cdot \frac{R1 + R2}{R2}$$

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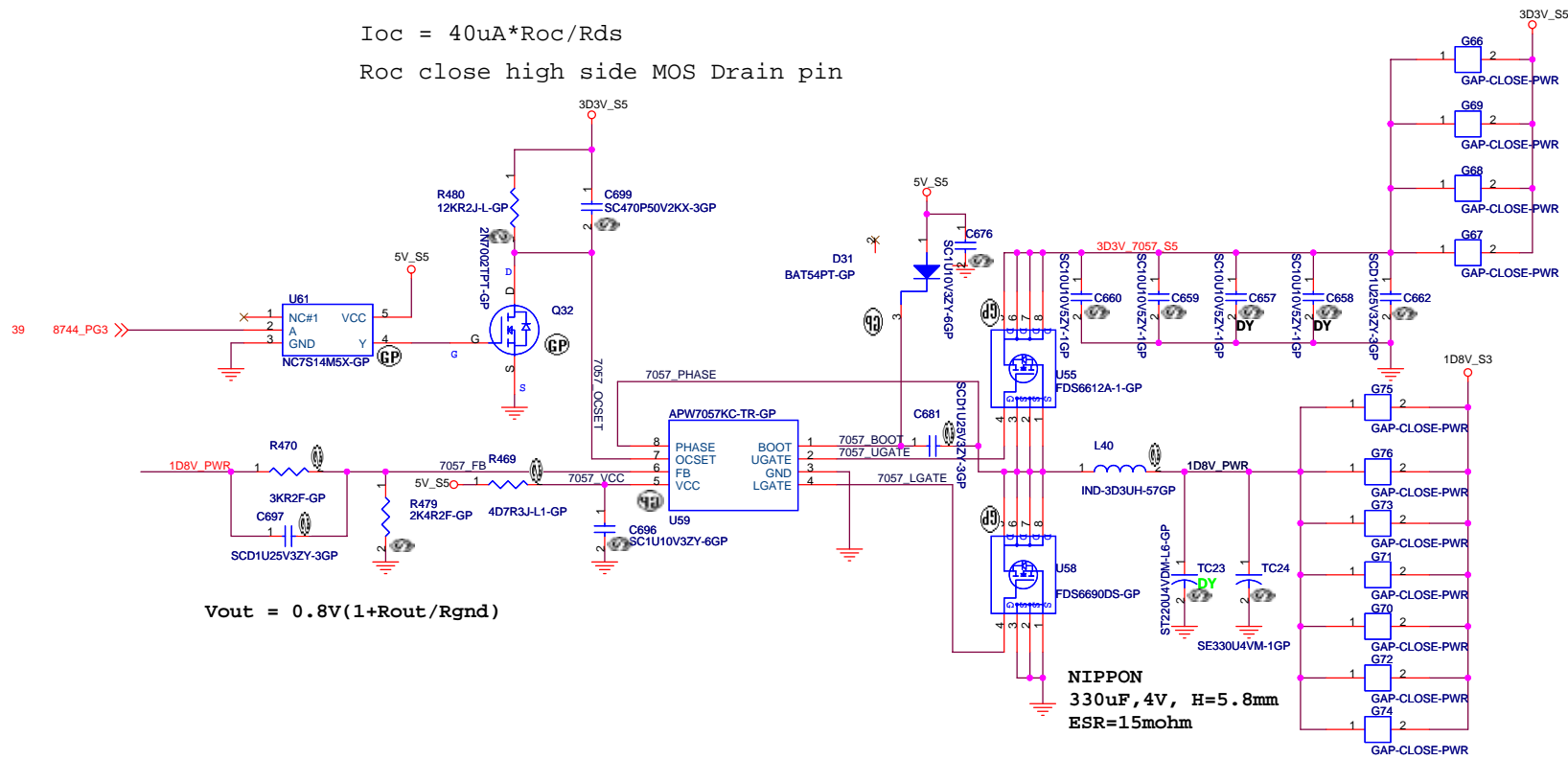
Title: **3D3V S5 & 5V S5**

Size: Document Number: **MYALL2** Rev: **MP**

Date: Thursday, March 30, 2006 Page: 39 of 57



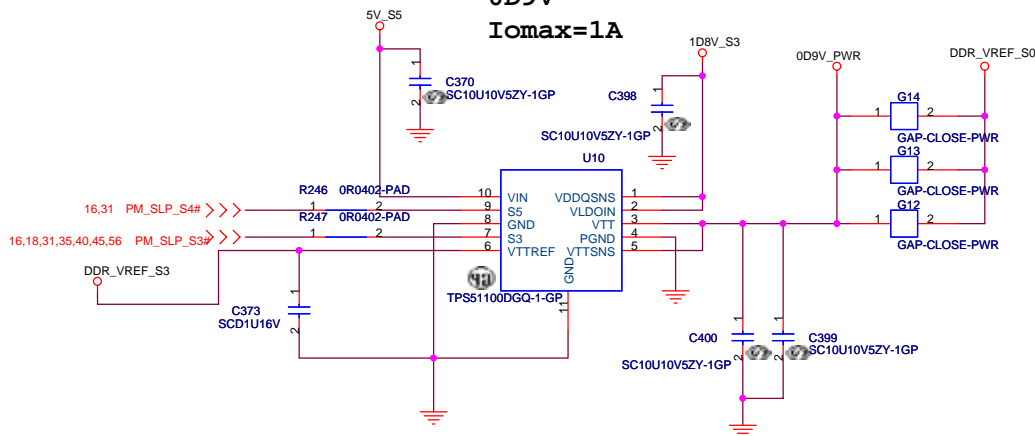
$I_{oc} = 40\mu A \cdot R_{oc} / R_{ds}$
 R_{oc} close high side MOS Drain pin

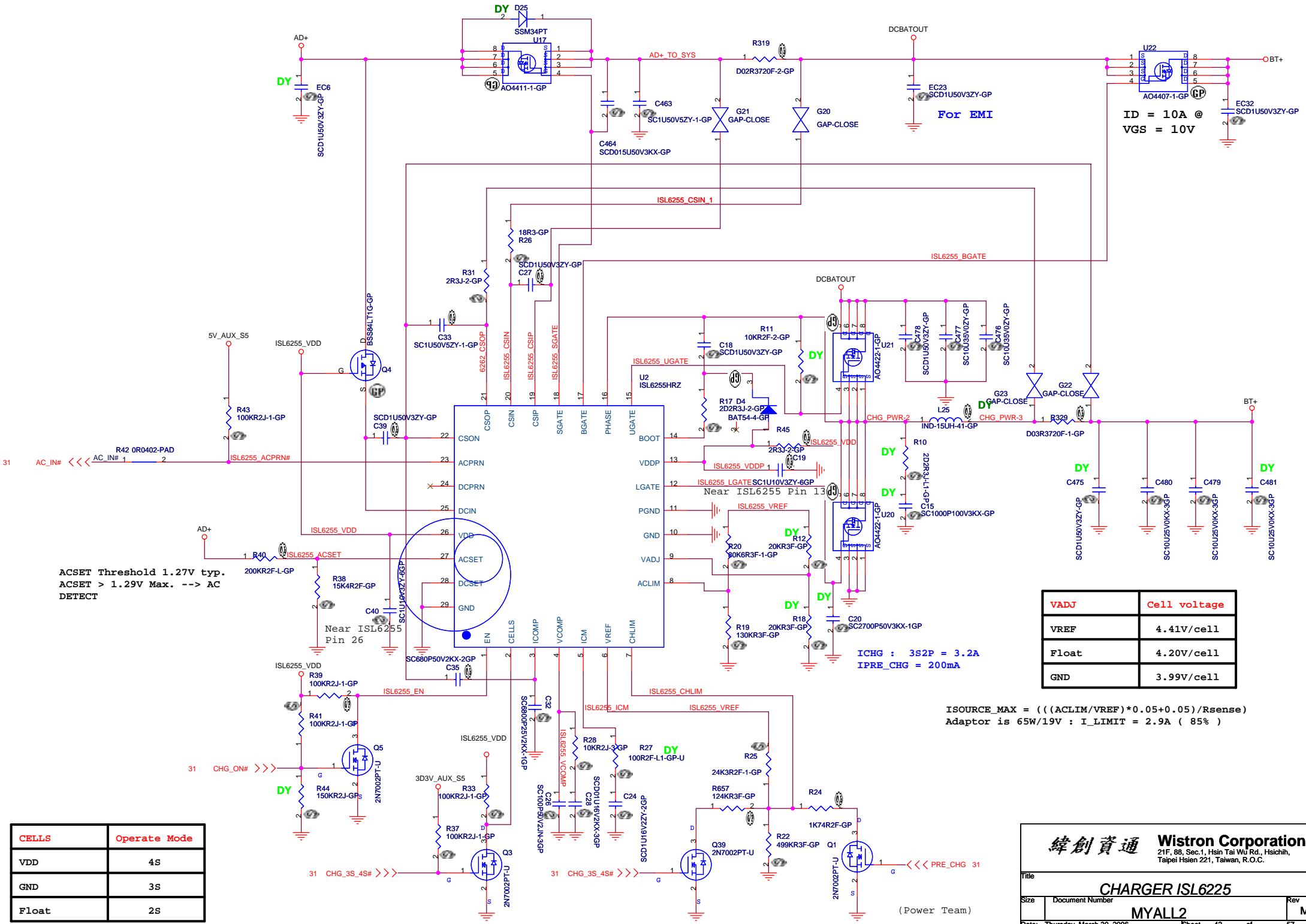


$V_{out} = 0.8V(1 + R_{out}/R_{gnd})$

NIPPON
 330uF, 4V, H=5.8mm
 ESR=15mohm

0D9V
 $I_{omax}=1A$





ACSET Threshold 1.27V typ.
 ACSET > 1.29V Max. --> AC
 DETECT

ICHG : 3S2P = 3.2A
 IPRE_CHG = 200mA

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
 Adaptor is 65W/19V : I_LIMIT = 2.9A (85%)

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

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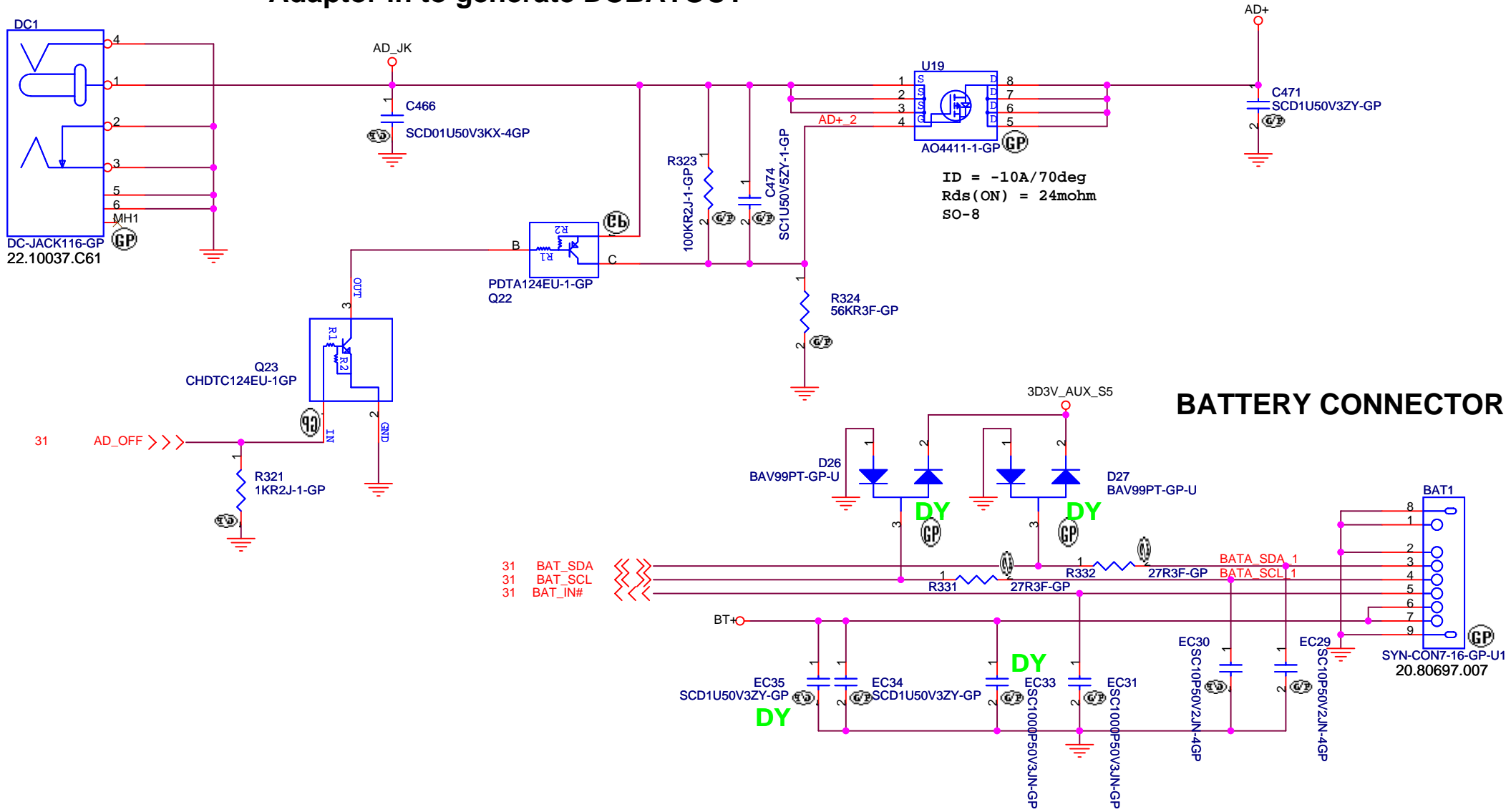
Title: **CHARGER ISL6255**

Size: Document Number: **MYALL2** Rev: **MP**

Date: Thursday, March 30, 2006 Sheet 42 of 57

(Power Team)

Adaptor in to generate DCBATOUT



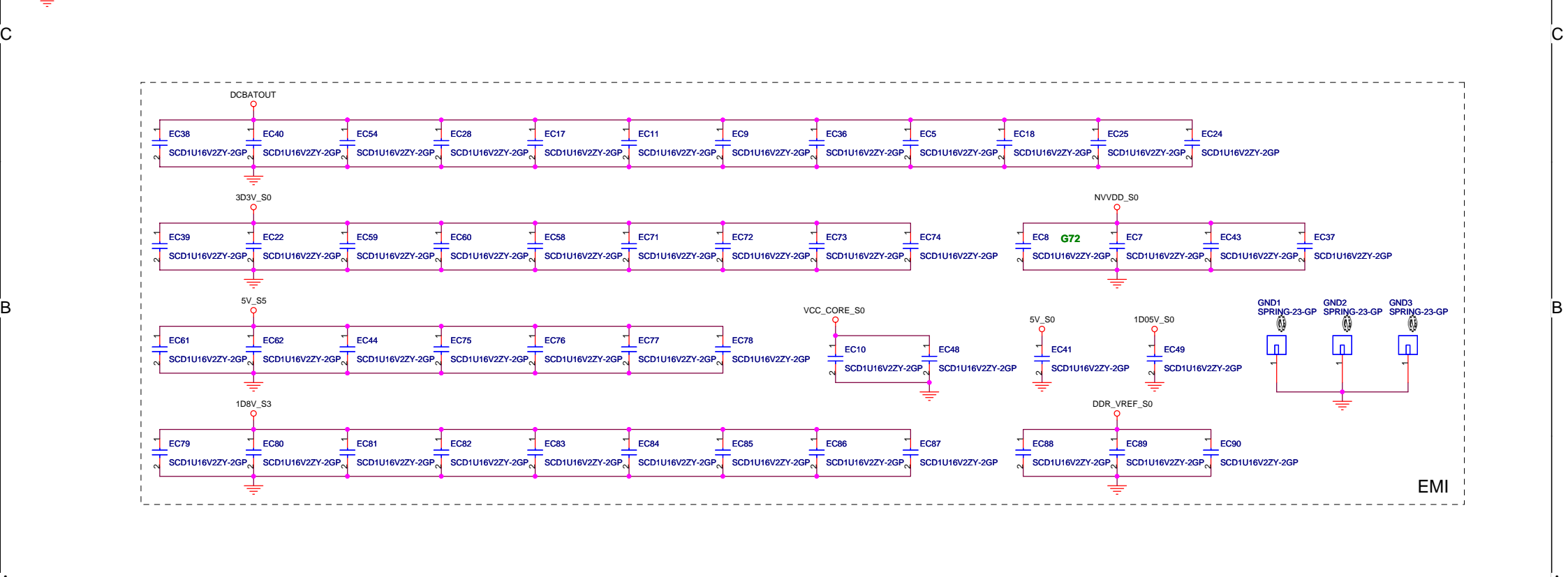
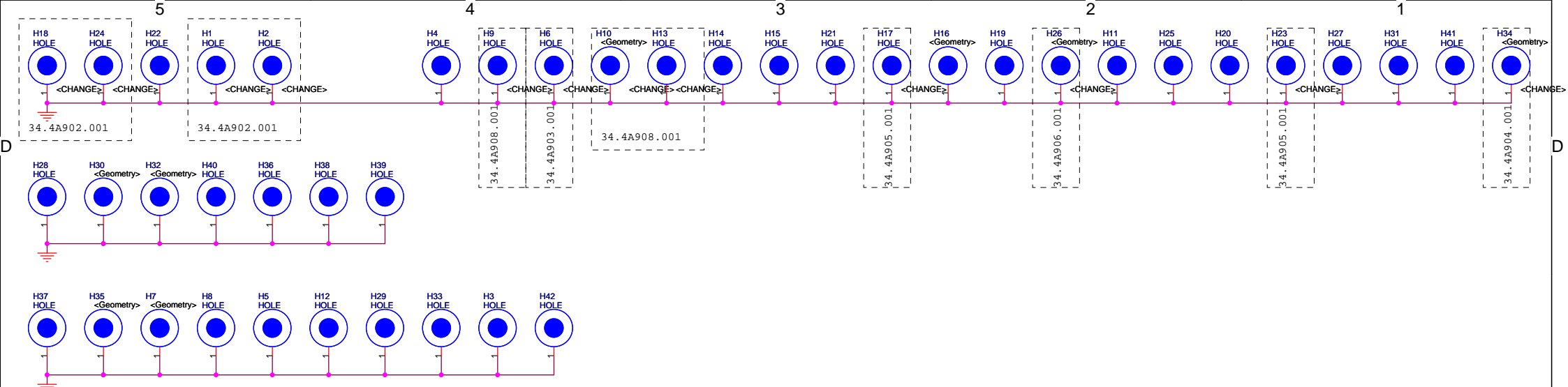
BATTERY CONNECTOR

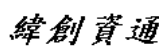
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiching
Taipei Hsien 221, Taiwan, R.O.C.

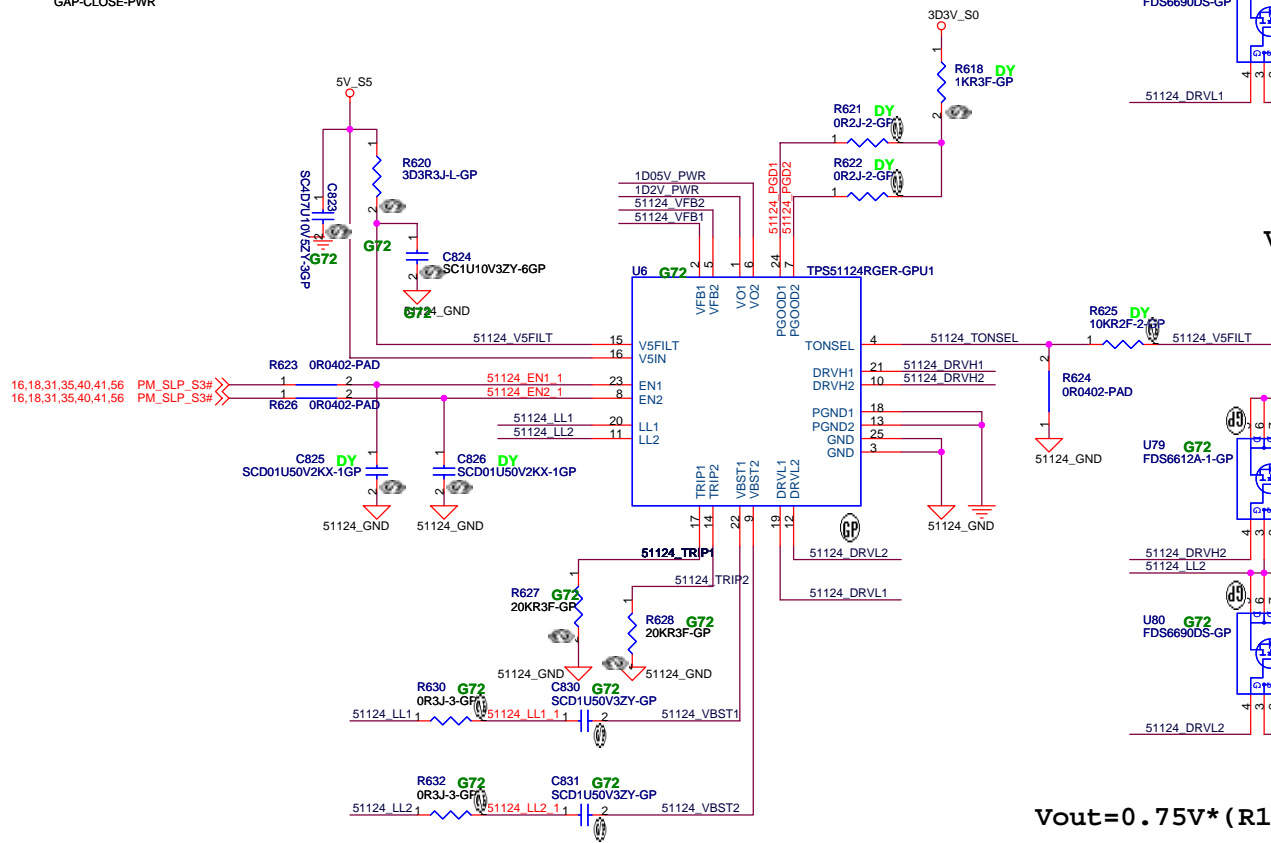
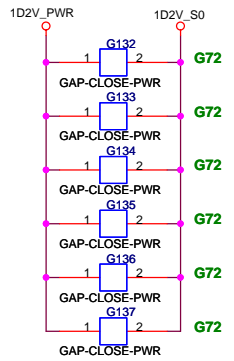
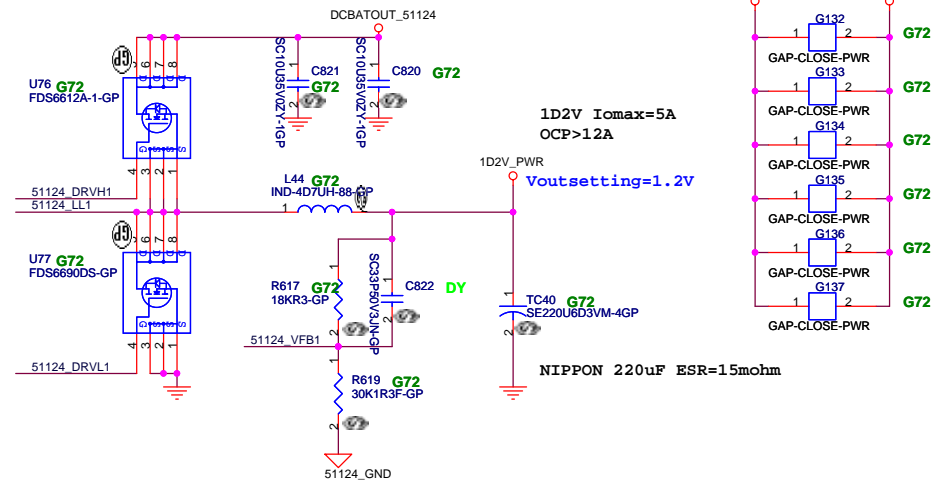
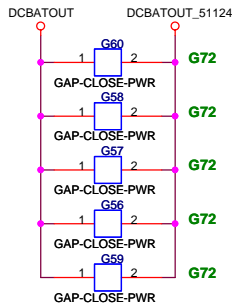
Title: **AD/BATT CONN**

Size: Document Number **MYALL2** Rev: **MP**

Date: Thursday, March 30, 2006 Sheet 43 of 57

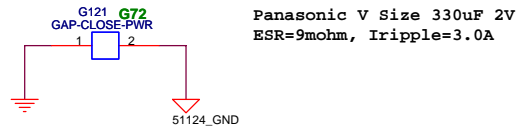


 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
EMI	
Size	Document Number
MYALL2	
Date: Friday, March 24, 2006	Rev MP
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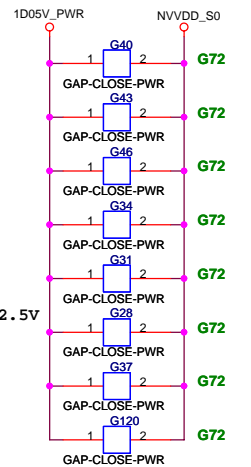


$$V_{out} = 0.75V * (R1 + R2) / R2$$

$$V_{out} = 0.75V * (R1 + R2) / R2$$



Panasonic V Size 330uF 2V
ESR=9mohm, Iripple=3.0A



<Variant Name>

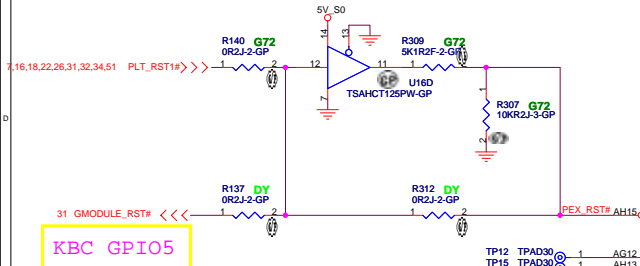
緯創資通 Wistron Corporation
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Title: **TPS51124 / NVDD / 1D2V**

Size: Document Number **MYALL2** Rev: **MP**

Date: Thursday, March 30, 2006 Sheet 45 of 57

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2



KBC GPIO5

3 CLK_PCIE_PEG >>> CLK_PCIE_PEG
 3 CLK_PCIE_PEG# >>> CLK_PCIE_PEG#

7 PEG_TXN[15..0] >>> PEG_TXN[15..0]
 7 PEG_TXP[15..0] >>> PEG_TXP[15..0]
 7 PEG_RXN[15..0] <<< PEG_RXN[15..0]
 7 PEG_RXP[15..0] <<< PEG_RXP[15..0]

- PEG_RXP0 1 >>> SCD1U10V2KX-5GP PEX_TX0# AH15
- PEG_RXN0 1 >>> SCD1U10V2KX-5GP PEX_TX0# AK15
- PEG_TXP0 >>> SCD1U10V2KX-5GP PEX_TX0# AK13
- PEG_TXN0 >>> SCD1U10V2KX-5GP PEX_TX0# AK14
- PEG_RXP1 1 >>> SCD1U10V2KX-5GP PEX_TX1# AH16
- PEG_RXN1 1 >>> SCD1U10V2KX-5GP PEX_TX1# AH16
- PEG_TXP1 >>> SCD1U10V2KX-5GP PEX_TX1# AM14
- PEG_TXN1 >>> SCD1U10V2KX-5GP PEX_TX1# AM15
- PEG_RXP2 1 >>> SCD1U10V2KX-5GP PEX_TX2# AG17
- PEG_RXN2 1 >>> SCD1U10V2KX-5GP PEX_TX2# AH17
- PEG_TXP2 >>> SCD1U10V2KX-5GP PEX_TX2# AL15
- PEG_TXN2 >>> SCD1U10V2KX-5GP PEX_TX2# AL16
- PEG_RXP3 1 >>> SCD1U10V2KX-5GP PEX_TX3# AG18
- PEG_RXN3 1 >>> SCD1U10V2KX-5GP PEX_TX3# AH18
- PEG_TXP3 >>> SCD1U10V2KX-5GP PEX_TX3# AK16
- PEG_TXN3 >>> SCD1U10V2KX-5GP PEX_TX3# AK17
- PEG_RXP4 1 >>> SCD1U10V2KX-5GP PEX_TX4# AK18
- PEG_RXN4 1 >>> SCD1U10V2KX-5GP PEX_TX4# AJ18
- PEG_TXP4 >>> SCD1U10V2KX-5GP PEX_TX4# AL17
- PEG_TXN4 >>> SCD1U10V2KX-5GP PEX_TX4# AL18
- PEG_RXP5 1 >>> SCD1U10V2KX-5GP PEX_TX5# AJ19
- PEG_RXN5 1 >>> SCD1U10V2KX-5GP PEX_TX5# AH19
- PEG_TXP5 >>> SCD1U10V2KX-5GP PEX_TX5# AM18
- PEG_TXN5 >>> SCD1U10V2KX-5GP PEX_TX5# AM19
- PEG_RXP6 1 >>> SCD1U10V2KX-5GP PEX_TX6# AG20
- PEG_RXN6 1 >>> SCD1U10V2KX-5GP PEX_TX6# AH20
- PEG_TXP6 >>> SCD1U10V2KX-5GP PEX_TX6# AK19
- PEG_TXN6 >>> SCD1U10V2KX-5GP PEX_TX6# AK20
- PEG_RXP7 1 >>> SCD1U10V2KX-5GP PEX_TX7# AG21
- PEG_RXN7 1 >>> SCD1U10V2KX-5GP PEX_TX7# AH21
- PEG_TXP7 >>> SCD1U10V2KX-5GP PEX_TX7# AL20
- PEG_TXN7 >>> SCD1U10V2KX-5GP PEX_TX7# AL21
- PEG_RXP8 1 >>> SCD1U10V2KX-5GP PEX_TX8# AK21
- PEG_RXN8 1 >>> SCD1U10V2KX-5GP PEX_TX8# AJ21
- PEG_TXP8 >>> SCD1U10V2KX-5GP PEX_TX8# AM21
- PEG_TXN8 >>> SCD1U10V2KX-5GP PEX_TX8# AM22
- PEG_RXP9 1 >>> SCD1U10V2KX-5GP PEX_TX9# AJ22
- PEG_RXN9 1 >>> SCD1U10V2KX-5GP PEX_TX9# AH22
- PEG_TXP9 >>> SCD1U10V2KX-5GP PEX_TX9# AK22
- PEG_TXN9 >>> SCD1U10V2KX-5GP PEX_TX9# AK23
- PEG_RXP10 1 >>> SCD1U10V2KX-5GP PEX_TX10# AG23
- PEG_RXN10 1 >>> SCD1U10V2KX-5GP PEX_TX10# AH23
- PEG_TXP10 >>> SCD1U10V2KX-5GP PEX_TX10# AL23
- PEG_TXN10 >>> SCD1U10V2KX-5GP PEX_TX10# AL24
- PEG_RXP11 1 >>> SCD1U10V2KX-5GP PEX_TX11# AK24
- PEG_RXN11 1 >>> SCD1U10V2KX-5GP PEX_TX11# AJ24
- PEG_TXP11 >>> SCD1U10V2KX-5GP PEX_TX11# AM24
- PEG_TXN11 >>> SCD1U10V2KX-5GP PEX_TX11# AM25
- PEG_RXP12 1 >>> SCD1U10V2KX-5GP PEX_TX12# AJ25
- PEG_RXN12 1 >>> SCD1U10V2KX-5GP PEX_TX12# AH25
- PEG_TXP12 >>> SCD1U10V2KX-5GP PEX_TX12# AK25
- PEG_TXN12 >>> SCD1U10V2KX-5GP PEX_TX12# AK26
- PEG_RXP13 1 >>> SCD1U10V2KX-5GP PEX_TX13# AH26
- PEG_RXN13 1 >>> SCD1U10V2KX-5GP PEX_TX13# AG26
- PEG_TXP13 >>> SCD1U10V2KX-5GP PEX_TX13# AL26
- PEG_TXN13 >>> SCD1U10V2KX-5GP PEX_TX13# AL27
- PEG_RXP14 1 >>> SCD1U10V2KX-5GP PEX_TX14# AK27
- PEG_RXN14 1 >>> SCD1U10V2KX-5GP PEX_TX14# AJ27
- PEG_TXP14 >>> SCD1U10V2KX-5GP PEX_TX14# AM27
- PEG_TXN14 >>> SCD1U10V2KX-5GP PEX_TX14# AM28
- PEG_RXP15 1 >>> SCD1U10V2KX-5GP PEX_TX15# AJ28
- PEG_RXN15 1 >>> SCD1U10V2KX-5GP PEX_TX15# AH27
- PEG_TXP15 >>> SCD1U10V2KX-5GP PEX_TX15# AL28
- PEG_TXN15 >>> SCD1U10V2KX-5GP PEX_TX15# AL29

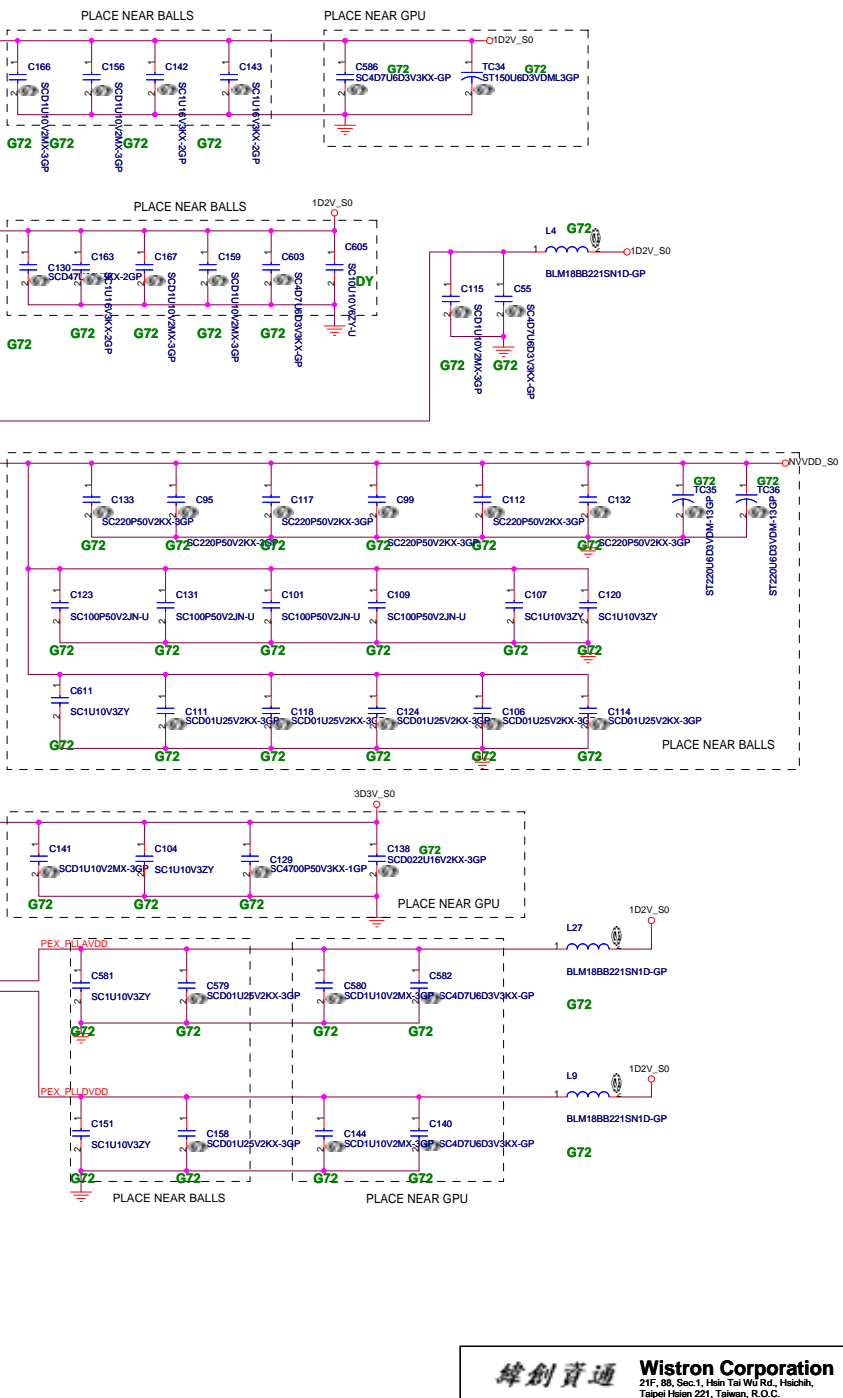
G72

- PEX_IOVDD0_0 AD23
- PEX_IOVDD0_1 AE23
- PEX_IOVDD0_2 AE24
- PEX_IOVDD0_3 AE25
- PEX_IOVDD0_4 AG24
- PEX_IOVDD0_5 AG25
- PEX_IOVDDQ_0 AC16
- PEX_IOVDDQ_1 AC17
- PEX_IOVDDQ_2 AC21
- PEX_IOVDDQ_3 AC22
- PEX_IOVDDQ_4 AE18
- PEX_IOVDDQ_5 AE21
- PEX_IOVDDQ_6 AE22
- PEX_IOVDDQ_7 AE18
- PEX_IOVDDQ_8 AE21
- PEX_IOVDDQ_9 AE22
- PEX_IOVDDQ_10 AE22

- VDD_0 K16
- VDD_1 K17
- VDD_2 N14
- VDD_3 N14
- VDD_4 N15
- VDD_5 N17
- VDD_6 N19
- VDD_7 N20
- VDD_8 P14
- VDD_9 P14
- VDD_10 P16
- VDD_11 P19
- VDD_12 P19
- VDD_13 R16
- VDD_14 T14
- VDD_15 T15
- VDD_16 T14
- VDD_17 T18
- VDD_18 T19
- VDD_19 T19
- VDD_20 U13
- VDD_21 U14
- VDD_22 U18
- VDD_23 U18
- VDD_24 U19
- VDD_25 U15
- VDD_26 U15
- VDD_27 W13
- VDD_28 W16
- VDD_29 W16
- VDD_30 W17
- VDD_31 W19
- VDD_32 Y13
- VDD_33 Y14
- VDD_34 Y17
- VDD_35 Y17
- VDD_36 Y19
- VDD_37 Y20
- VDD_LP_0 P20
- VDD_LP_1 T20
- VDD_LP_2 T23
- VDD_LP_3 U20
- VDD_LP_4 U20
- VDD_LP_5 W20

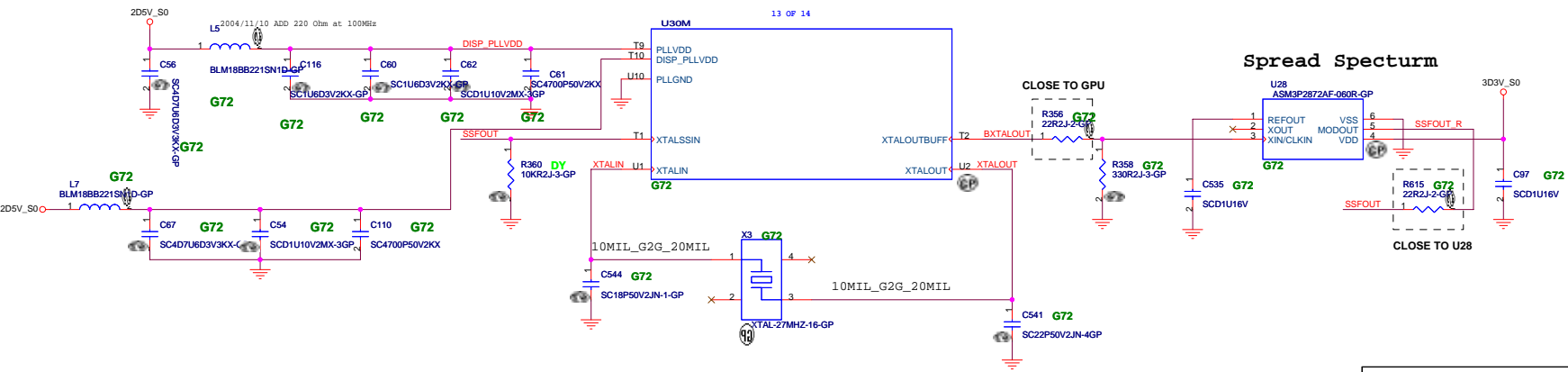
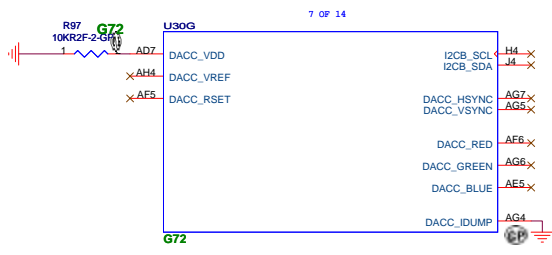
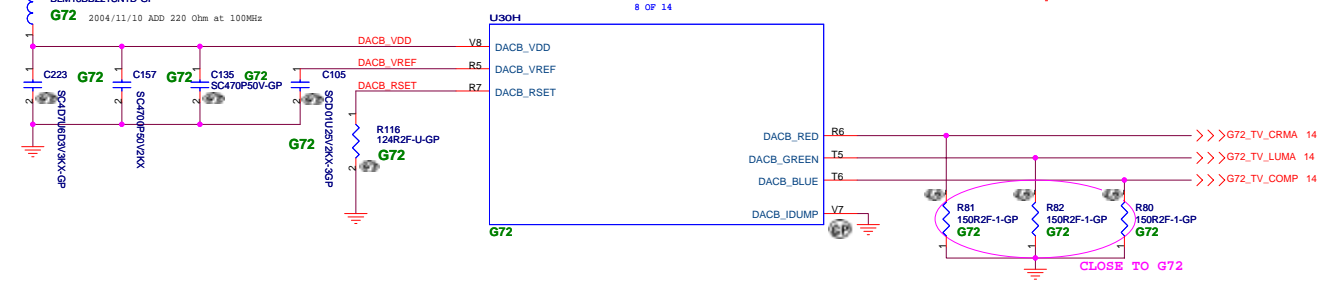
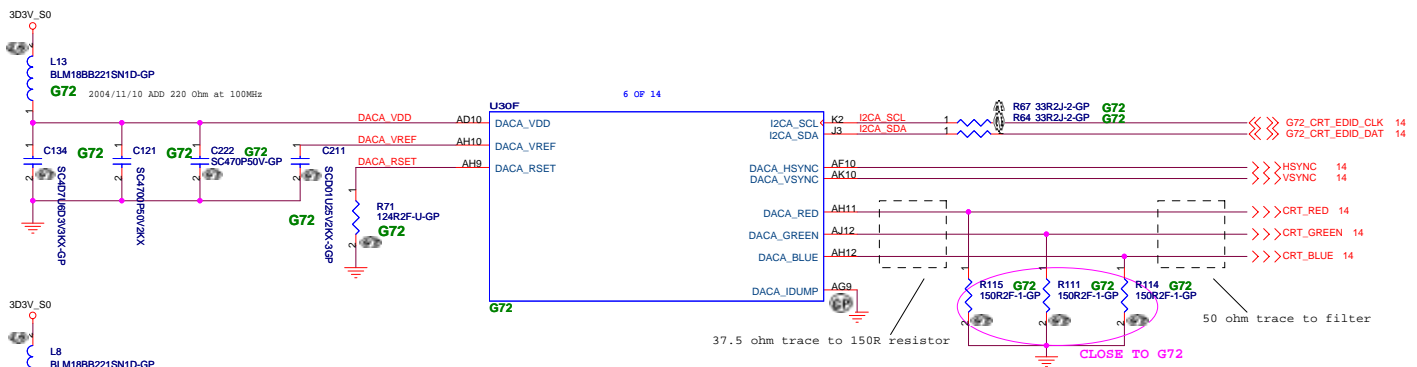
- VDD33_0 AC11
- VDD33_1 AC12
- VDD33_2 AC24
- VDD33_3 AD24
- VDD33_4 AE11
- VDD33_5 AE12
- VDD33_6 H7
- VDD33_7 K7
- VDD33_8 L10
- VDD33_9 L10
- VDD33_10 L10
- VDD33_11 L8
- VDD33_12 M10

- PEX_PLLA_VDD AE15
- PEX_PLLA_VDD AE16
- PEX_PLLA_VDD AE16
- NC#AM10 AM10
- NC#AM9 AM9
- NC#AM8 AM8
- NC#B32 B32
- NC#J6 J6

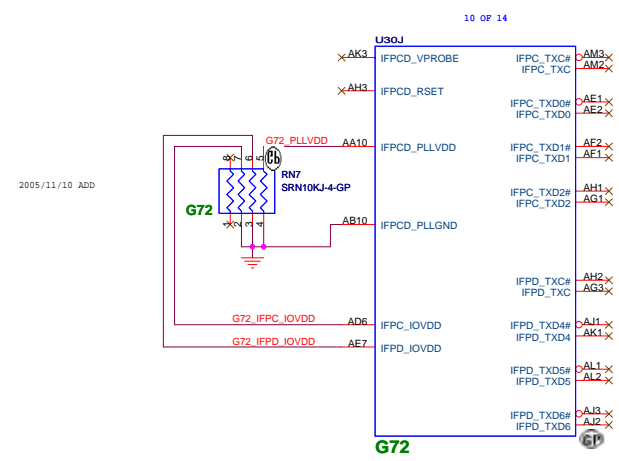
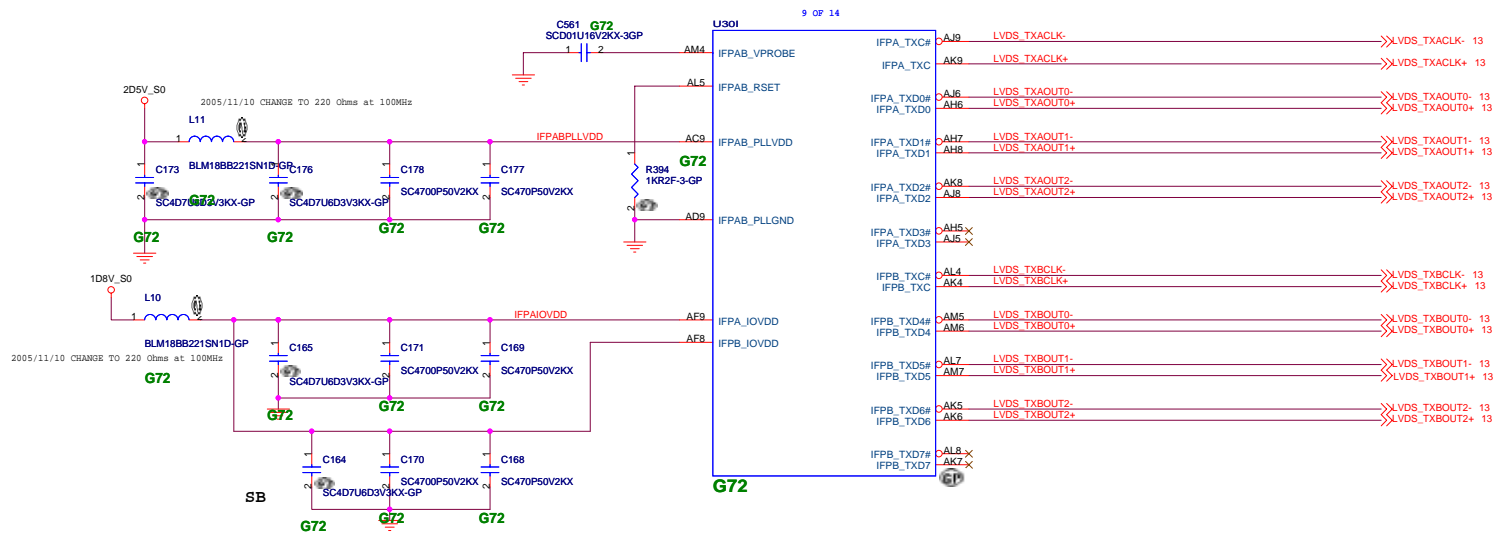


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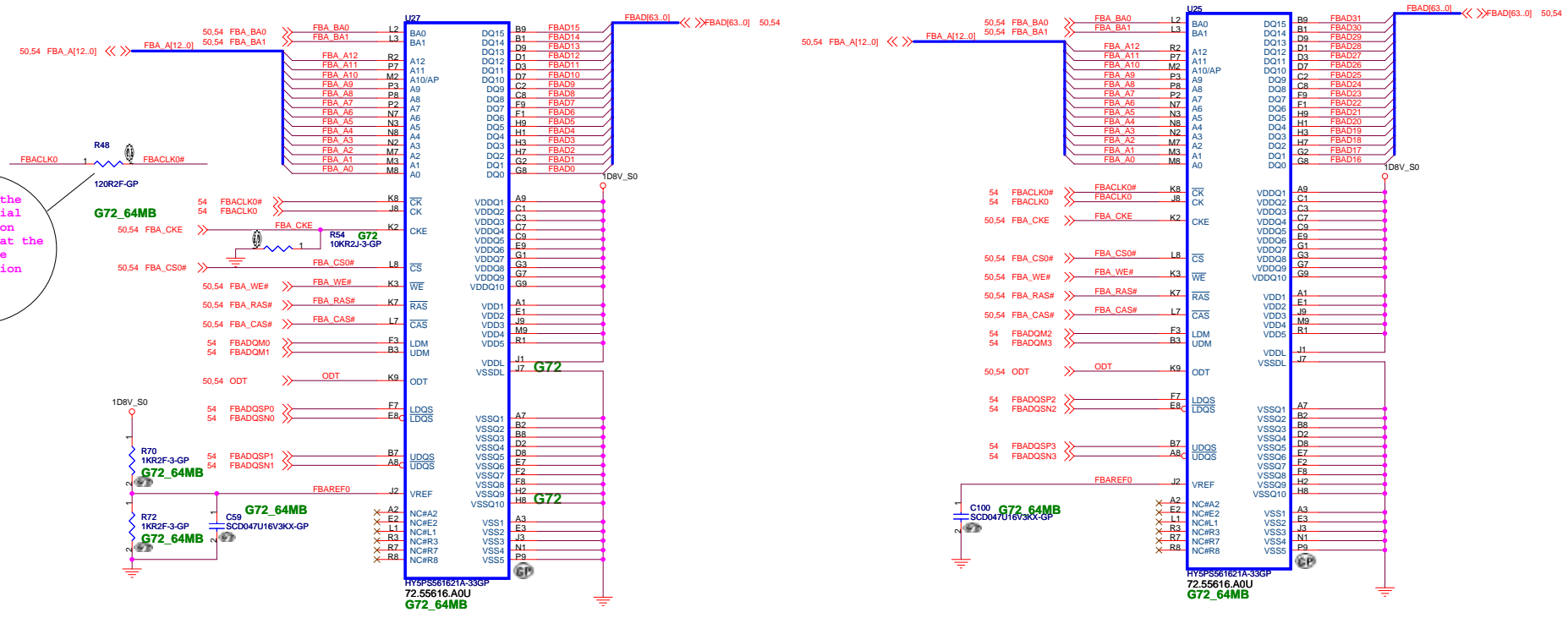
Title			G72M PCIE
Size	Document Number	Rev	
	MYALL2	MP	
Date: Thursday, March 30, 2006	Sheet 46	of 57	



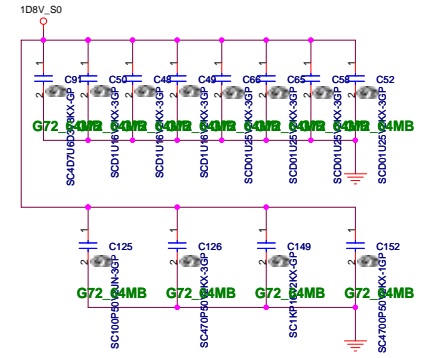
hexrain@hotmail.com



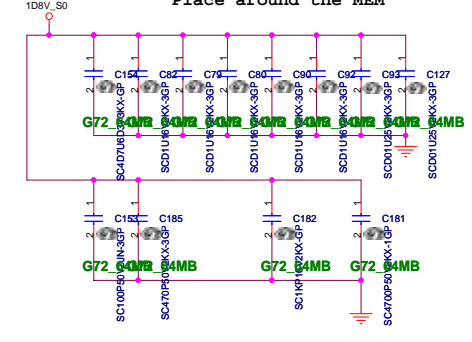
* "Place the differential termination resistor at the end of the transmission line"



Decoupling for left MEMORY
Place around the MEM



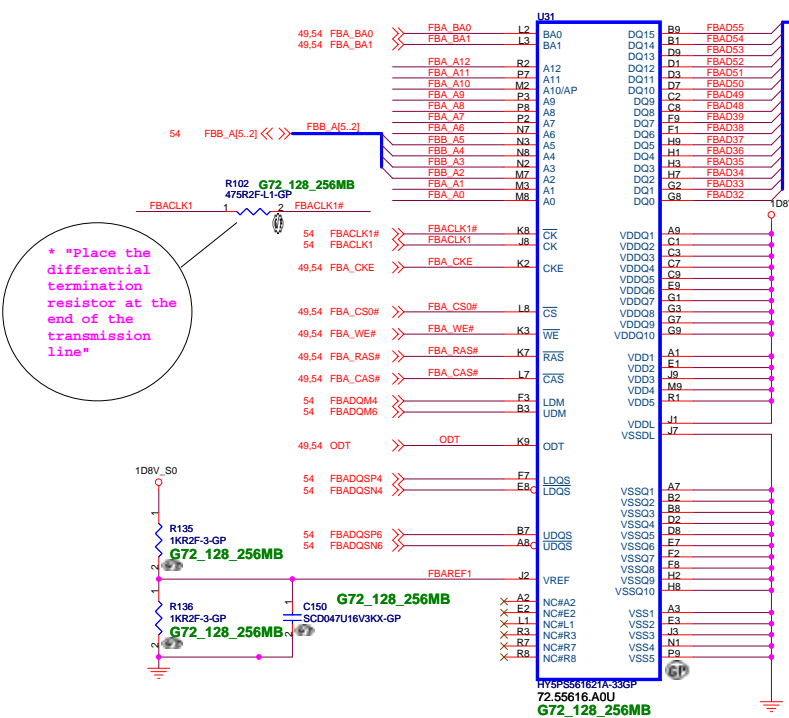
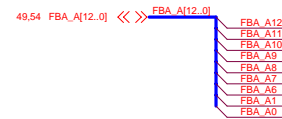
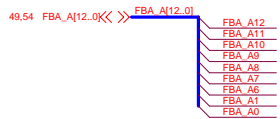
Decoupling for right MEMORY
Place around the MEM



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Title: G72M VRAM (1ST 1/2)		
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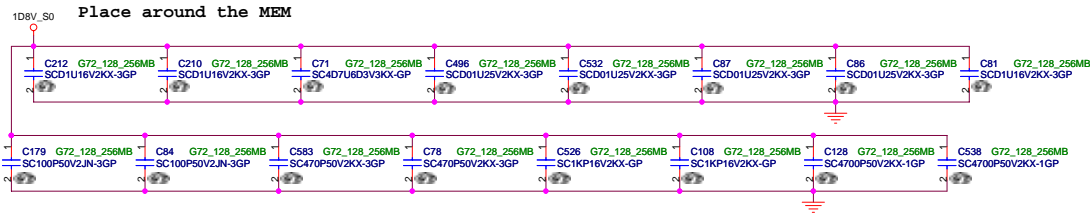
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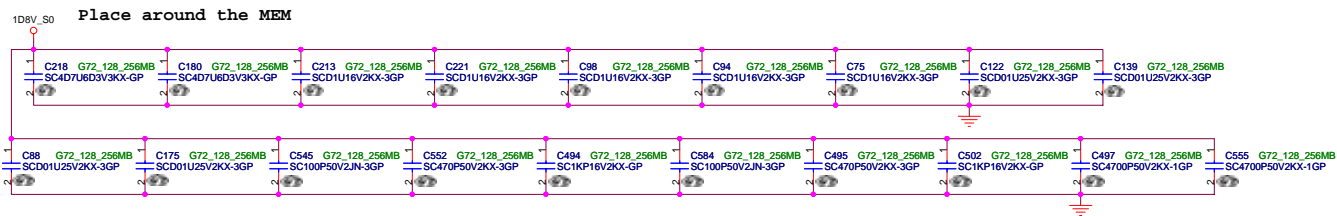
* "Place the differential termination resistor at the end of the transmission line"

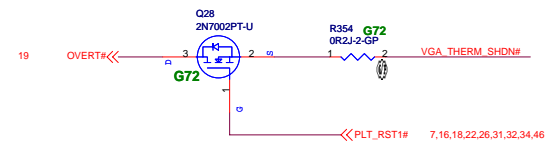
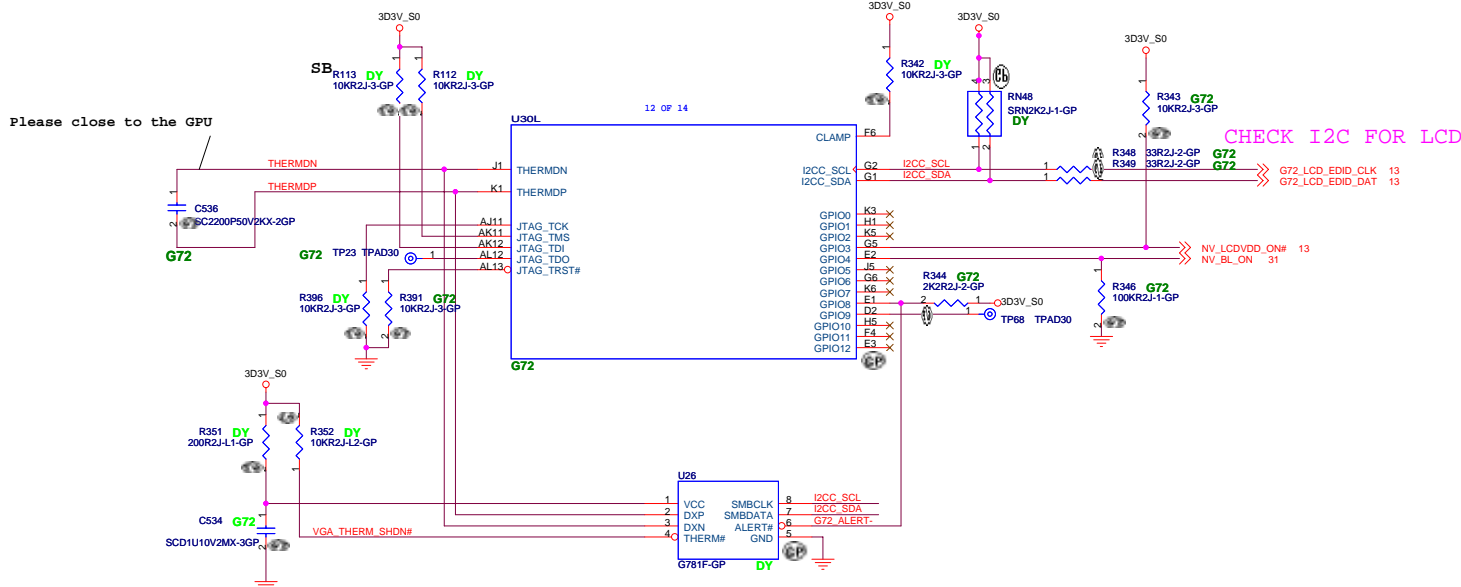
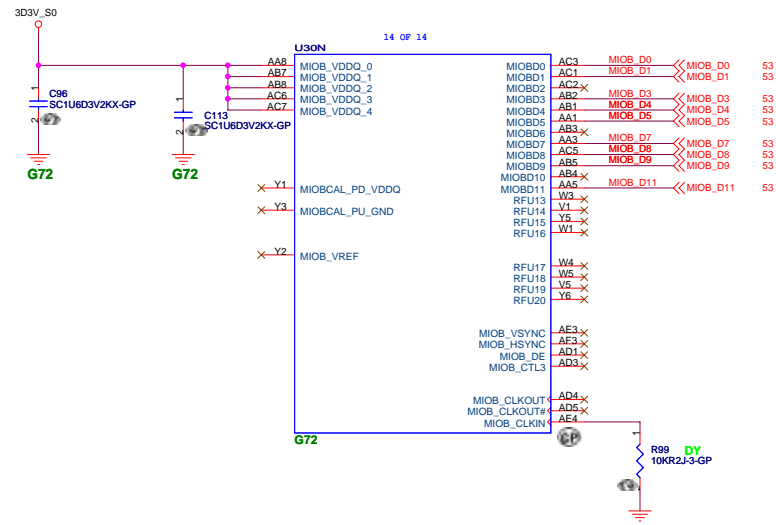
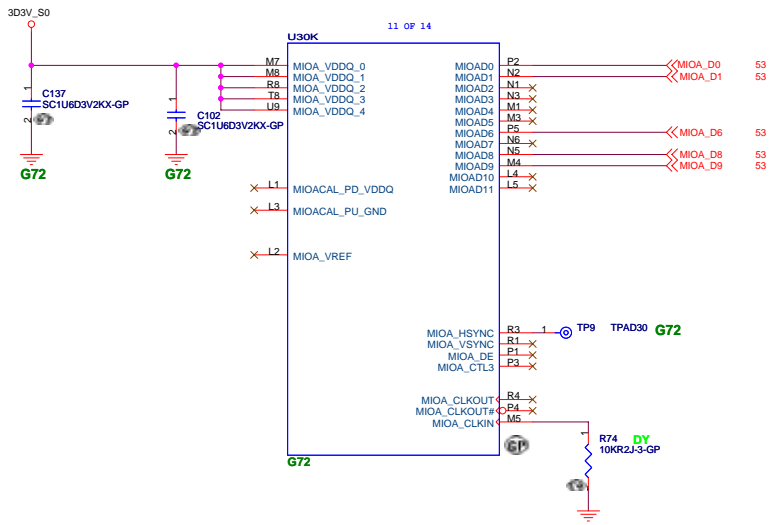


Decoupling for left MEMORY
Place around the MEM



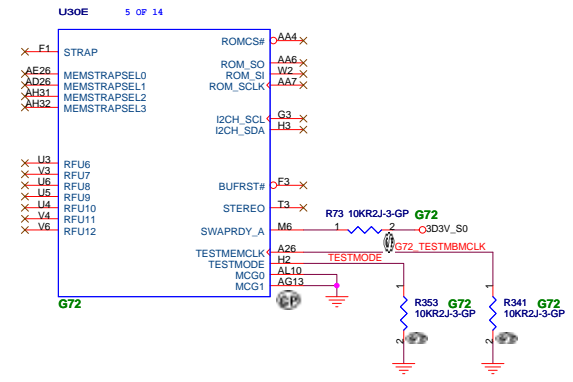
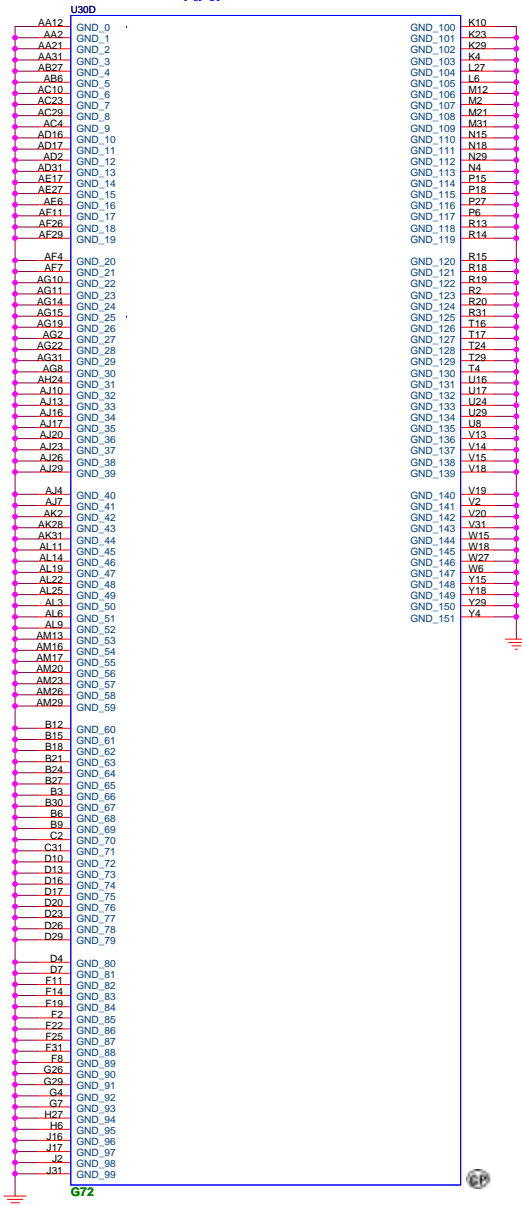
Decoupling for right MEMORY
Place around the MEM





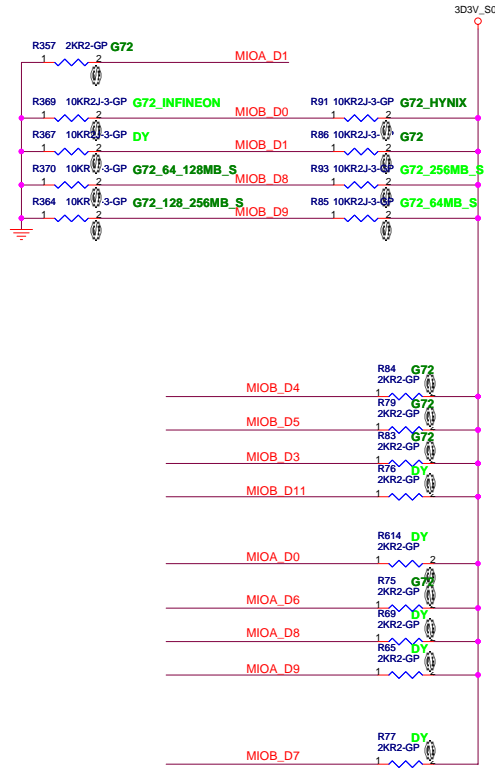
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Date: Thursday, March 30, 2006	Sheet 51 of	57

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STRAPS, Mechanical Parts

Hynix256MB :	R364_0	R93_1	R86_1	R91_1
Hynix128MB :	R364_0	R370_0	R86_1	R91_1
Hynix64MB :	R85_1	R370_0	R86_1	R91_1
Infineon256MB :	R364_0	R93_1	R86_1	R369_0
Infineon128MB :	R364_0	R370_0	R86_1	R369_0
Infineon64MB :	R85_1	R370_0	R86_1	R369_0



- 51 MIOA_D0 << MIOA_D0
- 51 MIOA_D1 << MIOA_D1
- 51 MIOA_D6 << MIOA_D6
- 51 MIOA_D8 << MIOA_D8
- 51 MIOA_D9 << MIOA_D9
- 51 MIOB_D0 << MIOB_D0
- 51 MIOB_D1 << MIOB_D1
- 51 MIOB_D3 << MIOB_D3
- 51 MIOB_D4 << MIOB_D4
- 51 MIOB_D5 << MIOB_D5
- 51 MIOB_D7 << MIOB_D7
- 51 MIOB_D8 << MIOB_D8
- 51 MIOB_D9 << MIOB_D9
- 51 MIOB_D11 << MIOB_D11

Bit Signal	Values
MIOA_D1: SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS
MIOB_D0: RAM_CFG_0	0000 RFU 0001 8Mx32 BGA 1.8V 0010 RFU 0011 RFU 0100 4Mx32 BGA 1.8V 0101 RFU 0110 RFU 0111 RFU 0011 16MX16
MIOB_D1: RAM_CFG_1	1000 RFU 1001 RFU 1010 RFU 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 RFU
MIOB_D8: RAM_CFG_2	
MIOB_D9: RAM_CFG_3	
MIOB_D2: CRYSTAL_0	00 13.500 MHz 01 14.31818 MHz 10 27.000 MHz 11 UNKNOWN
MIOB_D6: CRYSTAL_1	
MIOA_D7: TV_MODE_0	00 SECAM 01 NTSC 10 PAL 11 CRT
MIOA_D10: TV_MODE_1	
MIOB_D4: PCI_DEVID_0	
MIOB_D5: PCI_DEVID_1	1000 (default 0x00FC)
MIOB_D3: PCI_DEVID_2	
MIOB_D11: PCI_DEVID_3	0111 G72MV
MIOA_D0: PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED
MIOA_D6: 3GIO_PADCFG_LUT_ADDR[0]	0 DESKTOP 1 MOBILE
MIOA_D8: 3GIO_PADCFG_LUT_ADDR[1]	
MIOA_D9: 3GIO_PADCFG_LUT_ADDR[2]	010 DEFAULT
MIOB_D7: MOBILE_GPIO	0 GPIO_PULLDN 1 GPIO_FLOAT

For MEM strapping, Please use below table:

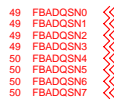
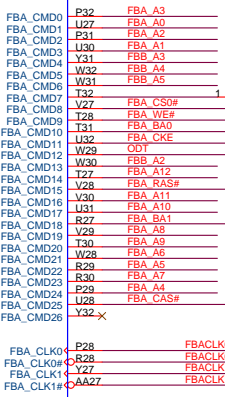
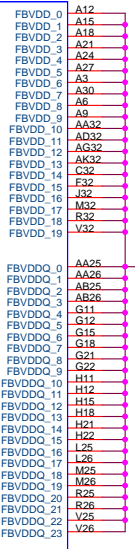
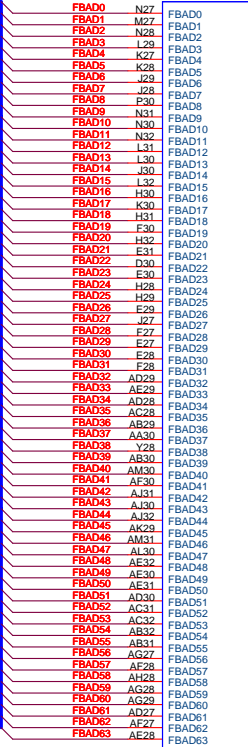
RAM_CFG[3:0]	Config	FB Bus Width	Definitions
0000	16Mx16 DDR2	64-bit	Elpida
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix
0100	32Mx16 DDR2	64-bit	Elpida
0101	32Mx16 DDR2	64-bit	Samsung
0110	32Mx16 DDR2	64-bit	Infineon
0111	32Mx16 DDR2	64-bit	Hynix

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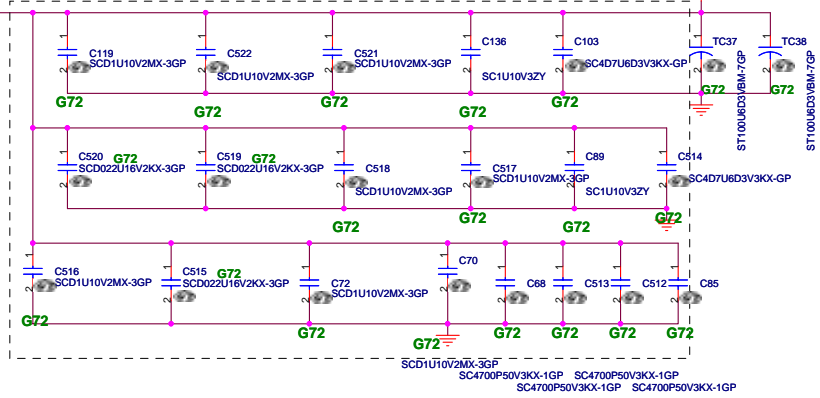
49.50 FBAD[63..0] <<< FBAD[63..0]

U30B

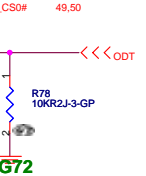
2 OF 14



PLACE BELOW GPU



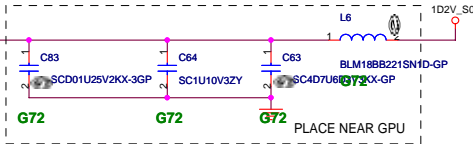
TPAD30 TP100 G72



TPAD30 TP6 G72



SB



PLACE NEAR GPU

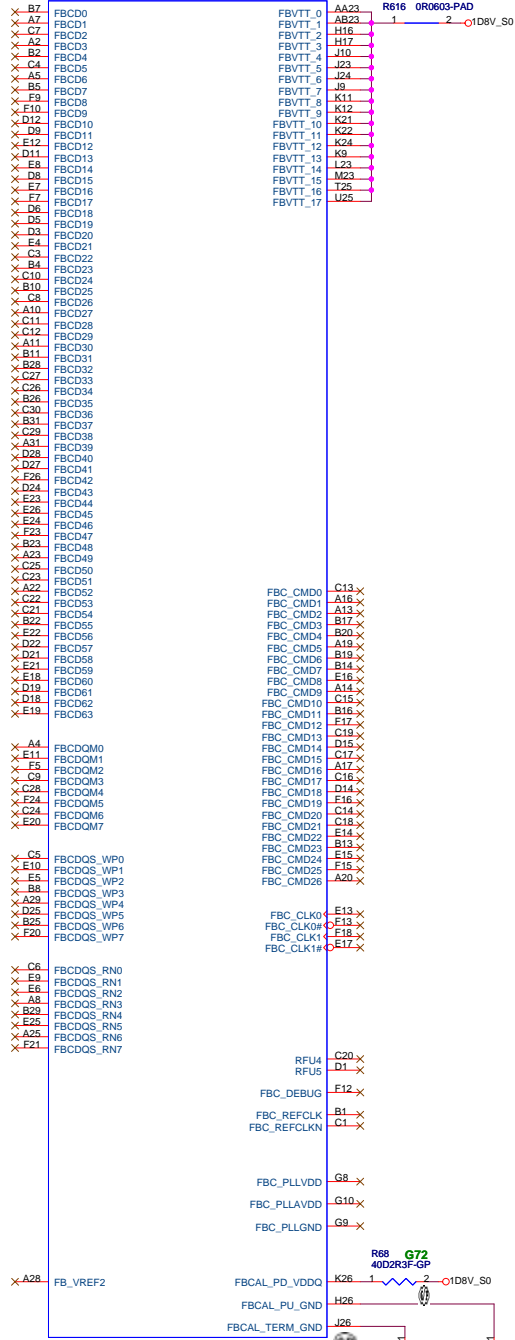
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Title: **G72M MEMORY IF 1**

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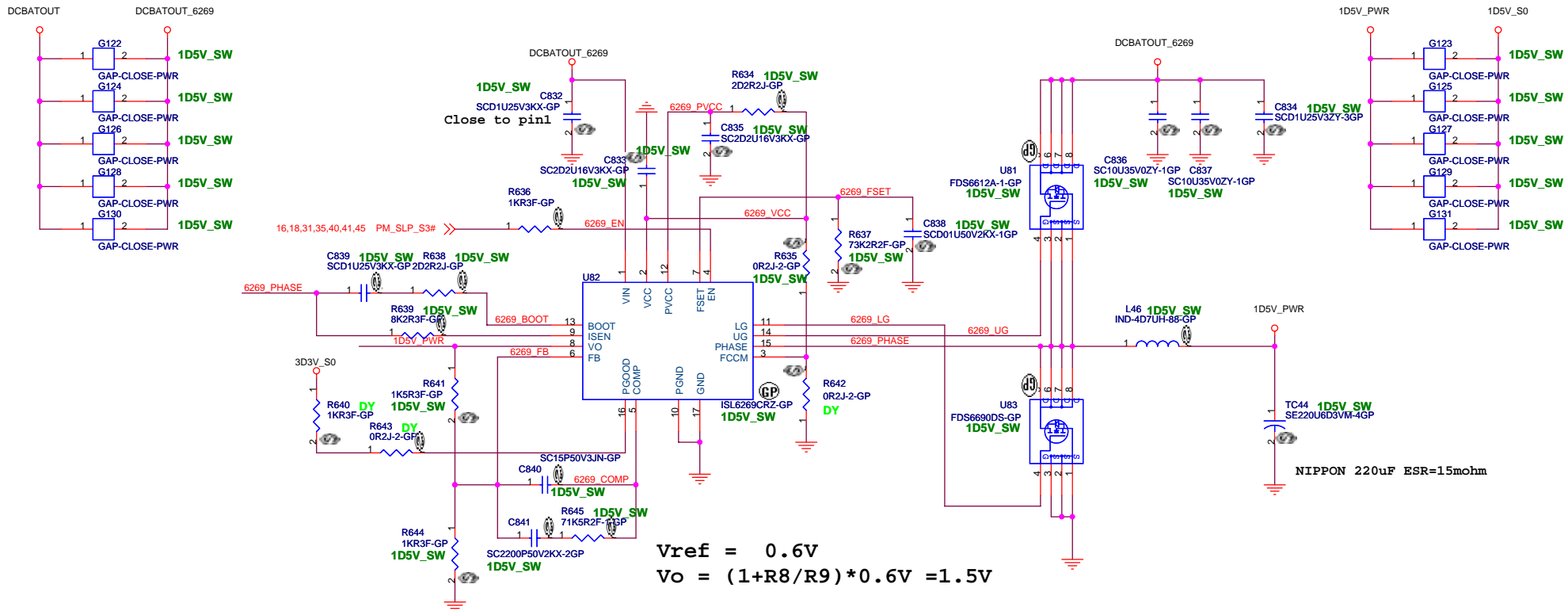
U30C



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1. 5V_S5_G913 chnge to 5V_AUX_S5 =====> 1229
2. Bluetooth USB change to port 7 =====> 1229
3. Add CPU frequency selection resistor =====> 1229
4. Change LVDS connector =====> 1229
5. Change C435 from 1uF to 0.47uF and for pop noise =====> 1230
6. Change T7 and T8 from 68uF to 22uF for pop noise =====> 1230
7. Add 579 ~ R584 / Q35 and Q36 for pop noise =====> 1230
8. Power change 1D05V_S0 and 1D5V_S0 power source =====> 0102
9. Power change 5D_PWR and 3D3V_PWR power source =====> 0107
10. R427 DY for PCIE bus clock =====> 0107
11. Delete Q14 / R543 / R254 for boot up =====> 0107
12. Power change R505 from 3.01K to 3.24K =====> 0107
13. Power change R142 from 2.21K to 8.2K =====> 0107
14. Power change R122 from 56.2K to 73.2K =====> 0107
15. Change R68 from 37ohm to 40.2ohm and R61 from 37ohm to 30ohm =====> 0107
16. Delete R401 for UMA boot up short =====> 0107
17. ME change TVOUT1 material from 22.10021.F41 to 22.10021.H61 =====> 0107
18. R568 DY for CIR working =====> 0109
19. Swap CARD1 pin18 and pin19 =====> 0110
20. Power change C699 from 510P/50V to 470P/50V =====> 0111
21. Power change R397 and R399 from resister to gap-close =====> 0111
22. Remove R392 / R393 / C560 / R62 / R92 / R123 =====> 0111
23. Add R615 for G72 SS =====> 0111
24. Dummy G72 external thermal sensor U26 / R351 / R352 / C534 =====> 0111
25. Add G72 strapping MIOA_DO R614 with dummy =====> 0111
26. EMI add capacitor EC66 ~ EC69 for 1000P/16V and EC70 ~ EC78 for 0.1U/16V =====> 0111
27. Power change R480 from 6.2K to 8.2K =====> 0112
28. Delete R533 and R534 for cardreader detect =====> 0112
29. Delete R210 for 1D5V_S0 power rail =====> 0112
30. Power delete R407 0 ohm =====> 0112
31. Add TC34 ~ TC38 for U39_G72 =====> 0112
32. Remove R362 =====> 0112
33. Change R282 and R283 from 22 ohm to 2.2K for internal mic record function failure =====> 0112
34. Change R306 / R308 / R313 / R311 from 47 ohm to 0 ohm for Hsync and Vsync input =====> 0112
35. Change R379 / R380 / R377 / R378 / R382 / R383 from 47 ohm to 0 ohm for TV input =====> 0112
36. Change CIR pull hi voltage from 5V to 3D3V =====> 0113
37. Delete G2 pad =====> 0113
38. Add GIGA LAN reset trace =====> 0113
39. Power change 1D5V power source =====> 0117
40. Power change NVVDD power source =====> 0117
41. Power add 1D5V power switching =====> 0117
42. Change C774 and C776 from 12pF to 15pF =====> 0119
43. Change C640 and C648 from 20pF to 27pF =====> 0119
44. Change C722 and C737 from 4.7pF to 2.7pF =====> 0119
45. Change C42 and C44 from 22pF to 18pF =====> 0119
46. Power delete R633 and pull hi voltage =====> 0119
47. Power delete TC39, TC43 and change TC41, TC42 to 79.33719.20C =====> 0120
48. Add CRT detect circuit =====> 0119
49. Change R594 pull hi voltage from 3D3V_S0 to 3D3V_S5 for S3 wake up issue =====> 0123
50. Power change material L44 and L46 from 68.3R310.20A to 68.4R710.20D
L45 from 68.3R310.20A to 68.2R210.20B =====> 0123
51. Power change R480 from 8.2K to 12K =====> 0124
52. Power change capacitor material from 78.10699.42L to 78.10622.53L as C685 ~ C692 =====> 0125
53. Delete U57 / C671 / C675 / C656 / C663 / U8 / D12 / D13 / C306 / R218 / R219 for don't boot up with battery only =====> 0205
54. Change R59 from 100K to 8.2K and add R649 / R650 for don't boot up with battery only =====> 0205

55. Change TC7 / TC8 to C844 / C845 from 22U/6.3V to 10U/6.3V for headphone system resume have "BO" sound =====> 0208-PD
56. EMC change U1 and U7 materials from G528 / G546 to TPS2061 / TPS2062 =====> 0208-PD
57. Add R651 0 ohm for vendor test =====> 0208-PD
58. Add R652 0 ohm for camera voltage =====> 0209-PD
59. Add R653 / Q37 / Q38 for quick discharge of 5V_S0 / 3D3V_S0 / 1D8V_S0 =====> 0209-PD
60. Change DIMM connector from 62.10017.741(DM1)/62.10017.751(DM2) to 62.10017.691(DM1)/62.10017.A71(DM2) =====> 0209-PD
61. Change G72 DACB net of DACA_VDD / DACA_VREF / DACA_RSET to DACB_VDD / DACB_VREF / DACB_RSET =====> 0209-PD
62. Delete R230 and C317 for non-delay RSMRST# =====> 0210-PD
63. Stuff R285 for internal mic record issue =====> 0210-PD
64. Change C541 and C544 from 27pF to 22pF with 18pF =====> 0210-PD
65. Change HDD1/ODD1/TVOUT1/TVIN1/LOUT1 symbol =====> 0210-PD
66. Delete R330 for BAT_IN# double pull hi issue =====> 0213-PD
67. EMI add EC79 ~ EC87 for 1D8V_S3 and EC88 ~ EC90 for DDR_VREF_S0 =====> 0213-PD
68. Add U84/C846/R654/R655/R656/L47 for camera function =====> 0213-PD
69. EMI add spring GND1 ~ GND3 =====> 0213-PD
70. Change TVOUT1 symbol for don't display TV issue =====> 0214-PD
71. Power change C805 and C806 from 51120_GND to GND =====> 0220-PD
72. Change DC1material from 22.10037.C51(yellow power jack) to 22.10037.C61(blue power jack) =====> 0223-PD
73. Power change C466 from 0.1uF to 0.01uF for U19 burned issue =====> 0303-PD
74. Power change material U47 / U48 / U53 / U54 from 84.07807.F37 to 84.06690.F37
U49 / U50 / U51 / U52 from 84.07805.A37 to 84.06676.A37 for burned issue =====> 0306-PD
75. Power change R523 / C738 from 3.57K / 5600pF to 4.42K / 47pF =====> 0306-MP
76. Charger change R19 from 15.8K to 130K =====> 0307-MP
77. Charger change R22 from 100K to 499K and add R657 124K / Q39 2N7002 for 6 cell 3.2A with 8 cell 3.8A issue =====> 0309-MP
78. Acer suggestion change JK1 AV-IN connector from 62.10059.011 to 20.90045.001 and delete R292 / R293 =====> 0315-MP
79. Change CRT1 / Q35 / Q36 footprint for SMT issue =====> 0317-MP
80. Change LED5 driver voltage from 5V_S0 to 3D3V_S0 for light leak issue =====> 0317-MP
81. Delete dual layout of dummy of L47 / L28 / L33 / L39 / L15 / L18 =====> 0317-MP
82. Short 0 ohm with pad =====> 0320-MP
S : R89 / R418 / R225 / R537 / R316 / R5 / R52 / R51 / R333 / R345 / R335 / R651 / R558 / R559 / R532 / R285 / R649 / R650
/ R49 / R448 / R204 / R437 / R96 / R562 / R410 / R211 / R208 / R177 / R406 / R194 / R237 / R226 / R245 / R243 / R322 / R326
/ R327 / R425 / R444 / R495 / R496 / R560 / R616
P : R515 / R516 / R491 / R492 / R494 / R482 / R485 / R486 / R487 / R517 / R506 / R508 / R510 / R511 / R591 / R589 / R592
/ R593 / R596 / R598 / R603 / R600 / R246 / R247 / R623 / R626 / R624 / R42
83. Power change materials for high frequency noise issue =====> 0324-MP
A. add TC45 ~ TC50
B. dummy C691 / C692 / C689 / C685 / C686 / C688
C. delete C797 / C798 / C808 / C809
84. Power change material TC23 from 79.3371T.30L to 80.22716.L08 and L42 / L43 from 68.4R750.10Z to 68.4R71A.10P =====> 0324-MP
85. Change C29 material from 78.10491.4FL to 78.10520.5FL for hot plug don't boot up issue =====> 0328-MP
86. Change BOM level that add 1394 / TVIN / TVOUT / IR function =====> 0331-MP
87. ME change 1394 connector material from 62.10027.121 to 62.10027.561 for RoSH issue =====> 0331-MP

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