MB82 IDTV
SERVICE MANUAL

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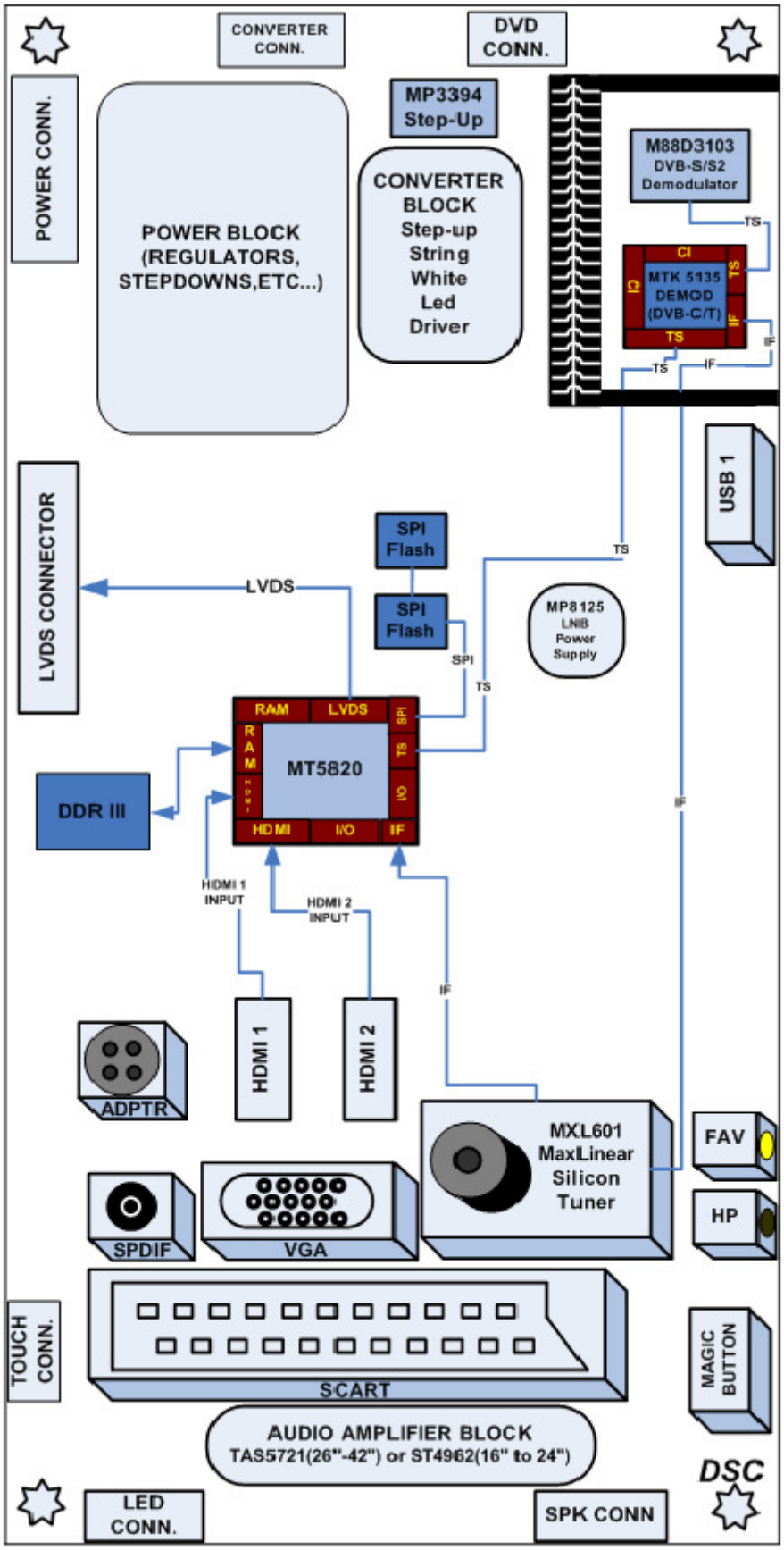
1. INTRODUCTION

17MB82 mainboard is driven by MediaTek MT5820. This IC is capable of handling Video and audio processing, Scaling-Display processing, 3D comb filter, OSD and text processing, LVDS/mini-LVDS transmitting, channel and MPEG2/4 decoding, integrated DVB-T/C demodulator and media center functionality.
TV supports PAL, SECAM, NTSC colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo. Also DVB T, DVB-C are supported internal demoulators of MediaTek IC and DVB-S/S2 is supported with externall demodulator.
Sound system output is supplying max. 2x8W (less 10%THD at max output) for stereo 8Ω speakers.
Supported peripherals are:

1 RF input VHF I, VHF III, UHF @ 75Ohm(Common)
1 Side AV (CVBS, R/L_Audio)
1 SCART socket(Common)
1 PC input(Common)
2 HDMI 1.3 input(1 HDMI input is common, 1 input is optional)
1 S/PDIF output(Optional)
1 Headphone(Optional)
1 Common interface(Common)
2 USB(1 USB input is common, 1 USB input is optional)
1 On-board Keypad(Optional)
1 External TouchPad(Optional)

1.1. General Block Diagram



1.2. MB82 Placement of Blocks

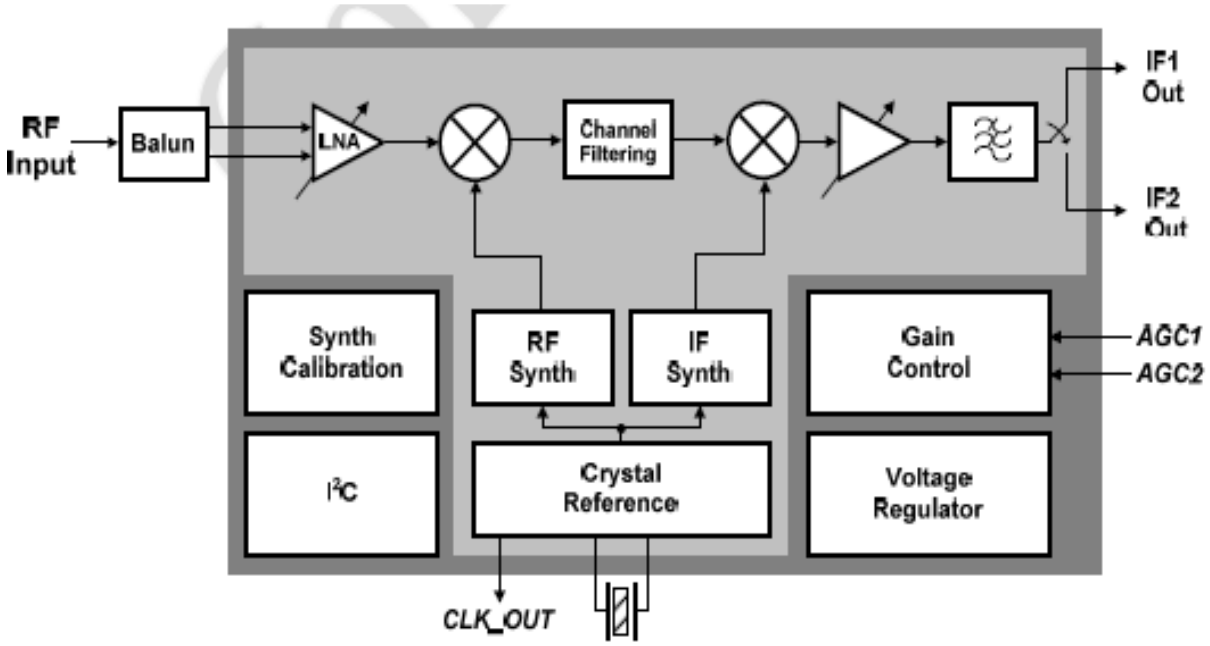
1. TUNER(MXL601)

MxL601 is a highly integrated low-power silicon tuner IC targeting all global analog and digital cable standards as well as digital terrestrial reception standards. Broadband input filtering and channel filtering have been completely integrated on-chip. This integration enables a very compact design requiring a small footprint, low bill-of-materials cost, and low power
consumption. A signal at the 753 RF input is filtered and converted to a programmable IF output up to 44MHz. Automatic gain control, LO generation, and channel selectivity functions are completely integrated on the chip, which simplifies boardlevel design. All functions of the IC can be controlled via I2C interface. MxL601 is available in a 4 x 4 mm2 24-pin QFN package.

Features :

- Tuning range from 44MHz to 1002MHz
- Programmable channel bandwidths of 6, 7,and 8MHz
- Integrated channel filtering requiring noexternal SAW filter for digital applications
- Low power consumption with 3.3V and1.8V dual-supply operation351 mW (Digital Terrestrial)
- On-chip voltage regulator enables singlesupply 3.3V operation
- Programmable IF frequency and IF spectrum inversion
- Reference clock output available for re-use by demodulators and additional tuners in multi-channel applications
- Input power reporting
- General purpose open-drain output GPO available for controlling off-chip circuitry
- Integrated on-chip programmable loading capacitors for the reference crystal
- I2C-compatible digital control interface
- RoHS compliance

BLOCK DIAGRAM



2. AUDIO AMPLIFIER STAGE

TAS5721 (optional)

2.1. General Description

The TAS5721 is a 15-W stereo or 2x10 W + 1x15 W2.1 device, efficient, digital audio-power amplifier fordriving stereo bridge-tied speakers. One serial datainput allows processing of up to two discrete audiochannels and seamless integration to most digitalaudio processors and MPEG decoders. The deviceaccepts a wide range of input data and data rates. Afully programmable data path routes these channelsto the internal speaker drivers.The TAS5721 is a slave-only device receiving allclocks from external sources. The TAS5721 operateswith a PWM carrier between a 384-kHz switching rateand a 352-KHz switching rate, depending on the inputsample rate. Oversampling combined with a fourth- order noise shaper provides a flat noise floorand excellent dynamic range from 20 Hz to 20 kHz.

2.2. Features

• **Audio Input/Output**
– 15Wx2 into 8Ω
– Supports Single Device 0.1, 2.0, 2.1 Modes
– Wide PVDD Range, From 4.5 V to 26 V Performance
– Efficient Class-D Operation Eliminates Need for Heatsinks
– Requires Only 3.3 V and PVDD
– One Serial Audio Input (Two Audio Channels)
– I2C Address Selection via PIN (Chip Select)
– Supports 8-kHz to 48-kHz Sample Rate (LJ/RJ/I2S)
– External Headphone-Amplifier Shutdown Signal
– Integrated CAP-Free Headphone Amplifier
– Stereo Headphone (Stereo 2-V RMS Line Driver) Outputs
• **Audio/PWM Processing**
– Independent Channel Volume Controls With The 24-dB to Mute
– Separate Dynamic Range Control for Satellite and Sub Channels
– 21 Programmable Biquads for Speaker EQ
– Programmable Coefficients for DRC Filters
– DC Blocking Filters
– Support for 3D Effects
• **General Features**
– Serial Control Interface Operational Without MCLK
– Factory-Trimmed Internal Oscillator for Automatic Rate Detection
– Surface Mount, 48-Pin, 7-mm × 7-mm HTQFP Package
– Thermal and Short-Circuit Protection

2.3. Absolute Ratings

2.3.1 ELECTRICAL CHARACTERISTICS

DC Characteristics

T_A = 25°C, PVCC_X = 13 V, DVDD = AVDD = 3.3 V, R_L = 8 Ω, BTL AD Mode, f_S = 48 kHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{FAULT}$ and SDA	I_{OH} = –4 mA DVDD = 3 V	2.4			V
V_{OL}	Low-level output voltage	$\overline{FAULT}$ and SDA	I_{OL} = 4 mA DVDD = 3 V			0.5	V
I_{IL}	Low-level input current		$V_I < V_{IL}$; DVDD = AVDD = 3.6V			75	µA
I_{IH}	High-level input current		$V_I > V_{IH}$; DVDD = AVDD = 3.6V			75	µA
I_{DD}	3.3 V supply current	3.3 V supply voltage (DVDD, AVDD)	Normal mode		48	70	mA
			Reset ($\overline{RESET}$ = low, $\overline{PDN}$ = high)		21	32	
I_{PVDD}	Half-bridge supply current	No load (PVDD_X)	Normal mode		20	34	mA
			Reset ($\overline{RESET}$ = low, $\overline{PDN}$ = high)		5	13	
$r_{DS(on)}$	Drain-to-source resistance, LS	T_J = 25°C, includes metallization resistance			200		mΩ
	Drain-to-source resistance, HS	T_J = 25°C, includes metallization resistance			200		
I/O Protection							
V_{uvp}	Undervoltage protection limit	PVDD falling			3.5		V
$V_{uvp,hyst}$	Undervoltage protection limit	PVDD rising			4.5		V
OTE	Overtemperature error				150		°C
OTE_{HYST}	Extra temperature drop required to recover from error				30		°C
I_{OC}	Overcurrent limit protection				4.5		A
I_{OCT}	Overcurrent response time				150		ns
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when drivers are tristated to provide bootstrap capacitor charge.			3		kΩ

AC Characteristics (BTL)

PVDD_X = 12 V, BTL AD mode, f_S = 48 kHz, R_L = 8 Ω, audio frequency = 1 kHz, (unless otherwise noted). All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	PVDD = 13 V, 10% THD, 1-kHz input signal		10		W
		PVDD = 8 V, 10% THD, 1-kHz input signal		4.1		
		PVDD = 18 V, 10% THD, 1-kHz input signal		15 (1)		
THD+N	Total harmonic distortion + noise	PVDD = 13 V; P_O = 1 W		0.13%		
		PVDD = 8 V; P_O = 1 W		0.2%		
V_n	Output integrated noise (rms)	A-weighted		56		µV
	Crosstalk	P_O = 0.25 W, f = 1 kHz (BD mode)		–82		dB
		P_O = 0.25 W, f = 1 kHz (AD mode)		–69		
SNR	Signal-to-noise ratio (2)	A-weighted, f = 1 kHz, maximum power at THD < 1%		–105		dB

(1) 15 W is supported only in the TAS5719.
(2) SNR is calculated relative to 0-dBFS input level.

AC Characteristics (Headphone/Line Driver)

PVDD_X = 12 V, BTL AD mode, f_S = 48 KHz, R_L = 8 Ω, audio frequency = 1 kHz, (unless otherwise noted). All performance is in accordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Po(hp)	Headphone power output per channel	HP_VDD = 3.3 V (Rhp = 32 Ω; THD 1%)		25		mW
HP_gain	Headphone gain	Adjustable via Rin and Rfb				
SNR_hp	Sgnal-to-noise ratio (headphone mode)	Rhp = 32 Ω		101		dB
SNR_ln	Sgnal-to-noise ratio (line driver mode)	2-V rms output		105		dB

2.3.2 OPERATING SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
	Digital/analog supply voltage	DVDD, AVDD	3	3.3	3.6	V
	Half-bridge supply voltage	PVDD_X	4.5			V
V_{IH}	High-level input voltage	5-V tolerant	2			V
V_{IL}	Low-level input voltage	5-V tolerant			0.8	V
T_A	Operating ambient temperature range		0		85	°C
T_J (1)	Operating junction temperature range		0		125	°C
R_L (BTL)	Load impedance	Output filter: L = 15 µH, C = 680 nF	4	8		Ω
L_O (BTL)	Output-filter inductance	Minimum output inductance under short-circuit condition	4.7			µH

(1) Continuous operation above the recommended junction temperature may result in reduced reliability and/or lifetime of the device.

RECOMMENDED OPERATING CONDITIONS FOR HEADPHONE/LINE DRIVER

			MIN	NOM	MAX	UNIT
	Digital/analog supply voltage	HPVDD	3	3.3	3.6	V
R_hp_L	Headphone-mode load imedance (HPL/HPR)		16	32		Ω
R_ln_L	Line-diver-mode load impedance (HPL/HPR)		0.6	10		kΩ

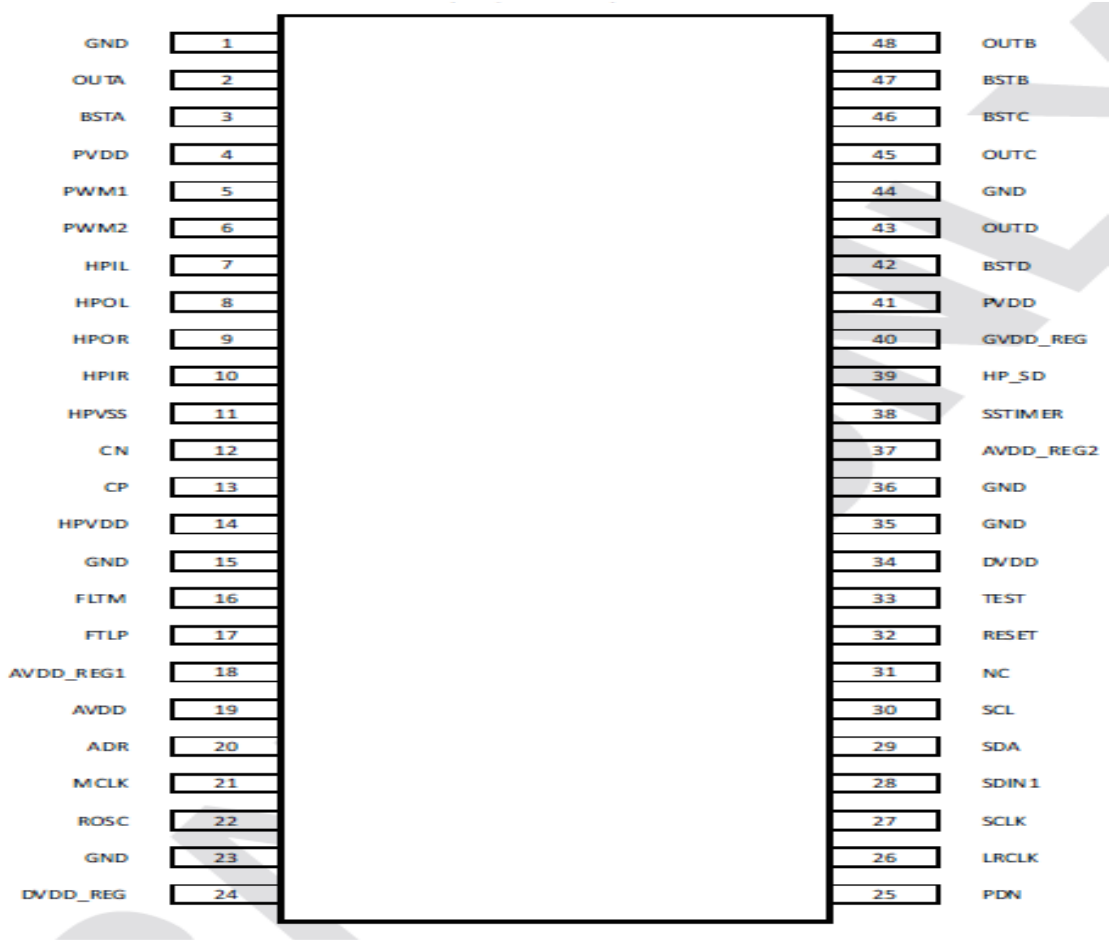
PWM OPERATION AT RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	VALUE	UNIT
Output sample rate	11.025/22.05/44.1-kHz data rate ±2%	352.8	kHz
	48/24/12/8/16/32-kHz data rate ±2%	384	

PLL INPUT PARAMETERS AND EXTERNAL FILTER COMPONENTS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MCLKI}	MCLK Frequency		2.8224		24.576	MHz
	MCLK duty cycle		40%	50%	60%	
tr / $tf_{(MCLK)}$	Rise/fall time for MCLK				5	ns
	LRCLK allowable drift before LRCLK reset				4	MCLKs
	External PLL filter capacitor C1	SMD 0603 Y5V		47		nF
	External PLL filter capacitor C2	SMD 0603 Y5V		4.7		nF
	External PLL filter resistor R	SMD 0603, metal film		470		Ω
Fcp	Charge Pump Switching Frequency		500		700	kHz

2.4. Pinning


GND 1
OUTA 2
BSTA 3
PVDD 4
PWM1 5
PWM2 6
HPIL 7
HPOL 8
HPOR 9
HPIR 10
HPVSS 11
CN 12
CP 13
HPVDD 14
GND 15
FLTM 16
FTLP 17
AVDD_REG1 18
AVDD 19
ADR 20
MCLK 21
ROSC 22
GND 23
DVDD_REG 24
48 OUTB
47 BSTB
46 BSTC
45 OUTC
44 GND
43 OUTD
42 BSTD
41 PVDD
40 GVDD_REG
39 HP_SD
38 SSTIMER
37 AVDD_REG2
36 GND
35 GND
34 DVDD
33 TEST
32 RESET
31 NC
30 SCL
29 SDA
28 SDIN1
27 SCLK
26 LRCLK
25 PDN

TAS5721 Pin Out

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
GND	1, 15, 23, 35, 36, 44	P	General ground connections
OUT_x	2, 43, 45, 48	AO	Outputs for the four half-bridges that are used to create the 2 Full Bridge Output Channels
BST_x	3, 42, 46, 47	P	Connection point for the boot strap capacitors for each of the output half-bridges
PVDD	4, 41	P	Power Supply inputs for each of the four output half-bridges
PWMx	5, 6	AO	Low-level PWM outputs
HPIx	7, 10	AI	Input for signal into either the right or left headphone input
HPOx	8, 9	AO	Right or Left Channel of Headphone Output
HPVSS	11	P	-3.3V supply generated by chargepump for ground centered headphone output
CN	12	AIO	Negative terminal capacitor connection for headphone charge pump
CP	13	AIO	Positive terminal capcitor connection for headphone charge pump

TAS5721 Pin Out (continued)

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
HPVDD	14	P	3.3V headphone power supply input
FLTx	16, 17	P	Connection point for PLL external filter components
AVDD_REG1	18	P	Internal low-voltage analog regulator, which is not to be used to power external circuitry
AVDD	19	P	3.3V power supply input for low-voltage analog circuitry
ADR	20	DI	Sets the I²C address of device
MCLK	21	DI	Master Clock Input
ROSC	22	P	Connection point for the oscillator reference resistor
DVDD_REG	24	P	Internal low-voltage digital regulator, which is not to be used to power external circuitry
PDN	25	DI	Hardware power down enable
LRCK	26	DI	Left/Right clock input for serial audio data port
SCLK	27	DI	Bit Clock Input
SDIN1	28	DI	Serial audio data input
SDA	29	DIO	Serial data line for I²C communication port
SCL	30	DI	Serial clock line for I²C communication port
N/C	31	DI	No Connection
RST	32	DO	Test pin (leave unconnected)
TEST	33	DI	Reset input, which asynchronously resets the internal registers to their default conditions and places the PWM outputs into their high impedance output state.
DVDD	34	P	3.3V power supply input for low-voltage digital circuitry
AVDD_REG2	37	P	Internal low-voltage analog regulator, which is not to be used to power external circuitry
SSTIMER	38	AI	Controls ramp time of OUT_x to minimize pop. Leave this pin floating for BD mode. Requires capacitor of 2.2 nF to GND in AD mode.
HP_SD	39	DI	Headphone Shutdown
GVDD_REG	40	P	Gate drive supply regulator output, which is not to be used to power external circuitry

TS4962M (optional 2,5W)

Features

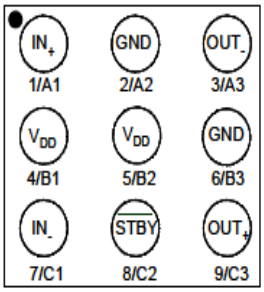
- Operating from V_{CC} = 2.4V to 5.5V
- Standby mode active low
- Output power: 3W into 4Ω and 1.75W into 8Ω with 10% THD+N max and 5V power supply.
- Output power: 2.3W @5V or 0.75W @ 3.0V into 4Ω with 1% THD+N max.
- Output power: 1.4W @5V or 0.45W @ 3.0V into 8Ω with 1% THD+N max.
- Adjustable gain via external resistors
- Low current consumption 2mA @ 3V
- Efficiency: 88% typ.
- Signal to noise ratio: 85dB typ.
- PSRR: 63dB typ. @217Hz with 6dB gain
- PWM base frequency: 250kHz
- Low pop & click noise
- Thermal shutdown protection
- Available in flip-chip 9 x 300µm (Pb-free)

Description

The TS4962M is a differential Class-D BTL power amplifier. It is able to drive up to 2.3W into a 4Ω load and 1.4W into a 8Ω load at 5V. It achieves outstanding efficiency (88%typ.) compared to classical Class-AB audio amps.

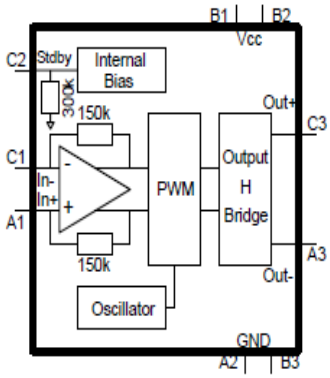
The gain of the device can be controlled via two external gain-setting resistors. Pop & click reduction circuitry provides low on/off switch noise while allowing the device to start within 5ms. A standby function (active low) allows the reduction of current consumption to 10nA typ.

Pin connections



IN+: positive differential input
IN-: negative differential input
VDD: analog power supply
GND: power supply ground
STBY: standby pin (active low)
OUT+: positive differential output
OUT-: negative differential output

Block diagram



3. POWER STAGE

The DC voltages required at various parts of the chassis and panel are provided by a main power supply unit. MB82 chassis can operate with PW05, IPS60, IPS70, IPS16, IPS17, IPS19, PW25, PW26, PW82-3, PW03, PW04, PW06, PW07 as main power supply and also with 12V adaptor.

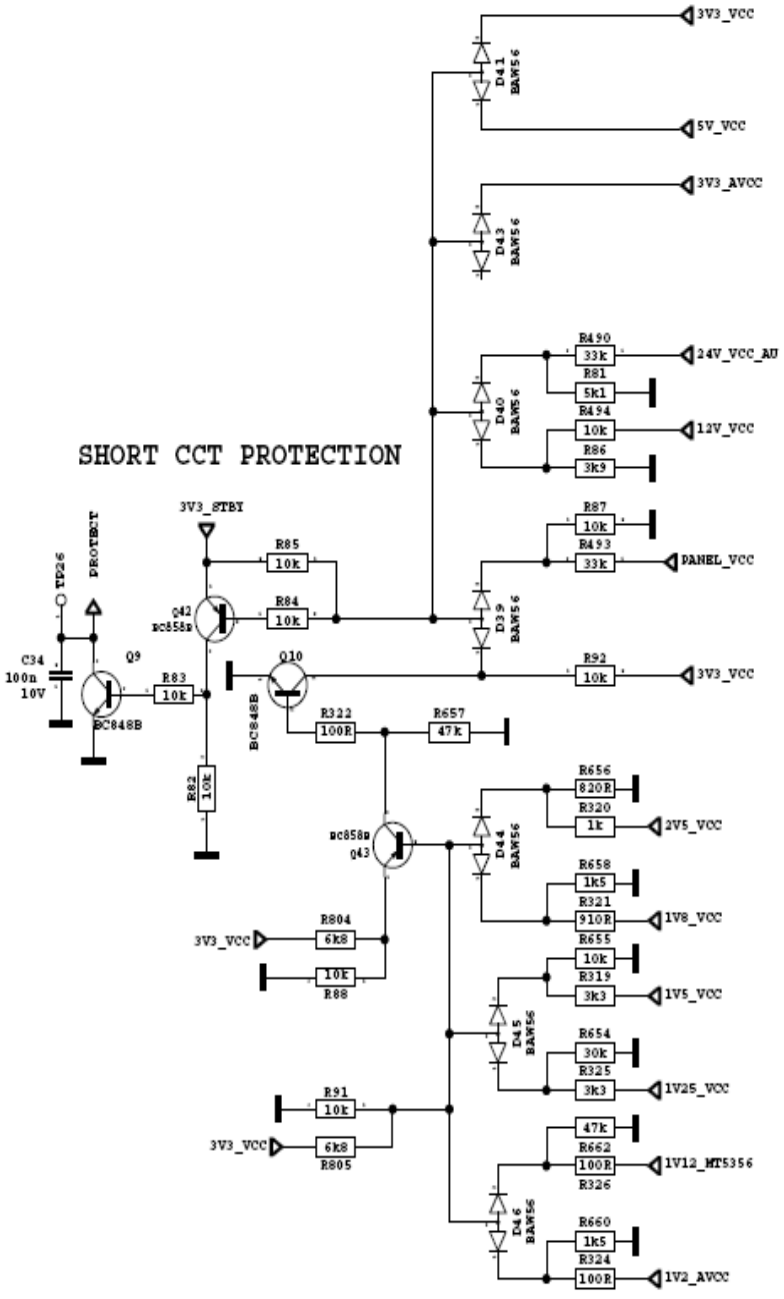
Which power board can be used for board to board or cable connection?

Board to board (BTB) : PW05, IPS60, IPS70, IPS16, IPS17, IPS19
Power Cable : PW25, PW26, PW82-3, PW03, PW04, PW06, PW07

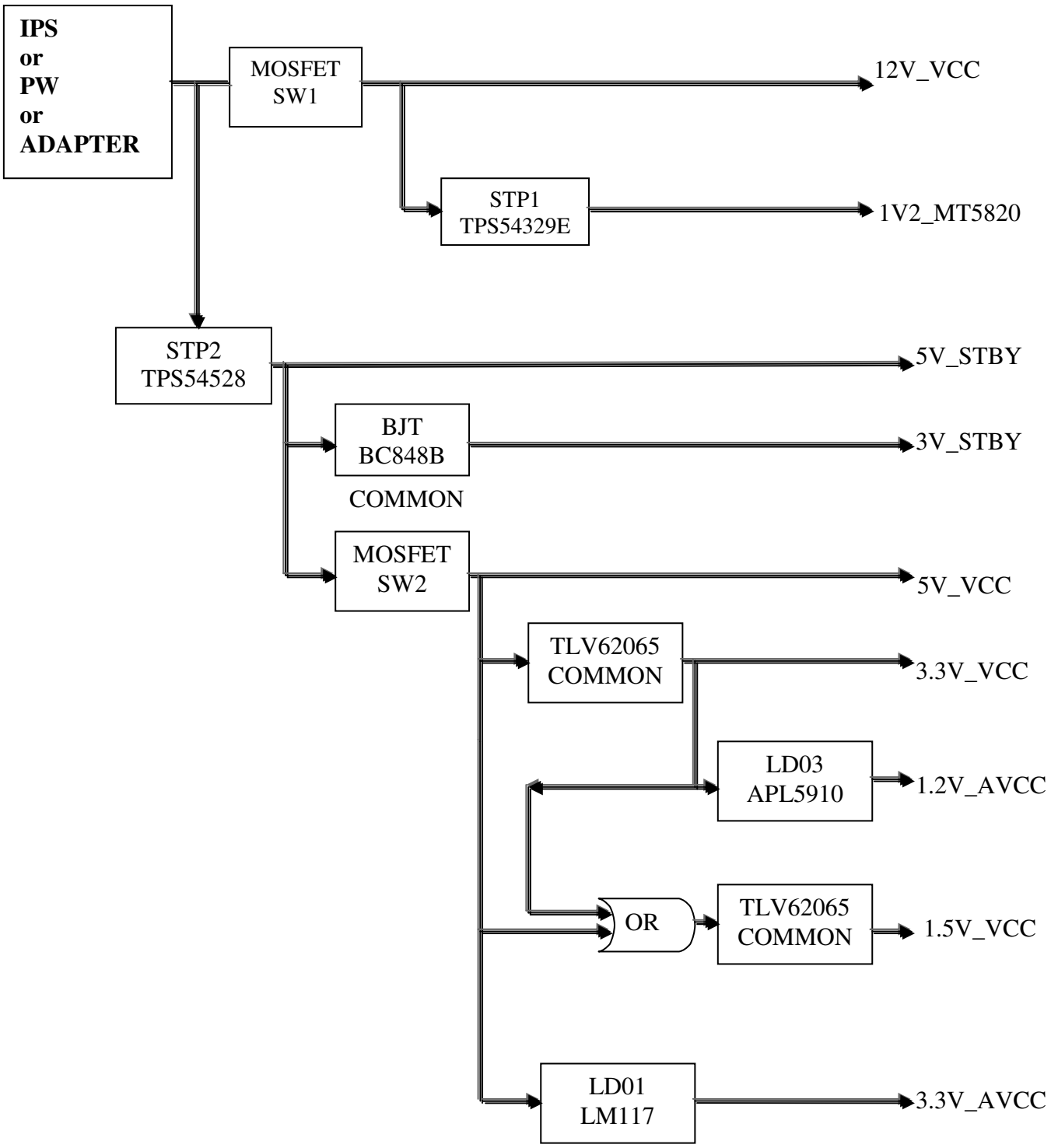
The power supplies generate 24V, 12V, 5V, 3,3V and 12V, 5V, 3.3V stand by mode DC voltages. Power stage which is on-chassis generates 5V, 3V3 stand by voltage and 12V, 8V, 5V, 3V3, 2.5V, 1,8V and 1,2V supplies for other different parts of the chassis. Chassis block diagram is indicated below.

The blocks on power block diagram is using dependent to main supply. For PW26 and PW27 just common blocks are enough for proper operation.

Short CCT Protection Circuit
Short circuit protection is necessary for protecting chassis and main IC against damages when any Vcc supply shorts to ground. Protect pin should be logic high while normal operation. When there is a short circuit protect pin shold be logic low. After any short detection, SW forces LEDs on LED card to blink.


SHORT CCT PROTECTION
3V3_VCC
5V_VCC
3V3_AVCC
24V_VCC_AU
12V_VCC
PANEL_VCC
3V3_VCC
2V5_VCC
1V8_VCC
1V5_VCC
1V25_VCC
1V12_MT5356
1V2_AVCC
3V3_STBY
PROTECT
TP26
C34
100n
10V
Q9
BC848B
R83
10k
R82
10k
R85
10k
R84
10k
Q42
BC858B
Q10
BC848B
R322
100R
R657
47k
R92
10k
R87
10k
R493
33k
R490
33k
R81
5k1
R494
10k
R86
3k9
D41
BAW56
D43
BAW56
D40
BAW56
D39
BAW56
D44
BAW56
D45
BAW56
D46
BAW56
BC858B
Q43
R804
6k8
R88
10k
R91
10k
R805
6k8
R656
820R
R320
1k
R658
1k5
R321
910R
R655
10k
R319
3k3
R654
30k
R325
3k3
47k
R662
100R
R326
R660
1k5
R324
100R

3.1. Power Management



4. MICROCONTROLLER – MediaTek

4.1. Description

MT5820 (Main IC) (U1)

The MediaTek MT5820 family consists of a backend decoder and a TV controller and offers high integration for advanced applications. It combines a transport de-multiplexer, a high definition video decoder, an audio decoder, a dual-link LVDS transmitter, a mini-LVDS transmitter, an EPI transmitter and an NTSC/PAL/SECAM TV decoder with a 3D comb filter (NTSC/PAL). The MT5820 enables consumer electronics manufactures to build high quality, low cost and feature-rich DTV.

World-Leading Audio/Video Technology: The MT5820 supports Full-HD MPEG1/2/4/h.264/DiviX/VC1/RM/AVS/VP6/VP8 (option) video decoder standards, and JPEG. The MT5820 also supports MediaTek MDDiTM de-interlace solution can reach very smooth picture quality for motions. A 3D comb filter added to the TV decoder recovers great details for still pictures. The special color processing technology provides natural, deep colors and true studio quality video. Also, the MT5820 family has built-in high resolution and high-quality audio codec.

Rich Features for High Value Products: The MT5820 family enables true single-chip experience. It integrates high-quality HDMI1.4a, high speed VGA ADC, LVDS, mini-LVDS, EPI, USB2.0 receiver, TCON (option), panel overdrive (option).

WW Common Platform Capability: Reserved transport stream input is for external demodulator for other countries or areas. TV maker can easily port the same UI to worldwide TV models. Excellent adjacent and co-channel rejection capability grants customers never miss any wonderful stream. Professional error-concealment provides stable, smooth and mosaic-free video quality.

Key Features:

1. Worldwide multi-standard analog TV demodulator
2. Powerful CPU core
3. A transport de-multiplexer
4. A muti-standard video decoder
5. Rich format audio codec
6. HDMI1.4a receiver
7. Local dimming (LED backlight) (option)
8. TCON (option)
9. Panel overdrive control (option)
10. LVDS, mini-LVDS, EPI

Note: All packages are lead free

General Features:

Host CPU
- ARM11 single core 700MHz
- Floating Point Unit
- 16K I-Cache and 16K D-Cache for ARM11 core
- 128K L2 Cache
- Boot ROM
- Boot from serial flash, NAND flash
- Supports security boot
- JTAG ICE interface
- Watch Dog timers

Transport Demultiplexer
- New generation 2 demux design for transport stream (TS) process
- Supports 1 serial TS input
- Supports DVB-T/T2, DVB-C, DVB-S/S2, ARIB and DTMB TS input data rate and format
- Supports multi standard hardware engines for TS encryption or decryption
- Up to12 even/odd keys for playback decryption use; 4 even/odd keys for playback for record encryption
- Supports 80 PID filters for playback use and another 64 PID filters for record use
- Supports 80 section filters with bit-wise positive / negative mask
- Supports hardware CRC-32 check
- Supports PCR recovery function without VCXO
- Supports a micro-processor for stream processing and video start code detection

General Copy Protection Unit
- Supports CPPM/CPRM
- Supports AES with 128/192/256 bit key
- Supports AACS
- Supports DES/3DES
- Supports SHA-1/224/256
- Supports MD5
- Supports CSS
- Supports RC4
- Random number generator

MPEG1 Decoder
MPEG2 Decoder
- MPEG MP@ML, MP@HL
- Supports de-blocking filter
- Full-HD 30P dual decoder

MPEG4 Decoder (option)
- ASP@L5
- Full-HD 30P dual decoder

H.264 (MPEG4.10 / AVC) HD Decoder (option)
 MP@L4.0, HP@L4.0, constrained BP@L3 video standard
 Full-HD 30P dual decoder

VC-1 (SMPTE421M) Decoder (option)
 MP@HL, AP@L3
 WMV9 decoder MP@HL
 Full-HD 30P dual decoder

DivX (XviD) Decoder (option)
 DIVX3 / DIVX4 / DIVX5 / DIVX6 / DIVX HD
 Full-HD 30P dual decoder

AVS Decoder (option)
 Jizhun profile @Level 6.2 (supports 4:2:0 format)
 Full-HD 30P dual decoder

RMVB Decoder (option)
 RealVideo8/9/10

Full-HD 30P dual decoder
VP6 Decoder (option)
VP8 Decoder (option)
 Supports 3D side-by-side Full-HD contents
 Full-HD 30P dual decoder

MVC
 H.264 stereo high profile Full-HD 60fps

2D Graphics
 Supports multiple color modes
 Point, horizontal/vertical line primitive drawings
 Rectangle fill and gradient fill functions
 Bitblt with transparent options
 Alpha blending and optional pre-multiplied alpha composition Bitblt
 Stretch Bitblt
 YCbCr to RGB color space conversion
 Supports index to direct mode bitblt

Image Resizer
 Supports 16bpp/32bpp direct color format
 Supports 420/422 video format
 Supports 420/422/444 JPEG format
 Arbitrary ratio vertical/horizontal scaling of video, from 1/128X to 128X
 Simple DMA
 Supports MMU in OSD mode

OSD Plane
 Three linking list OSDs with multiple color mode and all of them have up-scaler
 Supports stereo OSD

Video Plane
 Supports video freeze and over scan
 Flesh tone management
 Gamma correction
 Color Transient Improvement (CTI)
 2D Peaking
 Saturation/hue adjustment
 Brightness and contrast adjustment
 Black and White level extender
 Adaptive Luma management
 Automatic detect video, film and mixed-mode source
 3:2/2:2 pull down source detection
 Supports FHD motion-adaptive de-interlace
 Supports excellent low angle image processing
 Brilliant boundary shaping for moving object
 Advanced non-linear panorama scaling
 Programmable zoom viewer
 Progressive scan output
 Supports alpha blending for OSD on video plane
 Dithering processing for flat panel display
 Frame rate conversion
 Supports FHD panel and VGA dot-to-dot
 Supports PIP/POP, (dual de-interlace, one HD and one SD)

OD (option)
 Supports 60Hz Full-HD and WXGA panel over drive

TCON (option)
 Flexible timing control with programmable timing
 Horizontal timing control
 Vertical timing control
 Multi-line timing control
 Multi-frame timing control
 Supports gate power modulation timing
 Supports command-based timing
 Supports POL inversion every 30 seconds
 Supports 1/2/4/8 frame inversion, 1-line inversion, 2-line inversion, and could up to 255-line dot inversion

Local Dimming
 Block division: up to 800 total blocks, up to 100 horizontal blocks
 Supports 50K ~ 50M SPI clock rate

LVDS
 Supports 6/8/10-bit one-link, 6/8/10-bit dual-link LVDS transmitter
 Built-in spread spectrum for EMI performance
 Programmable panel timing output

Mini-LVDS
 Dual port 8-bit 6 pairs mini-LVDS output

EPI
 6 port, 8/10-bit EPI

CVBS In
 On-chip 54 MHz 10-bit video ADC
 Supports PAL (B,G,D,H,M,N,I,Nc), NTSC, NTSC-4.43, SECAM
 NTSC/PAL supports 3D/2D comb filter
 Built-in motion-adaptive 3D Noise Reduction
 VBI data slicer for CC/TT decoding
 Supports 1 S-Video
 Supports 2-channel CVBS
 Supports SCART connector

VGA In
 Supports VGA input up to UXGA 162 MHz
 Supports full VESA standards

Component Video In
 Supports 2 component video inputs
 Supports 480i / 480p / 576i / 576p / 720p / 1080i / 1080p

Audio ADC
 Supports 2-pair L/R input

Audio digital input
 Supports 1 bit (2 channel) I2S audio input

HDMI Receiver
 Four channel HDMI1.4a
 Maximum data rate can be up to 3.3 GHz
 Audio return channel
 EIA/CEA-861B
 CEC

Video bypass
 ATV bypass
 CVBS Monitor (any AV or S-video input)

TV audio demodulator
 Supports BTSC / EIA-J / A2 / NICAM / PAL FM / SECAM world-wide formats
 Standard automatic detection
 Stereo demodulation, SAP demodulation
 Mode selection (Main/SAP/Stereo

Audio DAC
 Supports 2-pair audio DACs

DRAM Controller
 16-bit DDR2/DDR3 interface
 Supports DDR2 1066Mhz, DDR3 1333Mhz

 Supports 512Mb or 1Gb or 2Gb DDR2 and DDR3 DRAM device
 Supports DDR2-1066/DDR3-1333/DDR3-1600 device

Audio DSP
 Supports AC-3 (Dolby Digital) decoding and E-AC3 (Dolby Digital Plus) decoding (option)
 MPEG-1 layer I/II decoding
 Supports WMA / HE-AAC (option)
 Support Dolby DDCO, and MS10 (option)
 Dolby Prologic II (option)
 Audio output: 5.1ch + 2ch (down mix) + 2ch(bypass)
 Pink noise and white noise generator
 Equalizer
 Bass management
 3D surround processing with virtual surround
 Audio and video lip synchronization
 Supports bass/treble
 Automatic volume control
 Supports 5-bit (10-channel) main audio I2S output interface, each of these channels is up to 24-bit resolution

S/PDIF interface
 Supports SPDIF in bypass
 SPDIF out

Analog TV IF Demodulator
 Supports world-wide analog TV standard
 Accept direct IF and low IF
 Full digital AGC control and carrier recovery
 Embedded SAW filter and IF Amplifier. Cost effective TV front-end structure and no more cost on:
 External analog SAW filters (Video/Audio)
 External analog IF demodulator
 External peripheral circuit on CVBS signal data path
 External SAW filter and IF VGA on tuner

Peripherals
 Three built-in UARTs with Tx and Rx FIFO
 Ten basic serial interfaces: one is for the tuner, four are the masters for general purpose and two of them can be
active in standby mode, one is the slave for VGA DDC, the other four extra slave serial interfaces used for HDMI

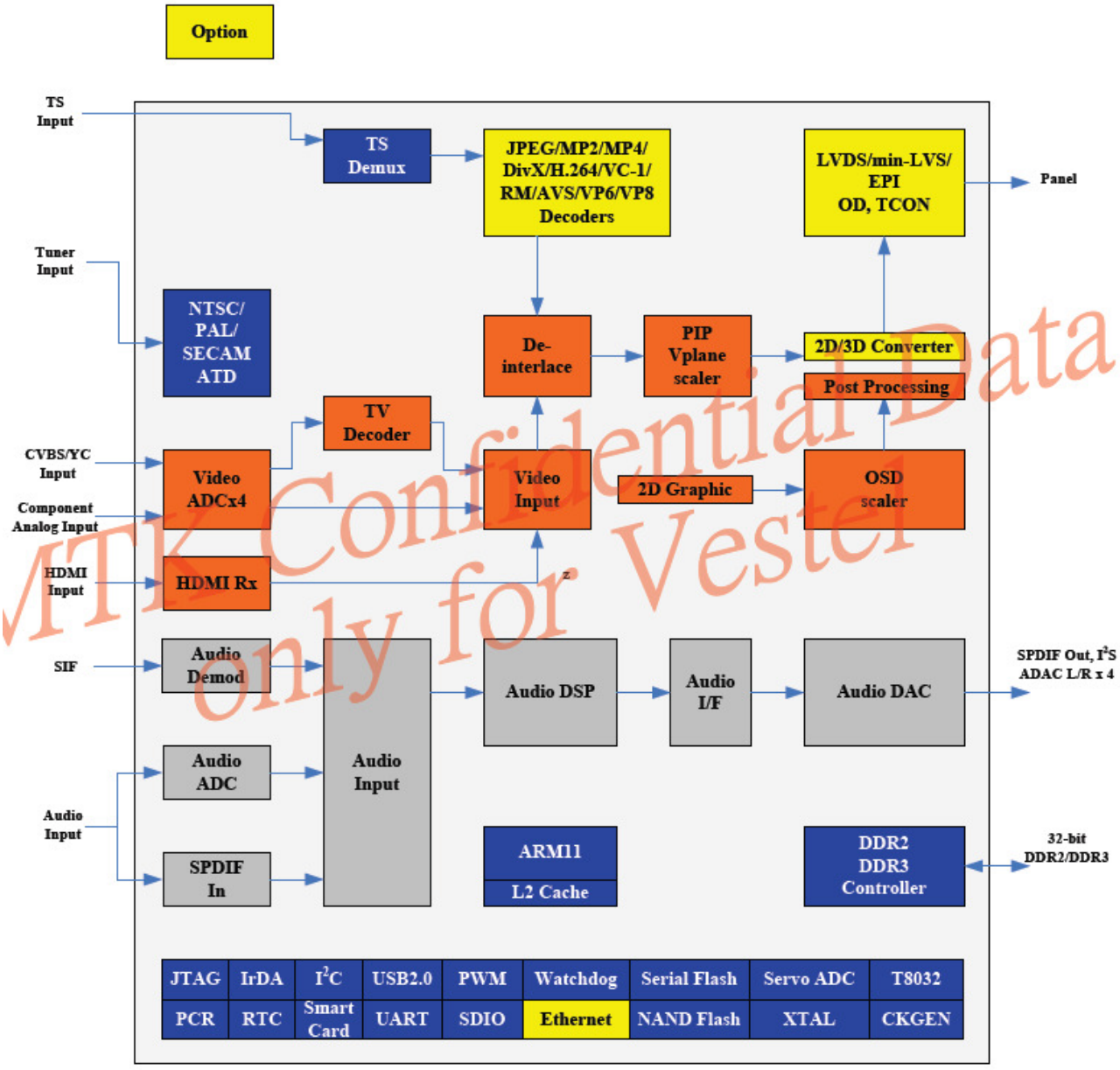
EDID data
 Five PWMs, two of them can be active in standby mode
 IR receiver
 Real-time clock and watchdog controller
 Built-in 2-link USB2.0/1.1, both of them support external hub with 16 endpoints.
 Built-in uP for standby mode
 Supports SDIO interface
 Supports smart card interface

- Supports two serial flash or one serial and one NAND flash
- Supports 4-input low-speed ADC
- Supports boundary scan (JTAG)

IC Outline

- LQFP Package 256 pins with E-pad
- 3.3V/1.2V and 1.8V for DDR2 or 1.5V for DDR3

4.2. MediaTek Block Diagram



4.3. Crystal Specification

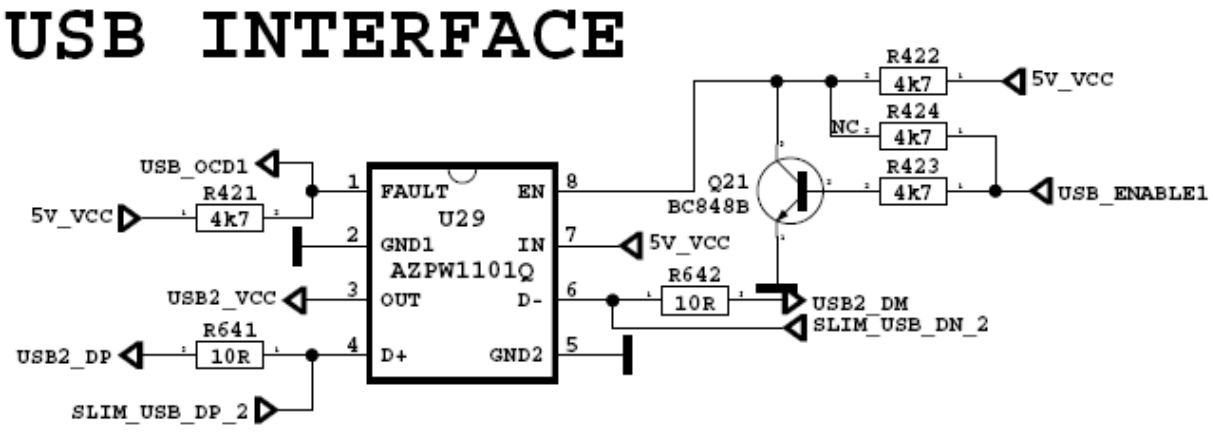
Parameters	Value	Unit
Nominal Frequency	27	MHz
Oscillation Mode	Fundamental	
Load Capacitance	20	pF
Frequency Tolerance (25°C)	±30	ppm
Effective Series Resistance	Max: 40	ohm
Operation Temperature Range	-20~ +80	°C
Stability Over Operation Temperature Range	±70	ppm

5. USB INTERFACE

Main Concept IC has integrated 2 USB 2.0 interface. One of them is used for ethernet function, the other one is used for USB connectivity for last user. Last user can play video, picture and audio files. Also digital channels can be record to externall storage device by this interface. All SW files can be updated with interface.

USB circuit has 3 main parts

- Integrated USB 2.0 Host interface of D3K
- Protection IC
- Over Curent Protection IC



6. DDR3 SDRAM 1Gb G-die

6.1 Description:

The 1Gb DDR3 SDRAM G-die is organized as a 8Mbit x 16 I/Os x 8banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 2133Mb/sec/pin(DDR3-2133)for general applications. The chip is designed to comply with the following key DDR3 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset . All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a RAS/CAS multiplexing style. The DDR3 device operates with a single 1.5V ± 0.075V power supply and 1.5V ± 0.075V VDDQ. The 1Gb DDR3 G-die device is available in 96ball FBGA(x16).

6.2 Features

• JEDEC standard 1.5V ± 0.075V Power Supply
• VDDQ = 1.5V ± 0.075V
• 533MHz fCK for 1066Mb/sec/pin, 667MHz fCK for 1333Mb/sec/pin, 800MHz fCK for 1600Mb/sec/pin, 933 MHz fCK for 1866Mb/sec/pin, 1066 MHz fCK for 2133Mb/sec/pin
• 8 Banks
• Programmable CAS Latency(posted CAS): 5, 6, 7, 8, 9, 10, 11, 12, 13, 14
• Programmable Additive Latency: 0, CL-2 or CL-1 clock
• Programmable CAS Write Latency (CWL) = 6 (DDR3-1066), 7 (DDR3-1333), 8 (DDR3-1600), 9 (DDR3-1866), 10 (DDR3-2133)
• 8-bit pre-fetch
• Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
• Bi-directional Differential Data-Strobe
• Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
• On Die Termination using ODT pin
• Average Refresh Period 7.8us at lower than TCASE 85℃, 3.9us at 85℃ < TCASE < 95 ℃
• Asynchronous Reset
• Package : 96 balls FBGA - x16
• All of Lead-Free products are compliant for RoHS
• All of products are Halogen-free

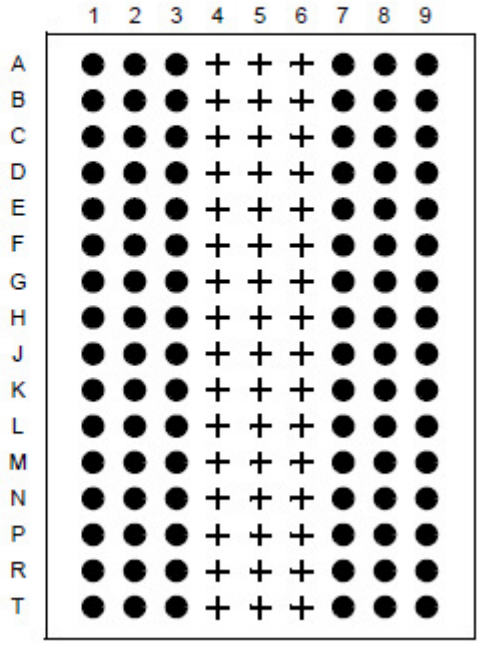
x16 Package Pinout (Top view) : 96ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	V_{DDQ}	DQU5	DQU7				DQU4	V_{DDQ}	V_{SS}	A
B	V_{SSQ}	V_{DD}	V_{SS}				$\overline{DQSU}$	DQU6	V_{SSQ}	B
C	V_{DDQ}	DQU3	DQU1				DQSU	DQU2	V_{DDQ}	C
D	V_{SSQ}	V_{DDQ}	DMU				DQU0	V_{SSQ}	V_{DD}	D
E	V_{SS}	V_{SSQ}	DQL0				DML	V_{SSQ}	V_{DDQ}	E
F	V_{DDQ}	DQL2	DQSL				DQL1	DQL3	V_{SSQ}	F
G	V_{SSQ}	DQL6	$\overline{DQSL}$				V_{DD}	V_{SS}	V_{SSQ}	G
H	V_{REFDQ}	V_{DDQ}	DQL4				DQL7	DQL5	V_{DDQ}	H
J	NC	V_{SS}	$\overline{RAS}$				CK	V_{SS}	NC	J
K	ODT	V_{DD}	$\overline{CAS}$				$\overline{CK}$	V_{DD}	CKE	K
L	NC	$\overline{CS}$	$\overline{WE}$				A10/AP	ZQ	NC	L
M	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}	M
N	V_{DD}	A3	A0				A12/$\overline{BC}$	BA1	V_{DD}	N
P	V_{SS}	A5	A2				A1	A4	V_{SS}	P
R	V_{DD}	A7	A9				A11	A6	V_{DD}	R
T	V_{SS}	$\overline{RESET}$	NC				NC	A8	V_{SS}	T

Ball Locations (x16)

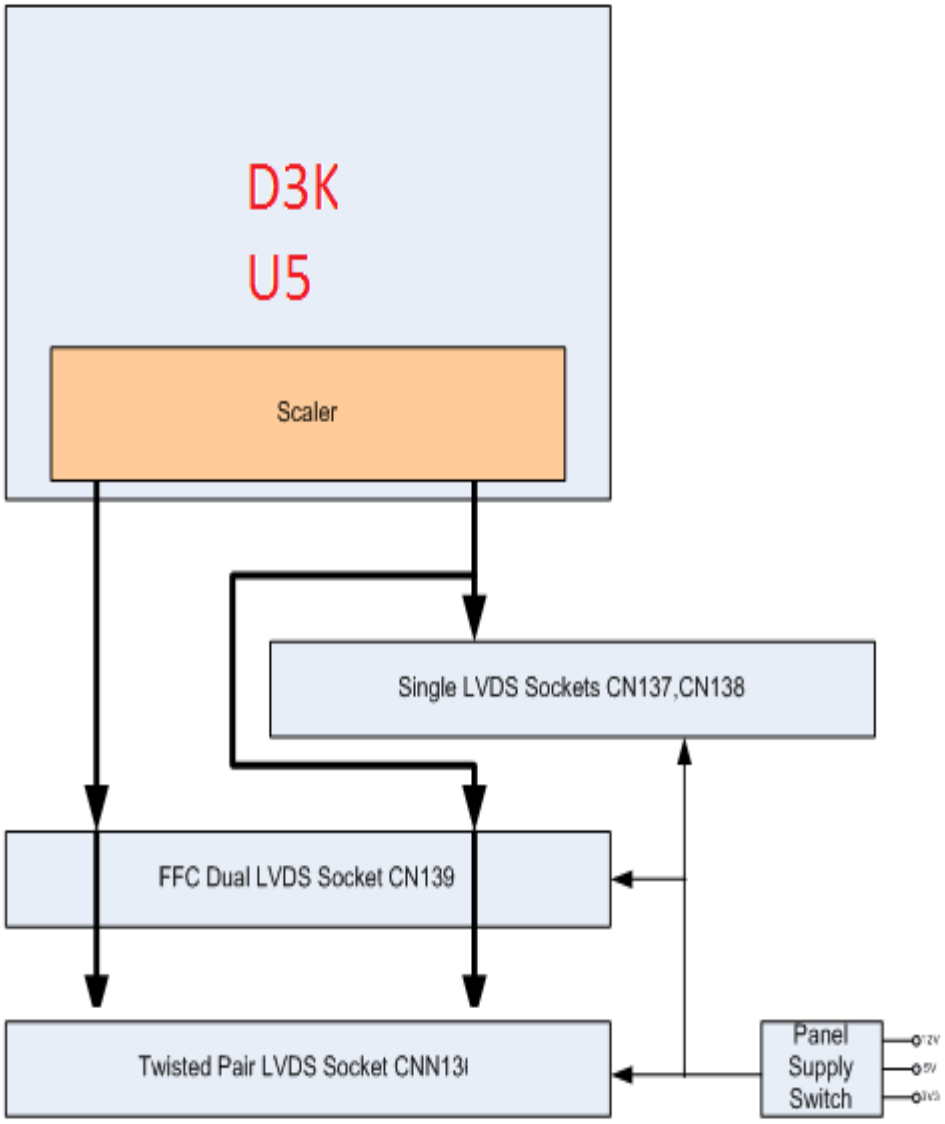
● Populated ball
\+ Ball not populated

Top view
(See the balls through the package)



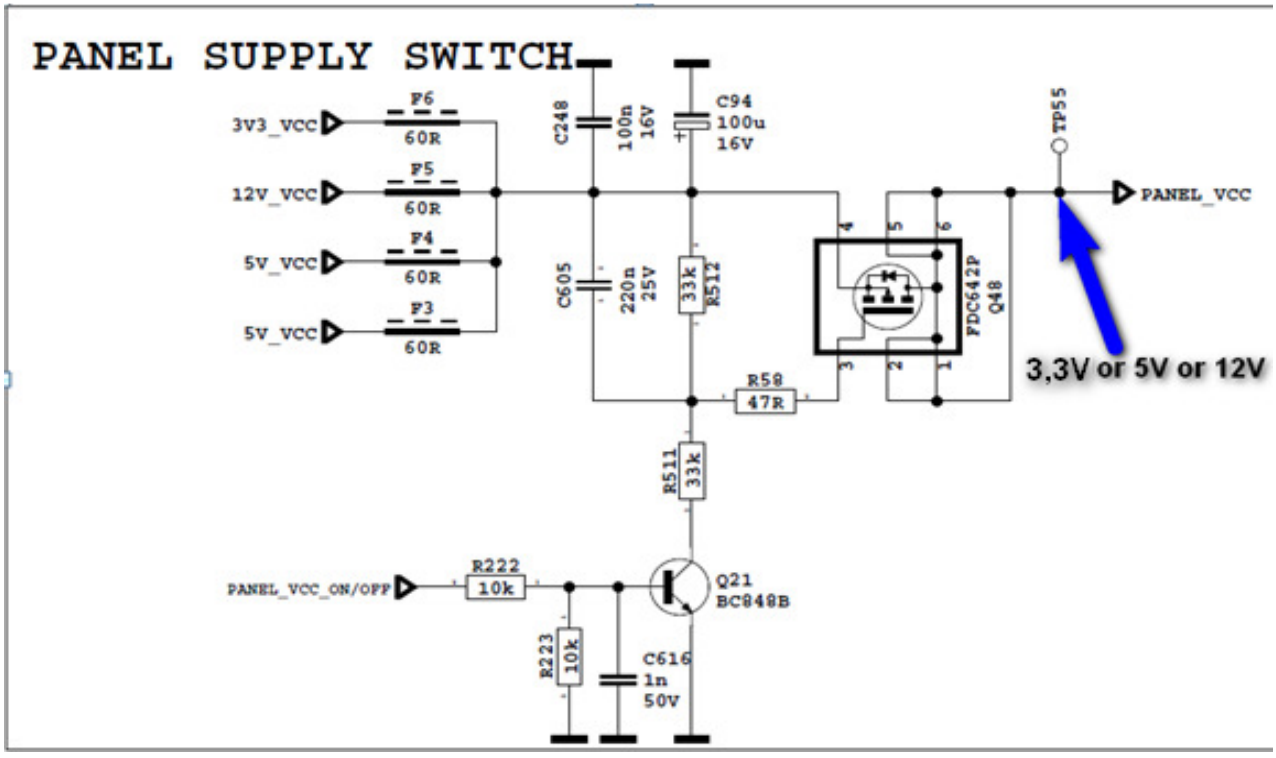
7. SCALER AND LVDS SOCKETS

7.1. LVDS sockets Block Diagram



7.2. Panel Supply Switch Circuit

This switch is used to open and close panel supply of TCON. It is controlled by port of main ucontroller. Also with this circit panel sequency could be adjusted correctly. 3 panel supplys are connected to this circuit. All of them are optional according to panels.



8. SPI FLASH MEMORY

8.1 EN25Q64 64 Megabit Serial Flash Memory with 4Kbyte Uniform Sector

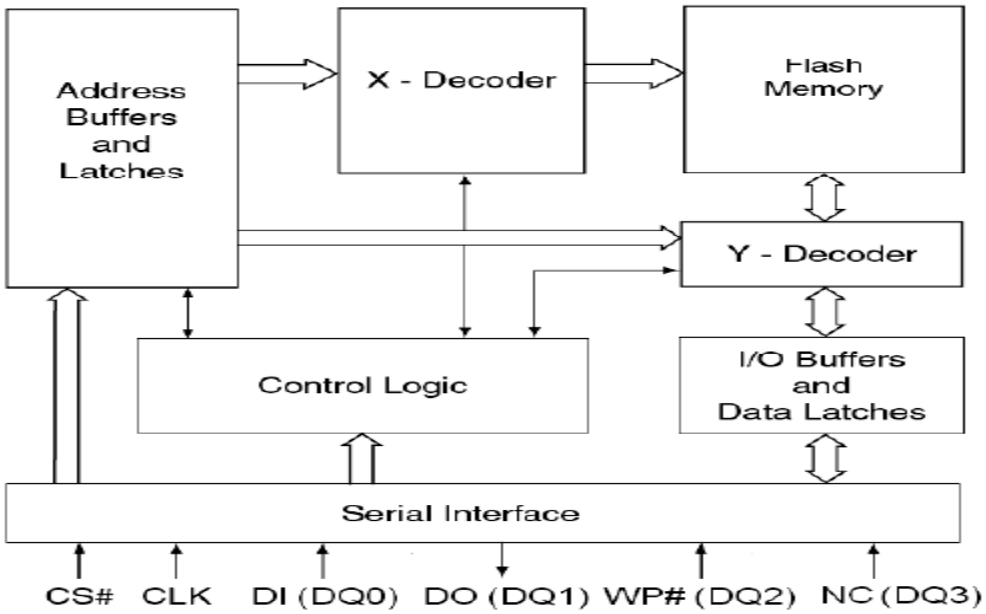
8.1.1 General Description

The EN25Q64 is a 64 Megabit (8192K-byte) Serial Flash memory, with advanced write protection mechanisms. The EN25Q64 supports the standard Serial Peripheral Interface (SPI), and a high performance Dual output as well as Quad I/O using SPI pins: Serial Clock, Chip Select, Serial DQ0(DI), DQ1(DO), DQ2(WP#) and DQ3(NC). SPI clock frequencies of up to 50MHz are supported allowing equivalent clock rates of 100MHz for Dual Output and 200MHz for Quad Output when using the Dual/Quad Output Fast Read instructions. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction. The EN25Q64 is designed to allow either single Sector/Block at a time or full chip erase operation. The EN25Q64 can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

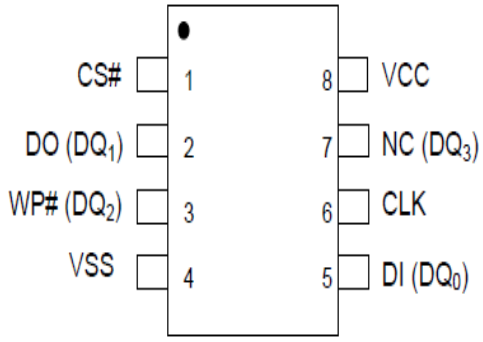
8.1.2 Features

- Single power supply operation
  - Full voltage range: 2.7-3.6 volt
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- 64 M-bit Serial Flash
  - 64 M-bit/8192 K-byte/32768 pages
  - 256 bytes per programmable page
- Standard, Dual or Quad SPI
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DQ_0, DQ_1, WP#
  - Quad SPI: CLK, CS#, DQ_0, DQ_1, DQ_2, DQ_3
- High performance
  - 104MHz clock rate for one data bit
  - 50MHz clock rate for two data bits
  - 50MHz clock rate for four data bits
- Low power consumption
  - 12 mA typical active current
  - 1 μA typical power down current
- Uniform Sector Architecture:
  - 2048 sectors of 4-Kbyte
  - 128 blocks of 64-Kbyte
  - Any sector or block can be erased individually
- Software and Hardware Write Protection:
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- High performance program/erase speed
  - Page program time: 1.3ms typical
  - Sector erase time: 90ms typical
  - Block erase time 500ms typical
  - Chip erase time: 30 seconds typical
- Write Suspend and Write Resume
- Lockable 512 byte OTP security sector
- Minimum 100K endurance cycle
- Package Options
  - 8 pins SOP 200mil body width
  - 8 contact VDFN (5x6mm)
  - 8 contact VDFN (6x8mm)
  - 16 pins SOP 300mil body width
  - All Pb-free packages are RoHS compliant
- Industrial temperature Range

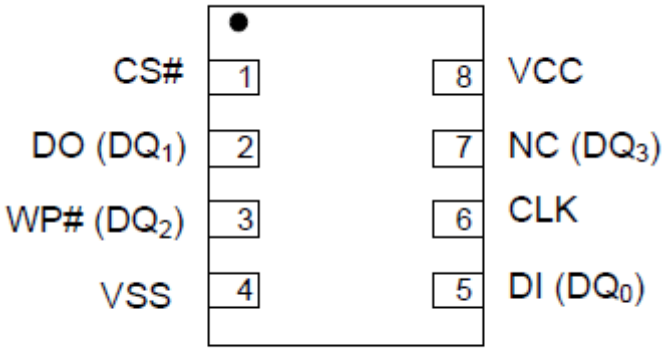
8.1.3 Block Diagram



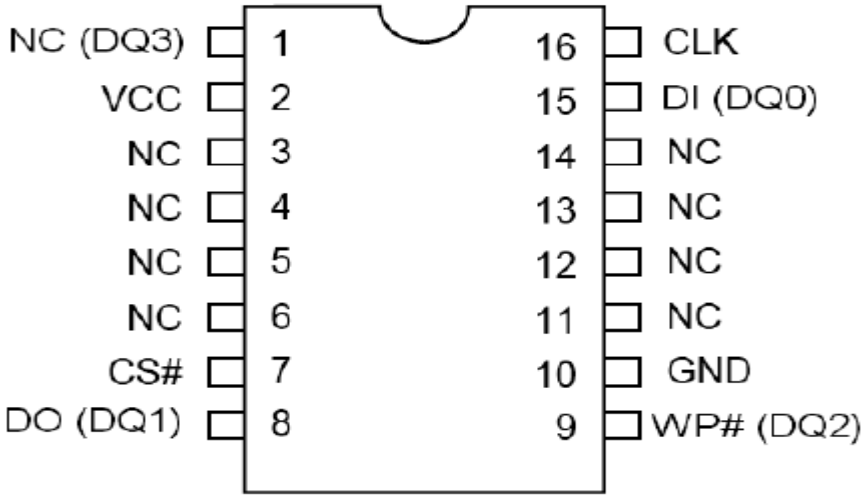
8.1.4 Pinning



8 - LEAD SOP / PDIP



8 - LEAD VDFN



Symbol	Pin Name
CLK	Serial Clock Input
DI (DQ_0)	Serial Data Input (Data Input Output 0)
DO (DQ_1)	Serial Data Output (Data Input Output 1)
CS#	Chip Enable
WP# (DQ_2)	Write Protect (Data Input Output 2)
NC(DQ_3)	Not Connect (Data Input Output 3)
Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground
NC	No Connect

8.2 EN25QH16 16 Megabit Serial Flash Memory with 4Kbyte Uniform Sector

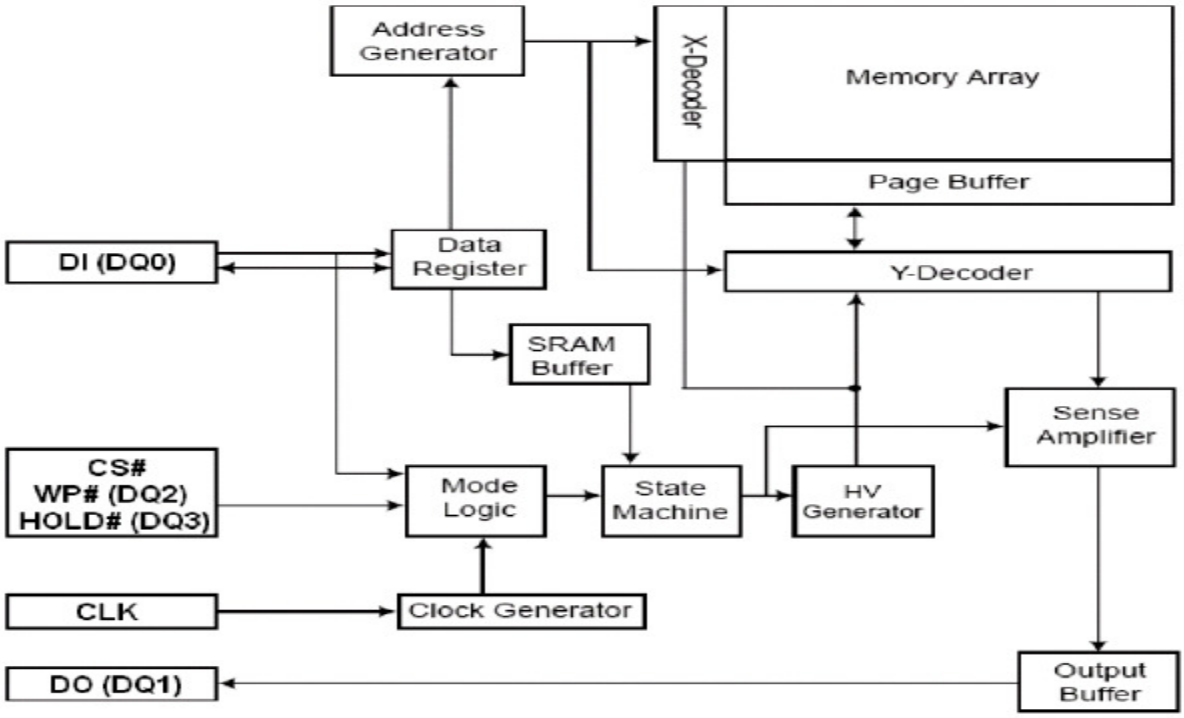
8.2.1 General Description

The EN25QH16 is a 16 Megabit (2,048 K-byte) Serial Flash memory, with enhanced write protection mechanisms. The EN25QH16 supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O using SPI pins: Serial Clock, Chip Select, Serial DQ0(DI), DQ1(DO), DQ2(WP#) and DQ3(HOLD#). SPI clock frequencies of up to 80MHz are supported allowing equivalent clock rates of 160MHz (80MHz x 2) for Dual Output and 320MHz (80MHz x 4) for Quad Output when using the Dual/Quad I/O Fast Read instructions. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction. The EN25QH16 is designed to allow either single Sector/Block at a time or full chip erase operation. The EN25QH16 can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

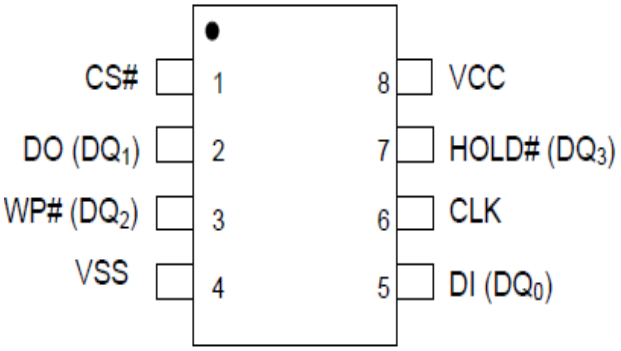
8.2.2 Features

- Single power supply operation
  - Full voltage range: 2.7-3.6 volt
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- 16 M-bit Serial Flash
  - 16 M-bit/2,048 K-byte/8,192 pages
  - 256 bytes per programmable page
- Standard, Dual or Quad SPI
  - Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
  - Dual SPI: CLK, CS#, DQ_0, DQ_1, WP#, HOLD#
  - Quad SPI: CLK, CS#, DQ_0, DQ_1, DQ_2, DQ_3
- High performance
  - 104MHz clock rate for Standard SPI
  - 80MHz clock rate for two data bits
  - 80MHz clock rate for four data bits
- Low power consumption
  - 12 mA typical active current
  - 1 μA typical power down current
- Uniform Sector Architecture:
  - 512 sectors of 4-Kbyte
  - 32 blocks of 64-Kbyte
  - Any sector or block can be erased individually
- Software and Hardware Write Protection:
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- High performance program/erase speed
  - Page program time: 1.3ms typical
  - Sector erase time: 60ms typical
  - Block erase time 400ms typical
  - Chip erase time: 12 seconds typical
- Lockable 512 byte OTP security sector
- Support Serial Flash Discoverable Parameters (SFDP) signature
- Read Unique ID Number
- Minimum 100K endurance cycle
- Package Options
  - 8 pins SOP 150mil body width
  - 8 pins SOP 200mil body width
  - 8 contact VDFN (5x6mm)
  - 8 pins PDIP
  - 24 balls TFBGA (6x8mm)
  - All Pb-free packages are RoHS compliant
- Industrial temperature Range

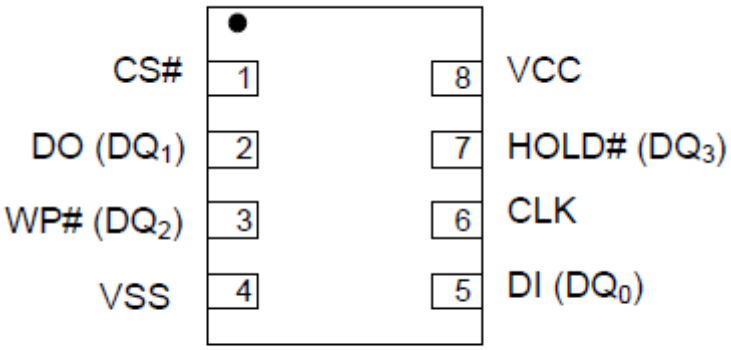
8.2.3 Block Diagram



8.2.4 Pinning

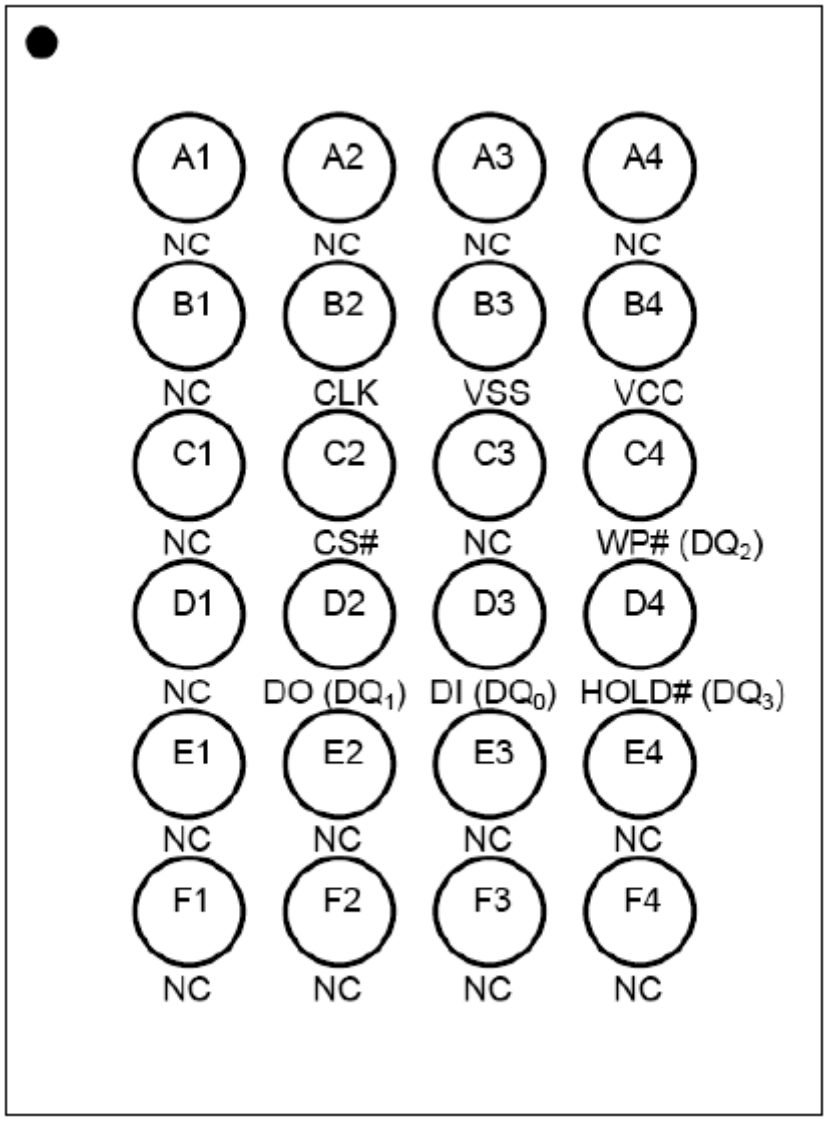


8 - LEAD SOP / PDIP



8 - LEAD VDFN

Top View, Balls Facing Down



24 - Ball TFBGA

9. I-LM1117/LM 800mA Low-Dropout Linear Regulator

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

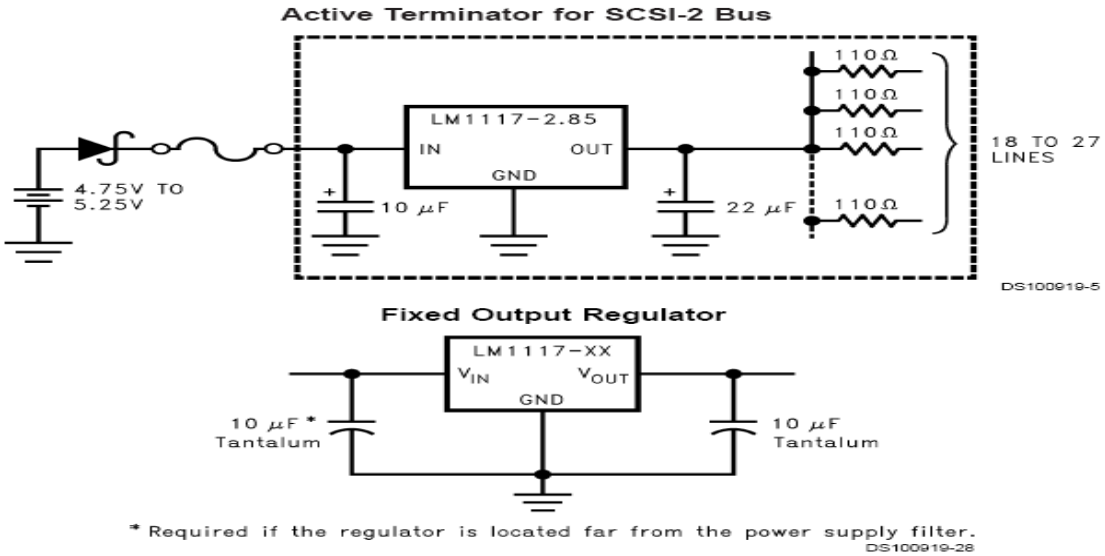
The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%. The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
-- Space Saving SOT-223 Package
-- Current Limiting and Thermal Protection
-- Output Current 800mA
-- Line Regulation 0.2% (Max)
-- Load Regulation 0.4% (Max)
-- Temperature Range
— LM1117 0℃ to 125℃
— LM1117I –40℃ to 125℃

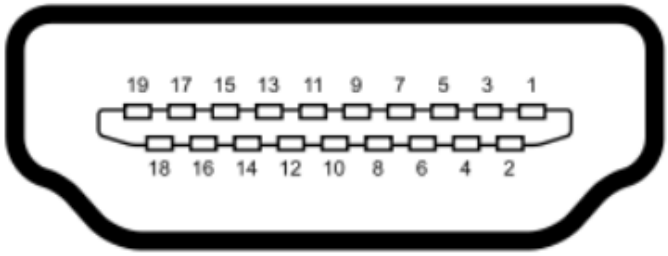
Applications

n 2.85V Model for SCSI-2 Active Termination
n Post Regulator for Switching DC/DC Converter
n High Efficiency Linear Regulators
n Battery Charger
n Battery Powered Instrumentation



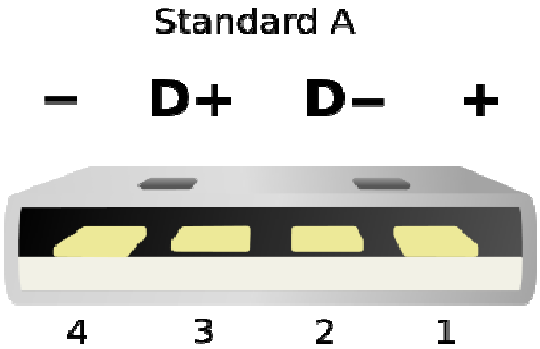
10. CONNECTORS

10.1. HDMI (CN707,CN708)



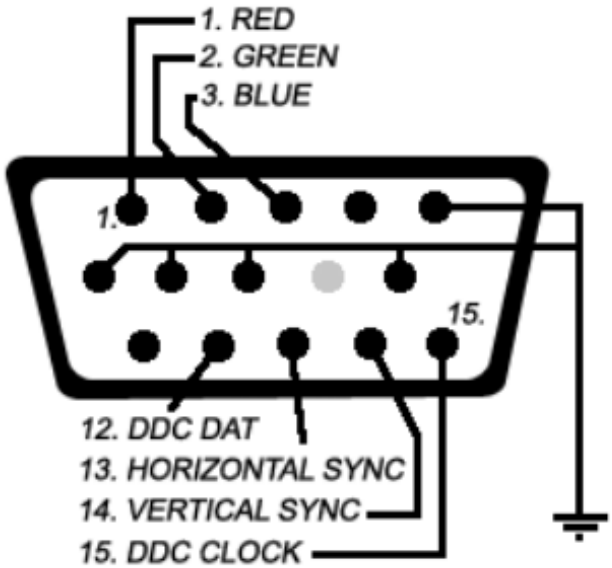
Pin Number	Signal Name	Pin Number	Signal Name
1	TMDS Data 2+	20	SHELL
2	TMDS Data 2 Shield	19	Hot Plug Detect
3	TMDS Data 2-	18	+5V Power
4	TMDS Data 1+	17	Ground
5	TMDS Data 1 Shield	16	DDC Data
6	TMDS Data 1-	15	DDC Clock
7	TMDS Data 0+	14	No Connect
8	TMDS Data 0 Shield	13	CEC
9	TMDS Data 0-	12	TMDS Clock-
10	TMDS Clock+	11	TMDS Clock Shield

10.2. USB(CN37, CN38)

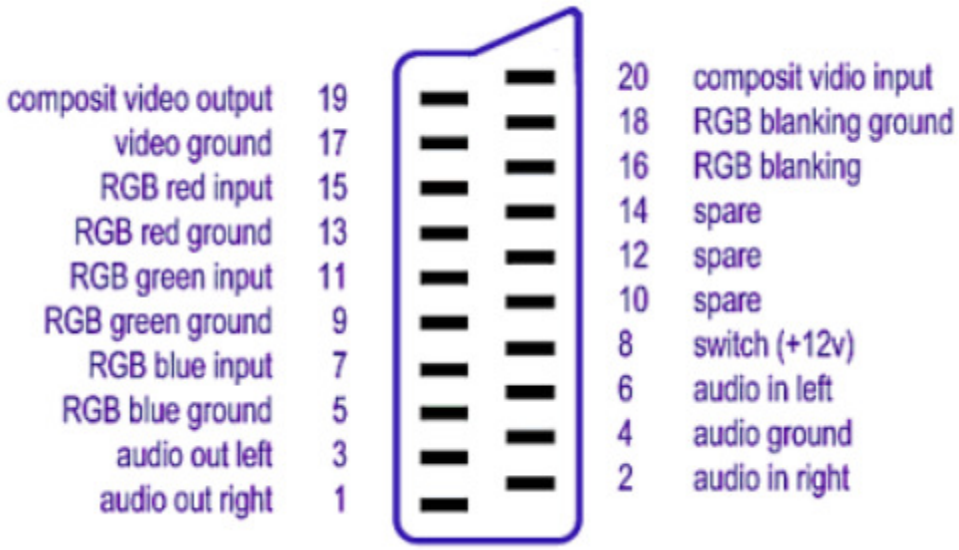


Pin	Name	Cable color	Description
1	VBUS	Red	5 V
2	D-	White (gold*)	Data –
3	D+	Green	Data+
4	GND	Black (blue*)	Ground

10.3. VGA (CN711)



10.4. SCART (SC1)

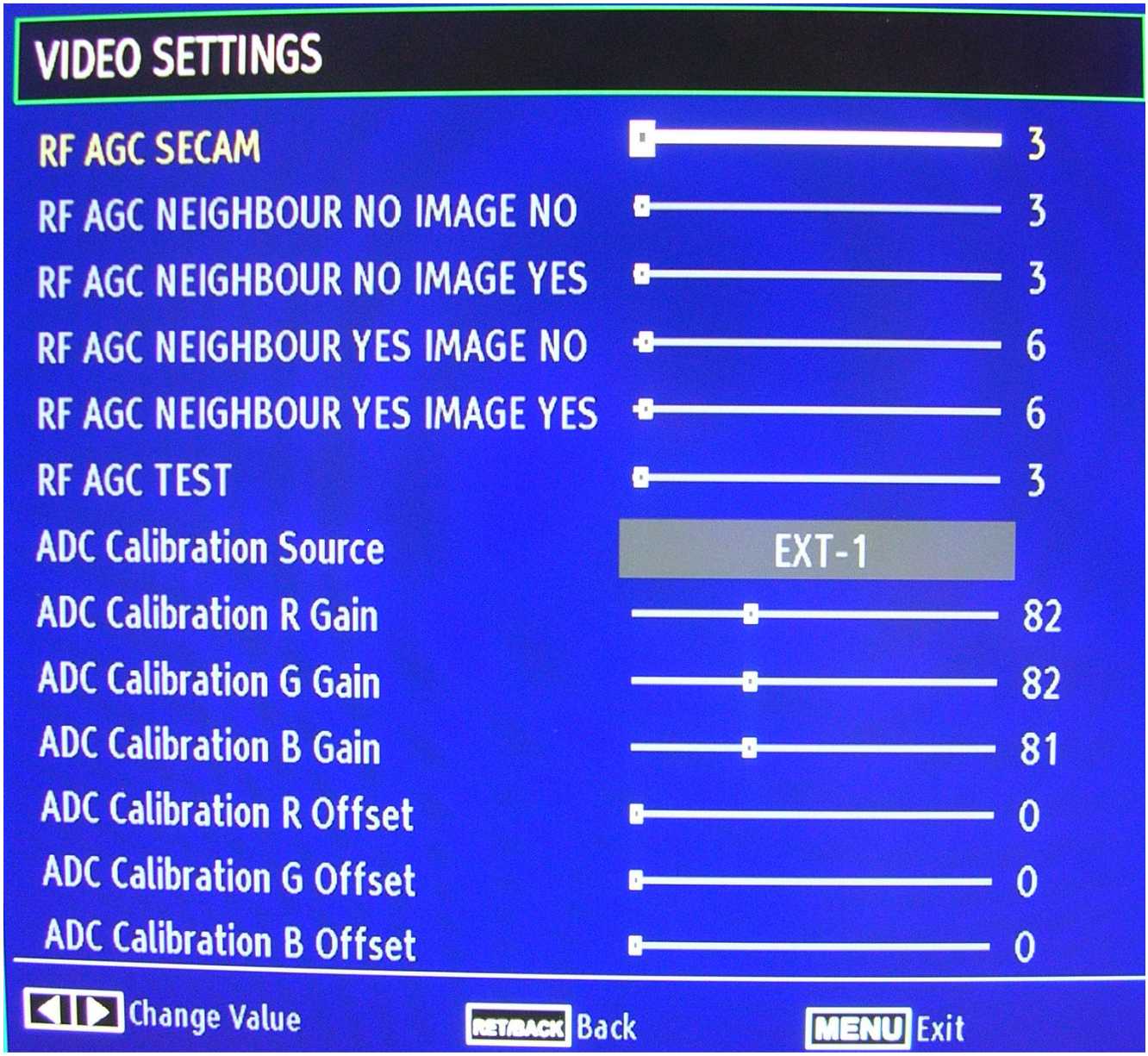


11. SERVICE MENU SETTINGS

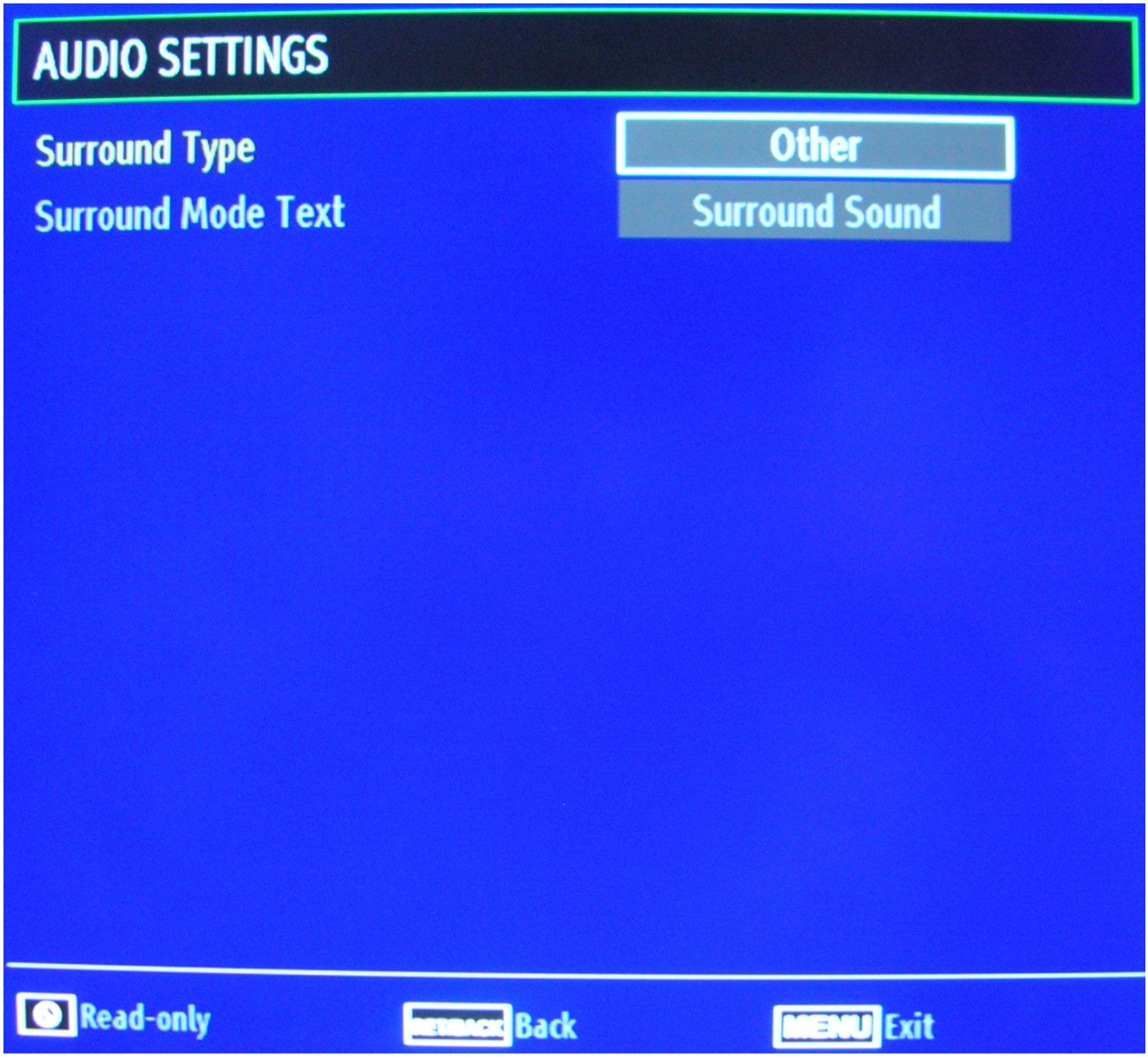
In order to reach service menu, First Press “MENU” Then press the remote control code two times, which is “4725”.

In first screen following items can be seen:

11.1. Video Settings

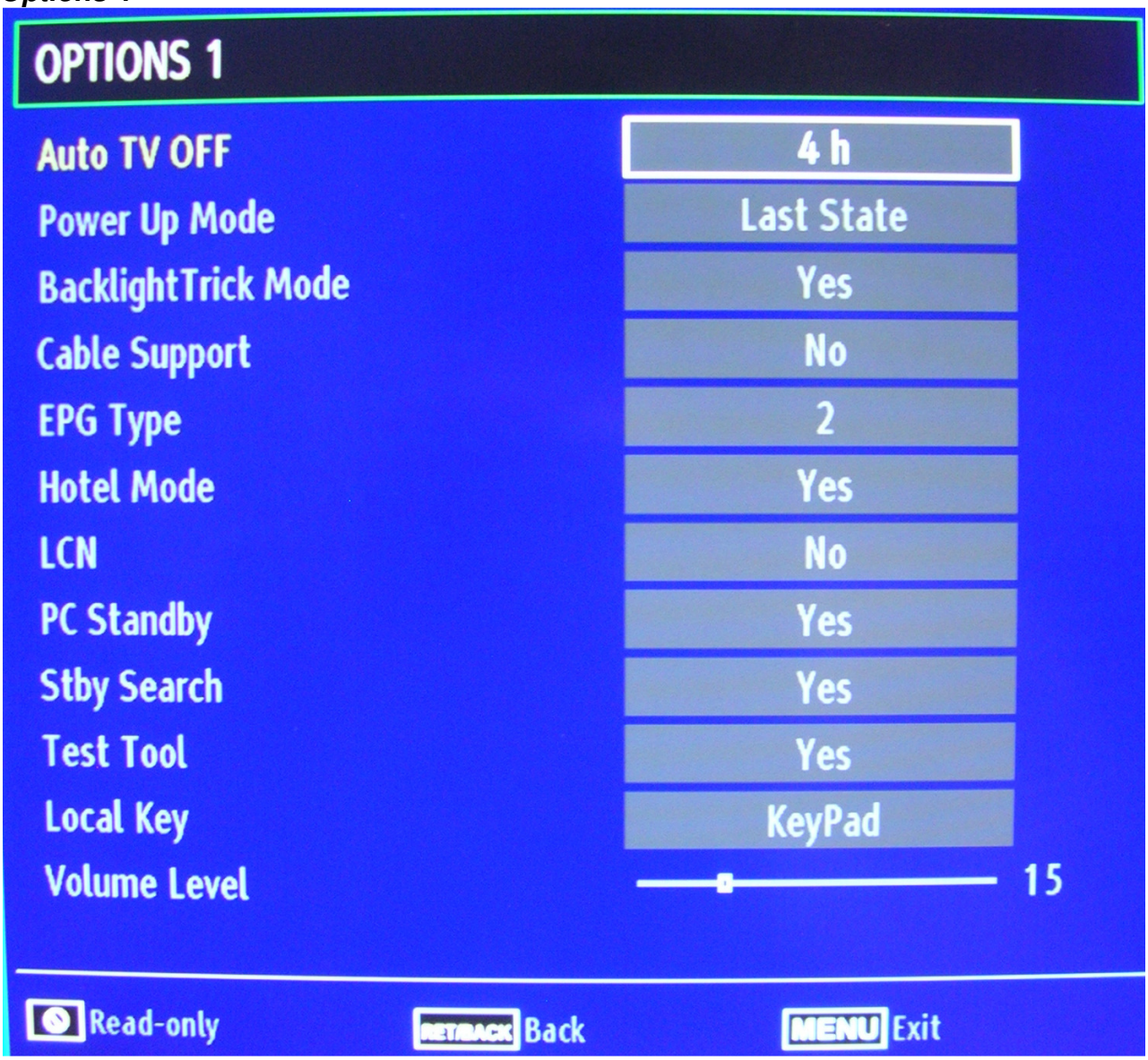


11.2. Audio Settings

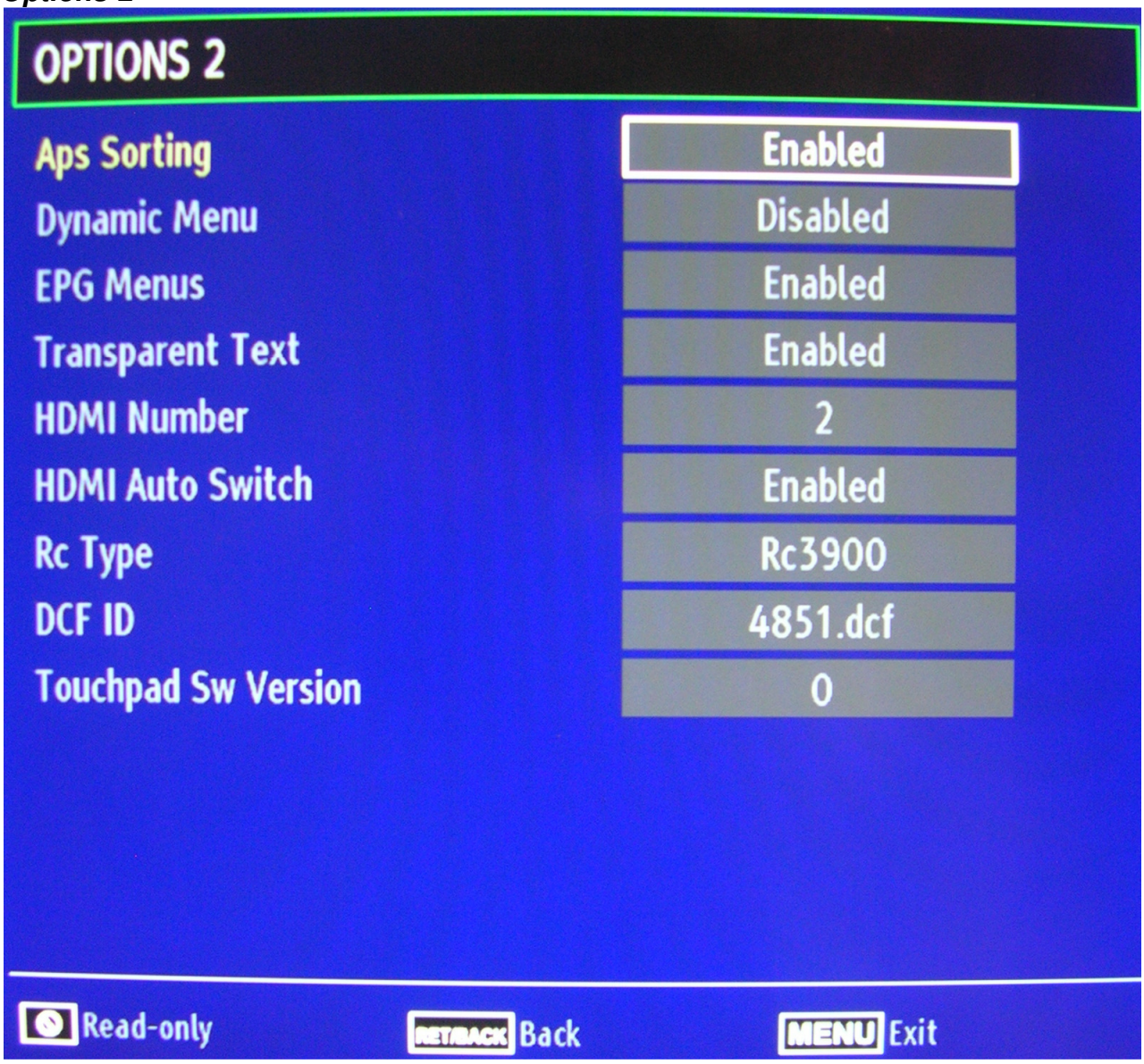


11.3. Options

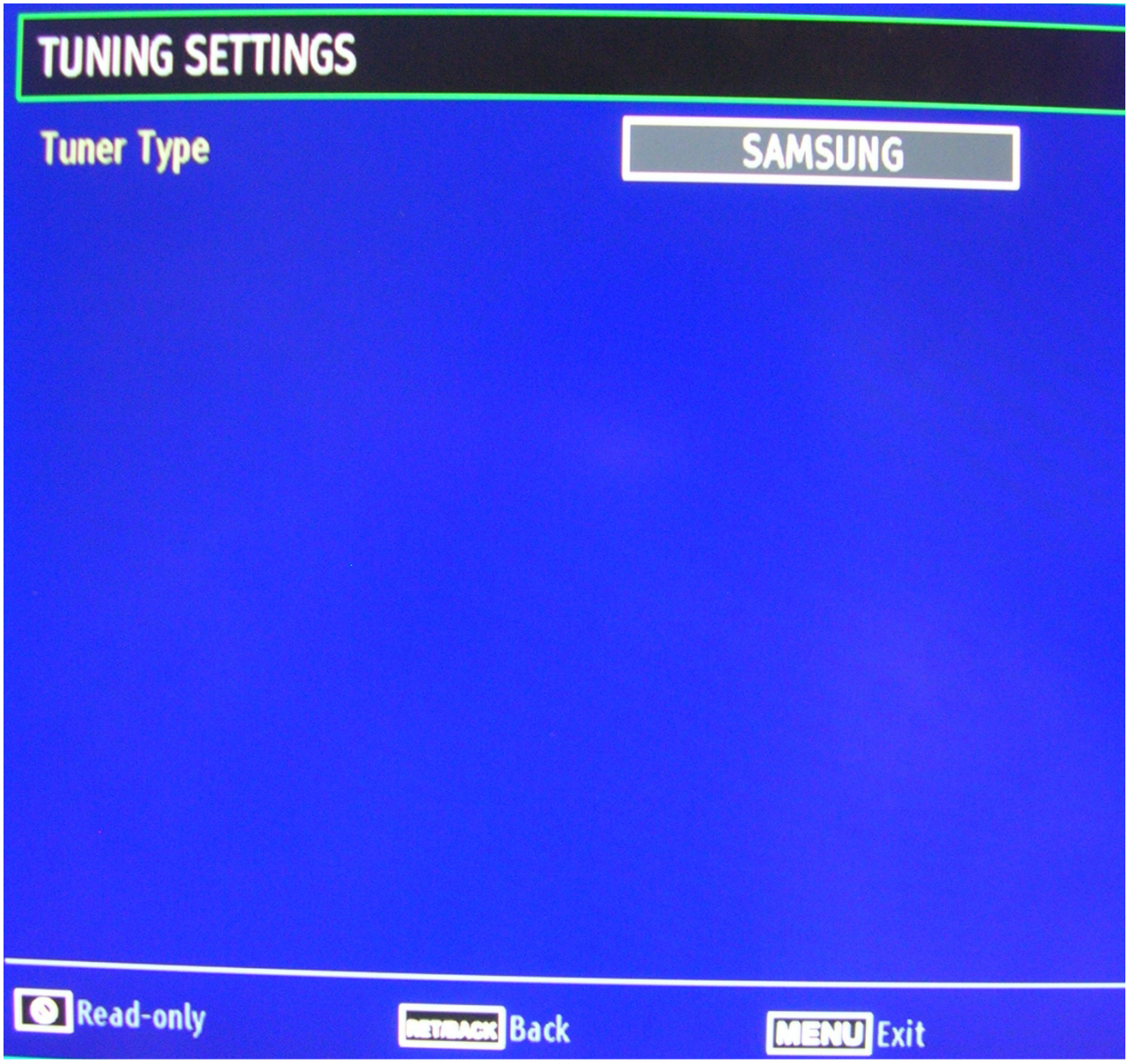
Options-1



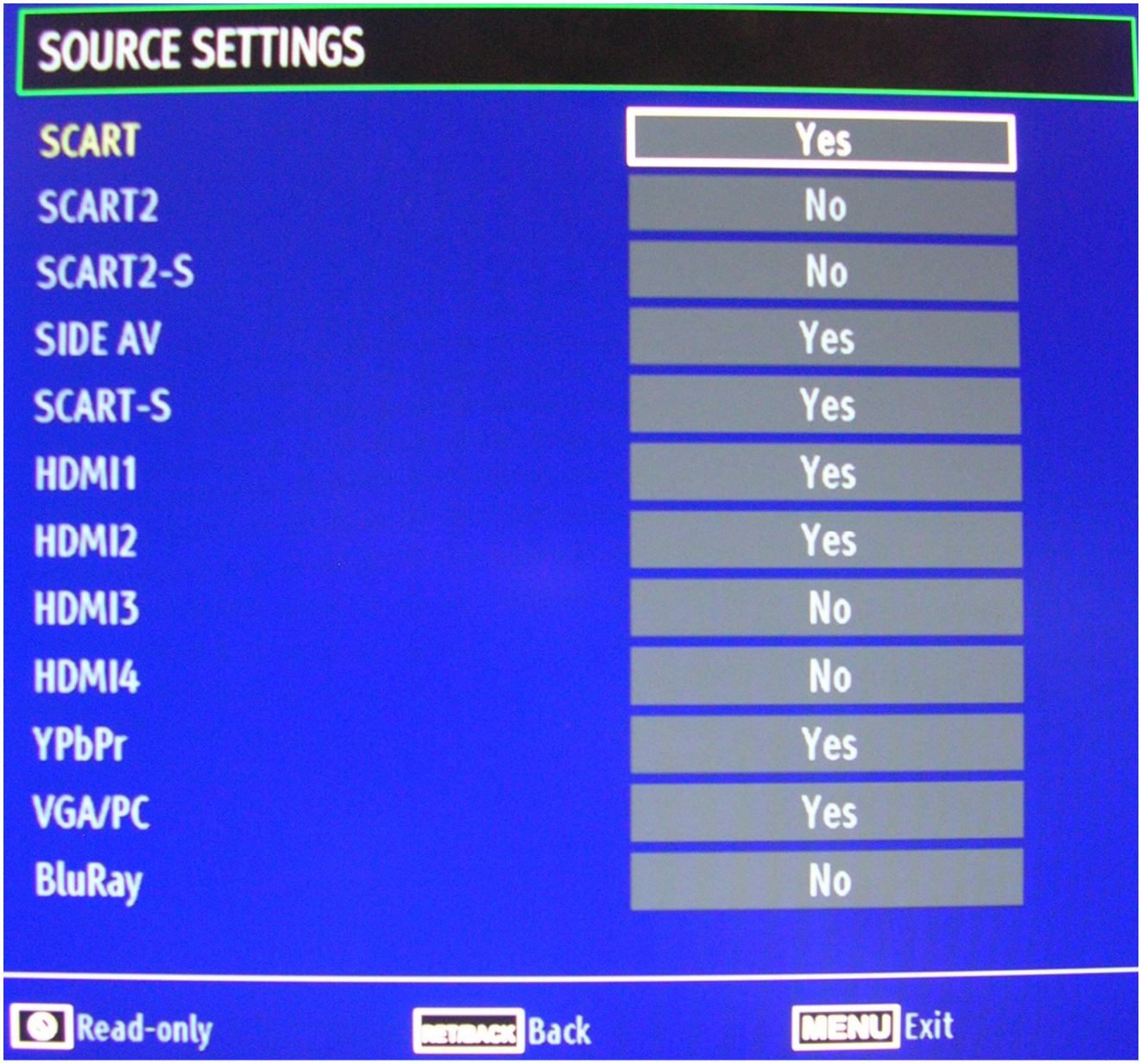
Options-2


OPTIONS 2
Aps Sorting
Enabled
Dynamic Menu
Disabled
EPG Menus
Enabled
Transparent Text
Enabled
HDMI Number
2
HDMI Auto Switch
Enabled
Rc Type
Rc3900
DCF ID
4851.dcf
Touchpad Sw Version
0
Read-only
RETBACK Back
MENU Exit

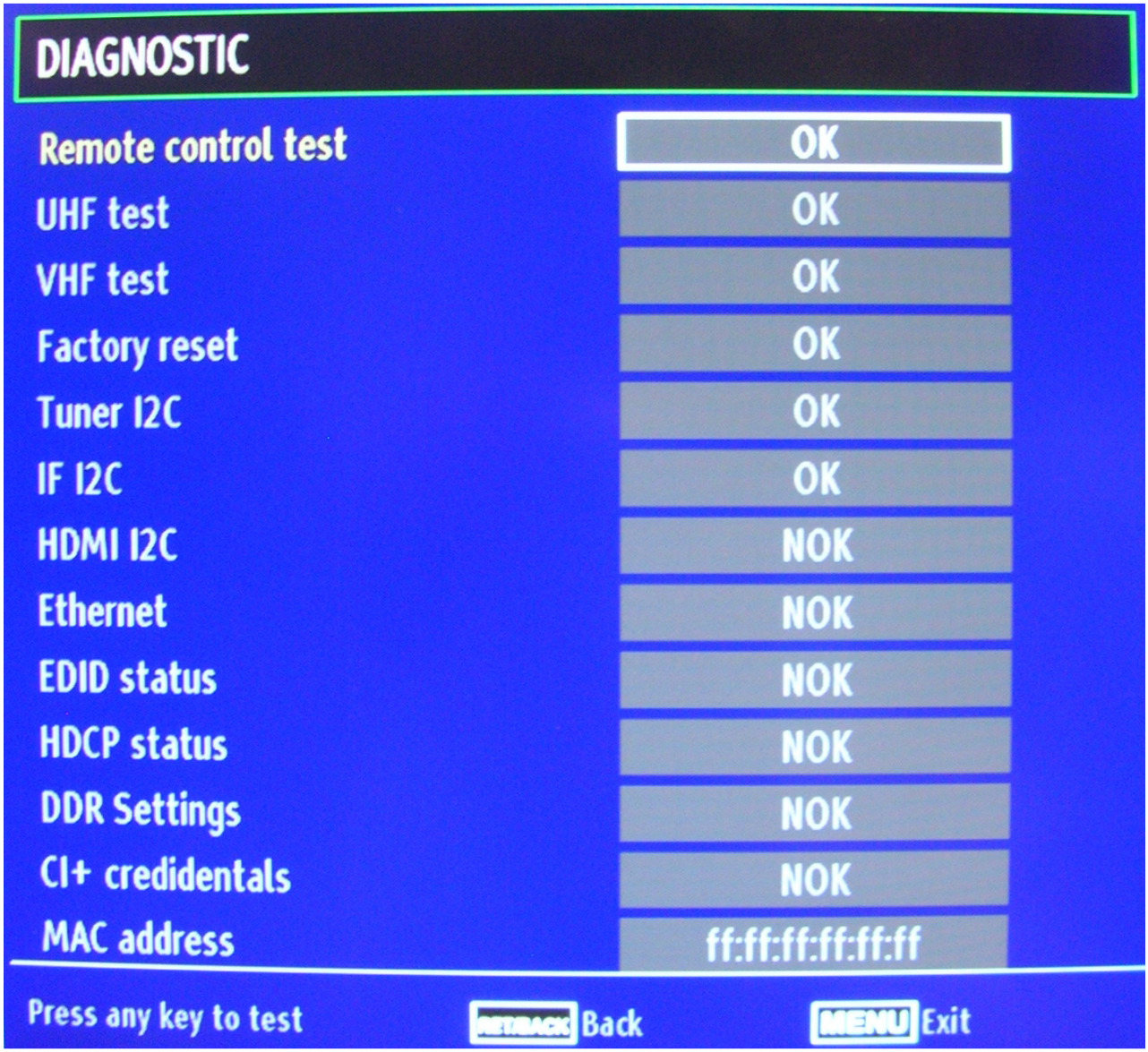
11.4. Tuning Settings



11.5. Source Settings



11.6. Diagnostic



11.7 USB Operations

USB operations option can not be used directly. It can be used for updating panel tool, hw congiguration etc.

12. SOFTWARE UPDATE

In MB82 project there is only one software. From following steps software update procedure can be seen:

1. MB82.bin directly inside of a flash memory(not in a folder).
2. Put flash memory to the tv when tv is powered off.
3. Power on the and pree OK button on the remote control when the tv is opened.
4. If First Time Installition screen comes, it means software update procedure is succesful.

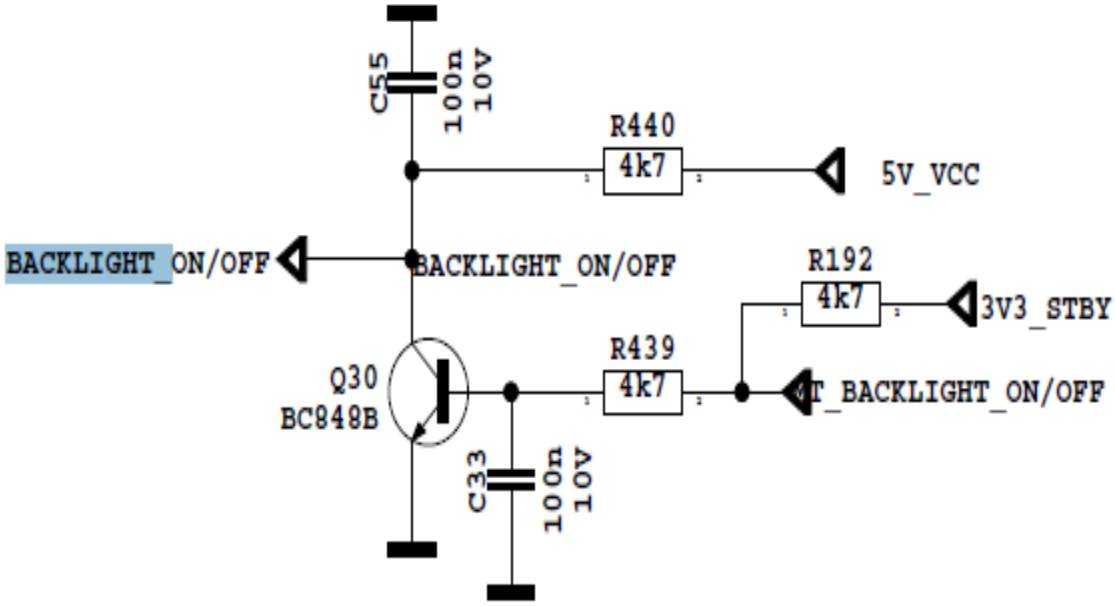
13. TROUBLESHOOTING

13.1. No Backlight Problem

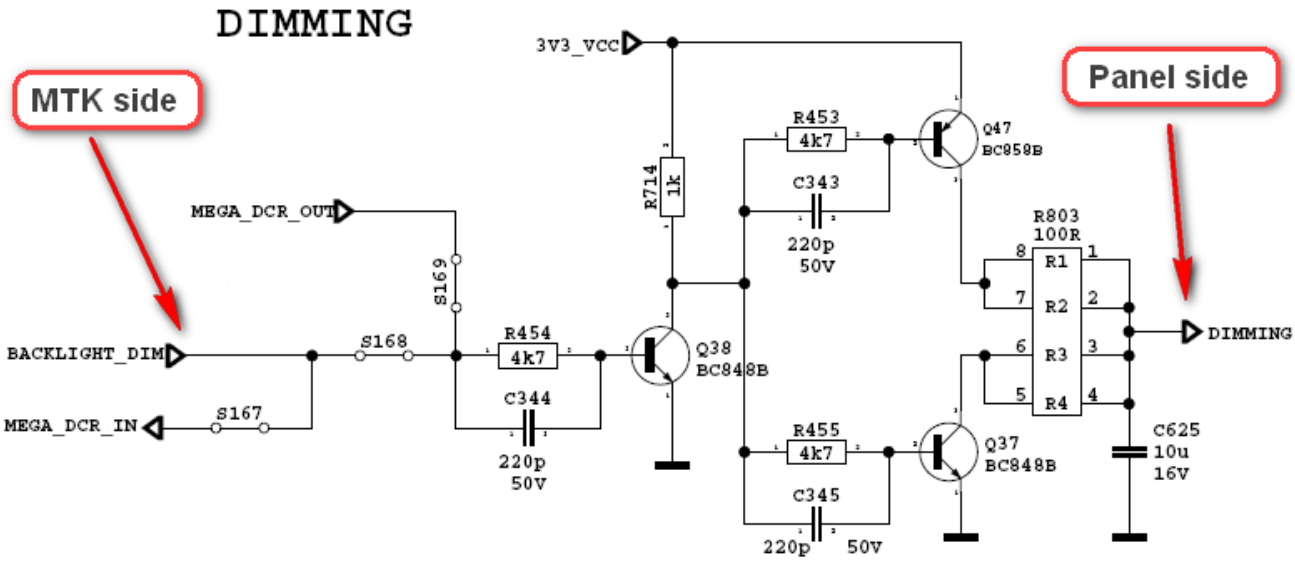
Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible couses: Backlight pin, dimming pin, backlight supply, stby on/off pin

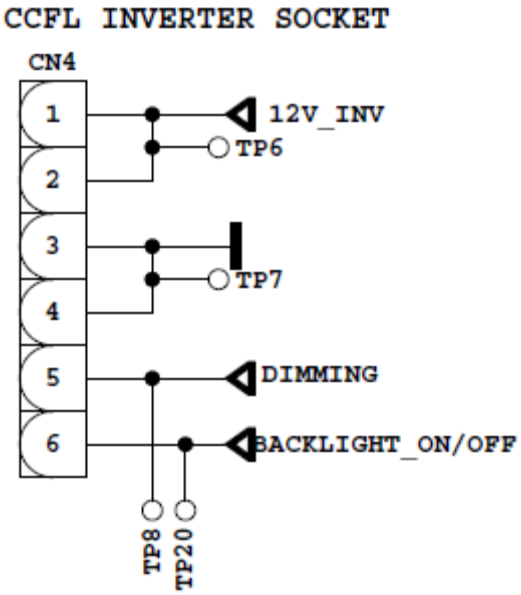
Backlight pin should be high in open position. If it is low, please check Q30 and panel cables.



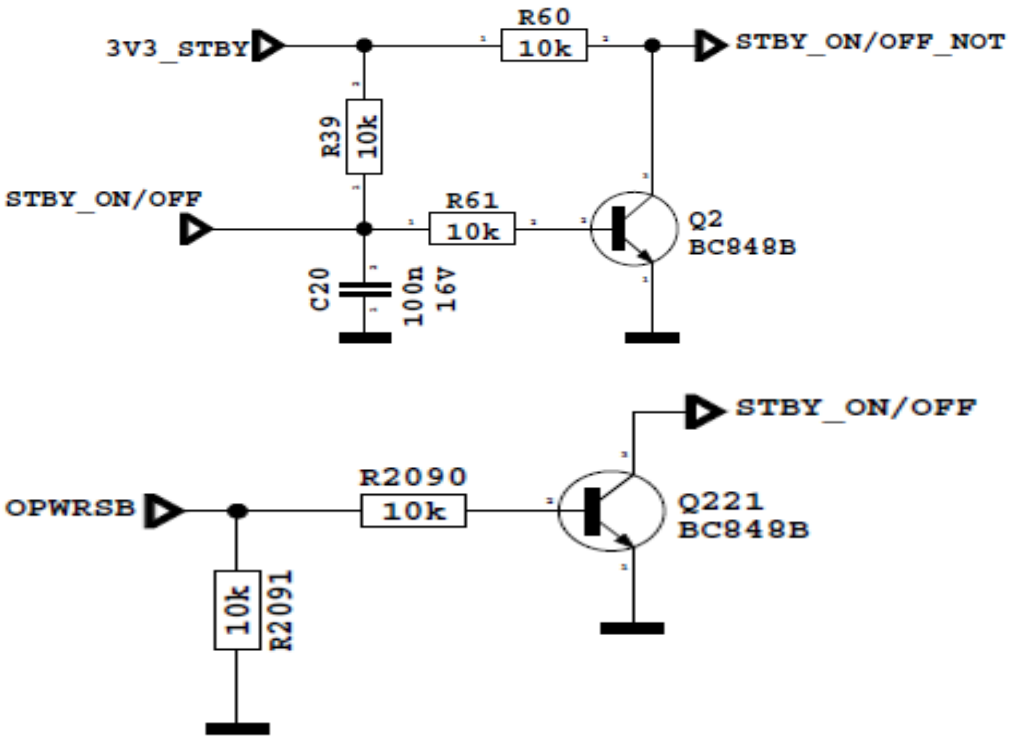
Dimming pin should be high or square wave in open position. If it is low, please check S16 for Mstar side and panel or power cables, connectors.



Backlight power supply should be in panel specs. Please check CN4 for MB82, related connectors for power supply cards.



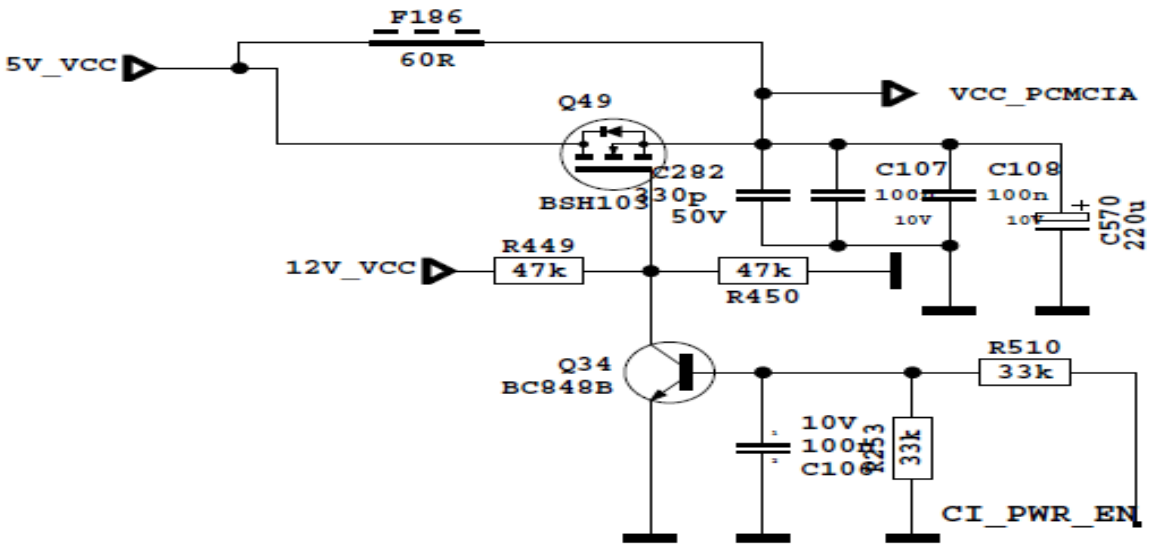
STBY_ON/OFF should be low for standby on condition, please check R2090.



13.2 CI Module Problem

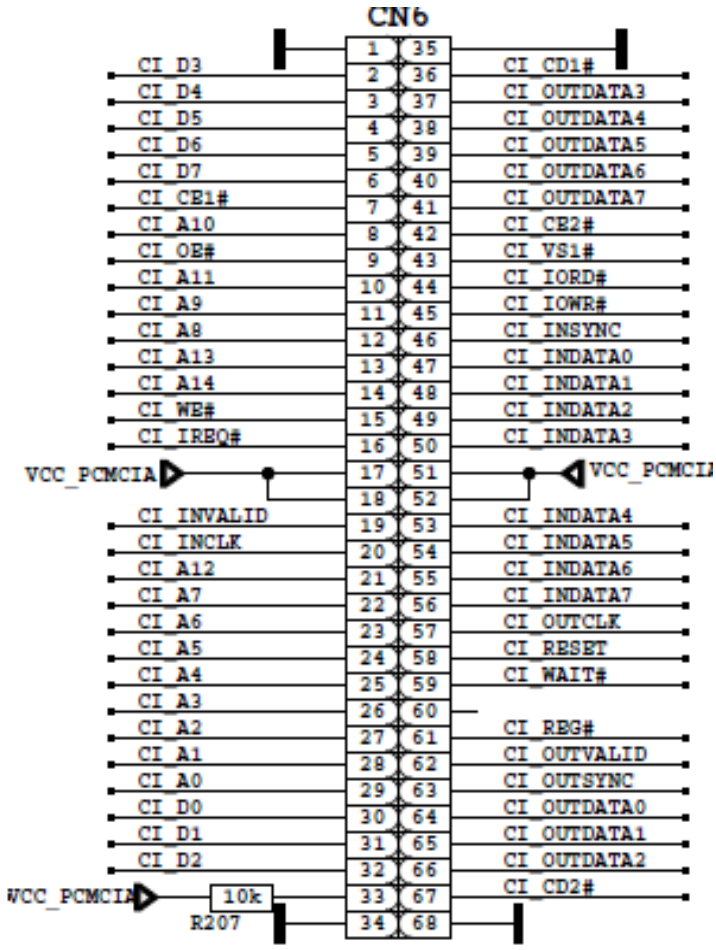
Problem: CI is not working when CI module inserted.

Possible couses: Supply, suply control pin, detect pins, mechanical positions of pins
CI supply shoul be 5V when CI module inserted. If it is not 5V please check CI_POWER_CTRL, this pin should be low.



Please check mechanical positions of CI module.

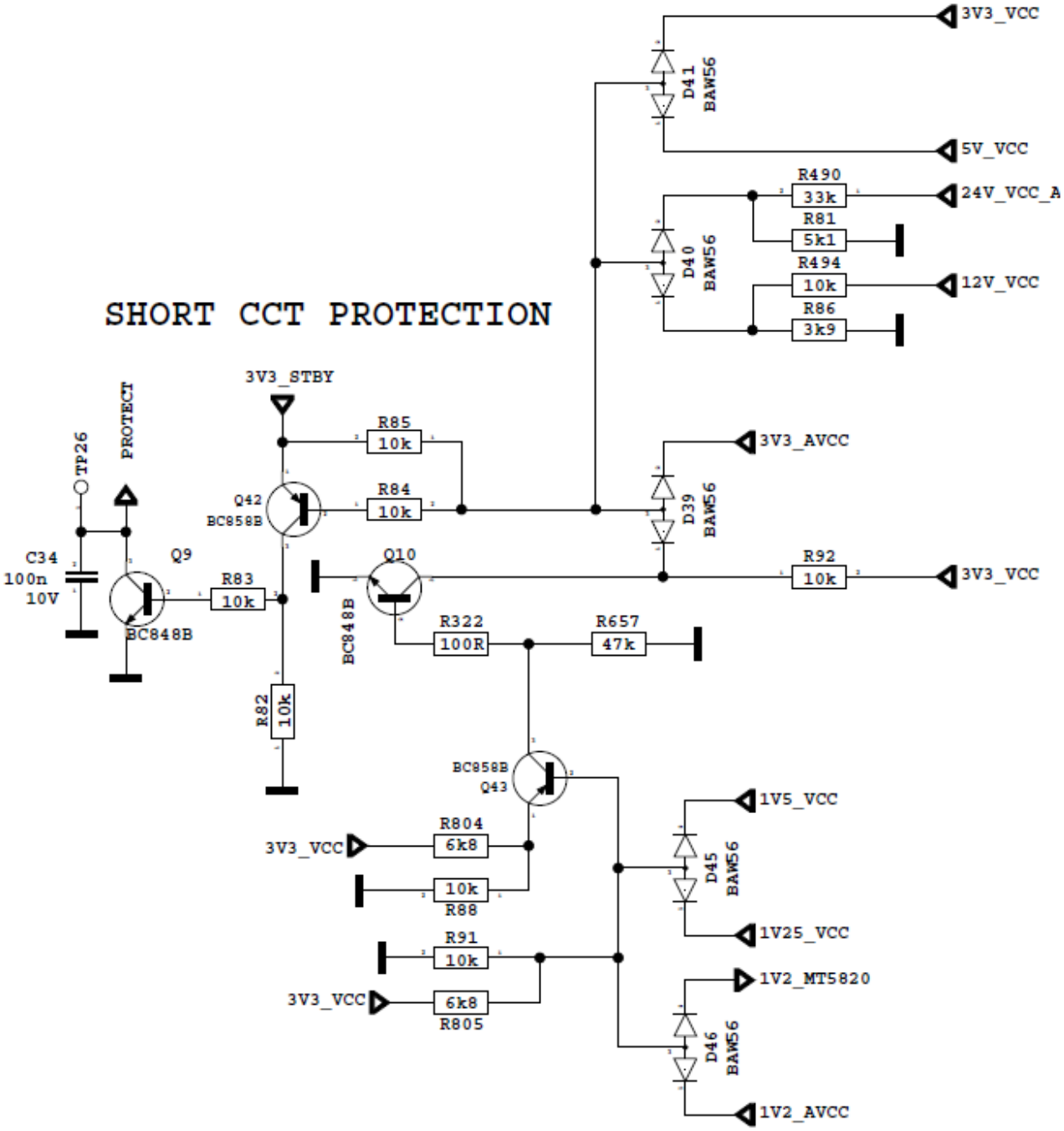
Detect ports should be low. If it is not low please check CI connector pins, CI module pins and 3V3_VCC on MB82.



13.3 Led Blinking Problem

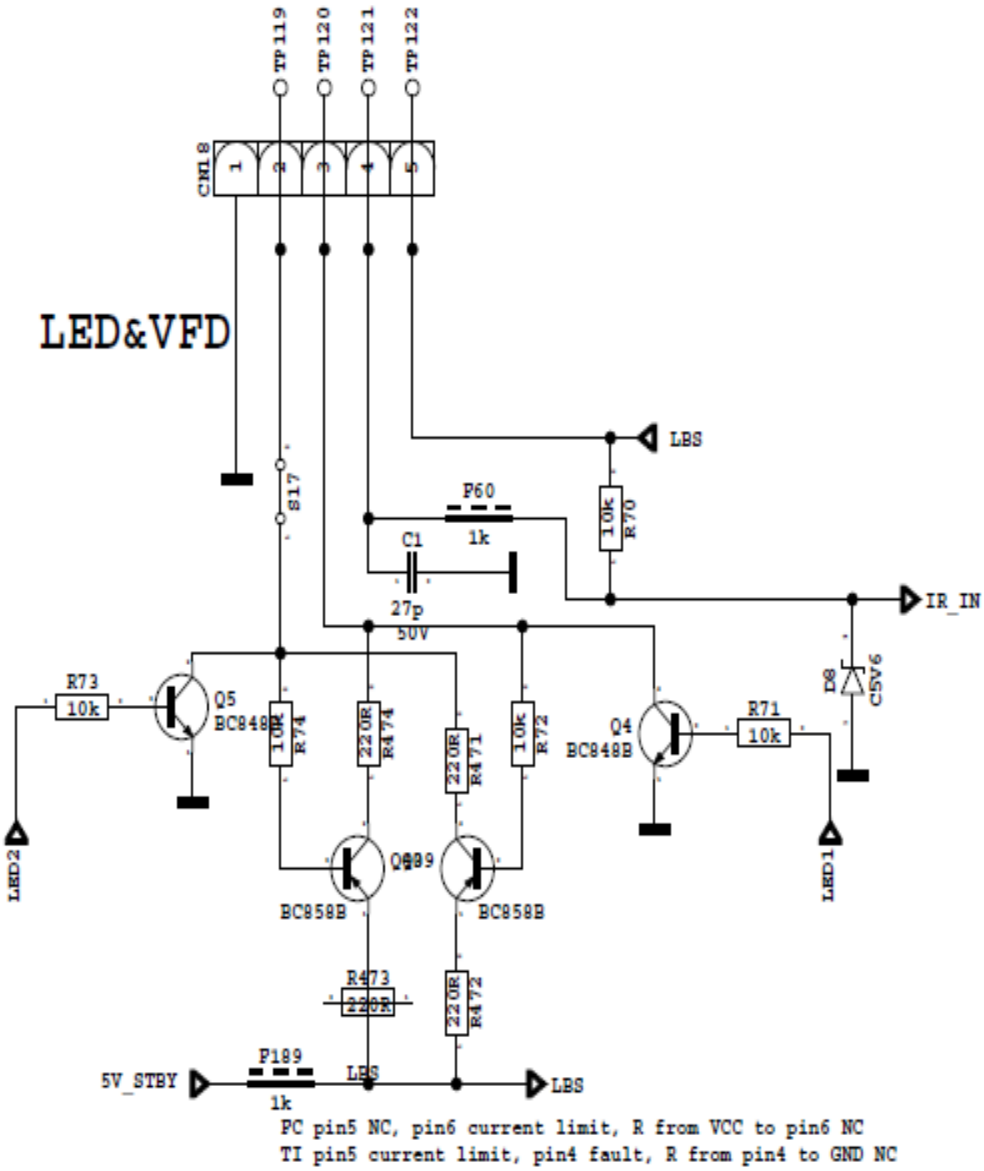
Problem: LED blinking, no other operation

This problem indicates a short on Vcc voltages. Protect pin should be logic high while normal operation. When there is a short circuit protect pin will be logic low. If you detect logic low on protect pin, unplug the TV set and control voltage points with a multimeter to find the shorted voltage to ground.



13.4 IR Problem

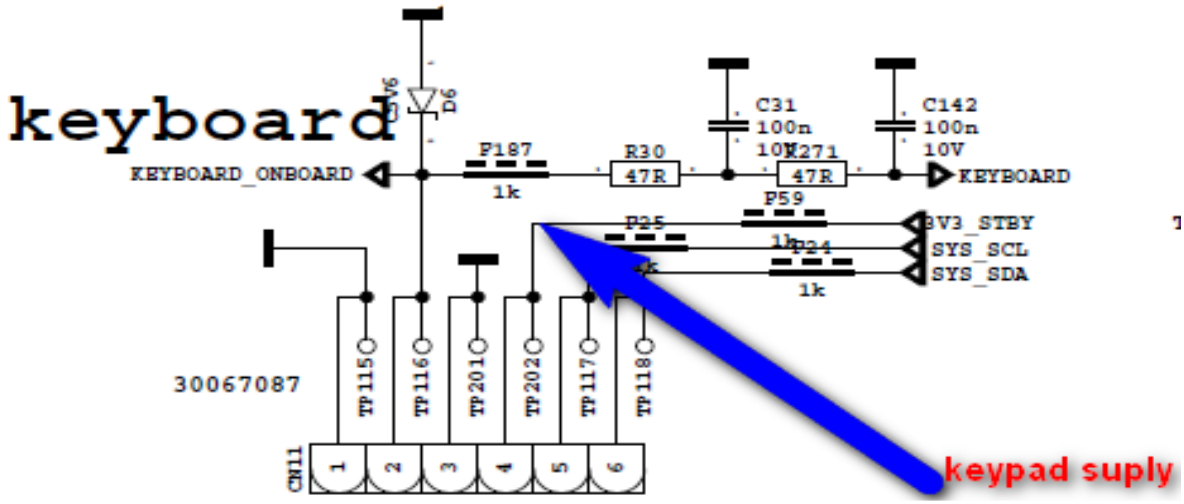
Problem: LED or IR not working
Check LED card supply on MB82 chasis.



13.5 Keypad Touchpad Problems

Problem: Keypad or Touchpad is not working

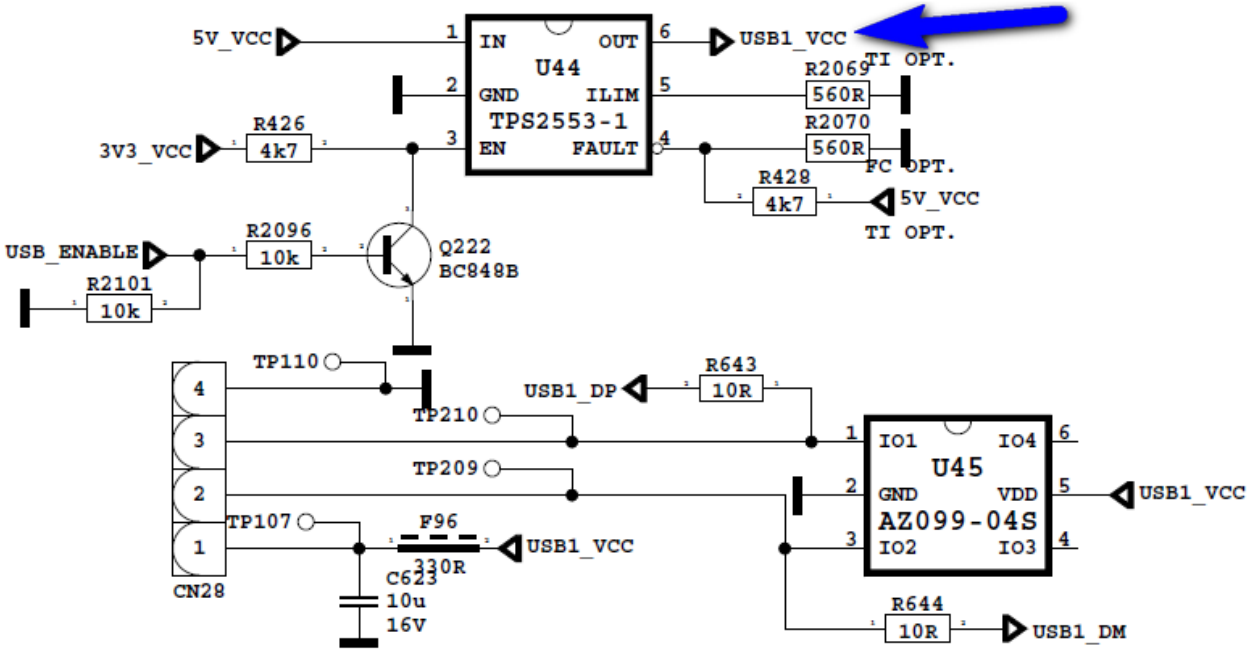
Check keypad supply and KEYBOARD pin on MB82



13.6 USB Problems

Problem: USB is not working or no USB Detection.

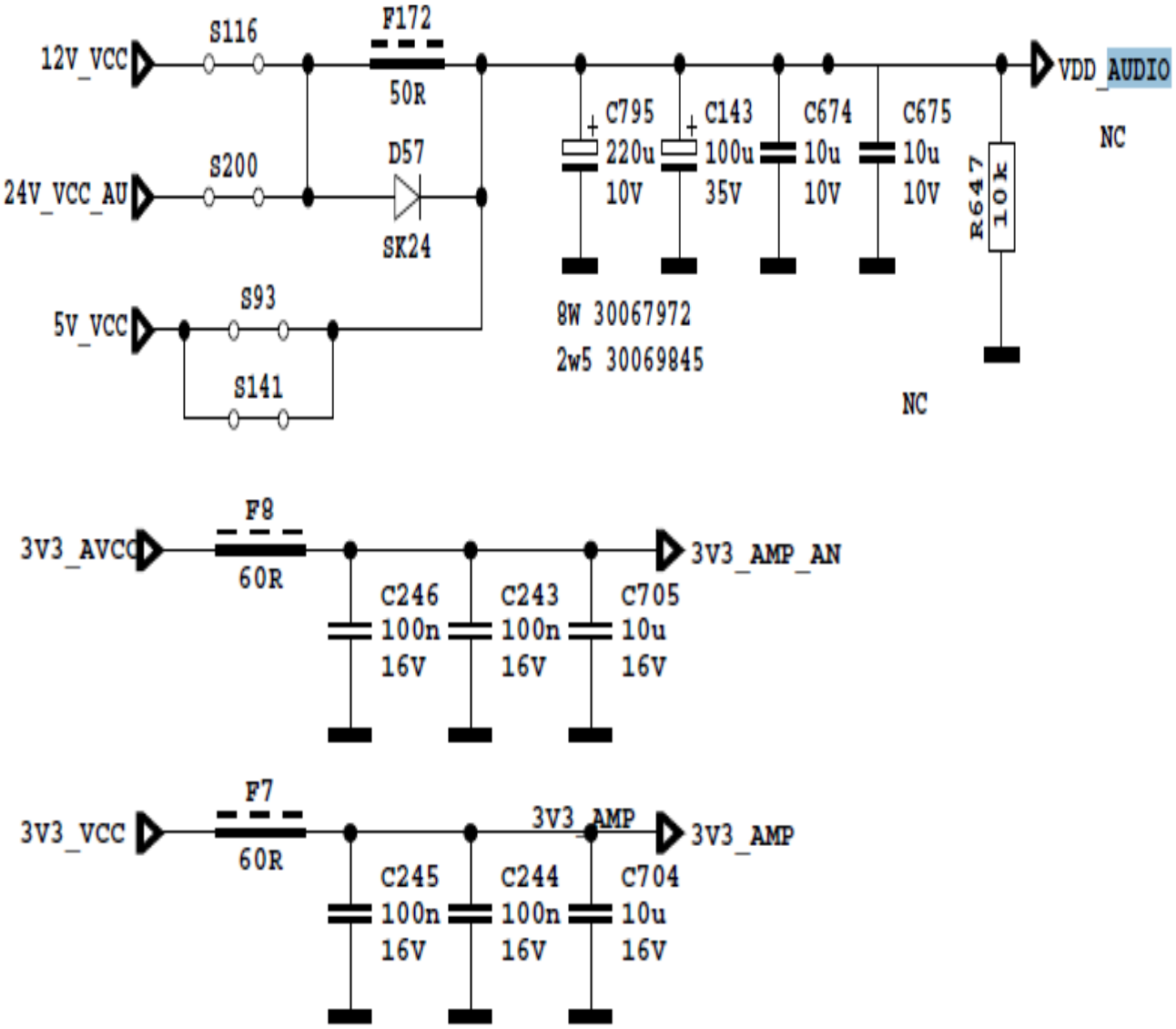
Check USB Supply, It should be nearly 5V.



13.7 No Sound Problem

Problem: No audio at main TV speaker outputs.

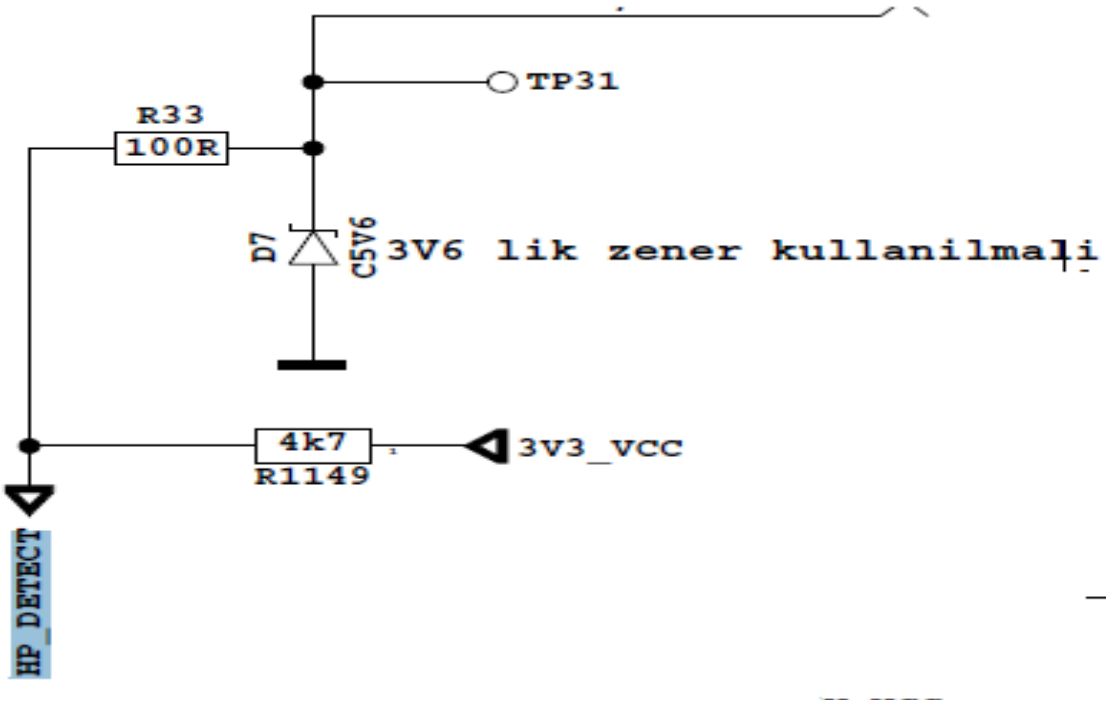
Check supply voltages of VDD_AUDIO, 5V_VCC or 12V_VCC with a voltage-meter.
There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.



13.8 No Sound Problem at Headphone

Problem: No audio at headphone output.

Check HP detect pin, when headphone is. Check 5V_VCC and 3V3_VCC with a voltage-meter.



13.9 Standby On/Off Problem

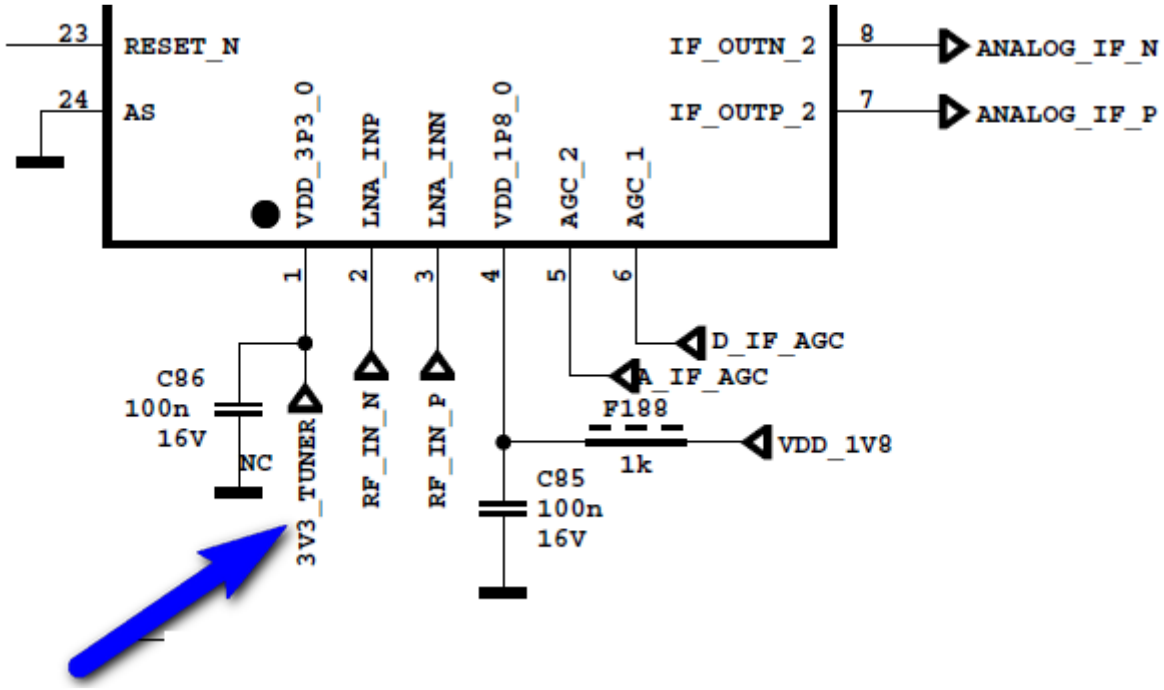
Problem:
Device cannot boot, TV hangs in standby mode.

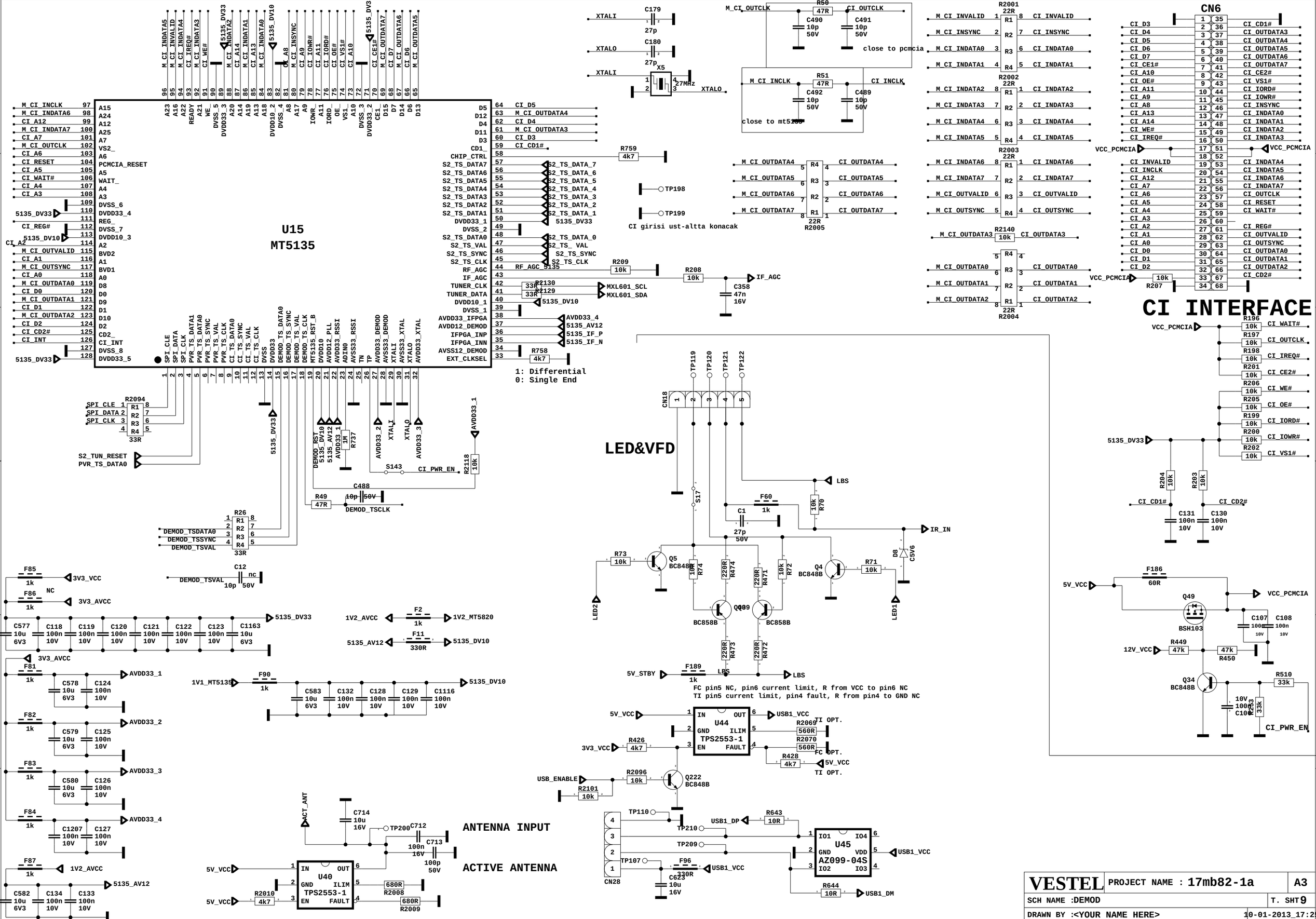
There may be a problem about power supply. Check 12V_VCC, 5V_VCC and 3V3_VCC with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is goood to check SW printouts via hyper-terminal (or Teraterm). These printouts may give a clue about the problem.

13.10 No Signal Problem

Problem: No signal in TV mode.

Check tuner supply voltage; 3V3_TUN. Check tuner options are correctly set in Service menu. Check AGC voltage at IF_AGC pin of tuner.





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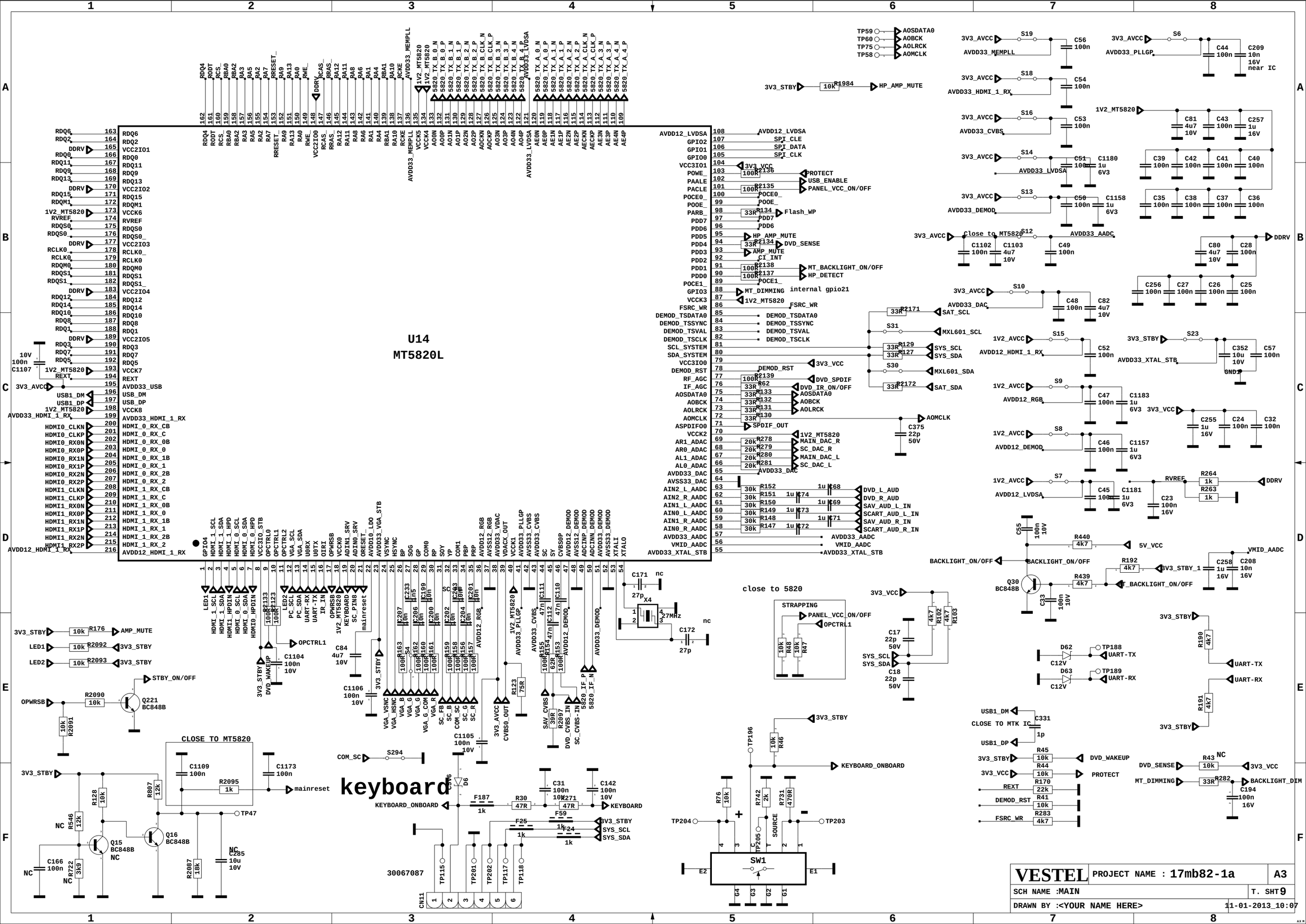
DRAWN BY :<YOUR NAME HERE>		10-01-2013_17:25	


U14
MT5820L
keyboard
close to 5820
STRAPPING
PANEL_VCC_ON/OFF
OPCTRL1
CLOSE TO MT5820
SW1
SOURCE
30067087
VESTEL
PROJECT NAME : 17mb82-1a
A3
SCH NAME :MAIN
T. SHT 9
DRAWN BY :<YOUR NAME HERE>
11-01-2013_10:07

BTB
CN5
power cable
CN30
PW03_PW04_PW07
PW06_IPS19
PW05_IPS60_IPS70_Adaptor
STP1
COMMON
1V2_MT5820
STP2
PW03_PW04_PW07
PW06_IPS19
PW05_IPS60_IPS70_Adaptor
5V_STBY
SW1
PW06_IPS19
PW05_IPS60_IPS70_Adaptor
COMMON
CCFL INVERTER SOCKET
3V3_AVCC
COMMON
5V_VCC
SW2
ADAPTER SOCKET
12V_STBY
1V2_AVCC
COMMON
1V5_AVCC
BOARD VOLTAGES
VESTEL
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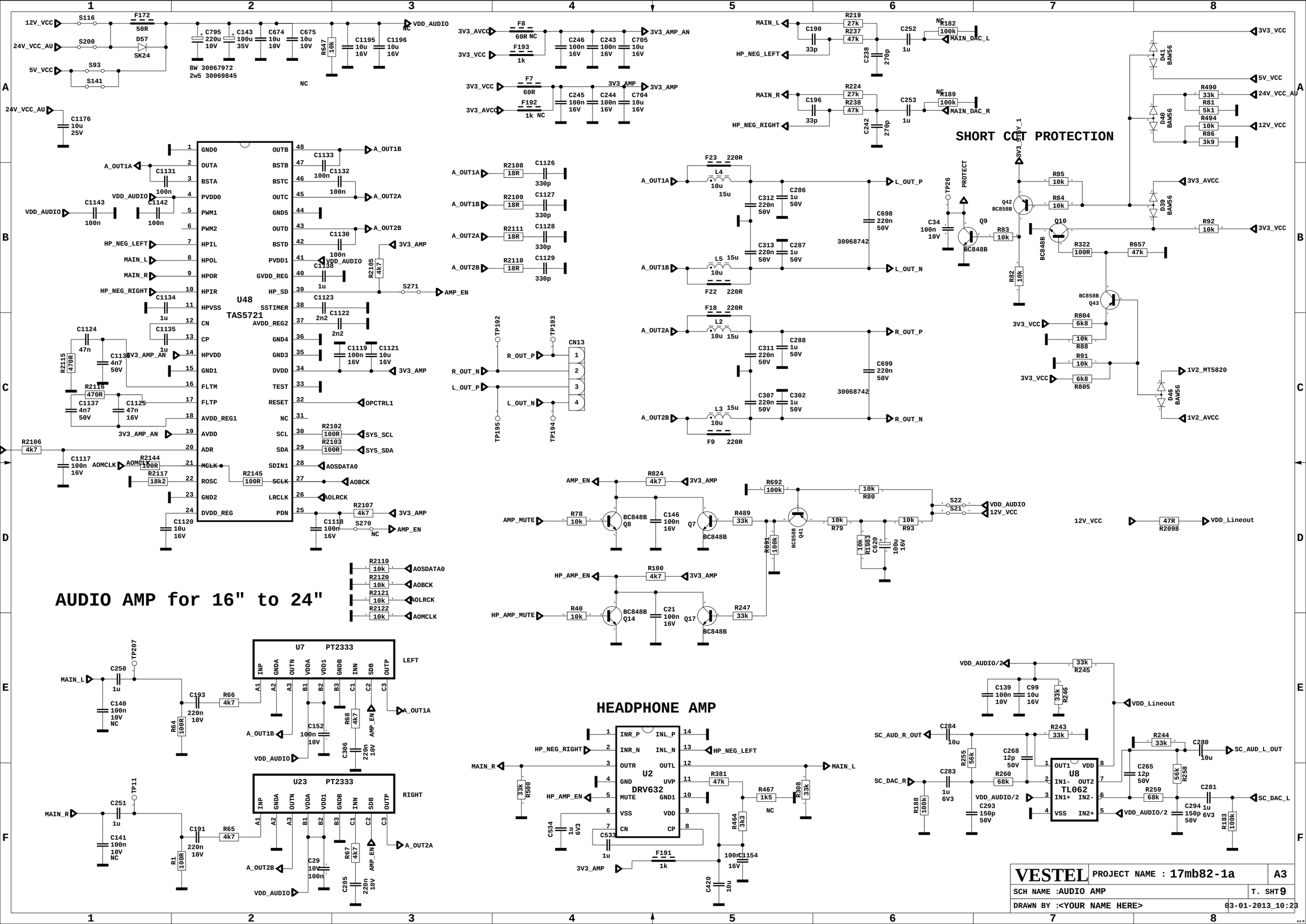
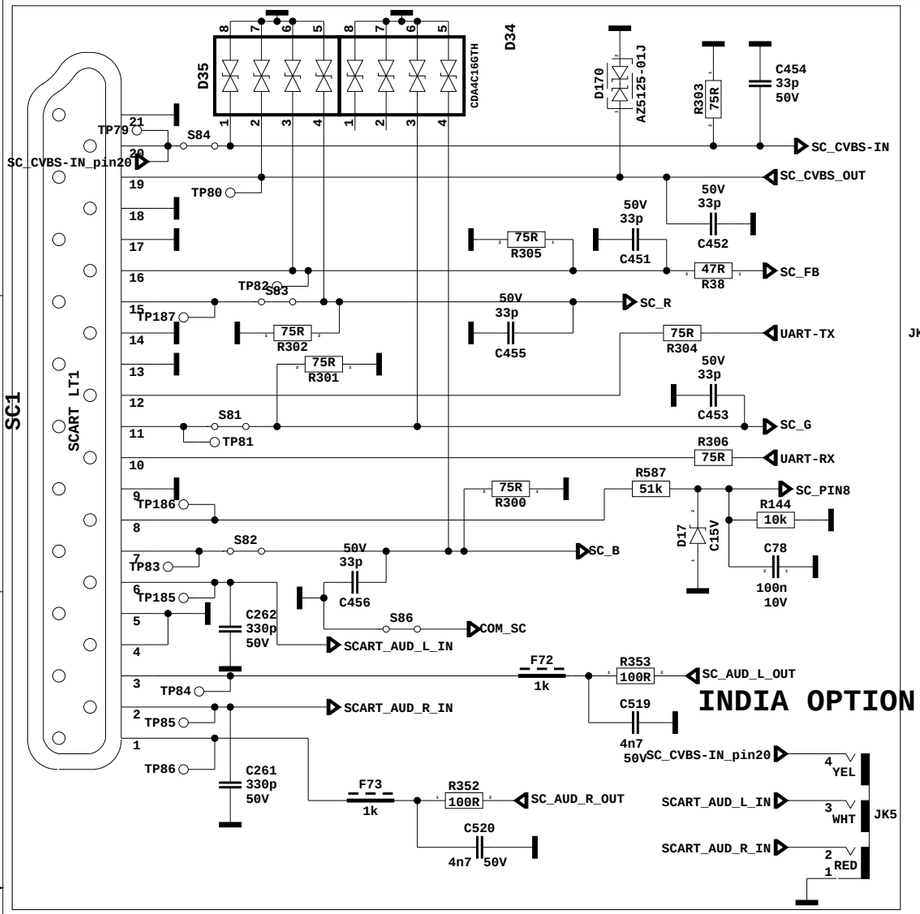
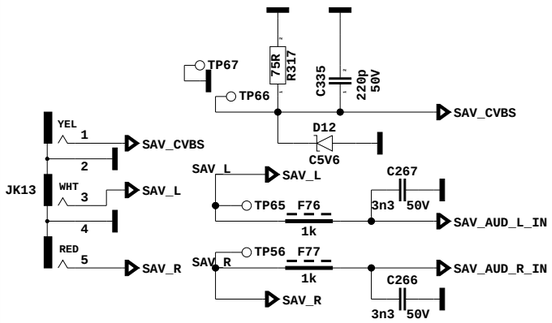
A3
SCH NAME :POWER
T. SHT 9
DRAWN BY :<YOUR NAME HERE>
15-01-2013_13:04


AUDIO AMP for 16" to 24"
SHORT CCT PROTECTION
HEADPHONE AMP
U48
TAS5721
U7 PT2333
U23 PT2333
LEFT
RIGHT
U2
DRV632
U8
TL062
PROJECT NAME : 17mb82-1a
A3
SCH NAME :AUDIO AMP
T. SHT 9
DRAWN BY :<YOUR NAME HERE>
03-01-2013_10:23

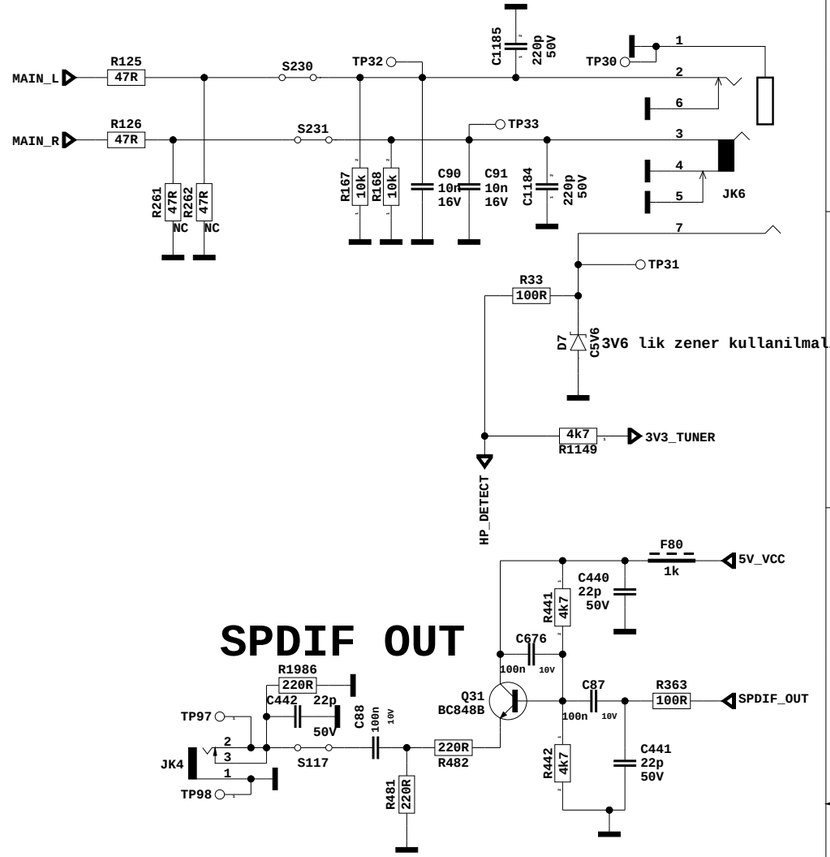


INDIA OPTION

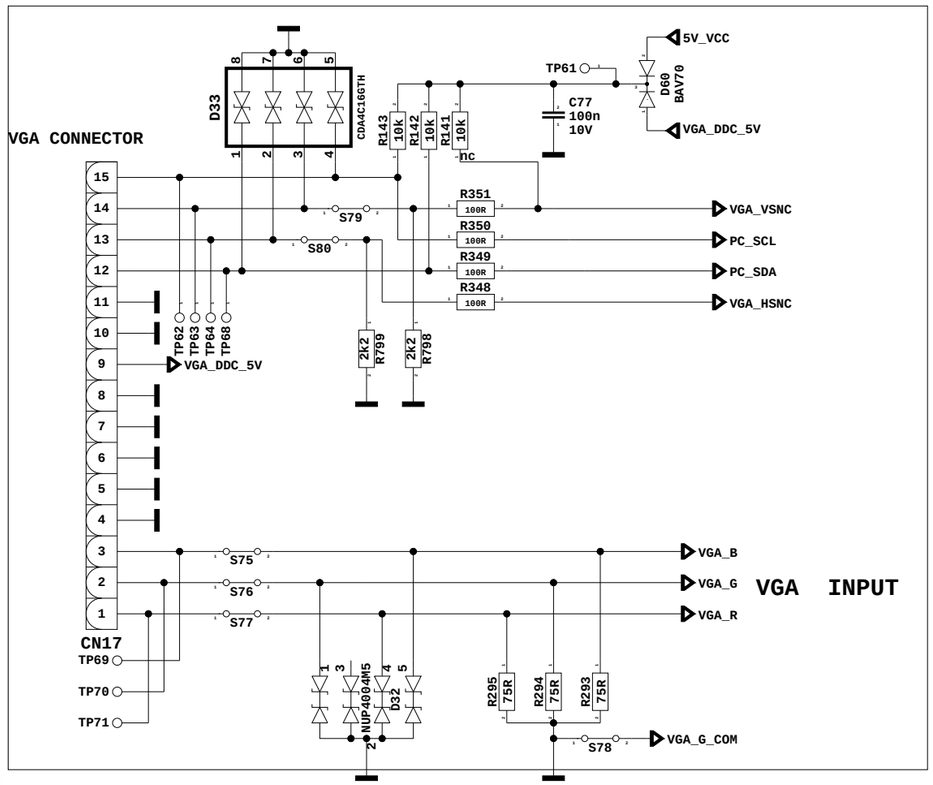
SAV Slim INPUT



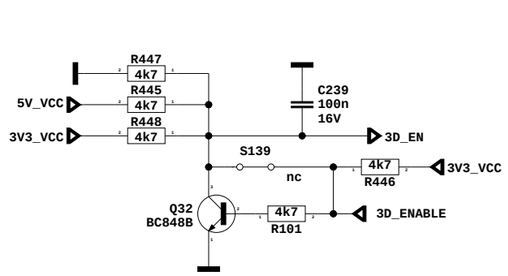
SLIM HEADPHONE OUTPUT



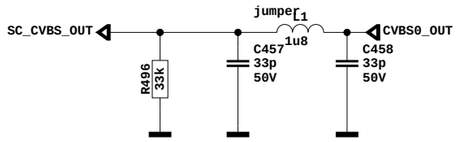
SPDIF OUT



VGA INPUT



30071260 kullanilacak



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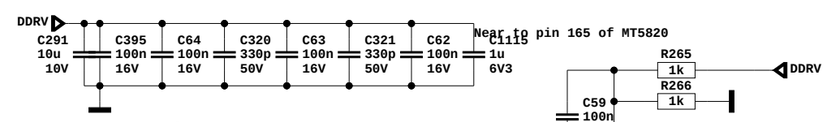
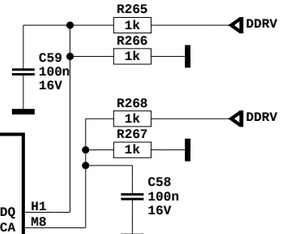
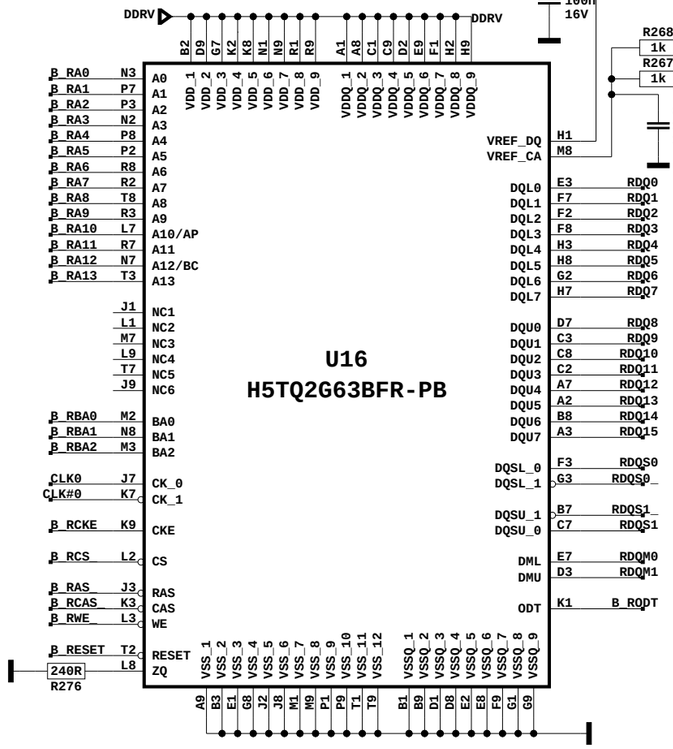
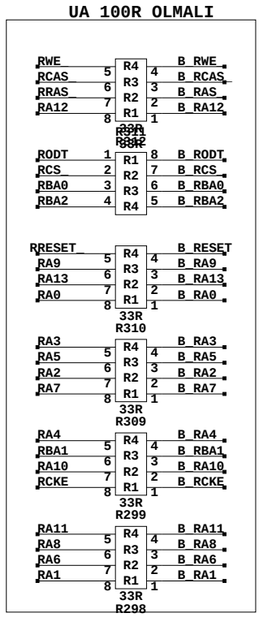
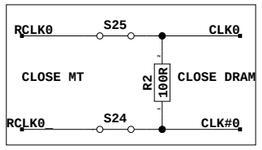
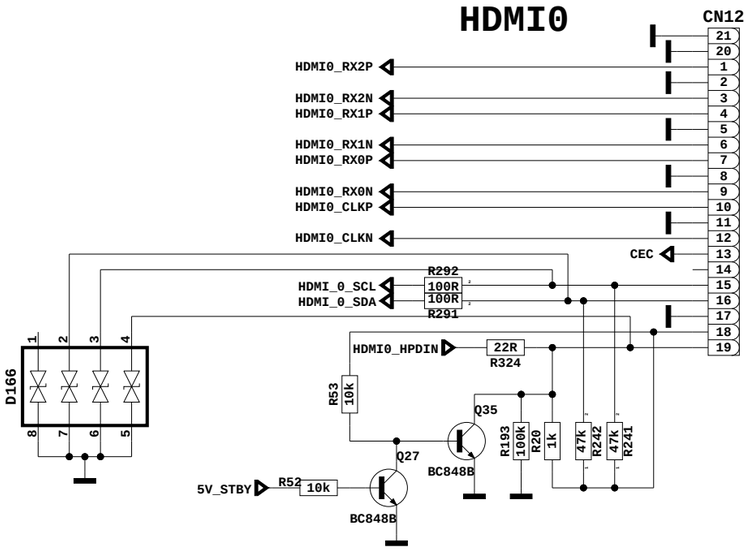


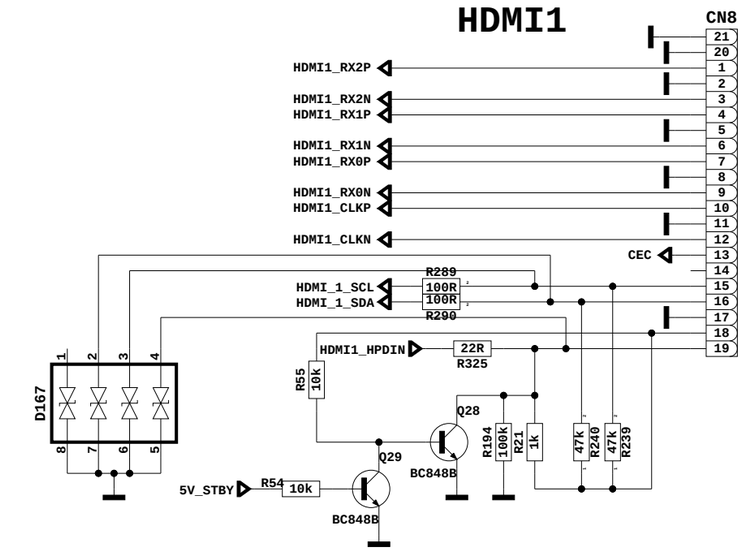


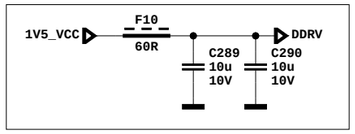


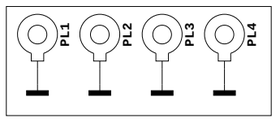


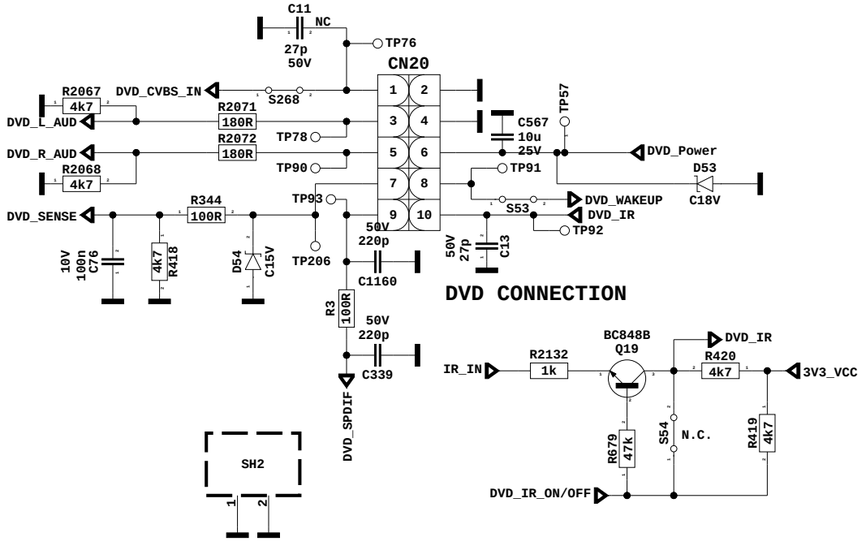


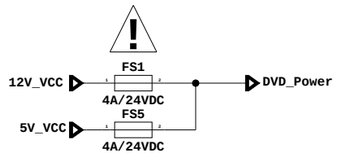


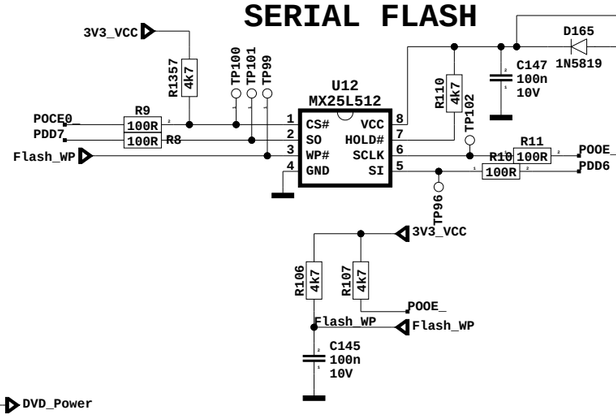


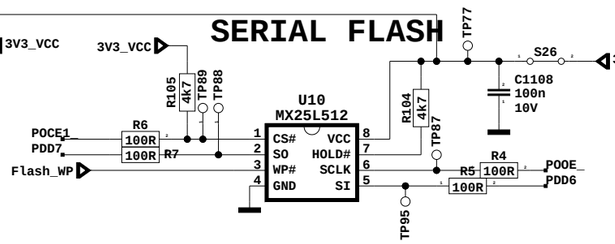






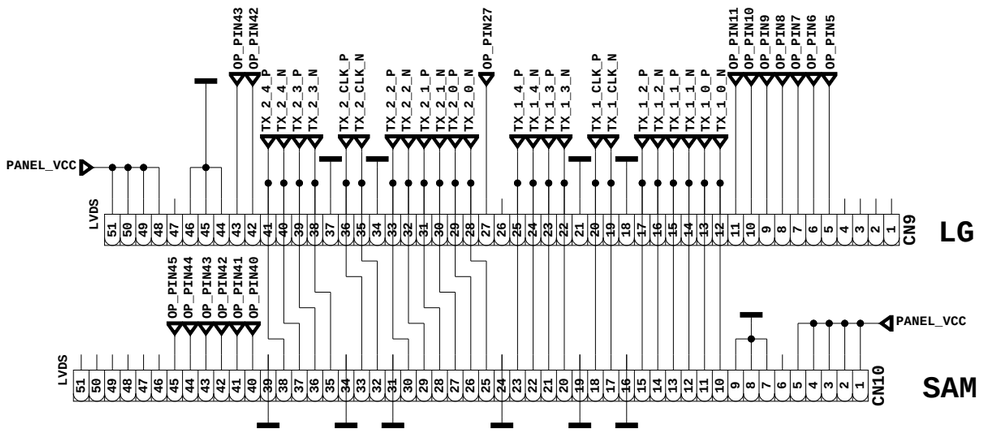






VESTEL	PROJECT NAME : 17mb82-1a	A3
SCH NAME :MEMORY/HDMI		T. SHT 9
DRAWN BY :<YOUR NAME HERE>		10-01-2013_17:24

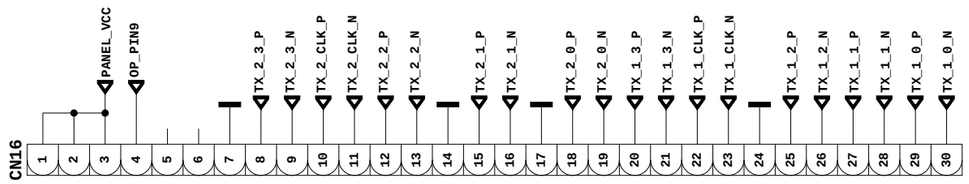
FHD 50Hz 3D FFC



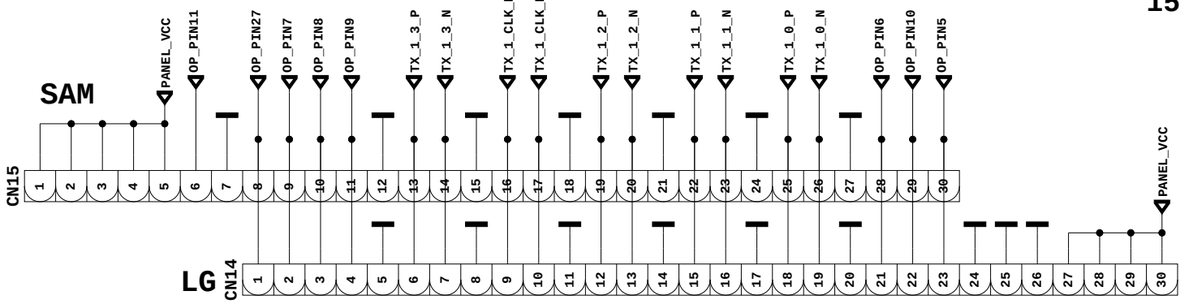
LG BASED 30070519

SAM BASED 30070519

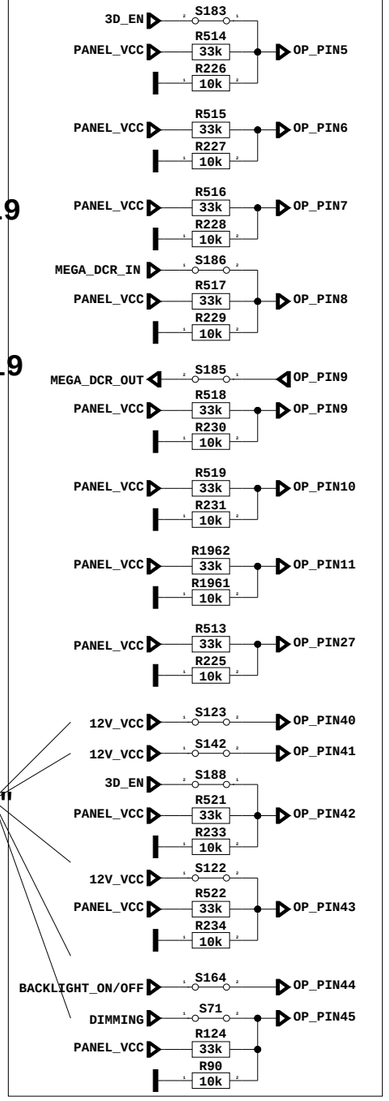
19" TO 22" DOUBLE LVDS FFC OPTIONS



WXGA FFC

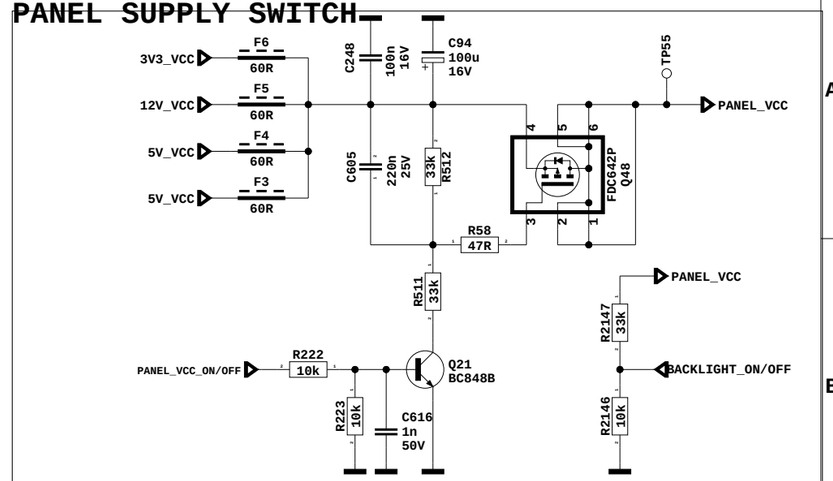


OPTIONS TABLE

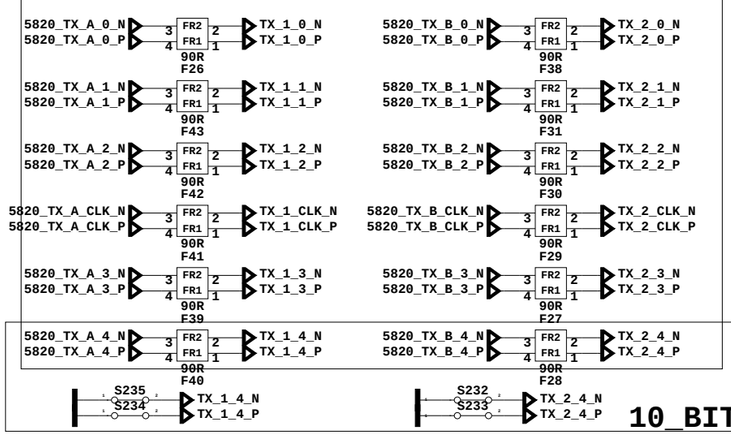


15.6"

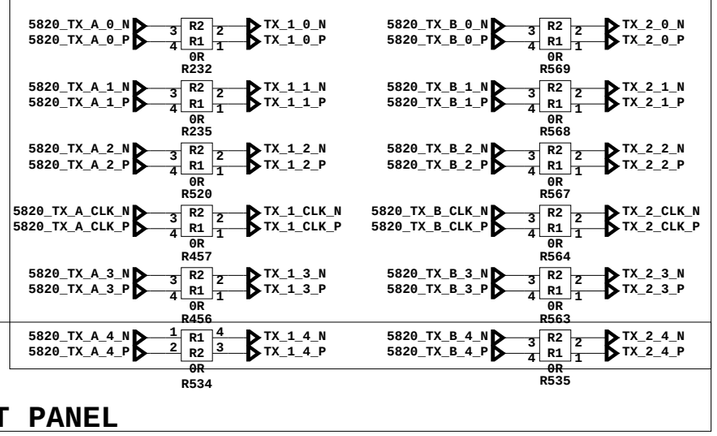
PANEL SUPPLY SWITCH



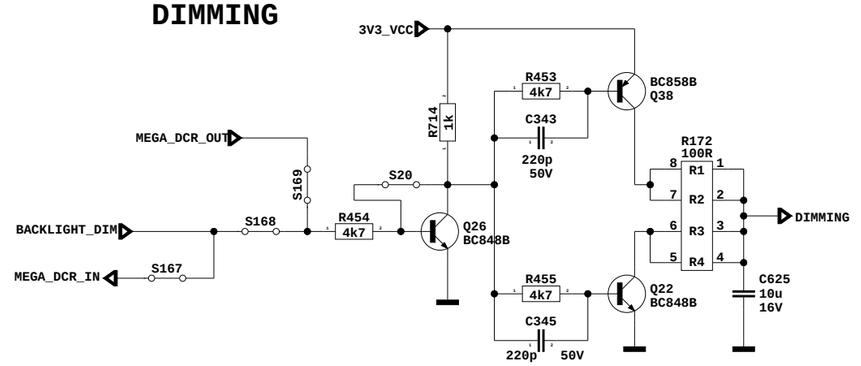
FERRITE



JUMPER



DIMMING



10_BIT PANEL

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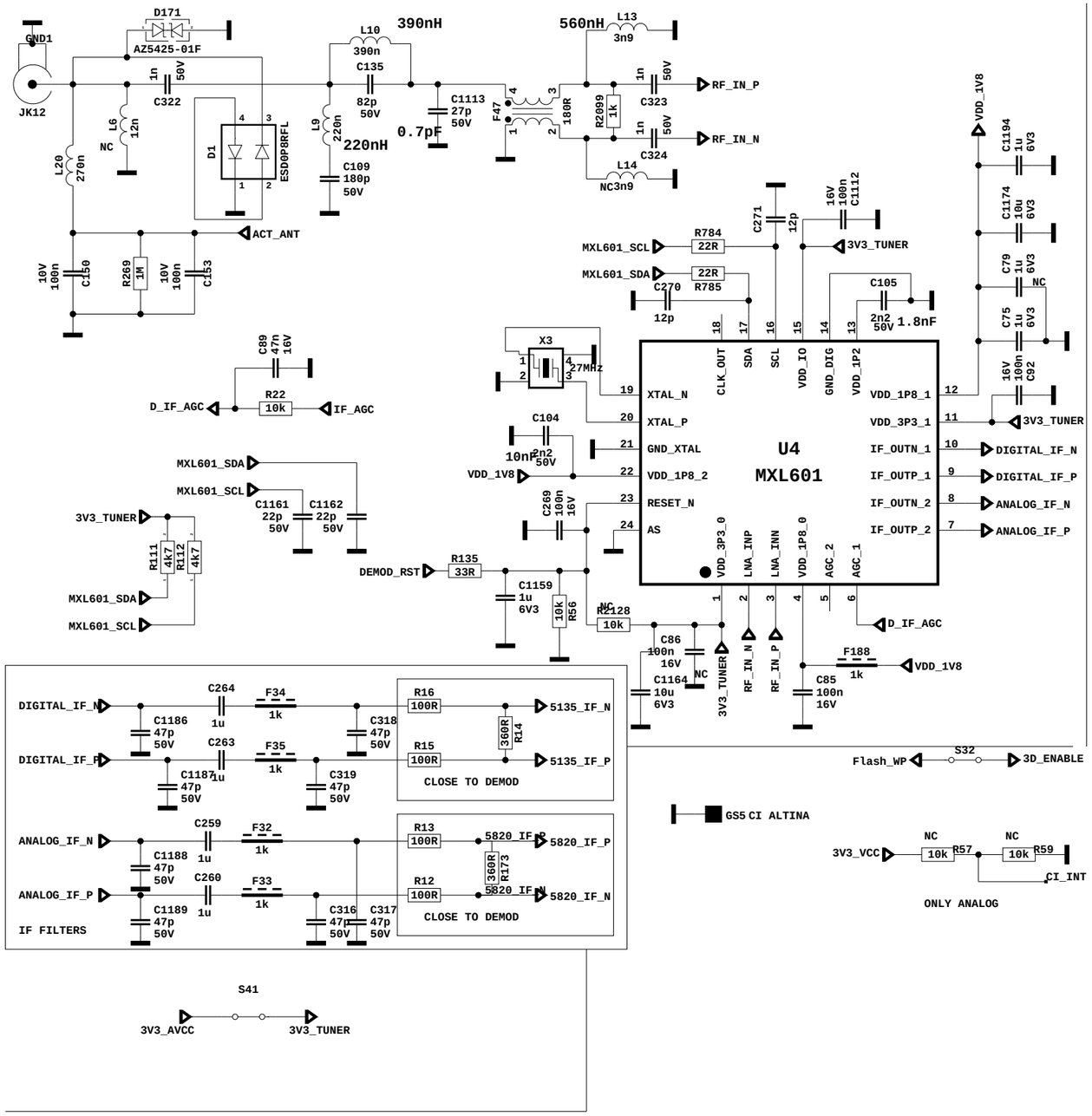
	DRAWN BY :<YOUR NAME HERE>	02-01-2013_15:04



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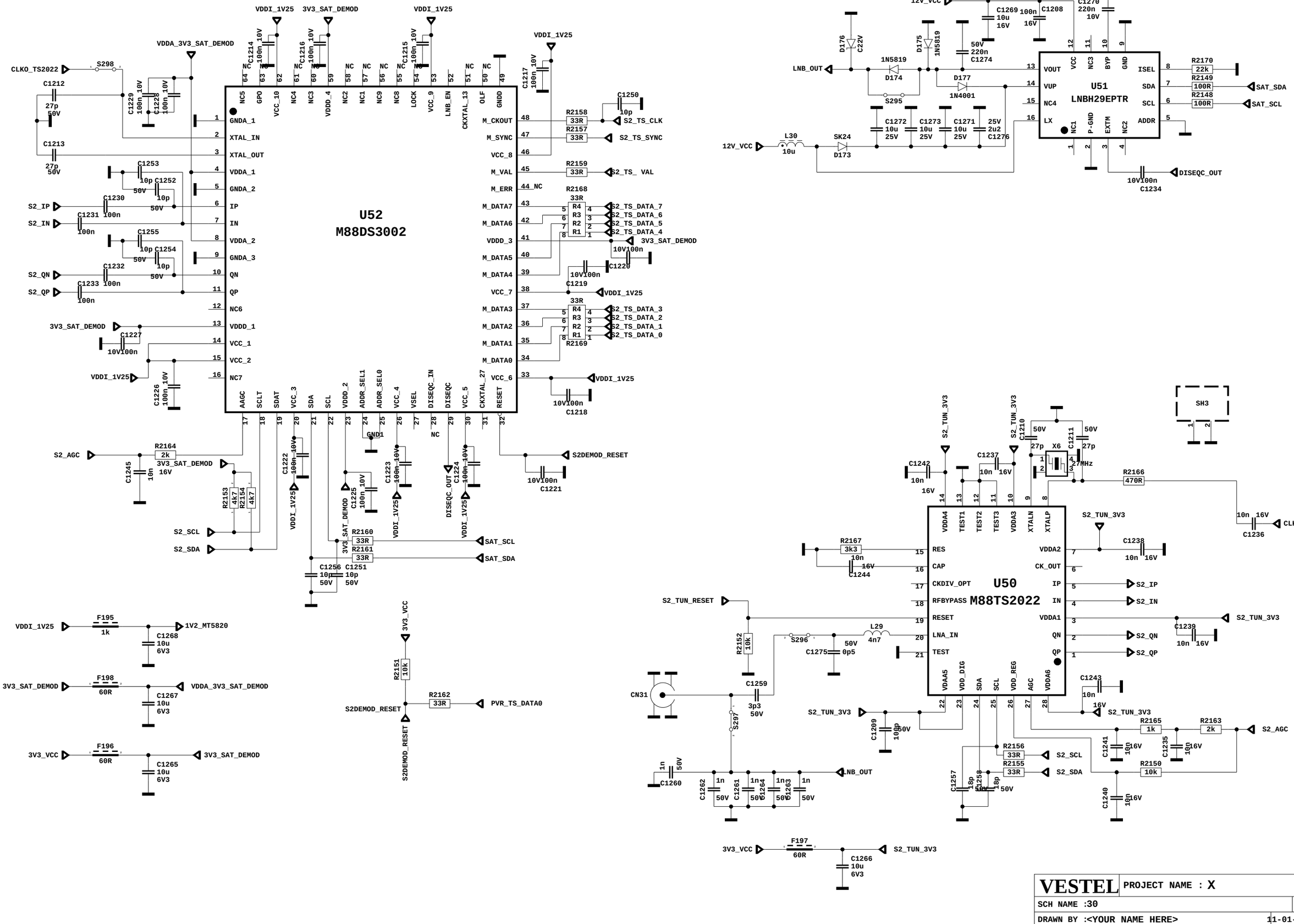
SCH NAME :TUNER		T. SHT 9
DRAWN BY :<YOUR NAME HERE>		02-01-2013_16:22


U52
M88DS3002
U51
LNBH29EPTR
U50
M88TS2022
CLKO_TS2022
VDDA_3V3_SAT_DEMOD
VDDI_1V25
3V3_SAT_DEMOD
S2_IP
S2_IN
S2_QN
S2_QP
S2_AGC
S2_SCL
S2_SDA
SAT_SCL
SAT_SDA
S2_TS_CLK
S2_TS_SYNC
S2_TS_ VAL
S2_TS_DATA_7
S2_TS_DATA_6
S2_TS_DATA_5
S2_TS_DATA_4
S2_TS_DATA_3
S2_TS_DATA_2
S2_TS_DATA_1
S2_TS_DATA_0
S2DEMOD_RESET
12V_VCC
LNB_OUT
DISEQC_OUT
SK24
L30
D173
D174
D175
D176
D177
S295
1N5819
1N4001
C22V
SH3
S2_TUN_3V3
S2_TUN_RESET
S296
S297
CN31
L29
4n7
0p5
3p3
NB_OUT
1V2_MT5820
VDDA_3V3_SAT_DEMOD
3V3_VCC
PVR_TS_DATA0
F195
F196
F197
F198
1k
60R
VESTEL
PROJECT NAME : X
A3
SCH NAME :30
T. SHT 10
DRAWN BY :<YOUR NAME HERE>
11-01-2013_11:12