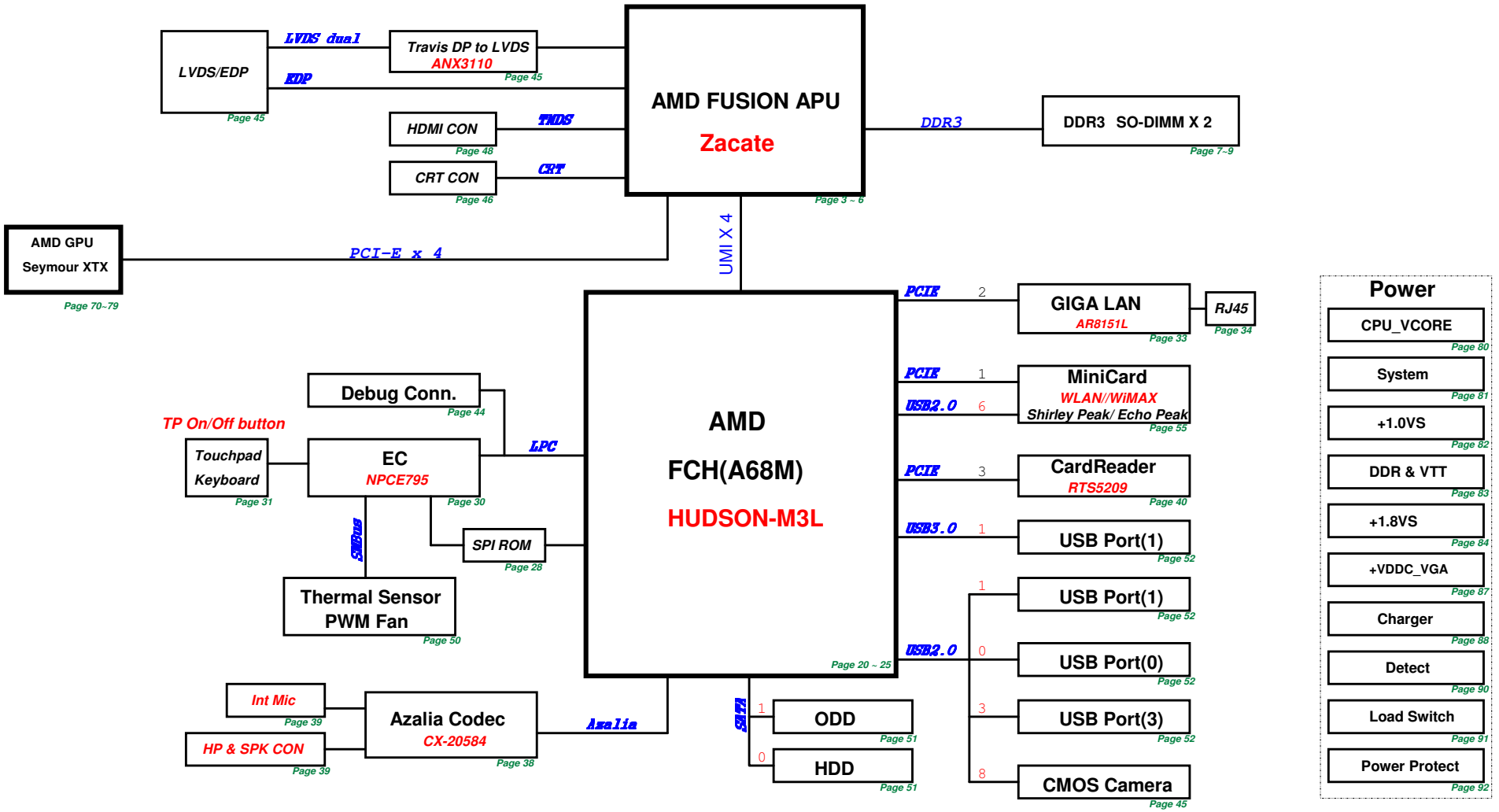
EG70 AMD Brazos-2 Platform Rev. 2.1

BLOCK DIAGRAM



Discharge Circuit (Page 57)	DC & BATT.Conn (Page 63)	LED/SCREW (Page 56)	TP_Button (Page 31,98)
Reset Circuit (Page 32)	Skew Holes (Page 56)	Power Button (Page 66,97)	I/O Board (Page 52,99)

PEGATRON	Title : BLOCK DIAGRAM			
	Engineer: Eric_Chung			
Size: Custom	Project Name: EG70			Rev: 1.1
Date: Monday, April 23, 2012	Sheet 1 of 99			

FCH Hudson M1	Use As	Signal Name	INT/EXT Pull-up/down	Power
General Events				
GA20IN/GEVENT0#	GPI	A20GATE	INT PU 8.2K	+3VS
KBRST#/GEVENT1#	GPI	EC_KB_RST#	INT PU 8.2K	+3VS
THRMTRIP#/GEVENT2#	GPI	CPU_THERMTRIP#	INT PU 10K	+3VSUS
LPC_PME#/GEVENT3#	GPI	EXT_SCI# @		+3VSUS
PCI_PME#/GEVENT4#	GPI	EXT_SMI# @		+3VSUS
SPI_CS3#/GBE_STAT1/GEVENT21#	GPI	EXT_SCI#	INT PU 10K	+3VSUS
RI#/GEVENT22#	GPI	EXT_SMI#	INT PU 10K	+3VSUS
GEVENT5#	GPI	USB30_EXT_SMI#	INT PU 10K	+3VSUS
WAKE#/GEVENT8#	GPI	PCIE_WAKE#	INT PU 10K	+3VSUS
USB_OC3#/AC_PRES/TDO/GEVENT15#		SATA_ODD_PRSNT#	INT PU 10K	+3VSUS
USB_OC4#/IR_RX0/GEVENT16#		SATA_ODD_DA#	INT PU 10K	+3VSUS
SLP_S3#	GPO	PM_SUSB#	EXT PD 100K	+3VSUS
SLP_S5#	GPO	PM_SUSC#	EXT PD 100K	+3VSUS
PWR_BTN#	GPI	PM_PWRBTN#		+3VSUS
PWR_GOOD	GPI	PM_PWROK		+3VSUS
RSMRST#	GPI	PM_RSMRST#	EXT PD 10K	+3VSUS
NB_PWRGD		NB_PWRGD	EXT PU 4.7K	+3VSUS
GPIO				
INTH#/GPIO35		VGA_PWRON	EXT PU 8.2K	+3VS
SCL0/GPIO43		SMB_CLK_S	EXT PU 2.2K	+3VS
SDA0/GPIO47		SMB_DAT_S	EXT PU 2.2K	+3VS
SERIRQ/GPIO48		INT_SERIRQ	INT PU 8.2K	+3VS
FANOUT0/GPIO53	GPO	WLAN_ON	INT PU 8.2K	+3VS
SATA_IS4#/FANOUT3/GPIO55	Native	SATA_ODD_PWRGT	INT PU 8.2K	+3VS
CLK_REQ1#/FANOUT4/GPIO61	Native	CLKREQ_MINICARD_WLAN#	EXT PD 10K @	+3VS
CLK_REQ2#/FANIN4/GPIO62	Native	CLKREQ2_LAN#	EXT PD 10K @	+3VS
CLKREQ3#/SATA_IS1#/GPIO63	Native	CLKREQ_PCIE_USB30#	EXT PU 10K EXT PD 10K @	+3VS
CLK_REQ4#/SATA_ISO#/GPIO64	Native	CLK_REQ4#_DP	EXT PD 10K	+3VS
CLK_REQG#/GPIO65/OSCIN/IDLEEXT#	Native	ATI_CLKREQ#	INT PU 8.2K	+3VS
SPKR/GPIO66		SB_SPKR	-	+3VS
SATA_ACT#/GPIO67		SATA_LED#	EXT PU 10K	+3VS
SPI_CLK/GPIO162		SPI_CLK	INT PD 10K	+3VSUS
SPI_DO/GPIO163		SPI_DO	INT PD 10K	+3VSUS
SPI_DI/GPIO164		SPI_DI	INT PD 10K	+3VSUS
SPI_CS1#/GPIO165		SPI_CS1#	INT PD 10K	+3VSUS
AZ_SDIN0/GPIO167		ACZ_SDIN0	EXT PD 10K @	+3VSUS
AZ_SDIN0/GPIO168		ACZ_SDIN1	EXT PD 10K @	
AZ_SDIN0/GPIO169		ACZ_SDIN2	EXT PD 10K @	
TEMPIN0/GPIO171			EXT PD 10K	+3VSUS
TEMPIN1/GPIO172			EXT PD 10K	+3VSUS
TEMPIN2/GPIO173			EXT PD 10K	+3VSUS
TEMPIN3/TELERT#/GPIO174		APU_ALERT#		+3VSUS
VIN0/GPIO175			EXT PD 10K	+3VSUS
VIN1/GPIO176			EXT PD 10K	+3VSUS
VIN2/GPIO177			EXT PD 10K	+3VSUS
VIN3/GPIO178			EXT PD 10K	+3VSUS
VIN4/GPIO179			EXT PD 10K	+3VSUS
VIN5/GPIO180			EXT PD 10K	+3VSUS
VIN6/GBE_STAT3/GPIO181			EXT PD 10K	+3VSUS
VIN7/GBE_LED3/GPIO182			EXT PD 10K	+3VSUS
USB_FSD0P/GPIO185		USB_CB0	INT PD 15K	+3VSUS
USB_FSD0P/GPIO186		USB_CB1	INT PD 15K	+3VSUS
PS2_DAT/SDA4/GPIO187		WLAN_LED	INT PU 10K	+3VSUS
SCL2/GPIO193			EXT PD 10K	
SDA2/GPIO194			EXT PD 10K	
SCL3_LV/GPIO195			EXT PD 10K	
SDA3_LV/GPIO196			EXT PD 10K	
EC_PWM2/EC_TIMER2/GPIO199		EC_PWM2	EXT PU 10K	
EC_PWM3/EC_TIMER3/GPIO200		EC_PWM3	EXT PD 2.2K @	
KSI_0/GPIO209		USB_SEL (DOS:1/WIN:0)	INT PU 10K	+3VSUS
KSO_1/GPIO210		BT_ON	INT PU 10K	+3VSUS
SCL1/GPIO227			EXT PD 10K	+3VSUS
SDA1/GPIO228			EXT PD 10K	+3VSUS

EC GPIO	Use As	Signal Name
GPIO0		RTCCLK
GPIO1		FAN0_TACH
GPIO2		-
GPIO3		PWR_SW#
GPIO4		BAT1_IN_OC#
GPIO5		AC_IN_OC
GPIO6		DC_IN_LED#
GPIO7		-
GPIO8		-
GPIO9		-
GPIO10		SUSB_EC#
GPIO11		PM_CLKRUN#
GPIO12		-
GPIO13		PM_PWROK
GPIO14		USB_OC2#_EC
GPIO15		PWR_GREEN_LED#
GPIO16		-
GPIO17		SMB0_CLK
GPIO18		-
GPIO19		-
GPIO20		USB_OC1#_EC
GPIO21		PWR_AMBER_LED#
GPIO22		SMB0_DAT
GPIO23		PLT_ID0
GPIO24		-
GPIO25		-
GPIO26		TP_CLK
GPIO27		TP_DAT
GPIO28		-
GPIO29		-
GPIO30		VSUS_ON
GPIO31		EC_LPCRST_GATE
GPIO32		LCD_BL_PWM
GPIO33		-
GPIO34		-
GPIO35		-
GPIO36		NUM_LED#
GPIO37		-
GPIO38		-
GPIO39		-
GPIO40		BAT_WHITE_LED#
GPIO41		TP_ON_OFF#
GPIO42		PM_PWRBTN#
GPIO43		PM_RSMRST#
GPIO44		ALL_SYSTEM_PWRGD
GPIO45		BAT_ORG_LED#
GPIO46		-
GPIO47		PM_SUSC#
GPIO48		-
GPIO49		-
GPIO50		LCD_BACKOFF#
GPIO51		CAP_LED#
GPIO52		THRO_CPU
GPIO53		SUS_PWRGD
GPIO54		EXT_SCI#
GPIO55		-
GPIO56		PLT_ID1
GPIO57		KSO17
GPIO58		-
GPIO59		-
GPIO60		KSO16
GPIO61		KSO15
GPIO62		KSO14
GPIO63		KSO13
GPIO64		KSO12
GPIO65		EXT_SMI#
GPIO66		FAN_PWM

EC GPIO	Use As	Signal Name
GPIO67		SUSC_EC#
GPIO68		-
GPIO69		-
GPIO70		OP_SD#
GPIO71		PM_SUSB#
GPIO72		LID_SW#
GPIO73		SMB1_CLK
GPIO74		SMB1_DAT
GPIO75		-
GPIO76		SHBM
GPIO77		-
GPIO78		-
GPIO79		-
GPIO80		-
GPIO81		CPU_VRON
GPIO82		USBSLP_EN#
GPIO83		-
GPIO84		USBP01_EN#
GPIO85		A20GATE
GPIO86		RCIN#
GPIO87		-
GPIO88		-
GPIO89		-
GPIO90		AD_IINP
GPIO91		-
GPIO92		-
GPIO93		-
GPIO94		-
GPIO95		-
GPIO96		CTL_FAN
GPIO97		VRM_PWRGD

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)
CPU Thermal IC(G780)	1001100x (98h)
VGA Thermal IC(G781-1)	1001100x (9Ah)

APU	DP0	LVDS
	DP1	HDMI
FCH	GPP0	N/A
	GPP1	WLAN
	GPP2	LAN
	GPP3	USB3.0_NEC
	GPP4	N/A
	GPP5	N/A

SATA0	SATA HDD
SATA1	SATA ODD
SATA2	N/A
SATA3	N/A
SATA4	N/A
SATA5	N/A

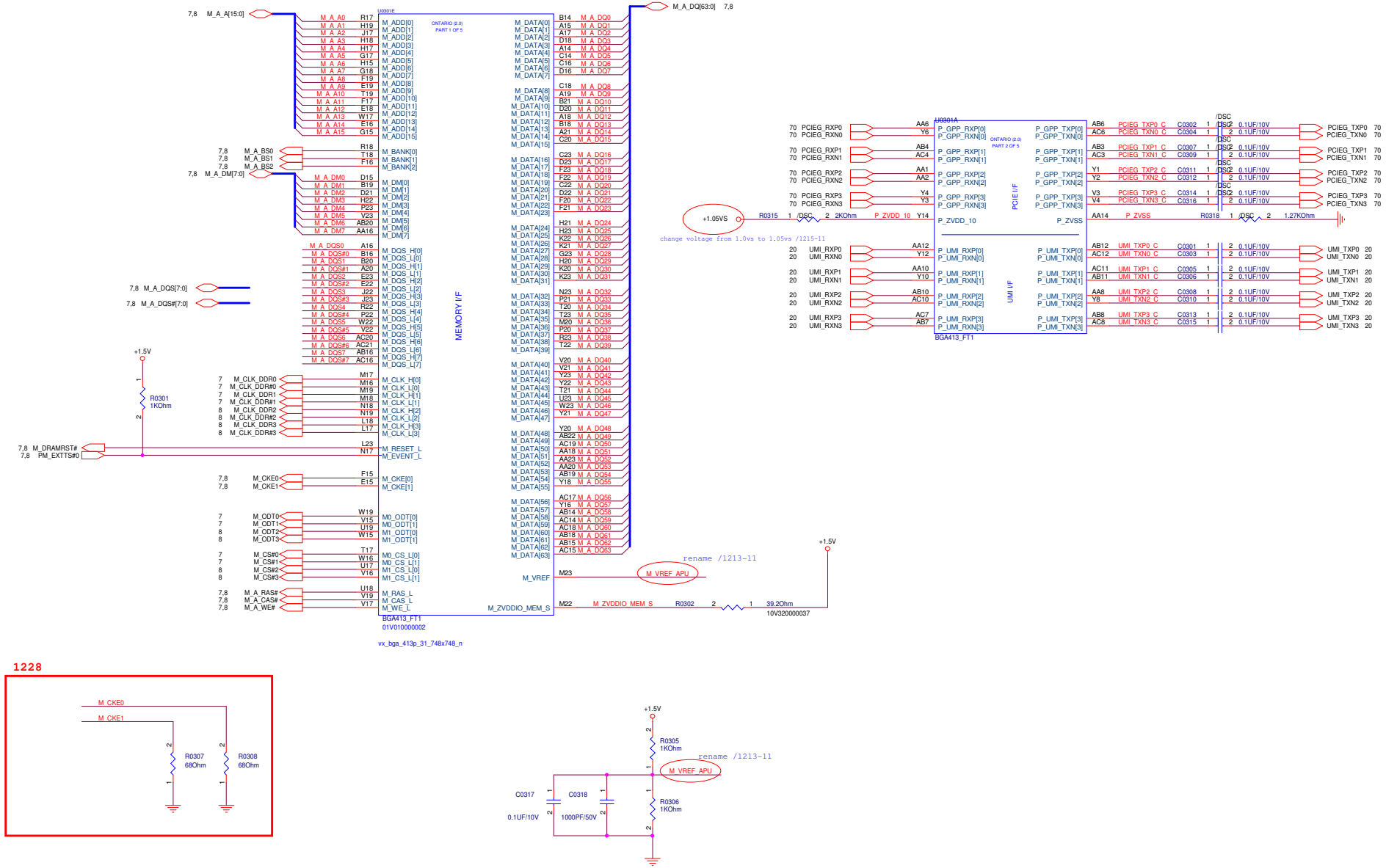
USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	N/A
USB 5	N/A
USB 6	N/A
USB 7	Card Reader
USB 8	CMOS Camera
USB 9	Bluetooth
USB 10	N/A
USB 11	N/A
USB 12	N/A
USB 13	N/A

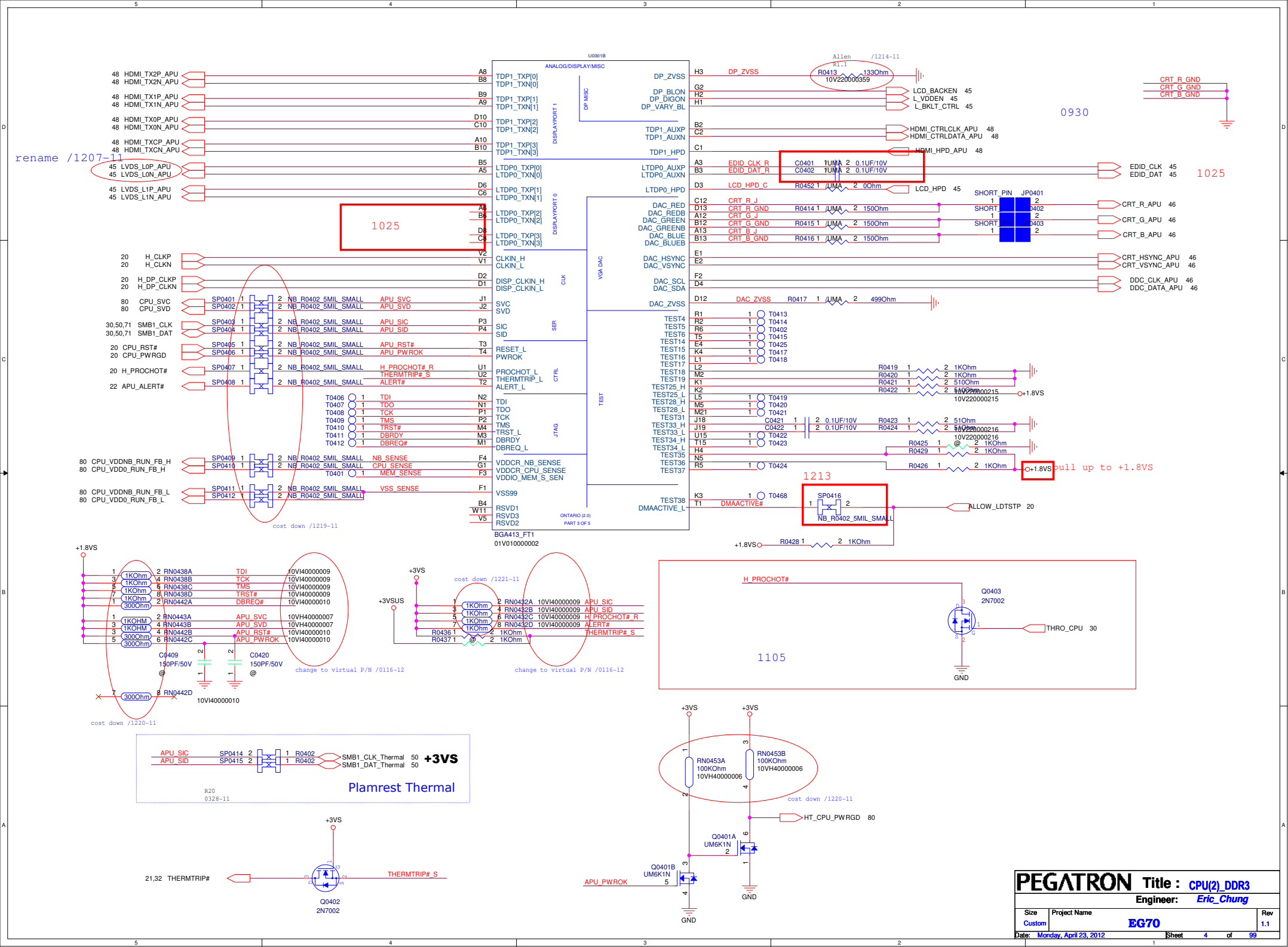
PEGATRON Title : System Setting

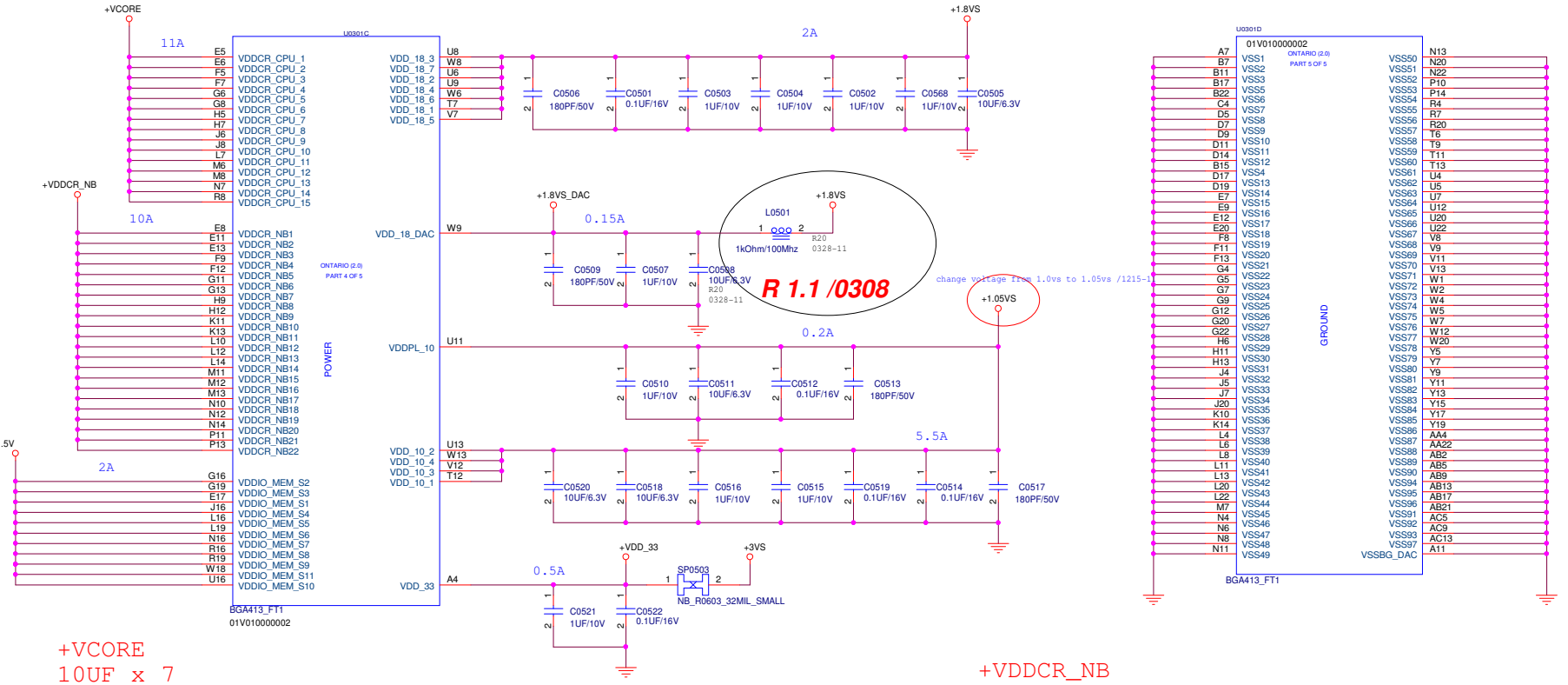
Engineer: Eric_Chung

Size	Project Name	Rev
C	EG70	1.1

Date: Monday, April 23, 2012 Sheet 2 of 99

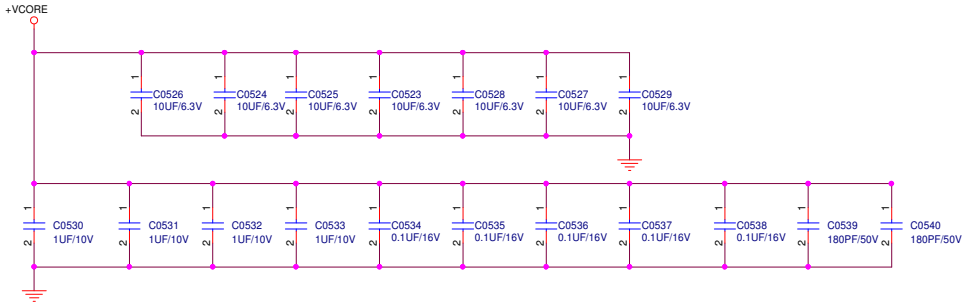

U0301E
ONTARIO (2.0)
PART 1 OF 5
MEMORY I/F
BGA413_FT1
01V010000002
vx_bga_413p_31_748x748_n
U0301A
ONTARIO (2.0)
PART 2 OF 5
PCIE I/F
UMI I/F
BGA413_FT1
change voltage from 1.0vs to 1.05vs /1215-11
rename /1213-11
M_VREF_APU
place within 1000mils with APU
1228

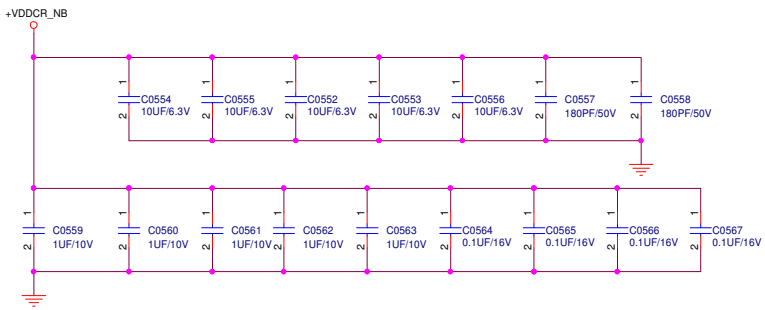

U0301B
ANALOG/DISPLAY/MISC
BGA413_FT1
01V010000002
rename /1207-11
1025
cost down /1219-11
cost down /1220-11
cost down /1221-11
change to virtual P/N /0116-12
0930
1213
1105
pull up to +1.8VS
Plamrest Thermal
R20
0328-11
PEGATRON
Title : CPU(2)_DDR3
Engineer: Eric_Chung
Size Custom
Project Name EG70
Rev 1.1
Date: Monday, April 23, 2012
Sheet 4 of 99

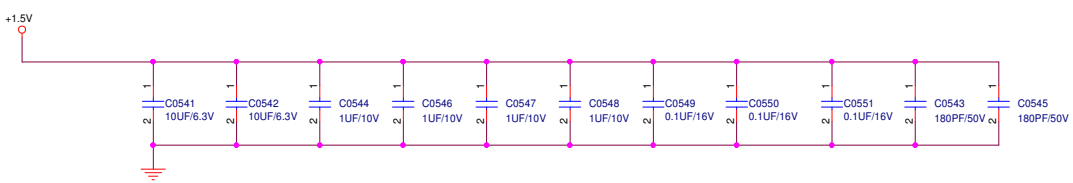


+VCORE
10UF x 7
1UF x 4
0.1UF x 5
180PF x 2

+VDDCR_NB
10UF x 7
1UF x 4
0.1UF x 5
180PF x 2







PEGATRON Title : CPU(3)_CFG,GND

Engineer: Eric_Chung

Size	Project Name	Rev
Custom	EG70	1.1

Date: Monday, April 23, 2012 Sheet 5 of 99

PEGATRON

Title : CPU(4)_PWR

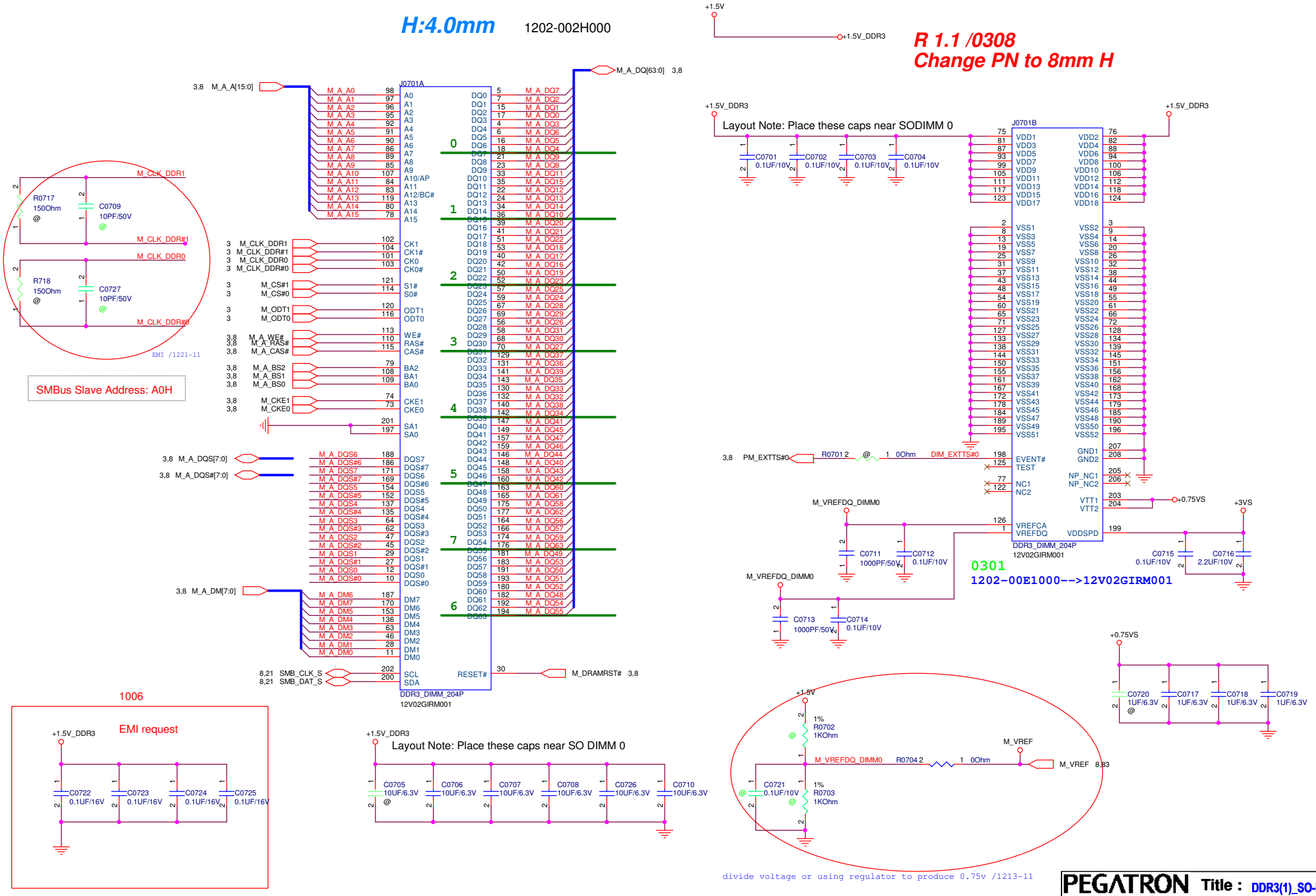
Engineer: Eric_Chung

Size	Project Name	Rev
Custom	EG70	1.1

Date: Monday, April 23, 2012 Sheet 6 of 99

H:4.0mm 1202-002H000

R 1.1 /0308
Change PN to 8mm H

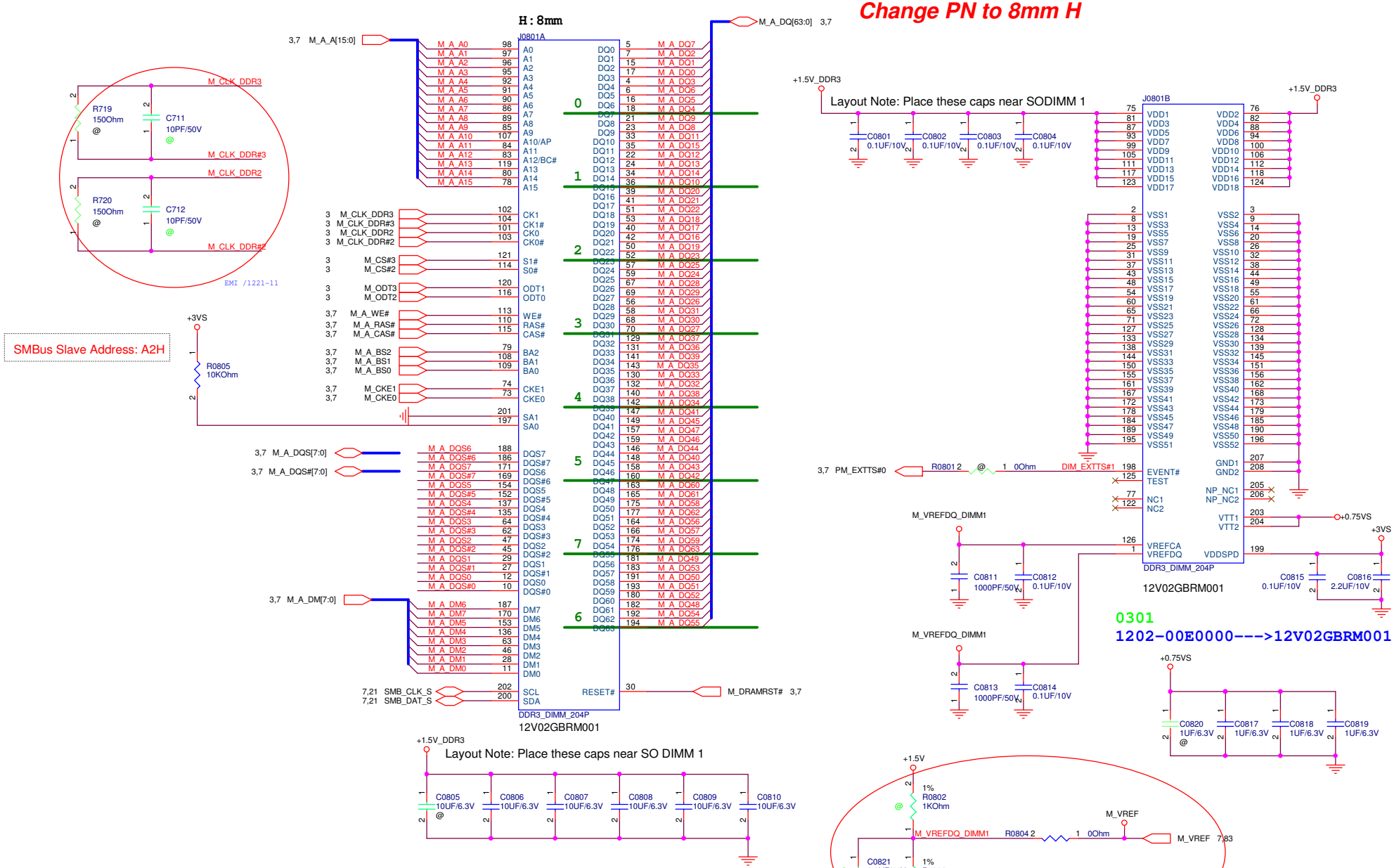


PEGATRON	Title : DDR3(1)_SO-DIMM0
	Engineer: Eric_Chung
Size: Custom	Project Name: EG70
Rev: 1.1	
Date: Monday, April 23, 2012	Sheet 7 of 99

H:8.0mm 1202-000P000

R 1.1 /0308
Change PN to 8mm H

H : 8mm



divide voltage or using regulator to produce 0.75v /1213-11

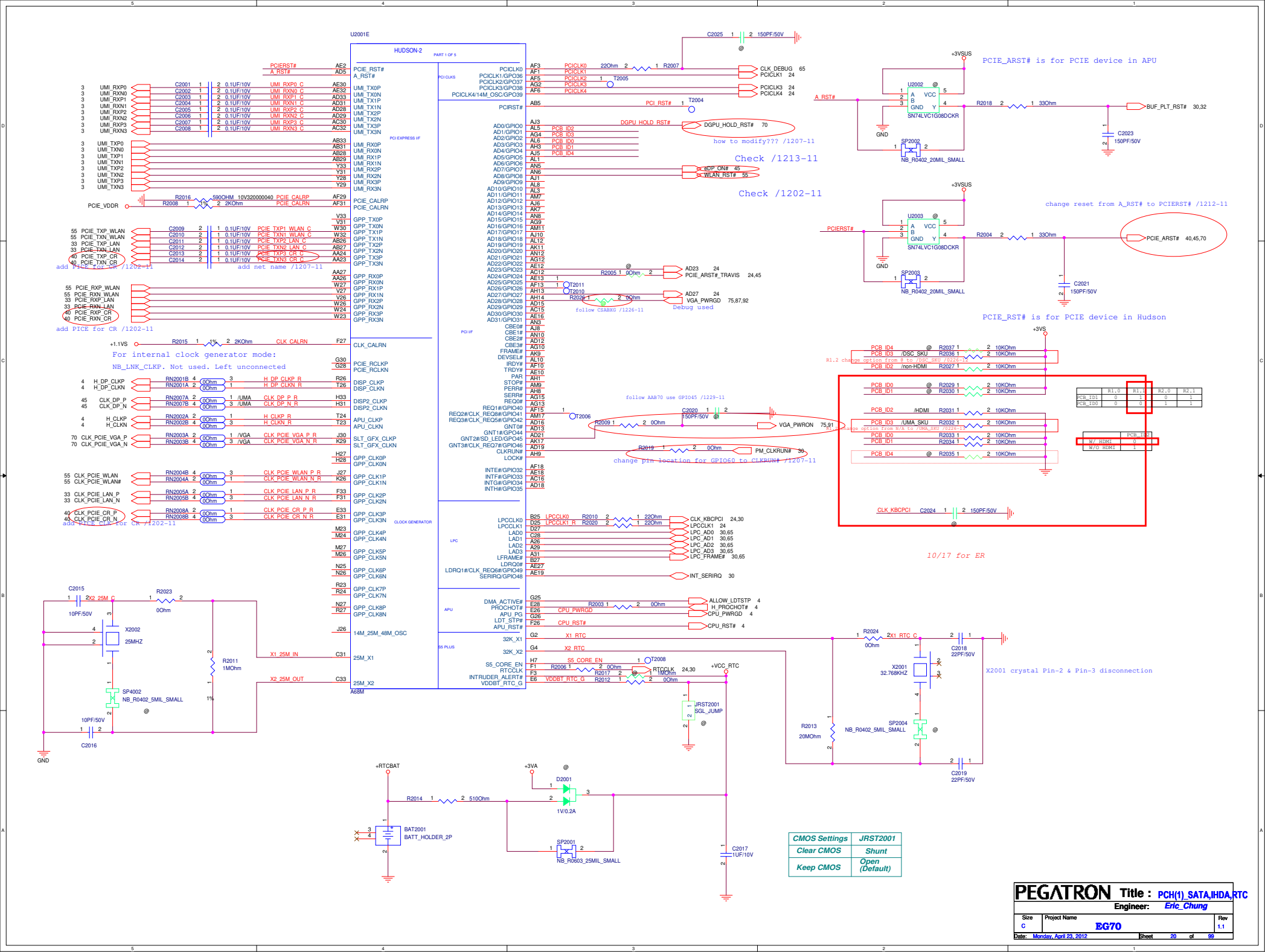
PEGATRON	Title : DDR3(2)_SO-DIMM1	
	Engineer: Eric_Chung	
Size: Custom	Project Name: EG70	Rev: 1.1
Date: Monday, April 23, 2012	Sheet 8 of 99	

PEGATRON Title : DDR3(3)_CA/DQ Voltage

Engineer: Eric_Chung

Size	Project Name	Rev
Custom	EG70	1.1

Date: Monday, April 23, 2012 Sheet 9 of 99

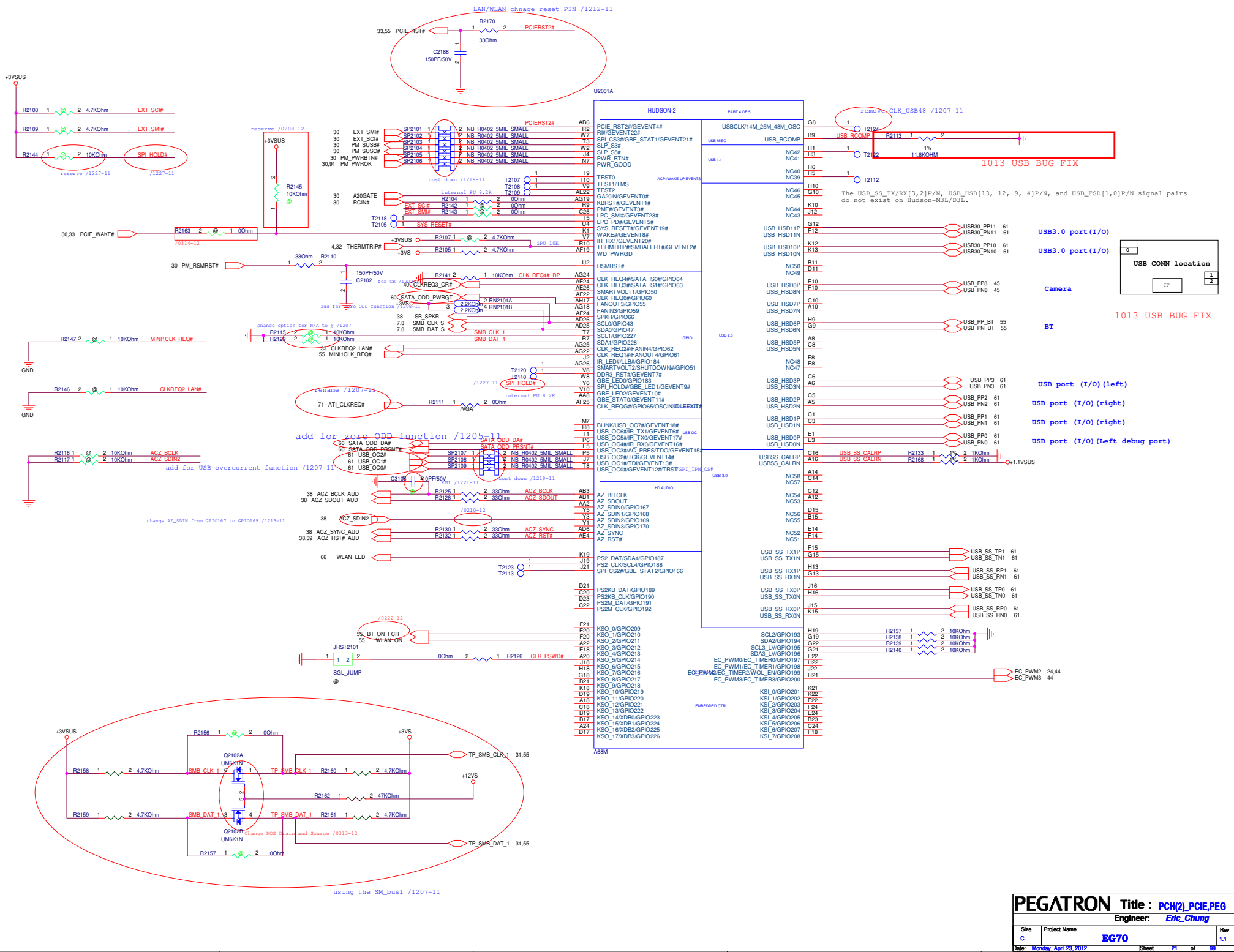


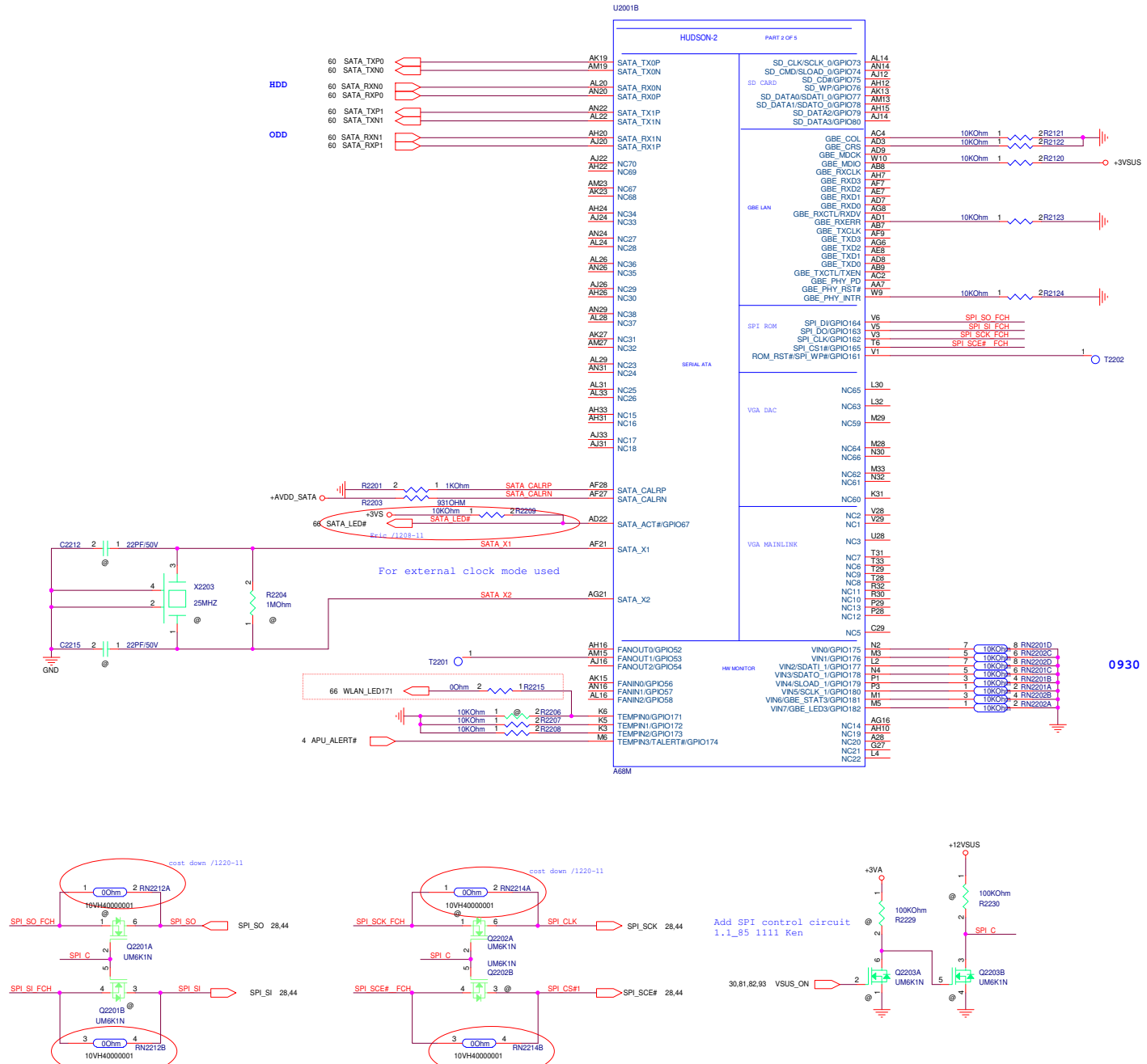
PEGATRON Title : PCH(1)_SATA,IHDA,RTC

Engineer: Eric_Chung

Size	Project Name	Rev
C	EG70	1.1

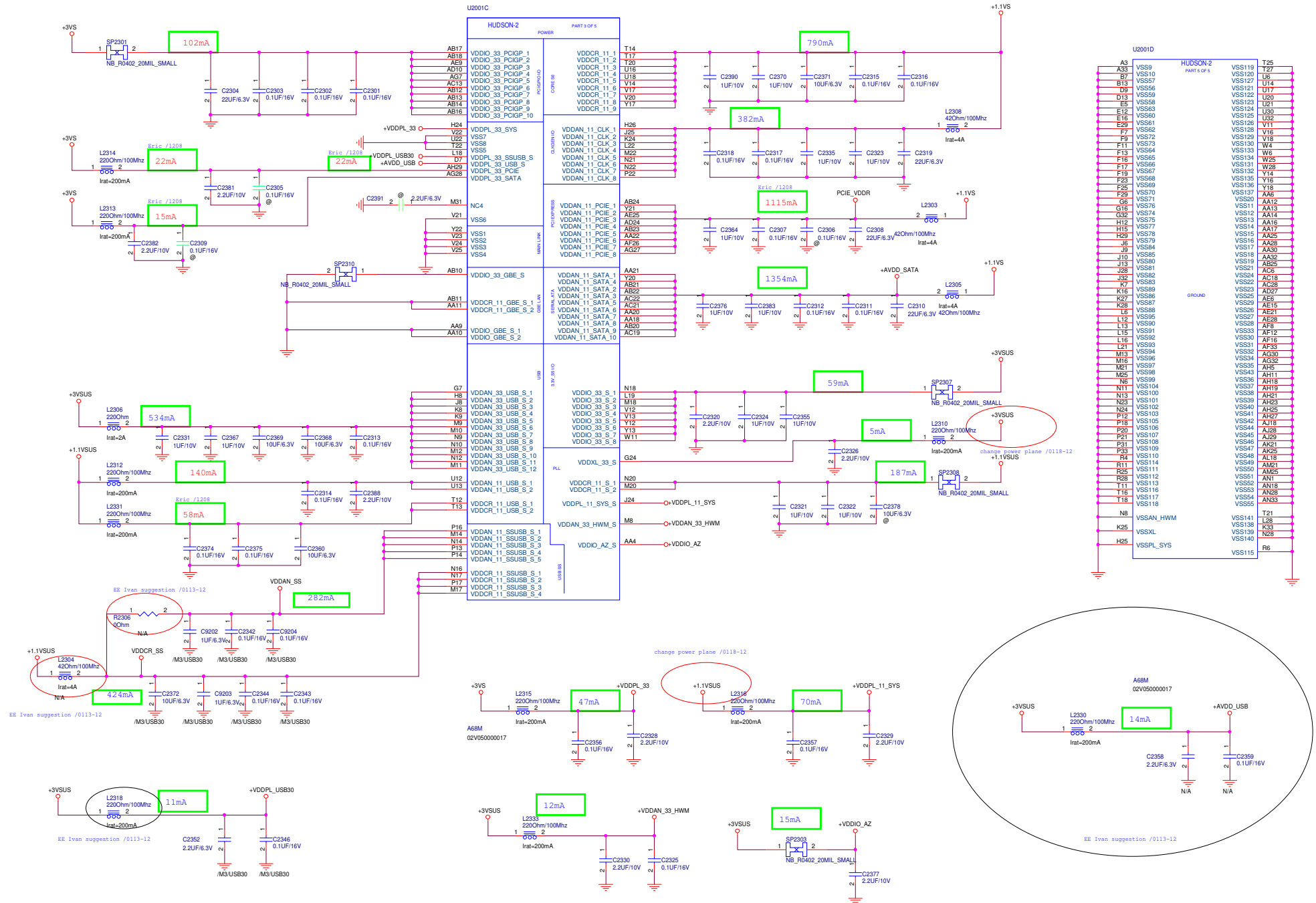
Date: Monday, April 23, 2012 Sheet 20 of 99


LAN/WLAN chnage reset PIN /1212-11
R2170
33Ohm
C2188
150PF/50V
33,55 PCIE_RST#
PCIERST2#
U2001A
HUDSON-2
PART 4 OF 5
remove CLK_USB48 /1207-11
1013 USB BUG FIX
The USB_SS_TX/RX[3,2]P/N, USB_HSD[13, 12, 9, 4]P/N, and USB_FSD[1,0]P/N signal pairs do not exist on Hudson-M3L/D3L.
USB3.0 port(I/O)
USB CONN location
Camera
BT
USB port (I/O)(left)
USB port (I/O)(right)
USB port (I/O)(Left debug port)
add for zero ODD function /1205-11
add for USB overcurrent function /1207-11
change AZ_SDIN from GPIO167 to GPIO169 /1213-11
using the SM_bus1 /1207-11
Change MOS Drain and Source /0313-12
SGL_JUMP
A68M
PEGATRON
Title : PCH(2)_PCIE,PEG
Engineer: Eric_Chung
Size C
Project Name EG70
Rev 1.1
Date: Monday, April 23, 2012
Sheet 21 of 99

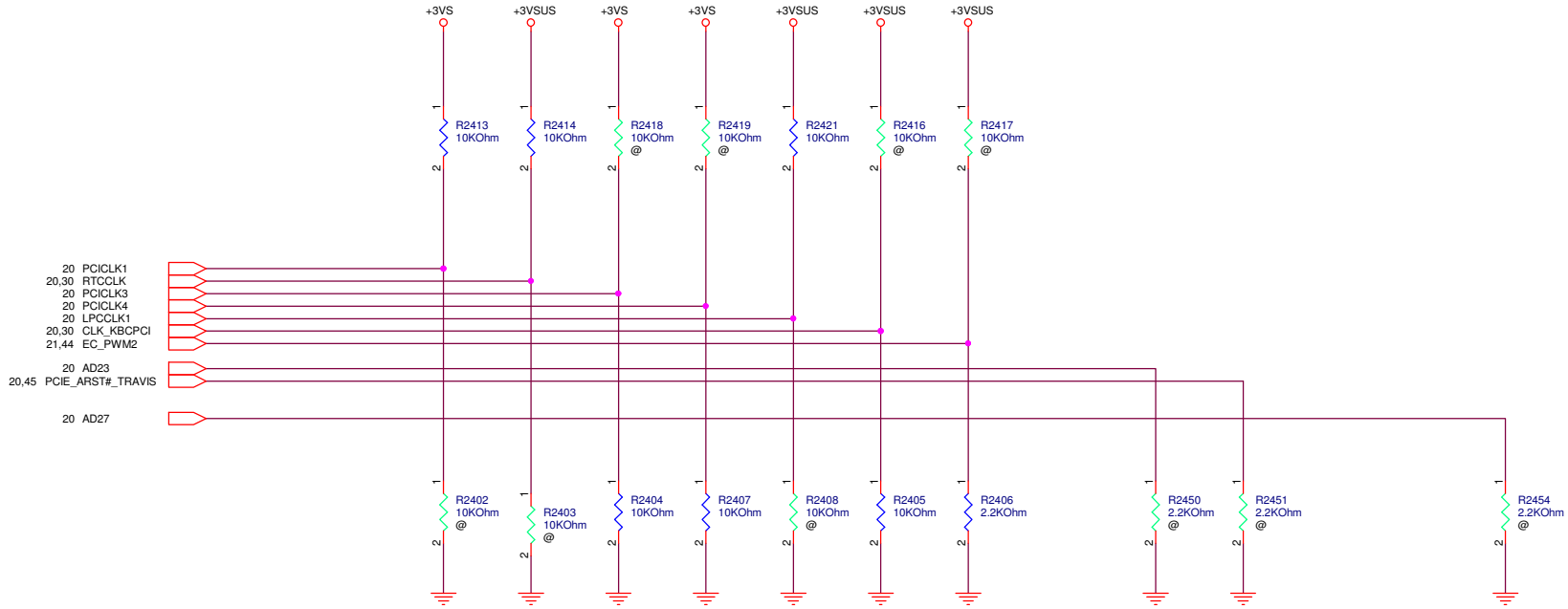


PEGATRON	Title : PCH(3)_FDI,DMI		
	Engineer: Eric_Chung		
Size: C	Project Name: EG70		Rev: 1.1
Date: Monday, April 23, 2012	Sheet 22 of 99		

Red ---> have been modified /1227-11



Strap Pins



		PCICLK1	RTCCLK	PCICLK3	PCICLK4	LPCCLK0 CLK_KBCPCI	LPCCLK1	EC_PWM2
High		***PCIE Gen2***	***S5 PLUS MODE Disable***	debug	no-Fusion clock mode	EC enable	***clock gen. enable***	LPC ROM
Low		PCIE Gen1	S5 PLUS MODE Enable	***ignore debug***	***Fusion clock mode***	***EC disable***	clock gen. disable	SPI ROM

Debug Straps

	AD23	PCIE_ARST#_TRAVIS AD24			AD27
High	***disable PCI mem boot***	***default PCIE straps***			***use PCI PLL***
Low	enable PCI mem boot	EEPROM PCIE straps			by pass PCI PLL

PEGATRON Title : PCH(5)_PCI,USB

Engineer: *Eric_Chung*

Size	Project Name	Rev
Custom	EG70	1.1

Date: Monday, April 23, 2012 Sheet 24 of 99

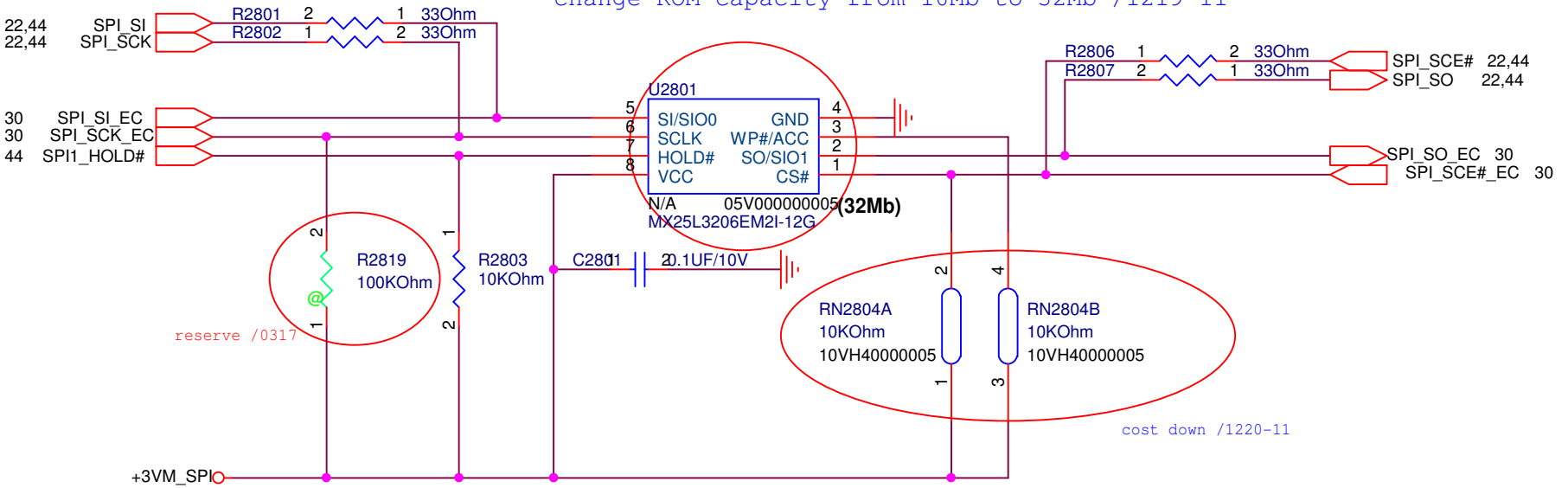
PEGATRON Title : PCH(6)_CPU,GPIO,MISC

Engineer: *Eric_Chung*

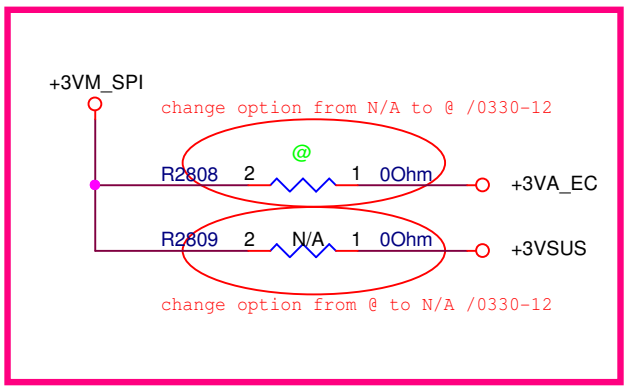
Size	Project Name	Rev
Custom	EG70	1.1

Date: Monday, April 23, 2012 Sheet 25 of 99

change ROM capacity from 16Mb to 32Mb /1219-11



1110



WINBOND:0500-00P4000 (16Mb)
MXIC: 0500-00TY000(16Mb)

reserved for BIOS testing

PEGATRON	Title : SPI ROM	
	Engineer: Eric_Chung	
Size: A	Project Name: EG70	Rev: 1.1
Date: Monday, April 23, 2012	Sheet 28 of 99	

PEGATRON

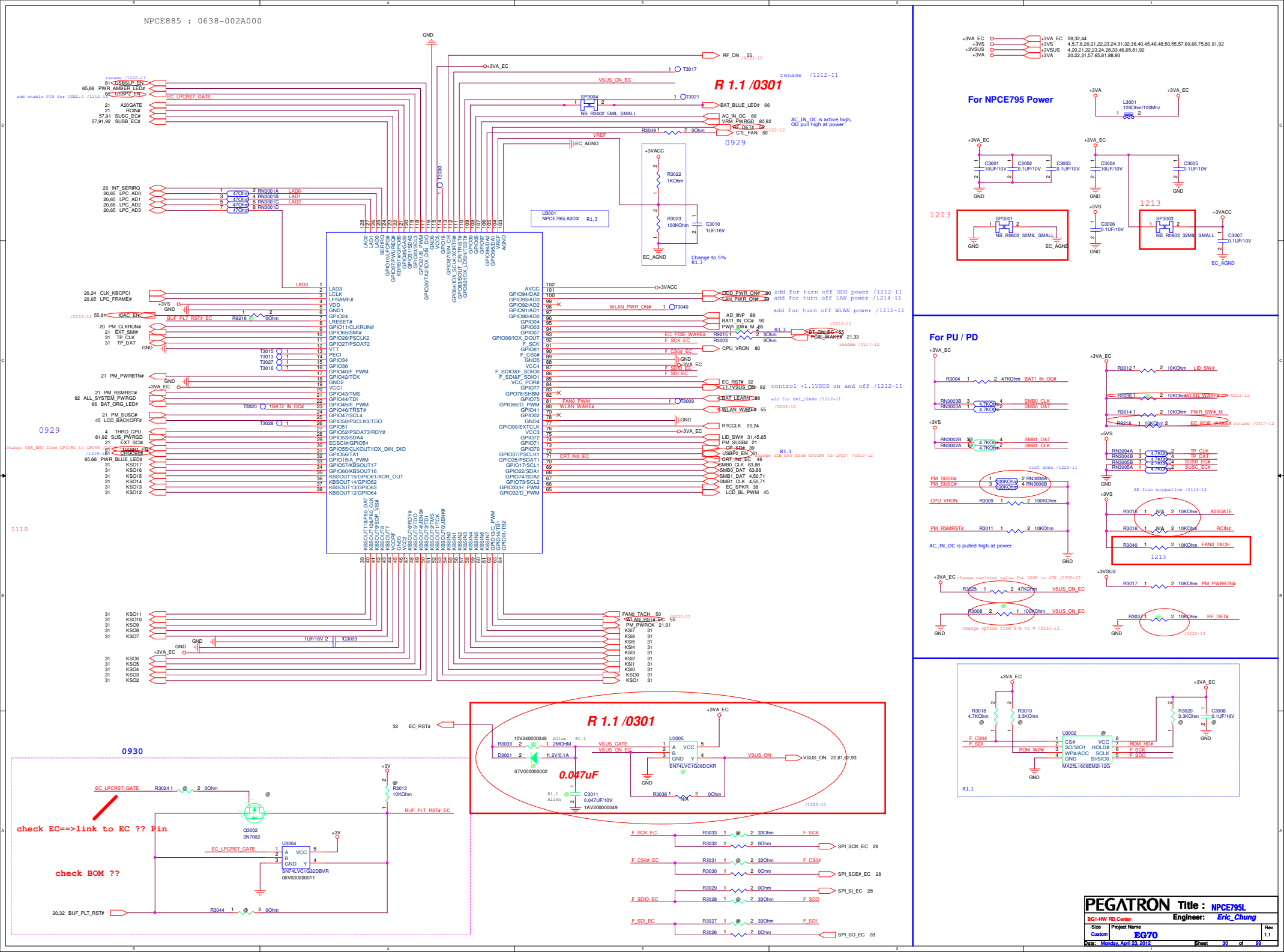
Title : CLK_SLG8SP585VTR

Engineer: *Eric_Chung*

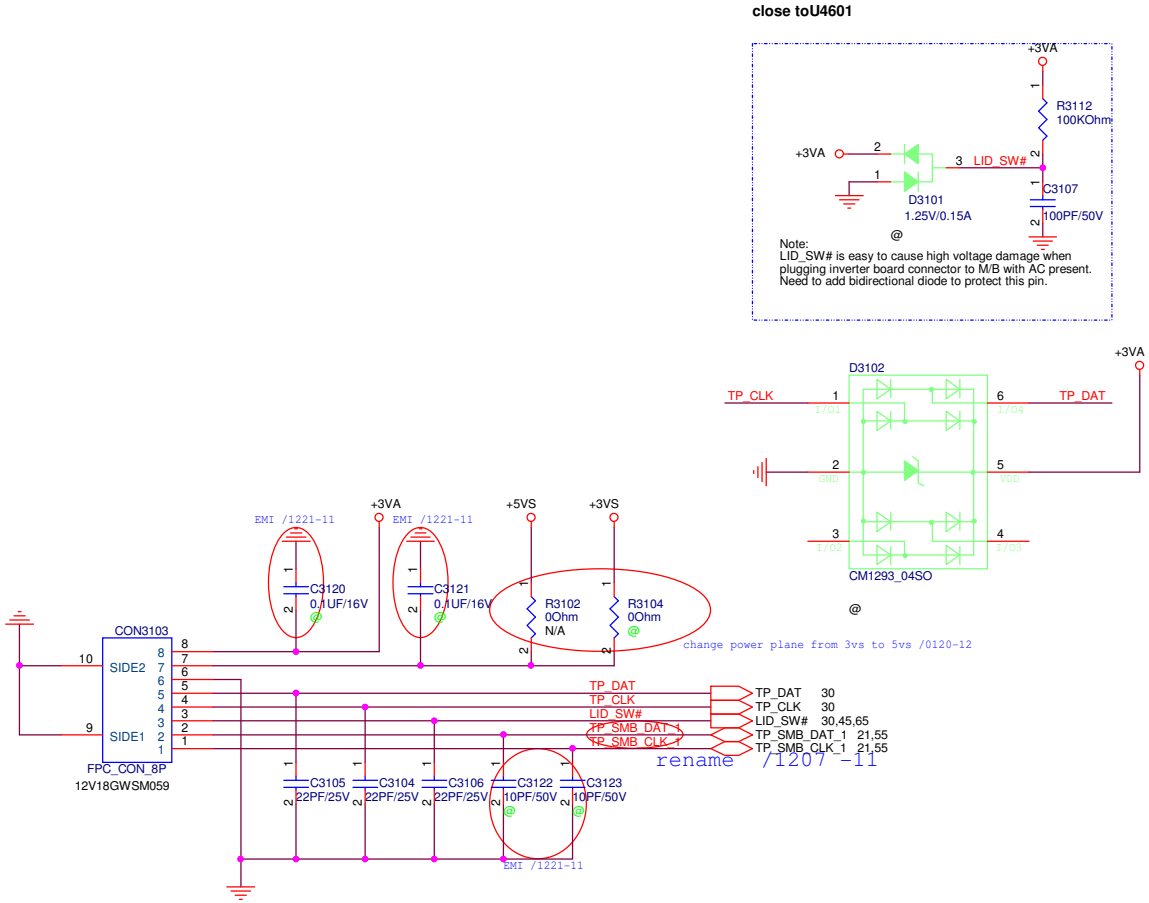
Size	Project Name	Rev
Custom	EG70	1.1

Date: Monday, April 23, 2012 Sheet 29 of 99

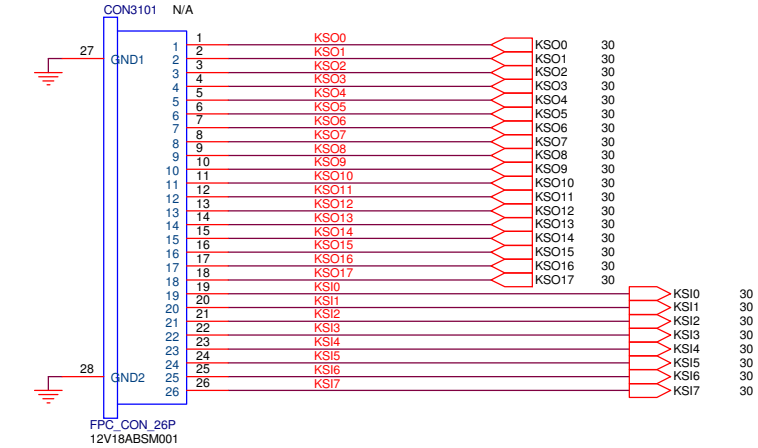
NPCE885 : 0638-002A000



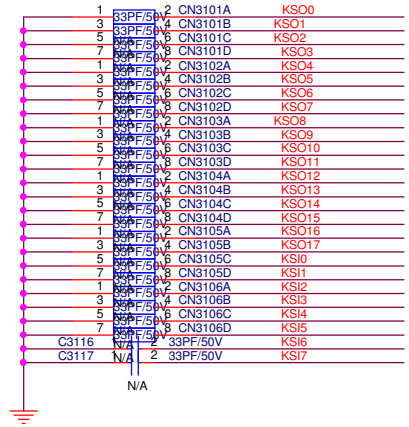
Touch Pad Button/ Hall Sensor



Keyboard



1218-00MW000



PEGATRON Title : KB/ TP/ FLASH

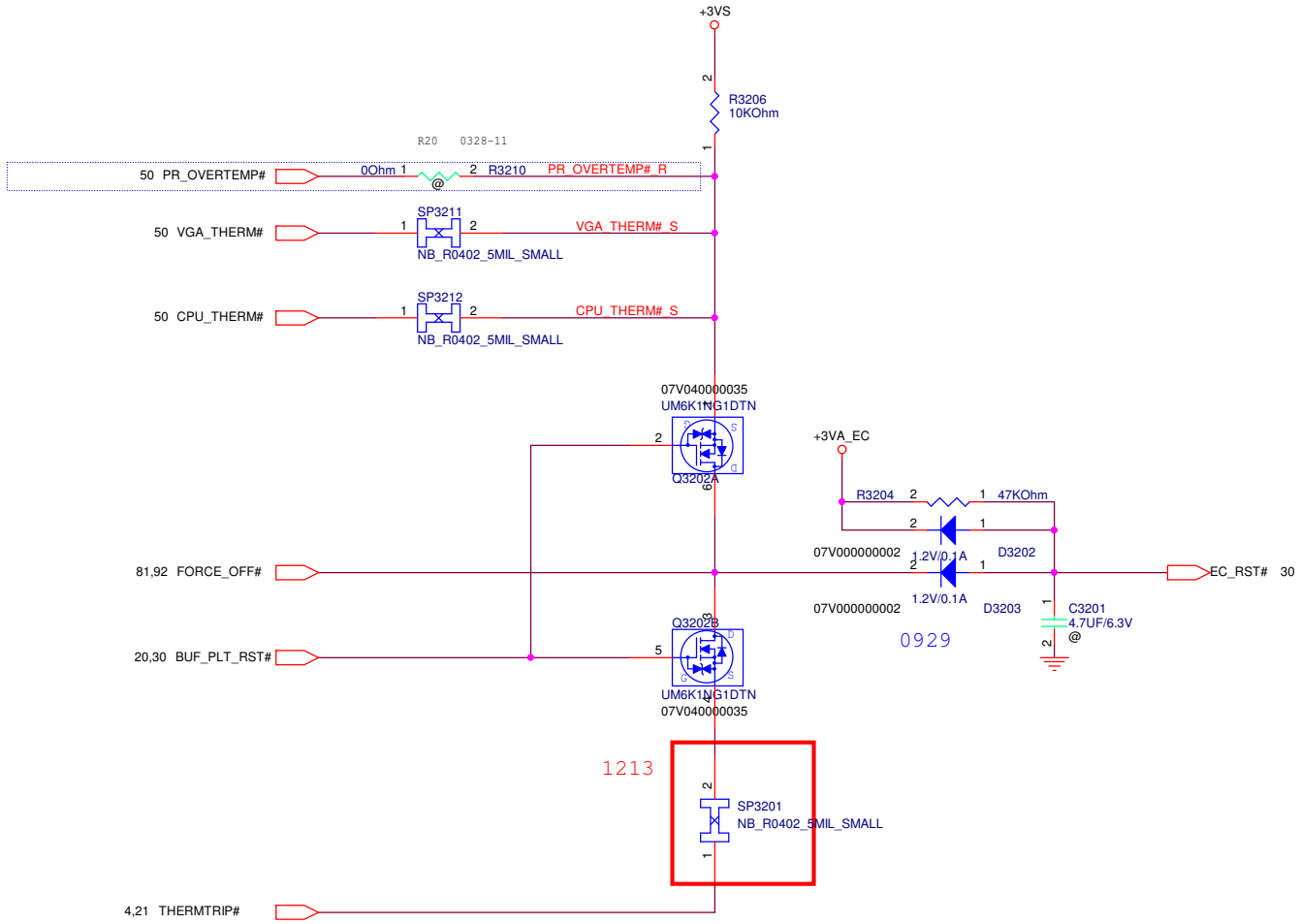
BG1-HW RD Center Engineer: Eric_Chung

Size	Project Name	Rev
Custom	EG70	1.0

Date: Monday, April 23, 2012 Sheet 31 of 99

Thermal Policy

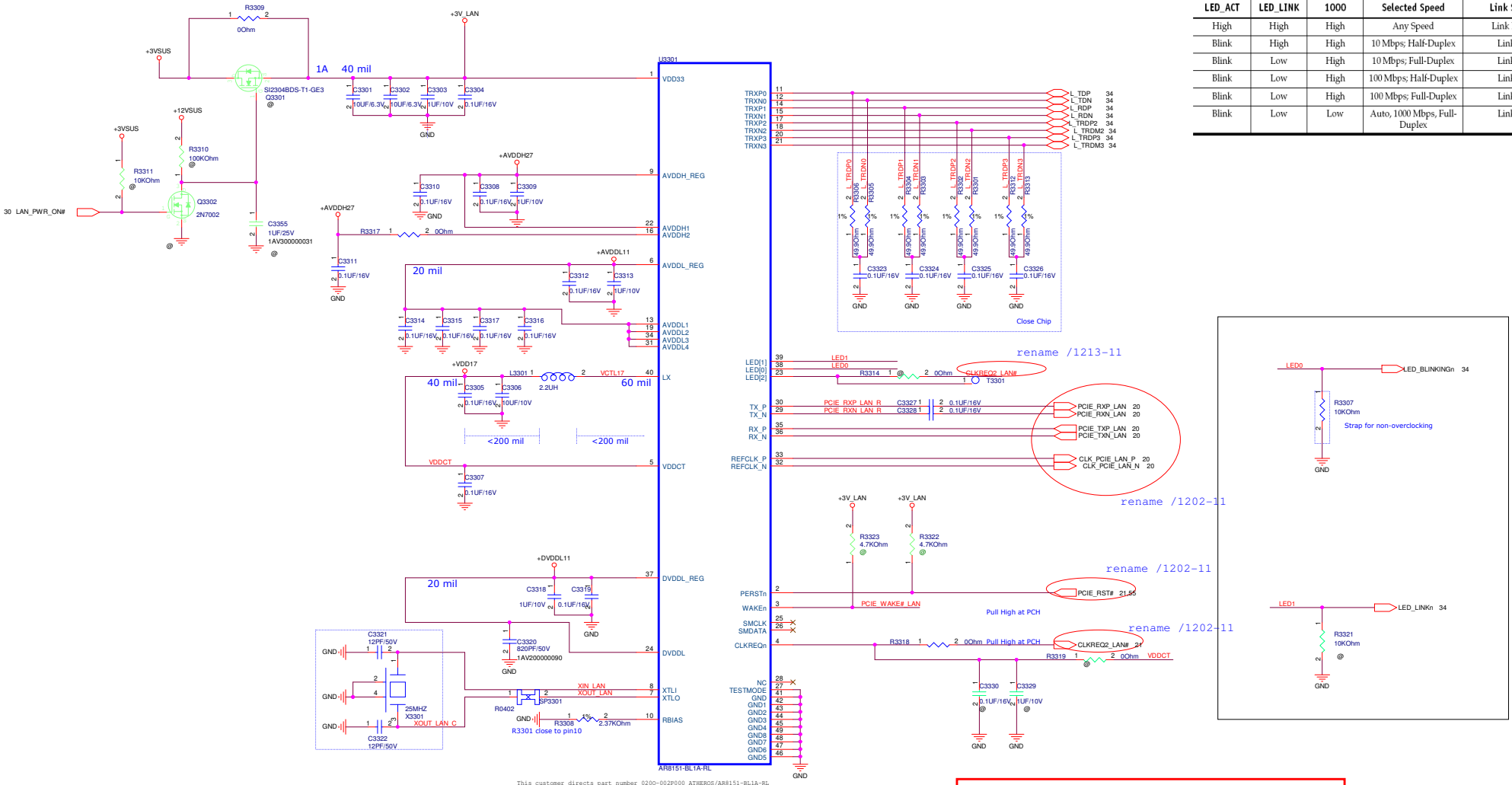
NPCE795 has internal power-on reset circuit
Use 47k ohm to make sure that raising time of POR is less than 10us



PEGATRON	Title : RST_Reset Circuit	
	Engineer: Eric_Chung	
Size: B	Project Name: EG70	Rev: 1.1
Date: Monday, April 23, 2012	Sheet 32 of 99	

Table 2-6. **LED Link Table**

LED[0] LED_ACT	LED[1] LED_LINK	LED[2] LED_LINK_ 1000	Selected Speed	Link Status
High	High	High	Any Speed	Link Down
Blink	High	High	10 Mbps; Half-Duplex	Link Up
Blink	Low	High	10 Mbps; Full-Duplex	Link Up
Blink	Low	High	100 Mbps; Half-Duplex	Link Up
Blink	Low	High	100 Mbps; Full-Duplex	Link Up
Blink	Low	Low	Auto, 1000 Mbps, Full-Duplex	Link Up



This customer directs part number 020O-002P000 ATHEROS/AR8151-BL1A-RL

PEGATRON Title : LAN_AR8151L

BG1-HW RD Center Engineer: Eric_Chung

Size	Project Name	Rev
Custom	EG70	1.0

Date: Monday, April 23, 2012 Sheet 33 of 99

EMI suggestion /0224-12

U3401
AZ1045_04F
N/A

L_TXP_T, L_TXN_T, L_RXP_T, L_RXN_T

LU3402
10/100MB
09V120000007

L_TDP, L_TDN, L_RDP, L_RDN, RDCT1, L_TXP, L_TXN, L_CMT0, L_CMT1, L_RXN, L_RXP

EMI suggestion /0224-12

U3402
AZ1045_04F
N/A

L_TRLP2_T, L_TRLM2_T, L_TRLP3_T, L_TRLM3_T

EMI Req /0223-12

D3401
N/A
AZ2025-01H.R7G

R3408 0Ohm
C3406 10PF/50V
C3407 10PF/50V
C3408 10PF/50V

LAN_GND

+VDD17

R3414 0Ohm

C3409 1UF/6.3V

FAE suggestion 1003

Co-Layout

LU3401
09V120000003
GST5009

L_TDP, L_TDN, L_RDP, L_RDN, L_TRDP2, L_TRDM2, L_TRDP3, L_TRDM3

L_TXP_T, L_TXN_T, L_RXP_T, L_RXN_T, L_TRLP2_T, L_TRLM2_T, L_TRLP3_T, L_TRLM3_T

L_TXP, L_CMT0, L_TXN, L_RXP, L_CMT1, L_RXN, L_TRLP2, L_CMT2, L_TRLM2, L_TRLP3, L_CMT3, L_TRLM3

RDCT1

C3404 0.1UF/16V

C3411 1000PF/50V
@

EMI suggest to change 0805 size 0921

R3401 75Ohm

07V180000007
275V
U3405 /HOME

C3405 1500PF/2KV

LAN_GND

U3403
AZ3028-04P
/HOME

U3404
AZ3028-04P
/HOME

swap for EMI suggestion /0224-12

swap for EMI suggestion /0224-12

+3V_LAN

R3409 0Ohm

R3413 0Ohm

510Ohm R3411

LED_LINKn

C3403 470PF/50V
@

R3412 510Ohm
@

33 LED_LINKn

C3401 470PF/50V
@

LAN_GND

LAN_JACK_8P
CON3401
12V23GBSD009

L_TXP, L_TXN, L_RXP, L_TRLP2, L_TRLM2, L_RXN, L_TRLP3, L_TRLM3

P_GND1, P_GND2

33 LED_BLINKINGn

R3410 510Ohm

C3402 470PF/50V
@
Close Connector

for Non-overclocking

<Variant Name>

PEGATRON Title : RJ45/RJ11

BG1-HW RD Center Engineer: Eric_Chung

Size	Project Name	Rev
Custom	EG70	1.0

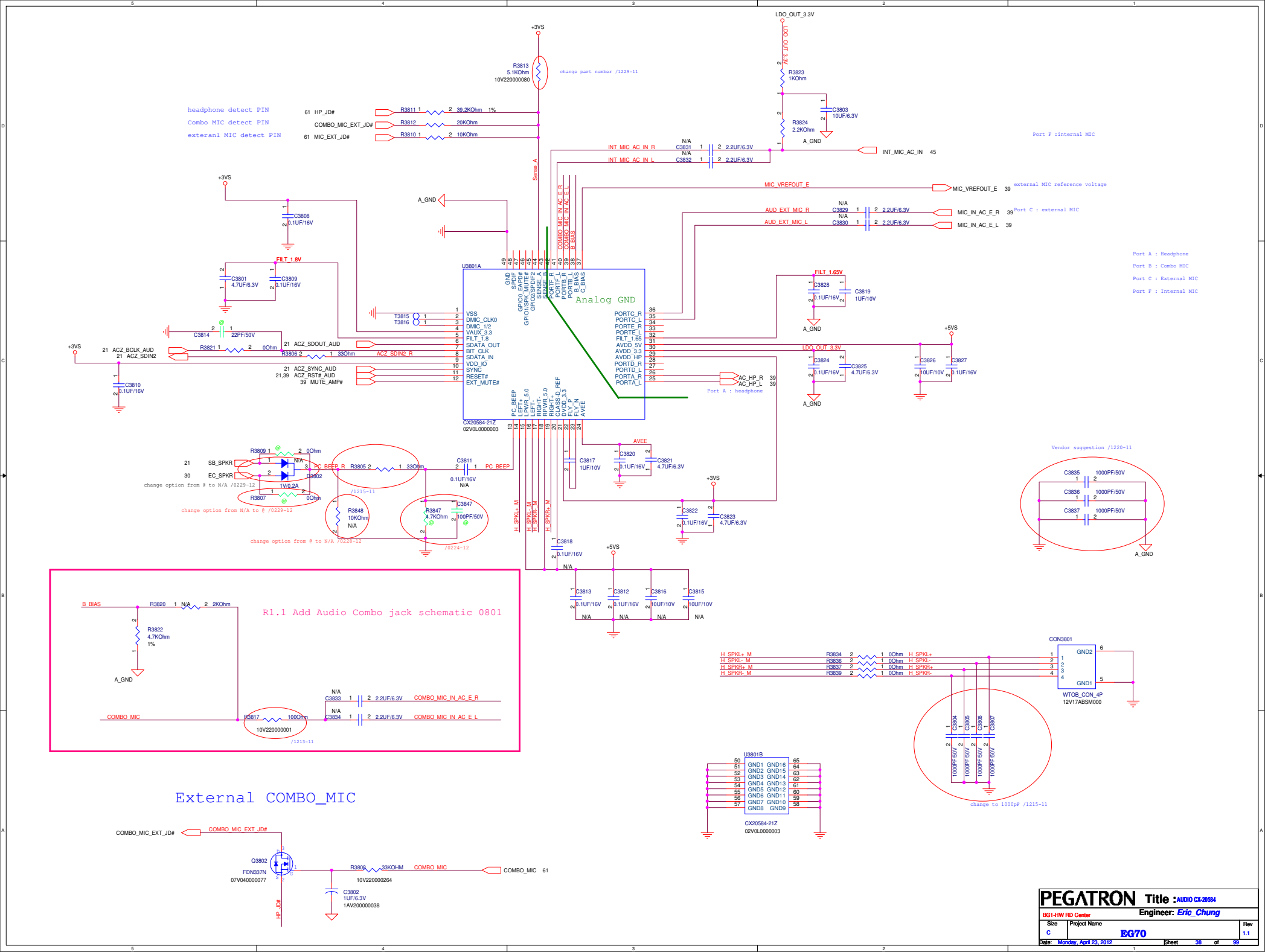
Date: Monday, April 23, 2012 Sheet 34 of 99

PEGATRON Title : MDC CONN

BG1-HW RD Center Engineer: Eric_Chung

Size	Project Name	Rev
C	EG70	1.1

Date: Monday, April 23, 2012 Sheet 35 of 99



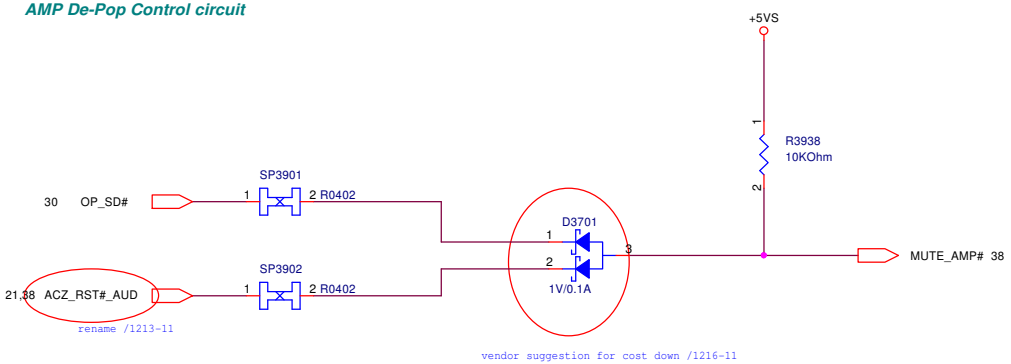
PEGATRON Title : AUDIO CX-20584

BG1-HW RD Center Engineer: Eric_Chung

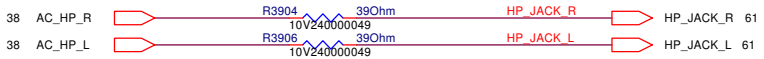
Size	Project Name	Rev
C	EG70	1.1

Date: Monday, April 23, 2012 Sheet 38 of 99

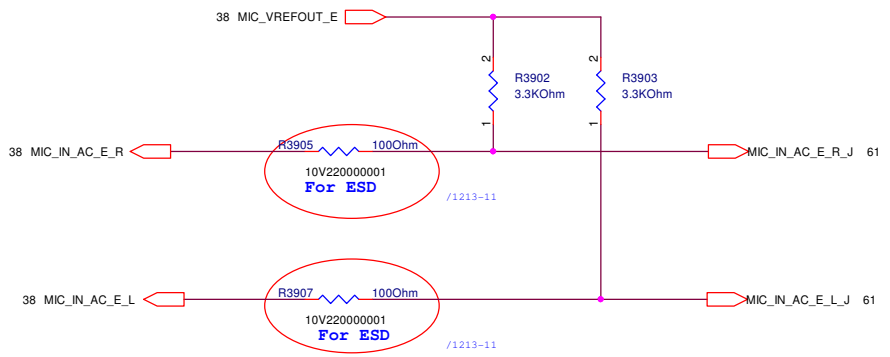
AMP De-Pop Control circuit



Headphone



External MIC



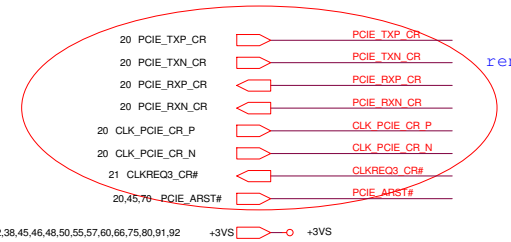
PEGATRON Title : AUDIO CX-20584

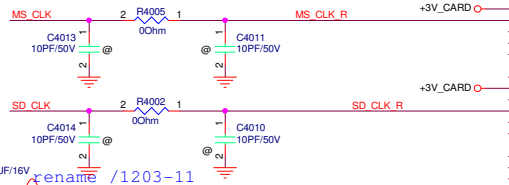
BG1-HW RD Center Engineer: Eric_Chung

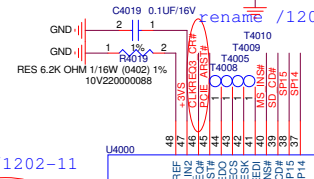
Size	Project Name	Rev
Custom	EG70	1.1

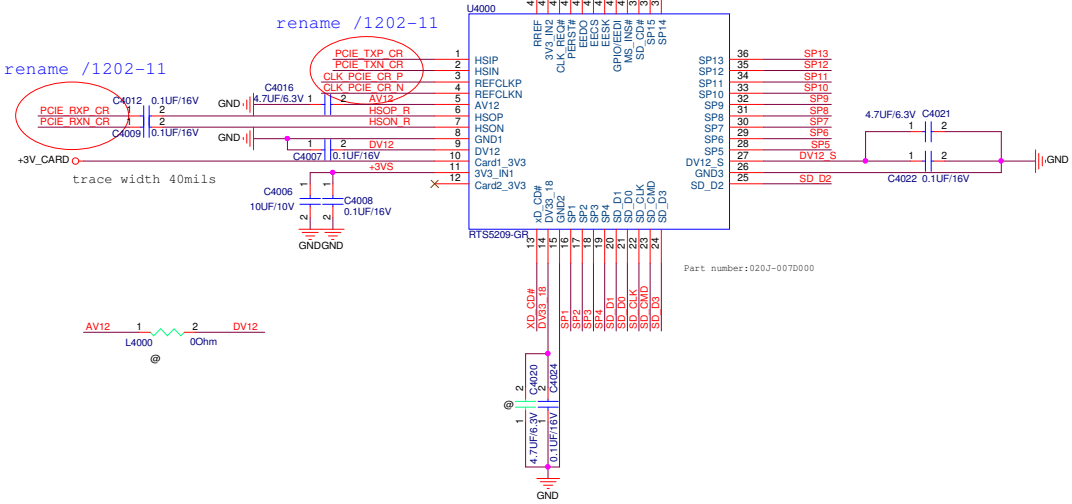
Date: Monday, April 23, 2012 Sheet 39 of 99

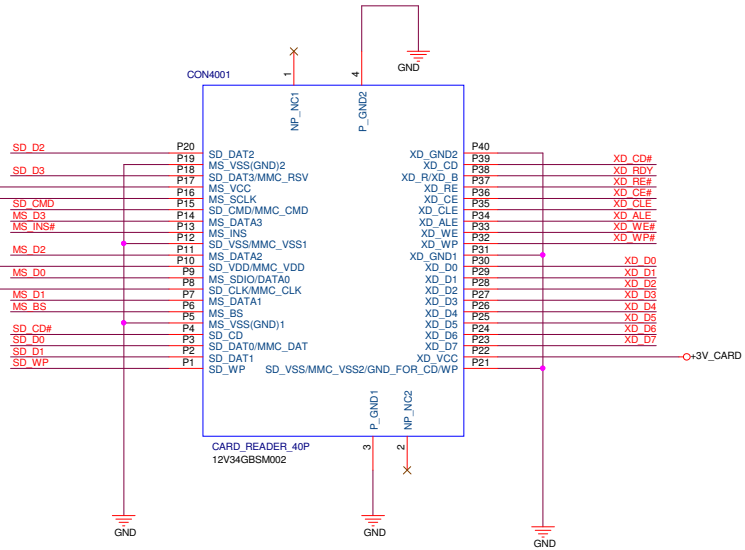
From System's PCIE interface



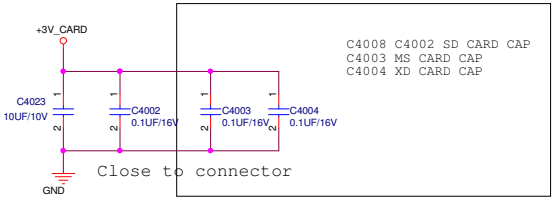








SD/MMC/MMC plus/MS/xD



Remove Serial Flash

Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15	SD_WP	XD_D7

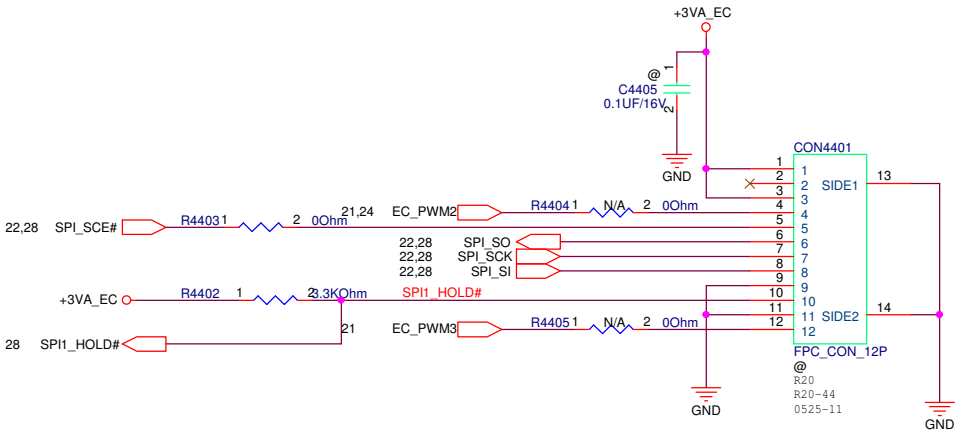
Share Pin

PEGATRON Title : RTS5209

BG1-HW RD Center Engineer: Eric_Chung

Size	Project Name	Rev
Custom	EG70	1.0

Date: Monday, April 23, 2012 Sheet 40 of 99



PEGATRON **Title :** DEBUG

BG1-HW RD Center **Engineer:** *Eric Chung*

Size	Project Name	Rev
B	EG70	1.1

Date: Monday, April 23, 2012 Sheet 44 of 99

1207-11 Reserve for EHCI controller may generate CRC errors issue.

LCD VDDEN / +LED_VCC

R 1.1 /0301

R 1.1 /0301

RN3733 close to EDP connector(CON3703)

LVDS connector

EDP connector

rename /1205-11

replace /1205-11

0930

iGPU to converter

rename /1207-11

add for EDP /1205-11

converter to LVDS connector (dual)

cost down /1220-11

+1.2VS LDO

Vout=0.8*(1+R4517/R4516)
=0.8*(1+0.51)=1.2

RT9041B-10GE

add for EDP /1205-11

follow CSABXG /0111-12

clock select and POR

add CON for EDP

check function /1214-11

check /1213-11

change part number /1229-11

for LVDS/eDP power sequence check

+3VS_DVDD and AVDD

0930

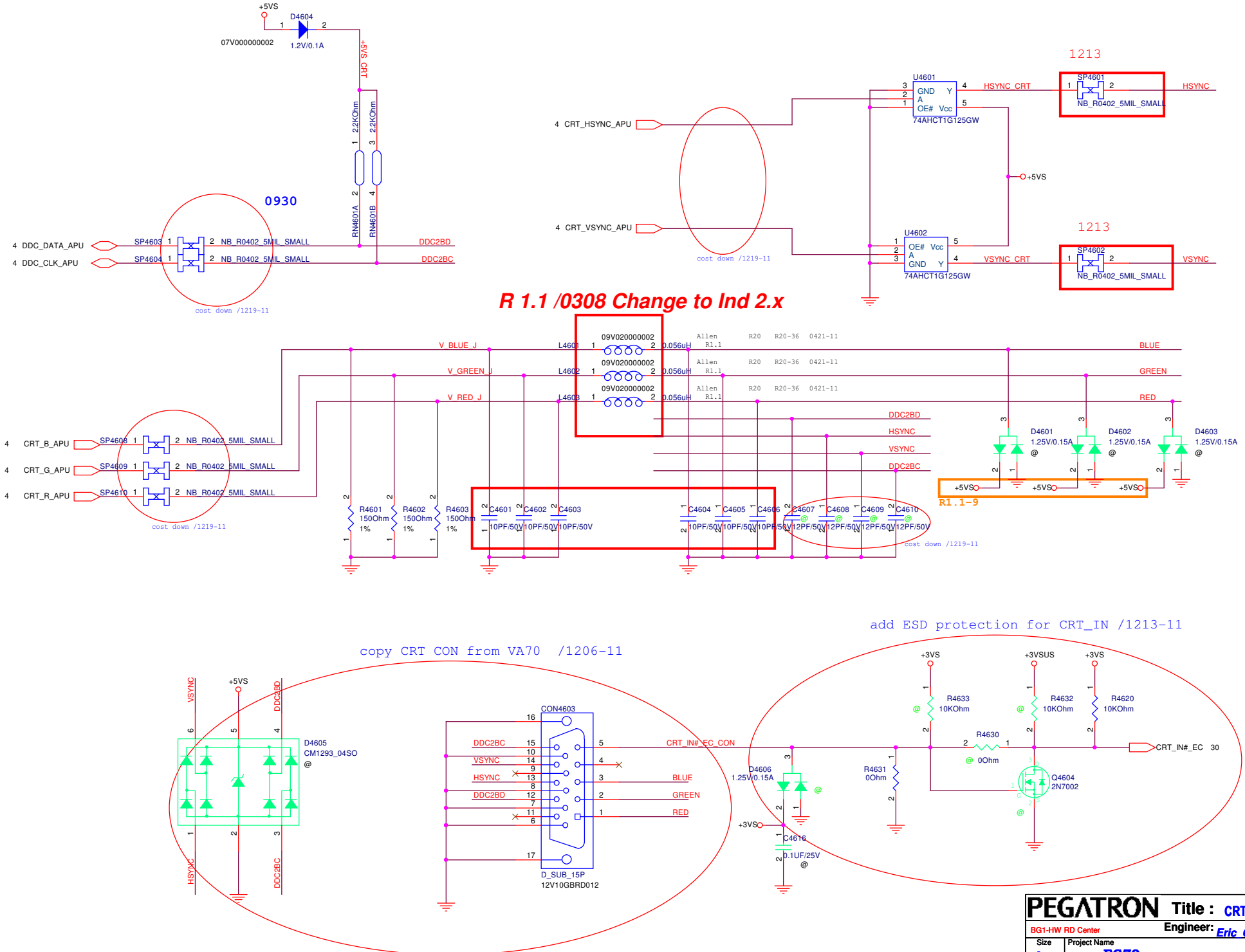
0929

EDP HDP

HPD high active for AMD

modify the EDP HPD circuit /1221-11

PEGATRON	Title : LVDS OUT		
BGI-HW RD Center	Engineer: Eric_Chung		
Size: Custom	Project Name: EG70	Rev: 1.1	
Date: Monday, April 23, 2012	Sheet 45 of 99		

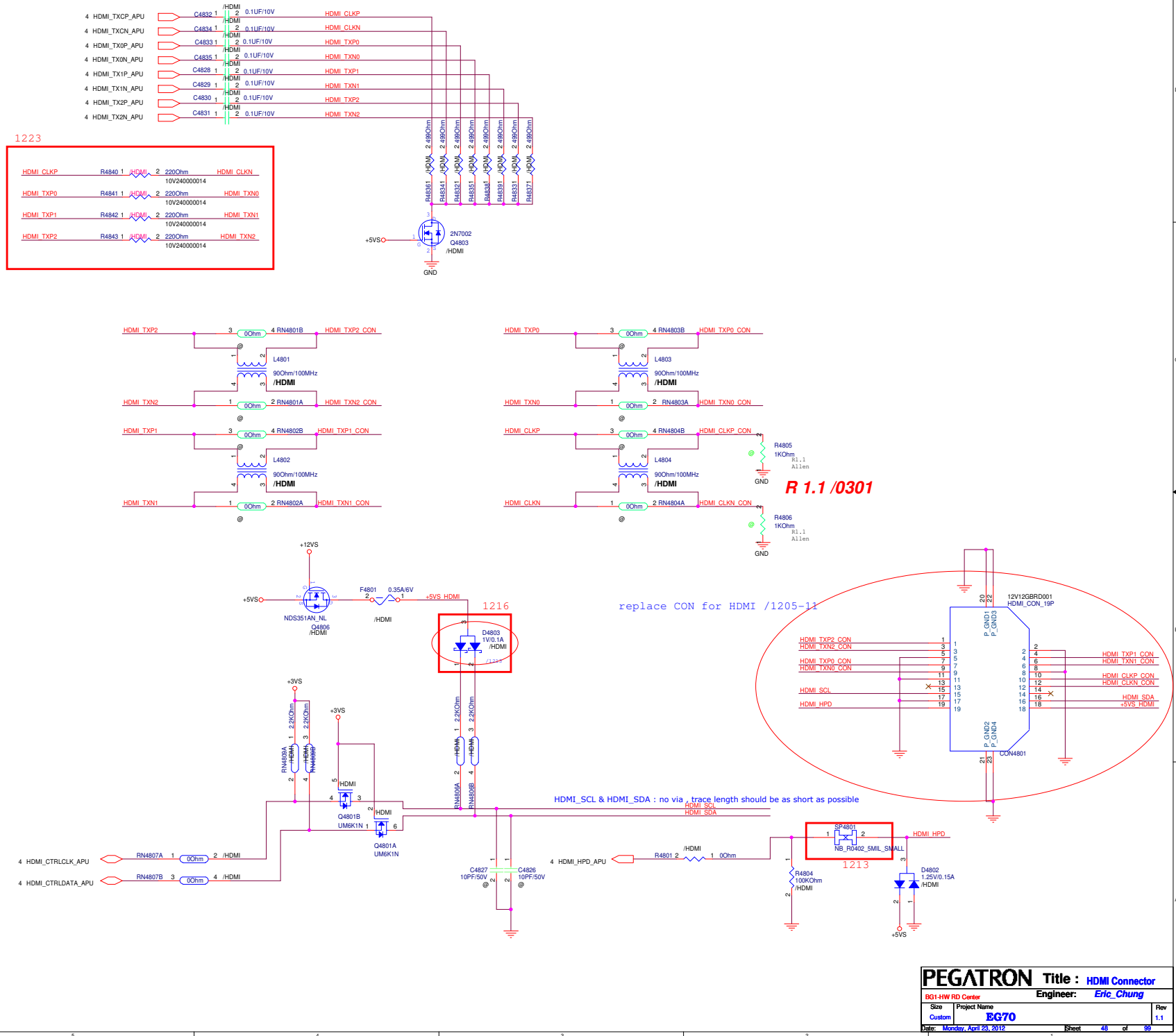


PEGATRON Title : CRT

BG1-HW RD Center Engineer: Eric_Chung

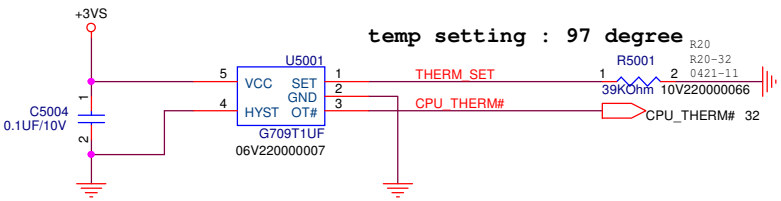
Size	Project Name	Rev
Custom	EG70	1.1

Date: Monday, April 23, 2012 Sheet 46 of 99

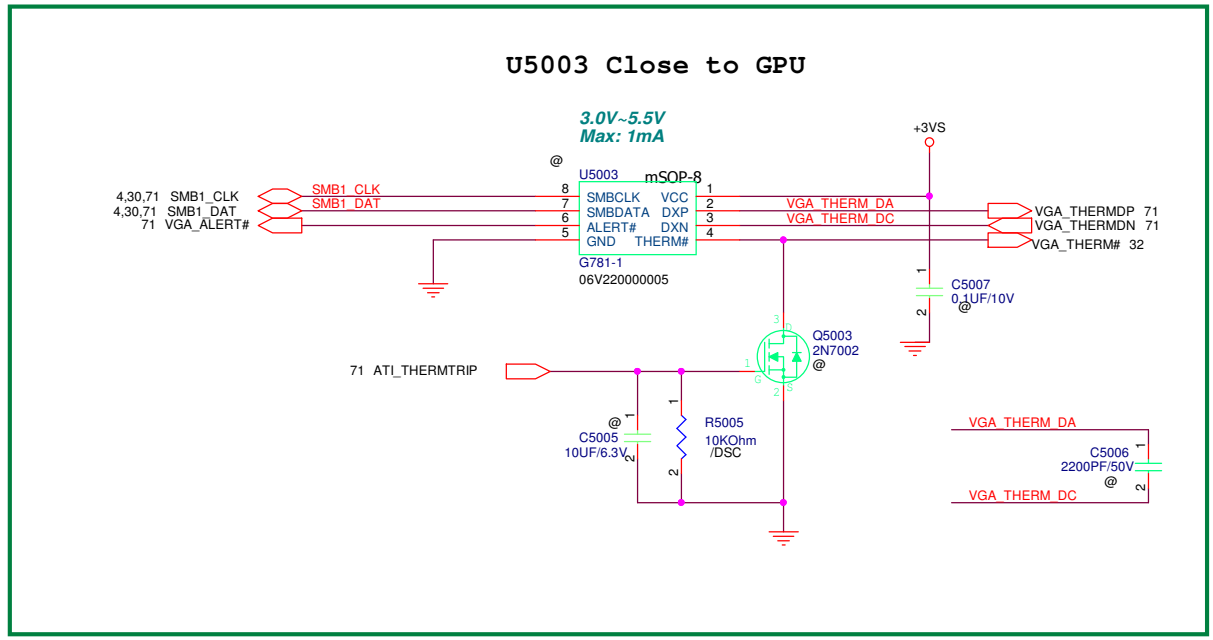


PEGATRON	Title : HDMI Connector		
BG1-HW RD Center	Engineer: Eric_Chung		
Size: Custom	Project Name: EG70		Rev: 1.1
Date: Monday, April 23, 2012	Sheet 48 of 99		

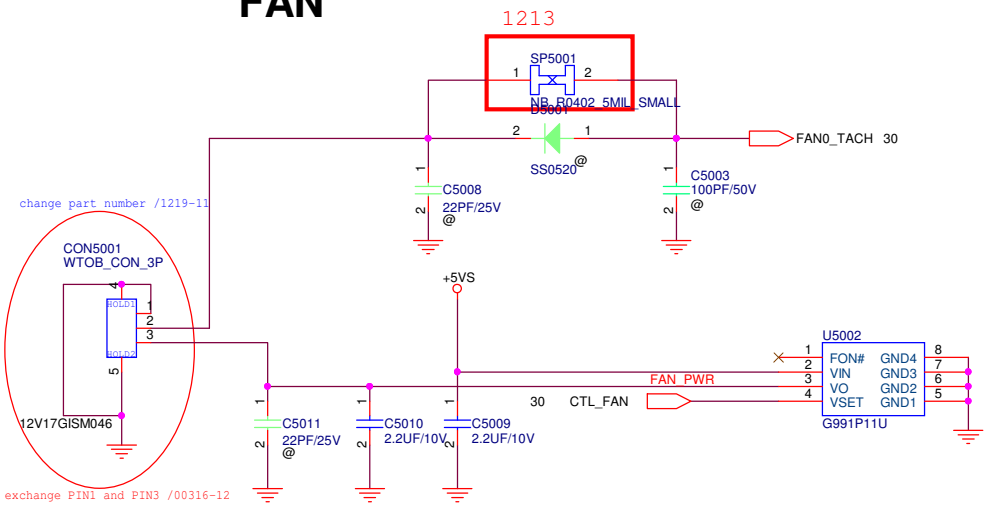
U5001 Close to CPU



U5003 Close to GPU

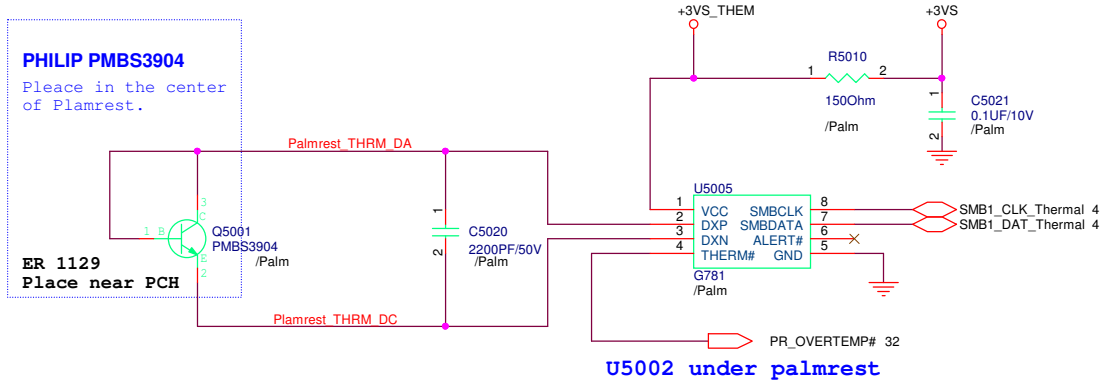


FAN



Plam Rest Thermal Sensor

R20 0328-11
R20-9 0330-11



U5002 under palmrest

SMBUS addr=1001100x (98)

U5002: Remote(Local) thermal sensor,use remote mode.

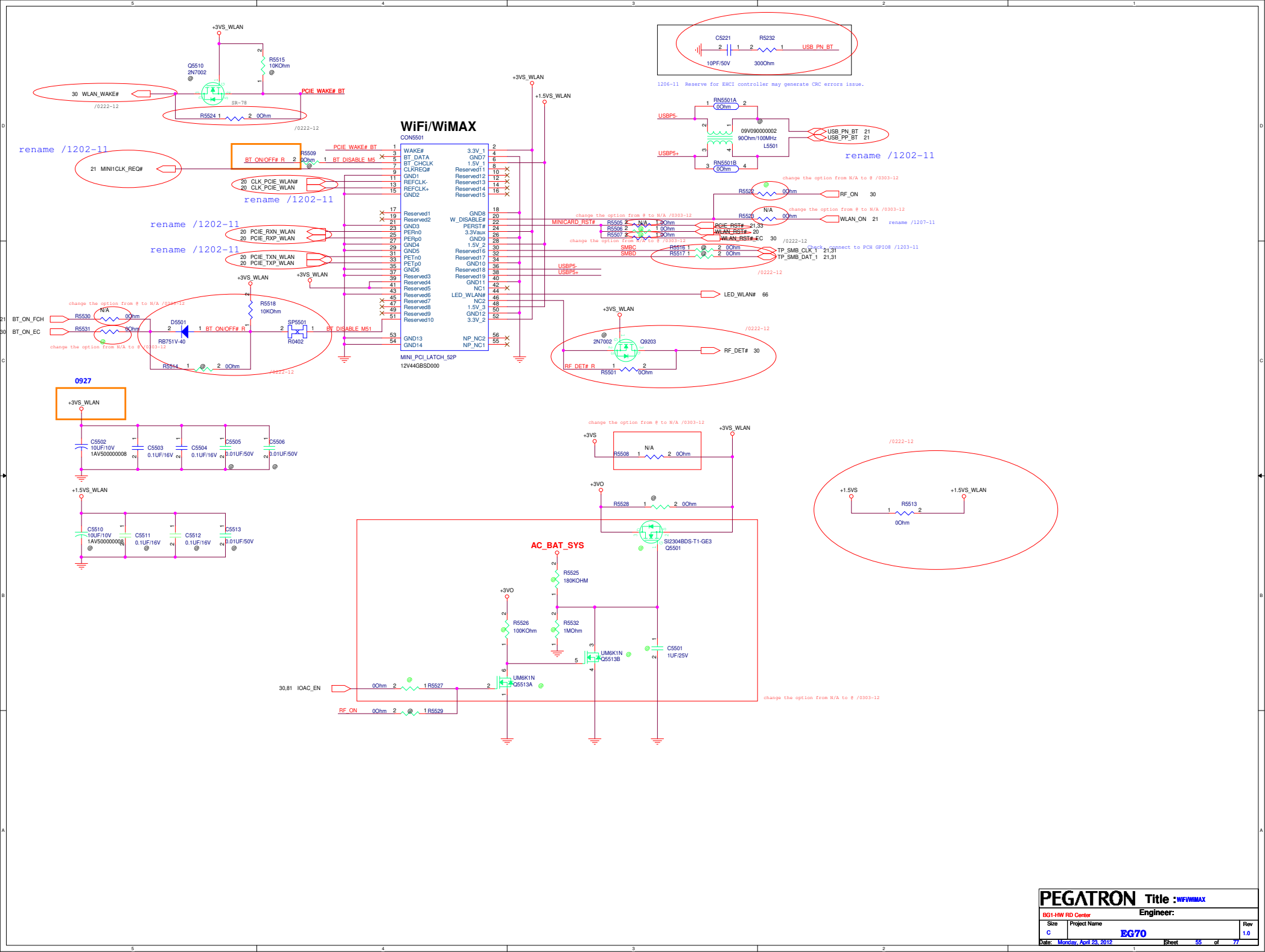
PEGATRON	Title : FAN_Fan,Sensor	
	Engineer: Eric_Chung	
Size: B	Project Name: EG70	Rev: 1.1
Date: Monday, April 23, 2012	Sheet 50 of 99	

PEGATRON Title : Mini Card HSDPA

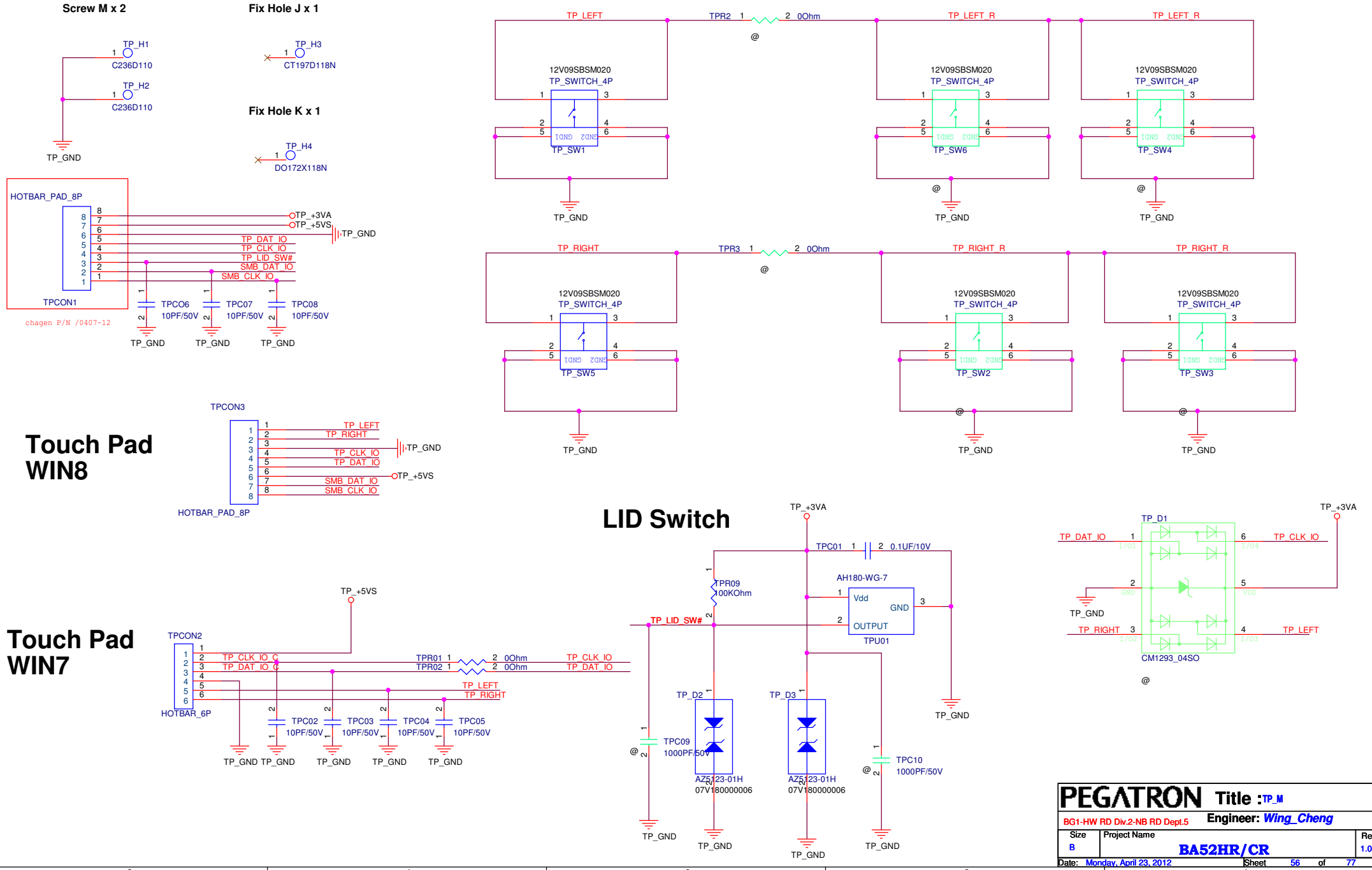
BG1-HW RD Center Engineer: Eric_Chung

Size	Project Name	Rev
Custom	EG70	1.1

Date: Monday, April 23, 2012 Sheet 54 of 99

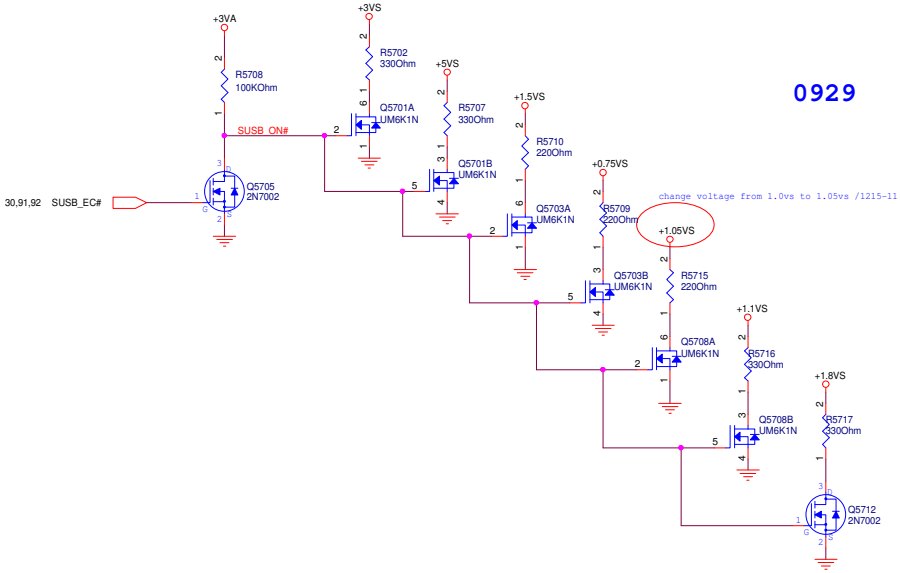


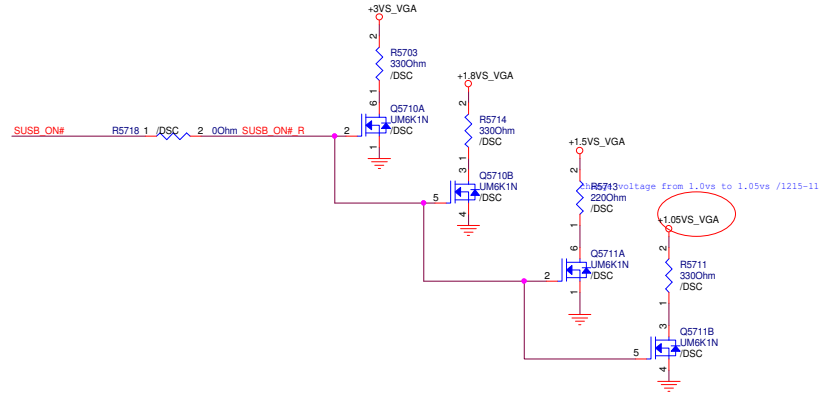
PEGATRON	Title : WiFi/WiMAX		
BG1-HW RD Center	Engineer:		
Size: C	Project Name: EG70		Rev: 1.0
Date: Monday, April 23, 2012	Sheet 55 of 77		

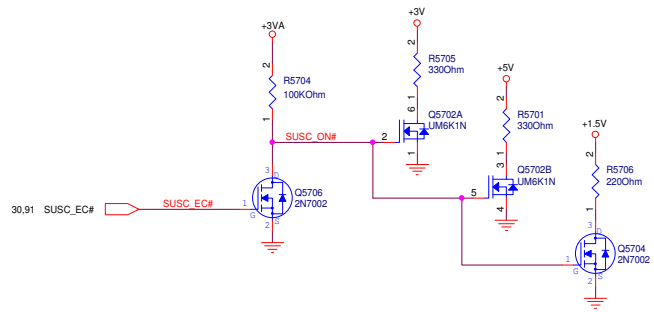

Screw M x 2
TP_H1
C236D110
TP_H2
C236D110
TP_GND
Fix Hole J x 1
TP_H3
CT197D118N
Fix Hole K x 1
TP_H4
DO172X118N
HOTBAR_PAD_8P
TP_+3VA
TP_+5VS
TP_GND
TP_DAT_IO
TP_CLK_IO
TP_LID_SW#
SMB_DAT_IO
SMB_CLK_IO
TPCON1
chagen P/N /0407-12
TPCO6
10PF/50V
TPC07
10PF/50V
TPC08
10PF/50V
TP_LEFT
TPR2 0Ohm
TP_LEFT_R
TP_LEFT_R
12V09SBSM020
TP_SWITCH_4P
TP_SW1
TP_SW6
TP_SW4
TP_RIGHT
TPR3 0Ohm
TP_RIGHT_R
TP_RIGHT_R
TP_SW5
TP_SW2
TP_SW3
Touch Pad
WIN8
TPCON3
TP_LEFT
TP_RIGHT
TP_CLK_IO
TP_DAT_IO
SMB_DAT_IO
SMB_CLK_IO
HOTBAR_PAD_8P
Touch Pad
WIN7
TPCON2
TP_CLK_IO_C
TP_DAT_IO_C
TPR01 0Ohm
TPR02 0Ohm
HOTBAR_6P
TPC02
10PF/50V
TPC03
10PF/50V
TPC04
10PF/50V
TPC05
10PF/50V
LID Switch
TPC01 0.1UF/10V
TPR09
100KOhm
AH180-WG-7
Vdd
GND
OUTPUT
TPU01
TP_D2
TP_D3
TPC09
1000PF/50V
TPC10
1000PF/50V
AZ5123-01H
07V180000006
TP_D1
CM1293_04SO
PEGATRON
Title :TP_M
BG1-HW RD Div.2-NB RD Dept.5
Engineer: Wing_Cheng
Size
B
Project Name
BA52HR/CR
Rev
1.0
Date: Monday, April 23, 2012
Sheet 56 of 77

Discharge Circuit

0929



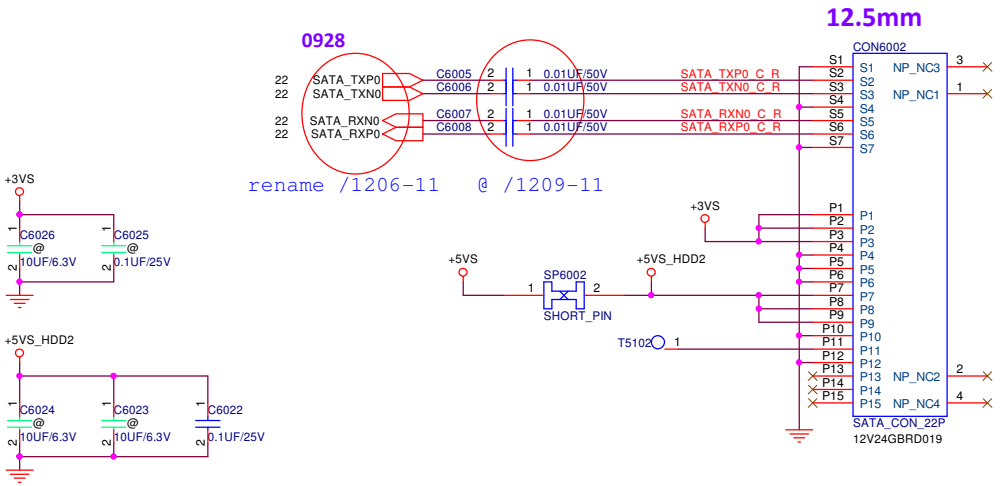




PEGATRON	Title : DISCHARGE CKT	
BG1-HW RD Center	Engineer: Eric_Chung	
Size: Custom	Project Name: EG70	Rev: 1.1
Date: Monday, April 23, 2012	Sheet 57 of 99	

HDD 1 (Reserve)

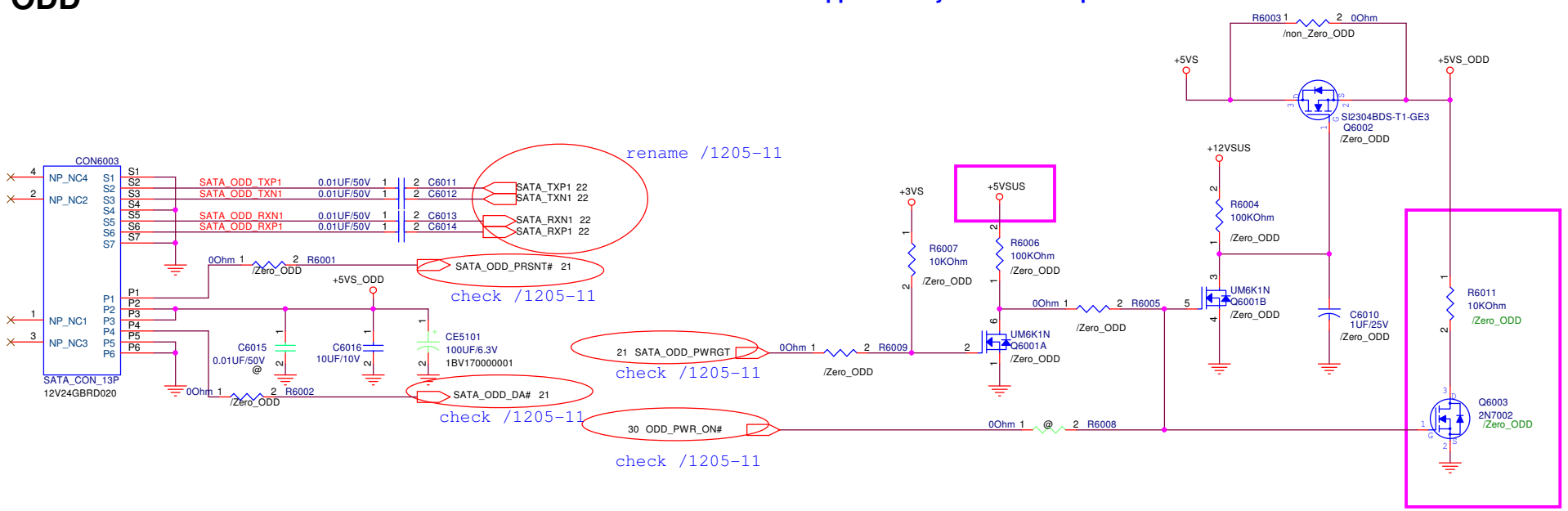
HDD 2 (Main)



ODD

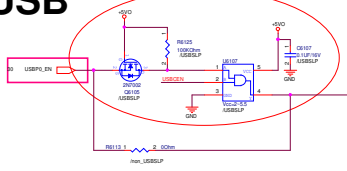
ZERO POWER ODD SUPPORT

support Hokey turn off ODD power

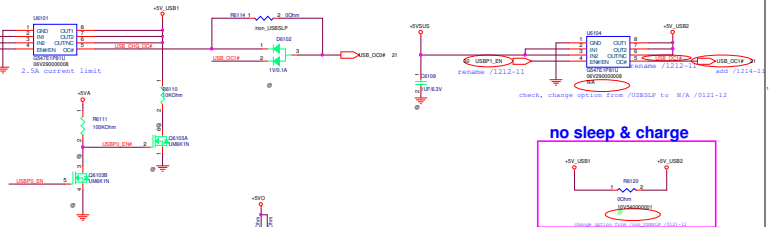


PEGATRON	Title : SATA HDD/ ODD	
BG1-HW RD Center	Engineer: Eric_Chung	
Size: Custom	Project Name: EG70	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 60 of 99	

MB USB



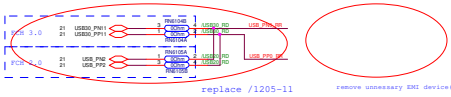
turn on +5VSUS in DC mode condition



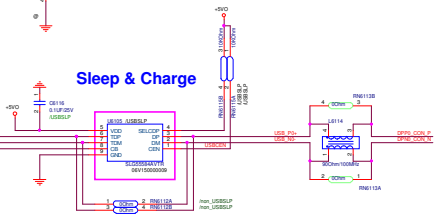
no sleep & charge

USB 3.0 (USB 2.0 colay) ports x 1 (Right Down)

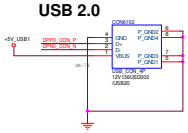
Sleep & Charge

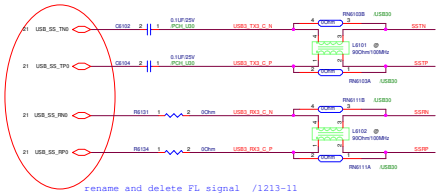


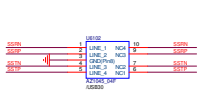
Sleep & Charge



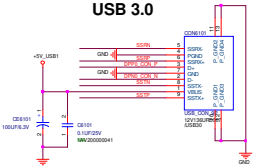
USB 2.0

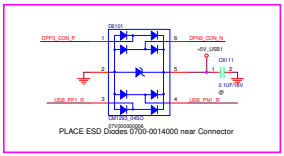




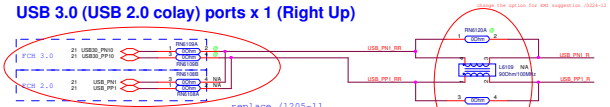


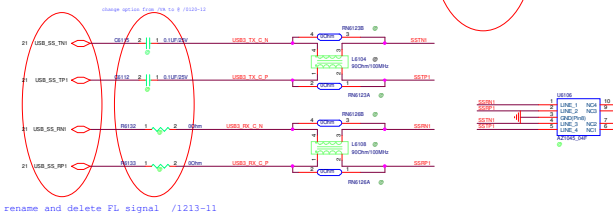
USB 3.0



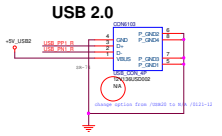


USB 3.0 (USB 2.0 colay) ports x 1 (Right Up)

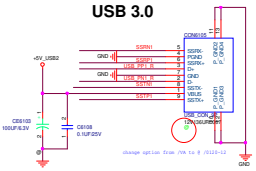


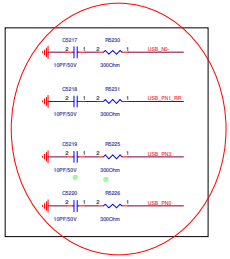


USB 2.0



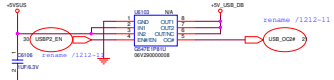
USB 3.0



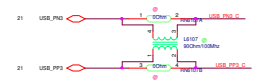


IO Board

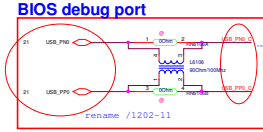
USB Power Switch for USB DB Main



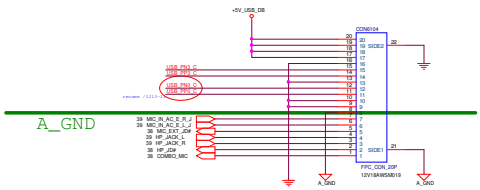
USB 2.0 port x2 (Left Up)



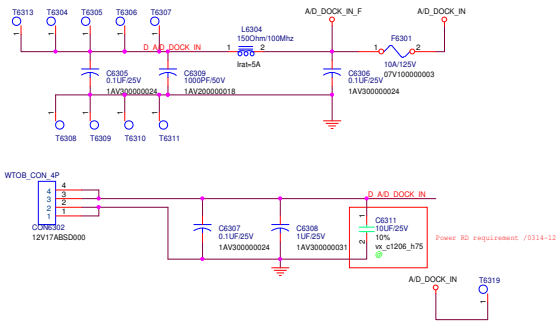
BIOS debug port



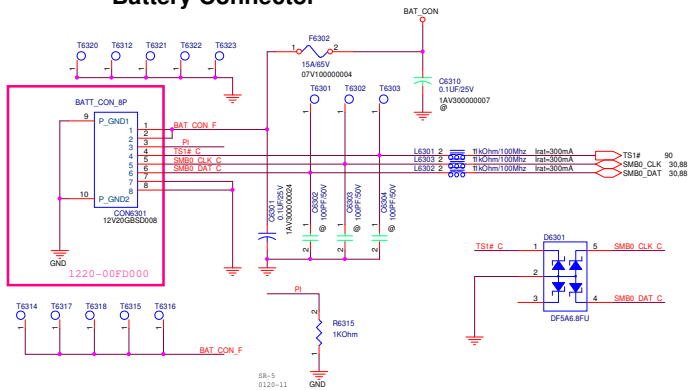
AUDIO BOARD / USB 2.0 port x2



DC IN

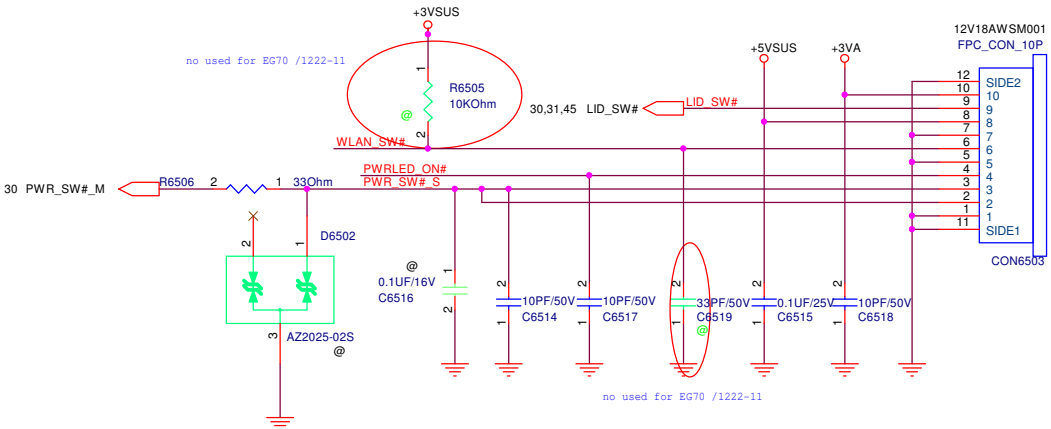


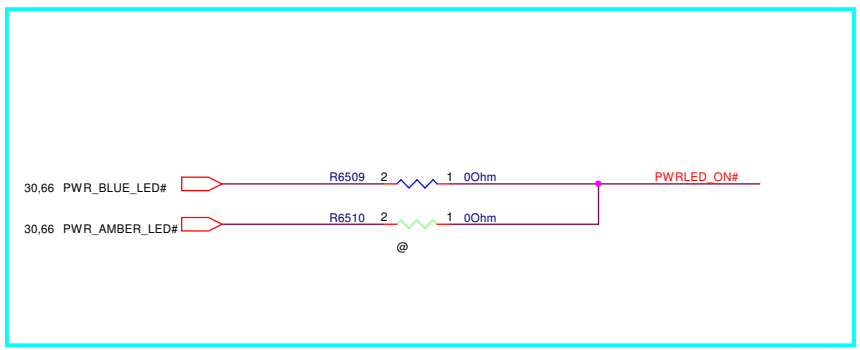
Battery Connector



PEGATRON	Title : DC-IN DISCHARGE		
BG1-HW RD Center	Engineer: Eric_Chung		
Size: Custom	Project Name: EG70		Rev: 1.0
Date: Monday, April 23, 2012	Sheet 63 of 99		

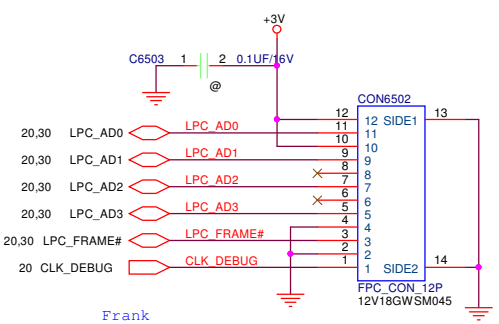
PWR BRD/ AMBIENT/ HALL CONN.





change Power LED CON6503 circuit

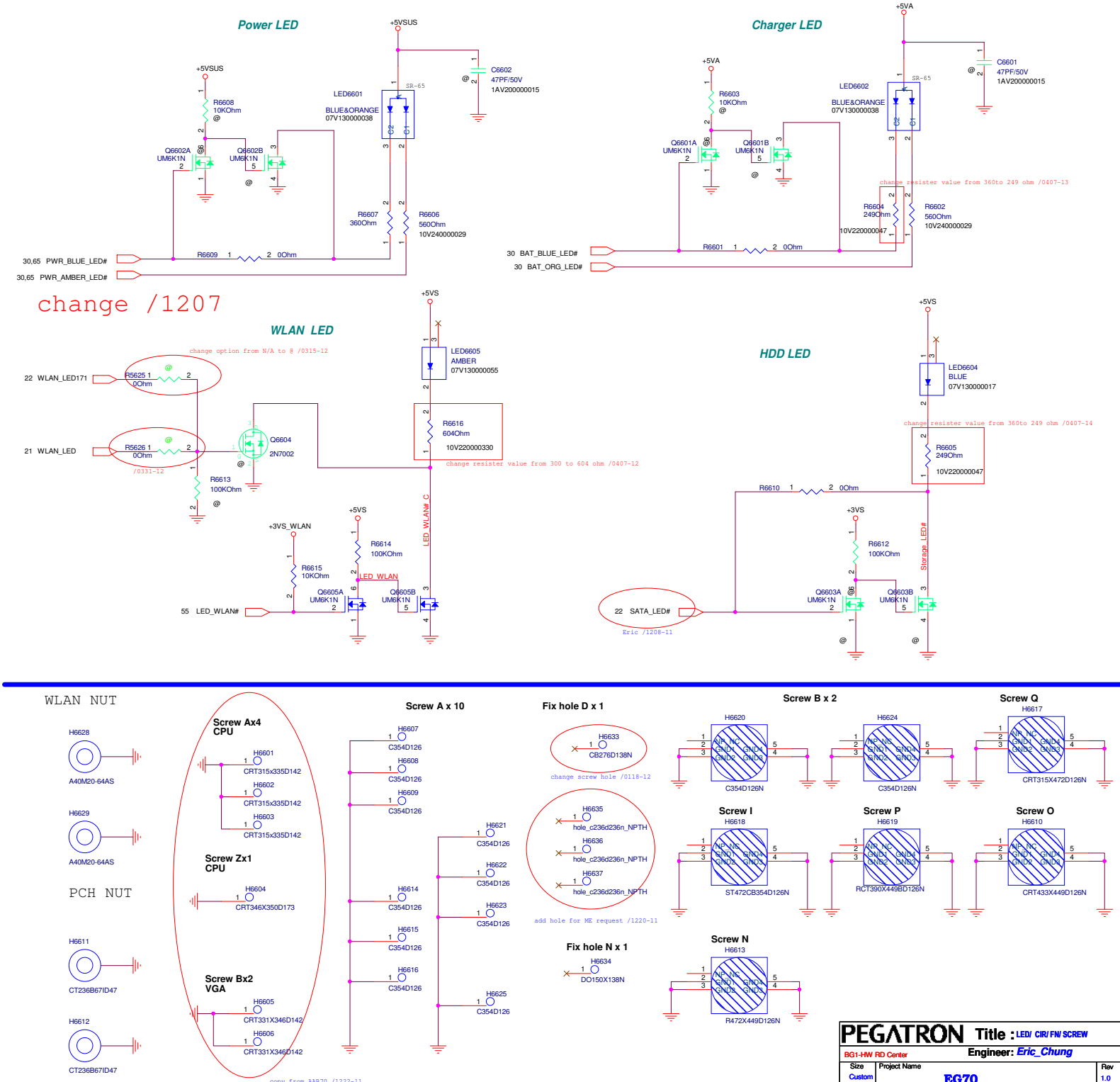
DEBUG CARD CONN.



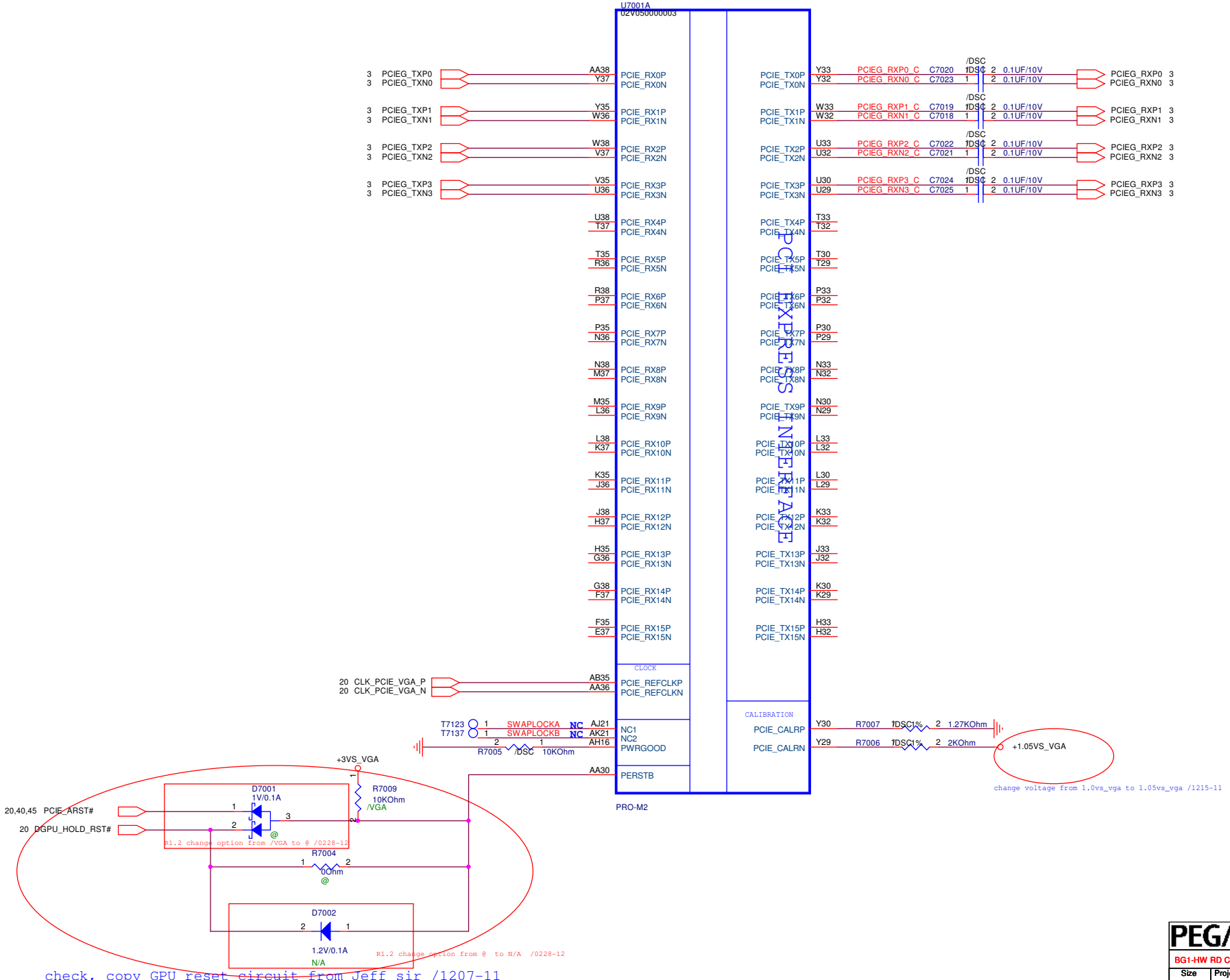
Frank
0425_modify Debug port
(add EXT_SMI#_C and INT_SERIRQ_C)

CR R1.0 change part for EOL. Joyoung0803
PS. Pin define is reverse.

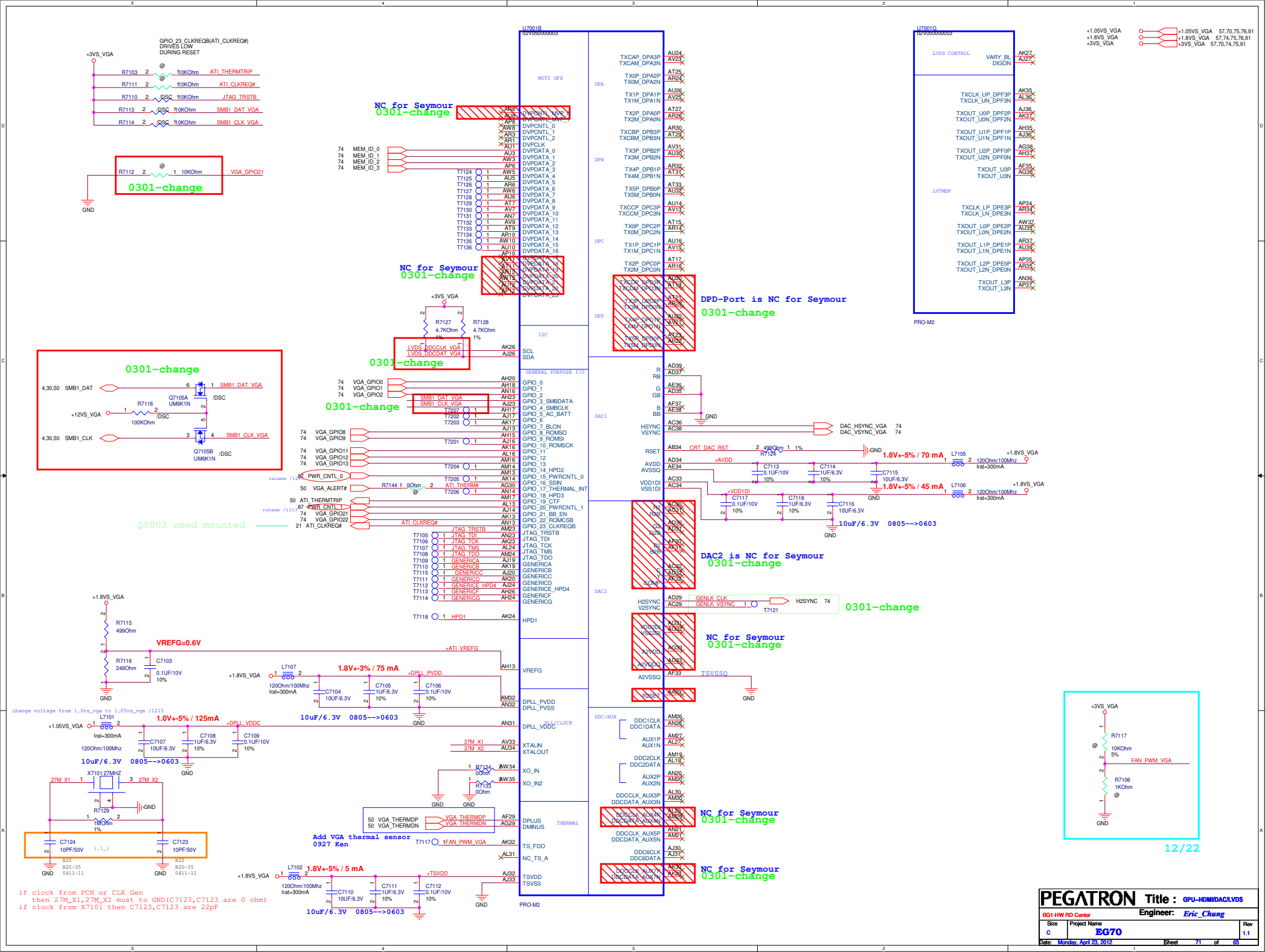
PEGATRON	Title : MDC/ PWR SW/ Debug	
BG1-HW RD Center	Engineer: Eric_Chung	
Size: Custom	Project Name: EG70	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 65 of 99	


Power LED
+5VSUS
R6608
10KOhm
LED6601
BLUE&ORANGE
07V130000038
SR-65
C6602
47PF/50V
1AV200000015
Q6602A
UM6K1N
Q6602B
UM6K1N
R6607
360Ohm
R6606
560Ohm
10V240000029
30,65 PWR_BLUE_LED#
30,65 PWR_AMBER_LED#
R6609 1 2 0Ohm
Charger LED
+5VA
R6603
10KOhm
LED6602
BLUE&ORANGE
07V130000038
SR-65
C6601
47PF/50V
1AV200000015
Q6601A
UM6K1N
Q6601B
UM6K1N
change resister value from 360to 249 ohm /0407-13
R6604
249Ohm
10V220000047
R6602
560Ohm
10V240000029
30 BAT_BLUE_LED#
30 BAT_ORG_LED#
R6601 1 2 0Ohm
change /1207
WLAN LED
change option from N/A to @ /0315-12
22 WLAN_LED171
R5625 1
0Ohm
21 WLAN_LED
R5626 1
0Ohm
/0331-12
Q6604
2N7002
R6613
100KOhm
+5VS
LED6605
AMBER
07V130000055
R6616
604Ohm
10V220000330
change resister value from 300 to 604 ohm /0407-12
+3VS_WLAN
R6615
10KOhm
R6614
100KOhm
LED_WLAN
LED_WLAN# C
Q6605A
UM6K1N
Q6605B
UM6K1N
55 LED_WLAN#
HDD LED
+5VS
LED6604
BLUE
07V130000017
change resister value from 360to 249 ohm /0407-14
R6605
249Ohm
10V220000047
R6610 1 2 0Ohm
+3VS
R6612
100KOhm
Storage_LED#
Q6603A
UM6K1N
Q6603B
UM6K1N
22 SATA_LED#
Eric /1208-11
WLAN NUT
H6628
A40M20-64AS
H6629
A40M20-64AS
PCH NUT
H6611
CT236B67ID47
H6612
CT236B67ID47
Screw Ax4
CPU
H6601
CRT315x335D142
H6602
CRT315x335D142
H6603
CRT315x335D142
Screw Zx1
CPU
H6604
CRT346X350D173
Screw Bx2
VGA
H6605
CRT331X346D142
H6606
CRT331X346D142
copy from AAB70 /1222-11
Screw A x 10
H6607
C354D126
H6608
C354D126
H6609
C354D126
H6614
C354D126
H6615
C354D126
H6616
C354D126
H6621
C354D126
H6622
C354D126
H6623
C354D126
H6625
C354D126
Fix hole D x 1
H6633
CB276D138N
change screw hole /0118-12
H6635
hole_c236d236n_NPTH
H6636
hole_c236d236n_NPTH
H6637
hole_c236d236n_NPTH
add hole for ME request /1220-11
Fix hole N x 1
H6634
DO150X138N
Screw B x 2
H6620
C354D126N
H6624
C354D126N
Screw Q
H6617
CRT315X472D126N
Screw I
H6618
ST472CB354D126N
Screw P
H6619
RCT390X449BD126N
Screw O
H6610
CRT433X449D126N
Screw N
H6613
R472X449D126N
PEGATRON
Title : LED/ CIR/ FN/ SCREW
BG1-HW RD Center
Engineer: Eric_Chung
Size
Custom
Project Name
EG70
Rev
1.0
Date: Monday, April 23, 2012
Sheet 66 of 99

R 1.1 /0301 Seymour XT/M2

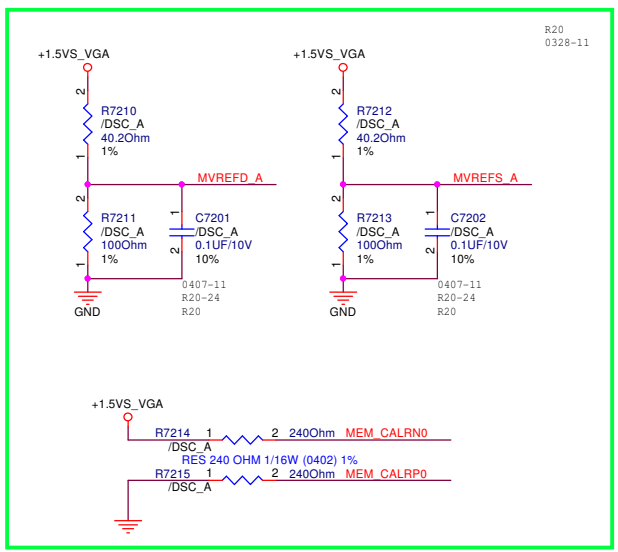


PEGATRON	Title :	GPU-PCIE
BG1-HW RD Center	Engineer:	Eric_Chung
Size: Custom	Project Name: EG70	Rev: 1.1
Date: Monday, April 23, 2012	Sheet 70 of 99	

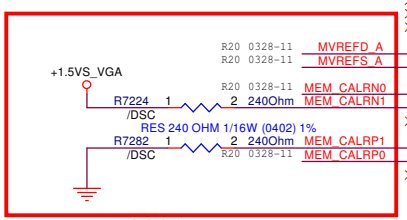

GPIO_23_CLKREQB(ATI_CLKREQ#)
DRIVES LOW
DURING RESET
+3VS_VGA
R7103 10KOhm ATI_THERMTRIP
R7111 10KOhm ATI_CLKREQ#
R7110 /DSC 10KOhm JTAG_TRSTB
R7113 /DSC 10KOhm SMB1_DAT_VGA
R7114 /DSC 10KOhm SMB1_CLK_VGA
R7112 10KOhm VGA_GPIO21
0301-change
GND
U7001B
MUT1 GFX
NC for Seymour
0301-change
DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
MEM_ID_0
MEM_ID_1
MEM_ID_2
MEM_ID_3
DPA
DPB
DPC
DPD
DPD-Port is NC for Seymour
0301-change
I2C
SCL
SDA
LVDS_DDCCLK_VGA
LVDS_DDCDAT_VGA
GENERAL PURPOSE I/O
GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
VGA_GPIO0
VGA_GPIO1
VGA_GPIO2
SMB1_DAT_VGA
SMB1_CLK_VGA
VGA_GPIO8
VGA_GPIO9
VGA_GPIO11
VGA_GPIO12
VGA_GPIO13
PWR_CNTL_0
VGA_ALERT#
ATI_THERMTRIP
PWR_CNTL_1
VGA_GPIO21
VGA_GPIO22
ATI_CLKREQ#
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
GENERICF
GENERICG
HPD1
Q5003 need mounted
DAC1
DAC2
DAC2 is NC for Seymour
0301-change
R
RB
G
GB
B
BB
HSYNC
VSYNC
DAC_HSYNC_VGA
DAC_VSYNC_VGA
RSET
CRT_DAC_RST
AVDD
AVSSQ
VDD1DI
VSS1DI
+AVDD
+VDD1DI
1.8V+-5% / 70 mA
1.8V+-5% / 45 mA
10uF/6.3V 0805-->0603
H2SYNC
V2SYNC
GENLK_CLK
GENLK_VSYNC
H2SYNC
NC for Seymour
0301-change
TSVSSQ
R2SET
DDC/AUX
DDC1CLK
DDC1DATA
AUX1P
AUX1N
DDC2CLK
DDC2DATA
AUX2P
AUX2N
DDCCLK_AUX3P
DDCDATA_AUX3N
DDCCLK_AUX4P
DDCDATA_AUX4N
DDCCLK_AUX5P
DDCDATA_AUX5N
DDC6CLK
DDC6DATA
DDCCLK_AUX7P
DDCDATA_AUX7N
PLL/CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
XTALIN
XTALOUT
XO_IN
XO_IN2
THERMAL
VGA_THERMDP
VGA_THERMDN
Add VGA thermal sensor
0927 Ken
TS_FDO
NC_TS_A
TSVDD
TSVSS
VREFG
VREFG=0.6V
+ATI_VREFG
1.8V+-3% / 75 mA
+DPLL_PVDD
1.0V+-5% / 125mA
+DPLL_VDDC
27M_X1
27M_X2
X7101 27MHZ
+TSVDD
1.8V+-5% / 5 mA
FAN_PWM_VGA
change voltage from 1.0vs_vga to 1.05vs_vga /1215
if clock from PCH or CLK Gen
then 27M_X1,27M_X2 must to GND(C7123,C7123 are 0 ohm)
if clock from X7101 then C7123,C7123 are 22pF
PRO-M2
U7001G
LVDS CONTROL
VARY_BL
DIGON
LVTMDP
PRO-M2
+1.05VS_VGA 57,70,75,76,91
+1.8VS_VGA 57,74,75,76,91
+3VS_VGA 57,70,74,75,91
R7117 10KOhm 5% FAN_PWM_VGA
R7106 1KOhm
12/22
PEGATRON
Title : GPU-HDMI/DAC/LVDS
BG1-HW RD Center
Engineer: Eric_Chung
Size C
Project Name EG70
Rev 1.1
Date: Monday, April 23, 2012
Sheet 71 of 65

The all balls are NC except N12 /M12 for seymour

Reserve,Unmount



The all balls are NC except N12 /M12 for seymour



0301-change

U7001C 02V050000003

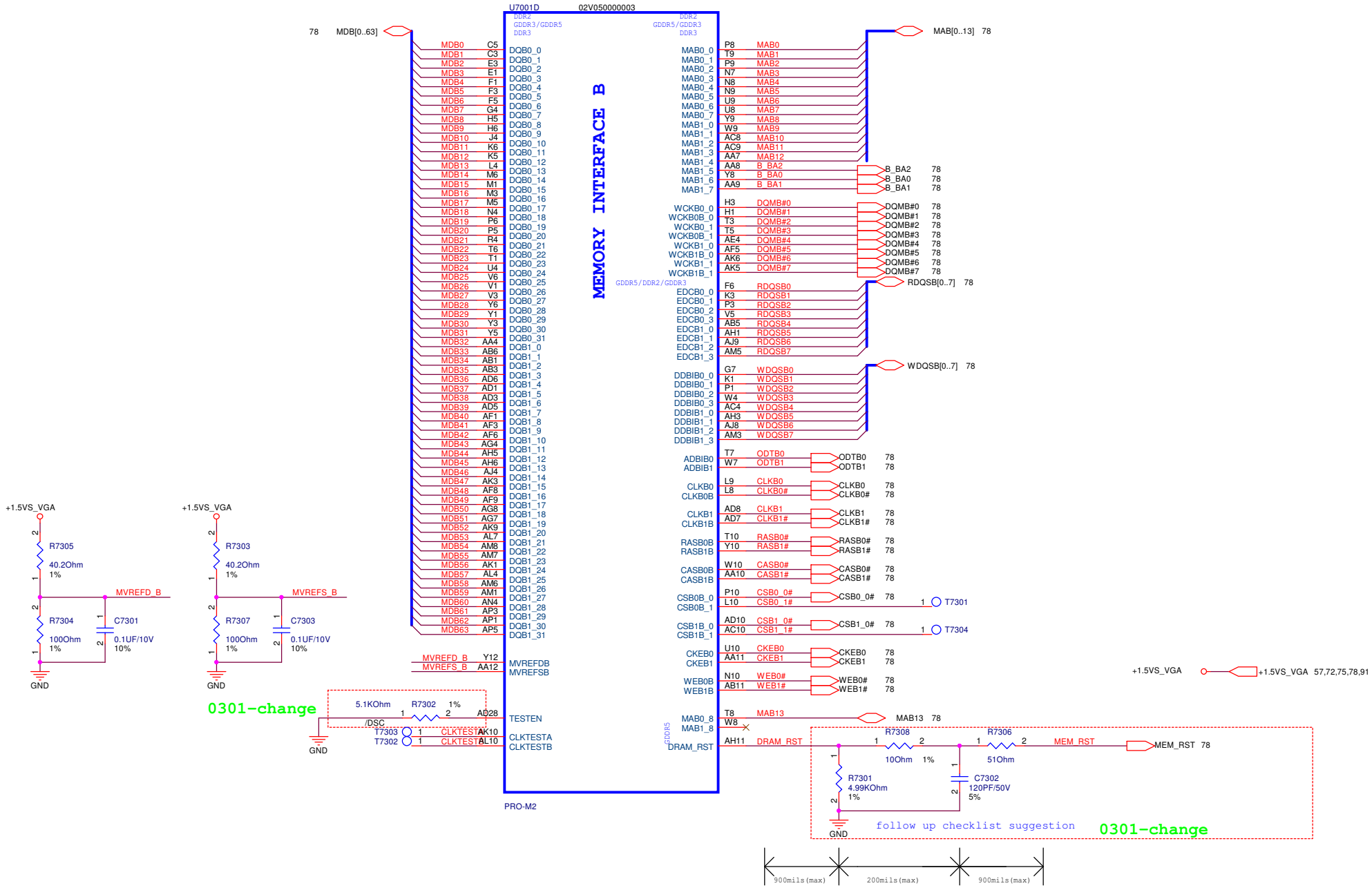
MEMORY INTERFACE A

C37	DQA0_0	MAA0_0	G24
C35	DQA0_1	MAA0_1	J23
A35	DQA0_2	MAA0_2	H24
E34	DQA0_3	MAA0_3	J24
G32	DQA0_4	MAA0_4	H26
D33	DQA0_5	MAA0_5	J26
F32	DQA0_6	MAA0_6	H21
E32	DQA0_7	MAA0_7	G21
D31	DQA0_8	MAA1_0	H19
F30	DQA0_9	MAA1_1	H20
C30	DQA0_10	MAA1_2	L13
A30	DQA0_11	MAA1_3	G16
F28	DQA0_12	MAA1_4	J16
C28	DQA0_13	MAA1_5	H16
A28	DQA0_14	MAA1_6	J17
E28	DQA0_15	MAA1_7	H17
D27	DQA0_16		
F26	DQA0_17	WCKA0_0	A32
C26	DQA0_18	WCKA0B_0	C32
A26	DQA0_19	WCKA0_1	D23
F24	DQA0_20	WCKA0B_1	E22
C24	DQA0_21	WCKA1_0	C14
A24	DQA0_22	WCKA1B_0	A14
E24	DQA0_23	WCKA1_1	E10
C22	DQA0_24	WCKA1B_1	D9
A22	DQA0_25	GDDR5/DDR2/GDDR3	
F22	DQA0_26	EDCA0_0	C34
D21	DQA0_27	EDCA0_1	D29
A20	DQA0_28	EDCA0_2	D25
F20	DQA0_29	EDCA0_3	E20
D19	DQA0_30	EDCA1_0	E16
E18	DQA0_31	EDCA1_1	E12
C18	DQA1_0	EDCA1_2	J10
A18	DQA1_1	EDCA1_3	D7
F18	DQA1_2		
D17	DQA1_3	DDBIA0_0	A34
A16	DQA1_4	DDBIA0_1	E30
F16	DQA1_5	DDBIA0_2	E26
D15	DQA1_6	DDBIA0_3	C20
E14	DQA1_7	DDBIA1_0	C16
F14	DQA1_8	DDBIA1_1	C12
D13	DQA1_9	DDBIA1_2	J11
F12	DQA1_10	DDBIA1_3	F8
A12	DQA1_11		
D11	DQA1_12	ADBIA0	J21
F10	DQA1_13	ADBIA1	G19
A10	DQA1_14		
C10	DQA1_15	CLKA0	H27
G13	DQA1_16	CLKA0B	G27
H13	DQA1_17		
J13	DQA1_18	CLKA1	J14
H11	DQA1_19	CLKA1B	H14
G10	DQA1_20		
G8	DQA1_21	RASA0B	K23
K9	DQA1_22	RASA1B	K19
K10	DQA1_23		
G9	DQA1_24	CASA0B	K20
A8	DQA1_25	CASA1B	K17
C8	DQA1_26		
E8	DQA1_27	CSA0B_0	K24
A6	DQA1_28	CSA0B_1	K27
C6	DQA1_29		
E6	DQA1_30	CSA1B_0	M13
A5	DQA1_31	CSA1B_1	K16
L18	MVREFDA	CKEA0	K21
L20	MVREFSA	CKEA1	J20
L27			
N12	MEM_CALRN0	WEA0B	K26
AG12	MEM_CALRN1	WEA1B	L15
	MEM_CALRN2		
M12			
M27	MEM_CALRP1	MAA0_8	H23
AH12	MEM_CALRP0	MAA1_8	J19
	MEM_CALRP2		

GDDR5

PRO-M2

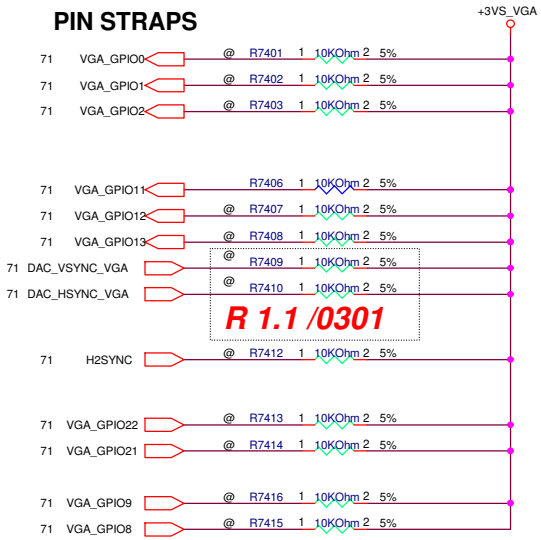
PEGATRON	Title :	GPU-MEM_CTRL_CHA
BG1-HW RD Center	Engineer:	Eric_Chung
Size: Custom	Project Name: EG70	Rev: 1.1
Date: Monday, April 23, 2012	Sheet 72 of 99	



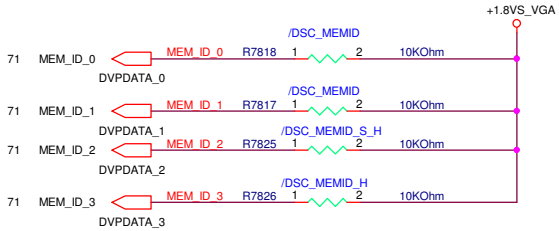
PEGATRON	Title :	GPU-MEM_CTRL_CHB
BG1-HW RD Center	Engineer:	Eric_Chung
Size: Custom	Project Name: EG70	Rev: 1.1
Date: Monday, April 23, 2012	Sheet 73 of 99	

GPIO21 MUST BE LOW DURING PERSTB WHEN BEING USED TO CONTROL MVDDQ

PIN STRAPS



VRAM size define by VBIOS



Seymour Straps

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing This setting can only be used if the PCIE bus design meets the "Low Loss interconnect" requirements.	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled MXM and add-in boards	0 (internal pull-down)
BIF_GEN2_EN_A	GPIO2	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0
VGA_DIS	GPIO9	0 - VGA Controller capacity enabled 1 - The device will not be recognized as the system's VGA controller	0 (internal pull-down)
ROMIDCFG(2:0)	GPIO(13:11)	If BIOS_ROM_EN=1,then Config[2:0]defines the ROM type. If BIOS_ROM_EN=0,then Config[2:0]deifnes the primary memoru apeture size. 128MB---000 32MB---Not Support 2GB---Not Support 256MB---001 512MB--Not Support 4GB---Not Support 64MB---010 1GB-----Not Support	0000 (internal pull-down)
BIOS_ROM_EN	GPIO22_ROMCSB	Enable external BIOS ROM device 0-Disable external BIOS ROM device 1-Enable external BIOS ROM device	0 (internal pull-down)
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0]: 00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected; 10: Audio for DisplayPort only; 11: Audio for both DisplayPort and HDMI.	0 (internal pull-down)
Reserved	GENLK_CLK GPIO_21_BB_EN GPIO8	ATI internal use only . THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET.	0 (internal pull-down)

Seymour XT:

Memory ID Board Straps

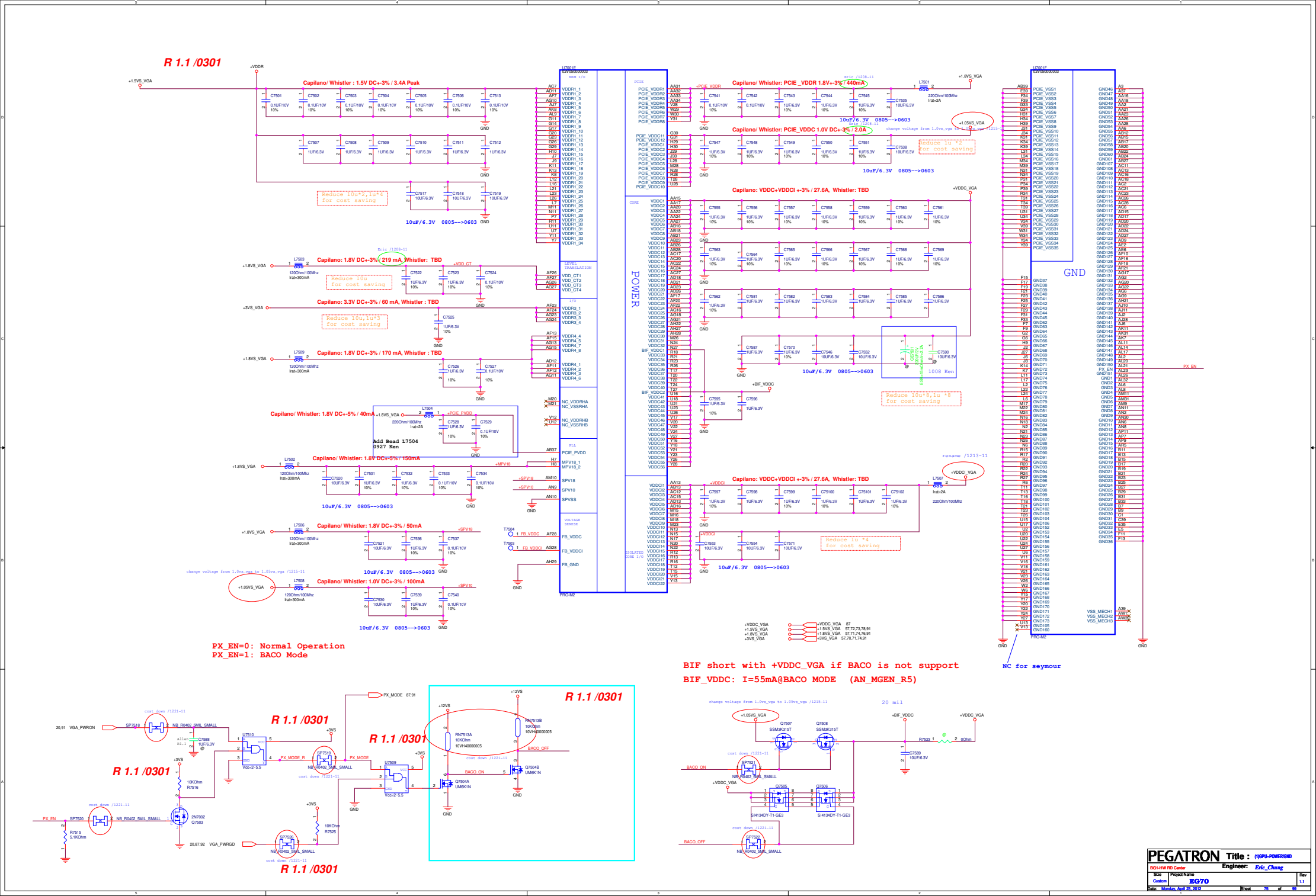
Vendor	DVPDATA(3,2,1,0)	ID	DDR3 Memory Type	VRAM Vendor Part
Hynix	0000	0	64M*16*4 pcs(512MB)	H5TQ1G63BFR-12 (1600Mbps)
	0001	1	64M*16*4 pcs(512MB)	H5TQ1G63DFR-12C (1600Mbps)
	0010	2	128M*16*4 pcs(1GB)	H5TQ2G63DFR-11C (1800Mbps) 0315-00UD0PB
	0011	3	128M*16*4 pcs(1GB)	H5TQ2G63BFR-11C LF (1800Mbps) 0315-00ND0PB
	0100	4		
	0101	5		
	0110	6		
	0111	7		
Samsung	1000	8	64M*16*4 pcs(512MB)	K4W1G1646E-HC12 (1600Mbps)
	1001	9	64M*16*4 pcs(512MB)	K4W1G1646G-BC12 (1600Mbps)
	1010	10	128M*16*4 pcs(1GB)	K4W2G1646C-HC12 (1600Mbps)
	1011	11	128M*16*4 pcs(1GB)	K4W2G1646C-HC11
	1100	12		
	1101	13		
	1110	14		
	1111	15		

PEGATRON Title : GPU-STRAP_MISC

BG1-HW RD Center Engineer: Eric_Chung

Size: Custom | Project Name: EG70 | Rev: 1.1

Date: Monday, April 23, 2012 | Sheet 74 of 99

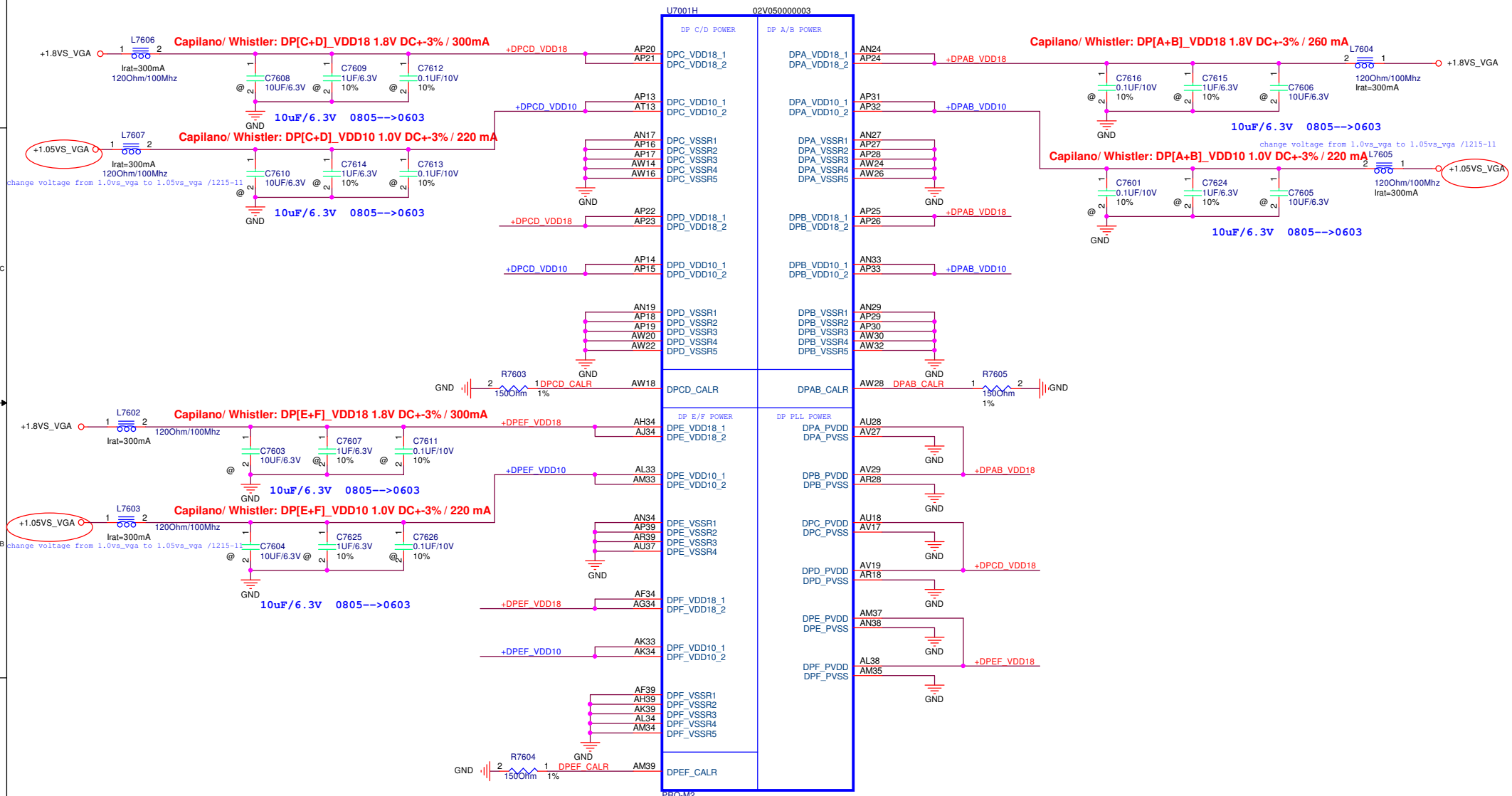

R 1.1 /0301
Capilano/ Whistler : 1.5V DC+-3% / 3.4A Peak
Capilano: 1.8V DC+-3% / 219 mA, Whistler: TBD
Capilano: 3.3V DC+-3% / 60 mA, Whistler : TBD
Capilano: 1.8V DC+-3% / 170 mA, Whistler : TBD
Capilano/ Whistler: 1.8V DC+-5% / 40mA
Capilano/ Whistler: 1.8V DC+-5% / 150mA
Capilano/ Whistler: 1.8V DC+-3% / 50mA
Capilano/ Whistler: 1.0V DC+-3% / 100mA
Capilano/ Whistler: PCIE _VDDR 1.8V+-3% / 440mA
Capilano/ Whistler: PCIE_VDDC 1.0V DC+-3% / 2.0A
Capilano: VDDC+VDDCI +-3% / 27.6A, Whistler: TBD
Capilano: VDDC+VDDCI +-3% / 27.6A, Whistler: TBD
Add Bead L7504 0927 Ken
10uF/6.3V 0805-->0603
Reduce 10u*2,1u*4 for cost saving
Reduce 10u for cost saving
Reduce 10u,1u*3 for cost saving
Reduce 1u *2 for cost saving
Reduce 1u *4 for cost saving
Reduce 10u*8,1u *8 for cost saving
rename /1213-11
change voltage from 1.0vs_vga to 1.05vs_vga /1215-11
PX_EN=0: Normal Operation
PX_EN=1: BACO Mode
BIF short with +VDDC_VGA if BACO is not support
BIF_VDDC: I=55mA@BACO MODE (AN_MGEN_R5)
NC for seymour
POWER
GND
PEGATRON
Title : (1)GPU-POWER/GND
Engineer: Eric_Chang
BG1-HW RD Center
Size: Custom
Project Name: EG70
Rev: 1.1
Date: Monday, April 23, 2012
Sheet 75 of 99

+1.05VS_VGA
+1.8VS_VGA

+1.05VS_VGA 57,70,71,75,91
+1.8VS_VGA 57,71,74,75,91

0301-change

PX with BACO mode all displays are always driven by APU
DPA&DPB share power ;DPC&DPD share power ;DPE&DPF share power



PEGATRON	Title :	(2)GPU-DP POWER	
BG1-HW RD Center	Engineer:	*Eric_Chung*	
Size: Custom	Project Name: EG70		Rev: 1.1
Date: Monday, April 23, 2012	Sheet 76 of 99		

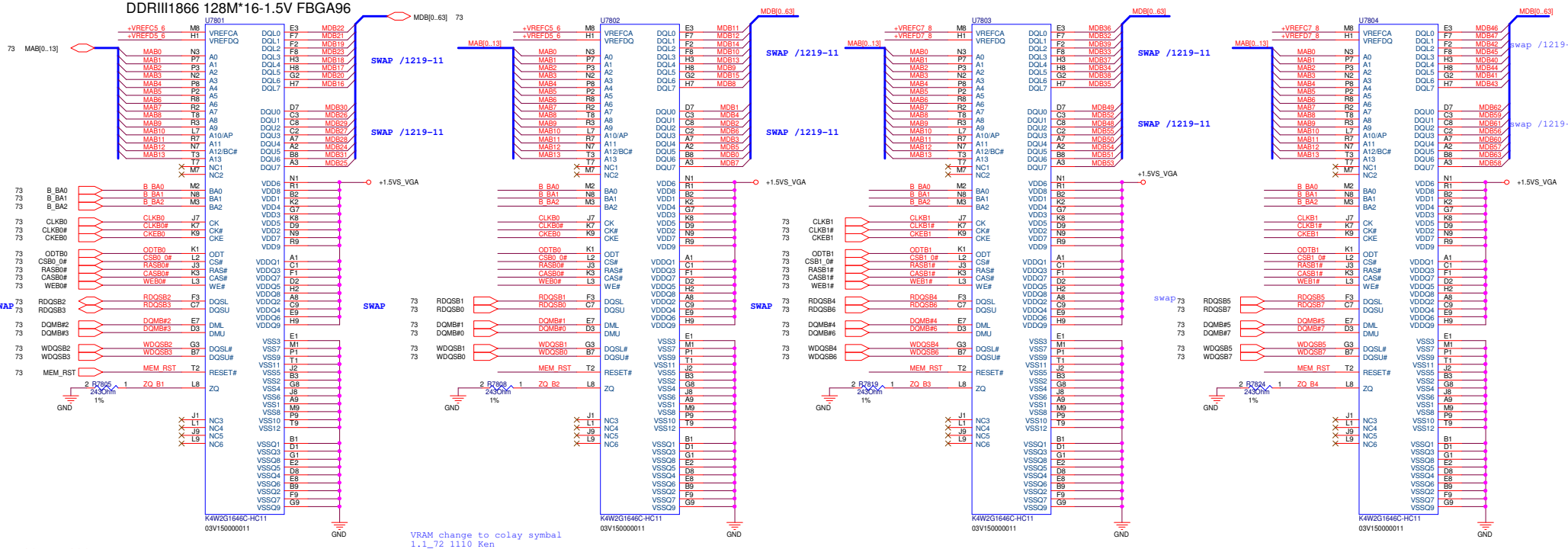
PEGATRON Title : GPU-MEM CHA

BG1-HW RD Center Engineer: Eric_Chung

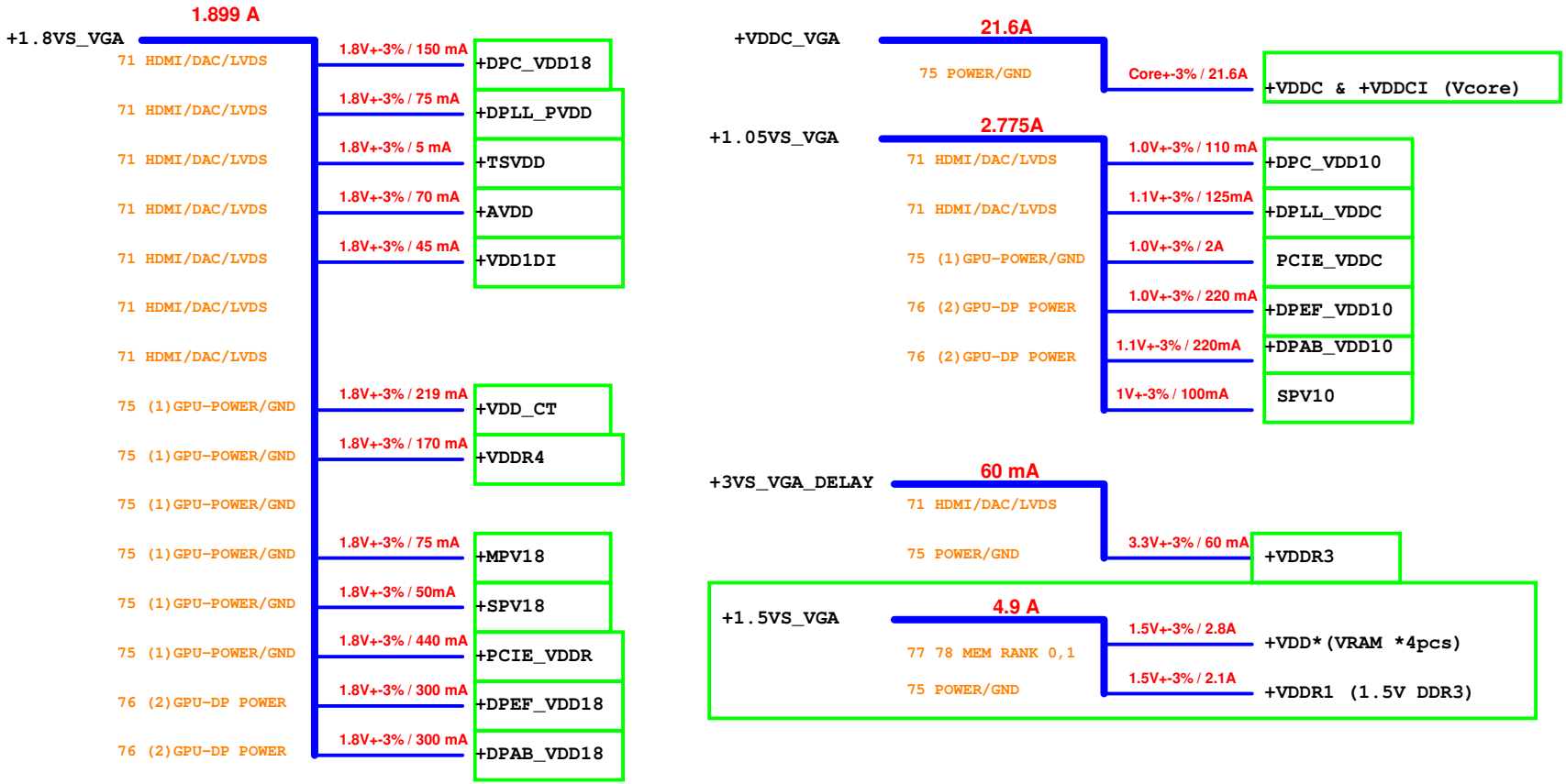
Size	Project Name	Rev
C	EG70	1.1

Date: Monday, April 23, 2012 Sheet 77 of 99

DDRIII1866 128M*16-1.5V FBGA96



PEGATRON	Title : GPU-MEM CHB		
BG1-HW RD Center	Engineer: Eric_Chung		
Size: C	Project Name: EG70		Rev: 1.1
Date: Monday, April 23, 2012	Sheet 78 of 99		



Total:15W (w/o VRAM)

Power Up Sequence :
+VGA_VCORE -> +1.05VS_VGA -> +1.5VS_VGA -> +1.8VS_VGA -> +3VS_VGA_DELAY

Power Down Sequence :
+3VS_VGA_DELAY -> +1.8VS_VGA -> +1.5VS_VGA -> +1.05VS_VGA -> +VGA_VCORE

PEGATRON	Title : ATI_Robson	
BG1-HW RD Center	Engineer: Eric_Chung	
Size: Custom	Project Name: EG70	Rev: 1.1
Date: Monday, April 23, 2012	Sheet 79 of 99	

DSC +VCORE POWER SUPPLY

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V Pre_metal	X	X

VFIXEN VID Codes

SVC	SVD	Output	Pre_metal
0	0	1.4	1.1
0	1	1.2	1.0
1	0	1.0	0.9
1	1	0.8	0.8

SVC	SVD	Output
R8076	R8077	1.4
R8076	R8074	1.2
R8075	R8077	1.0
R8075	R8074	0.8

Change Footprint For Net_IN

<Variant Name>

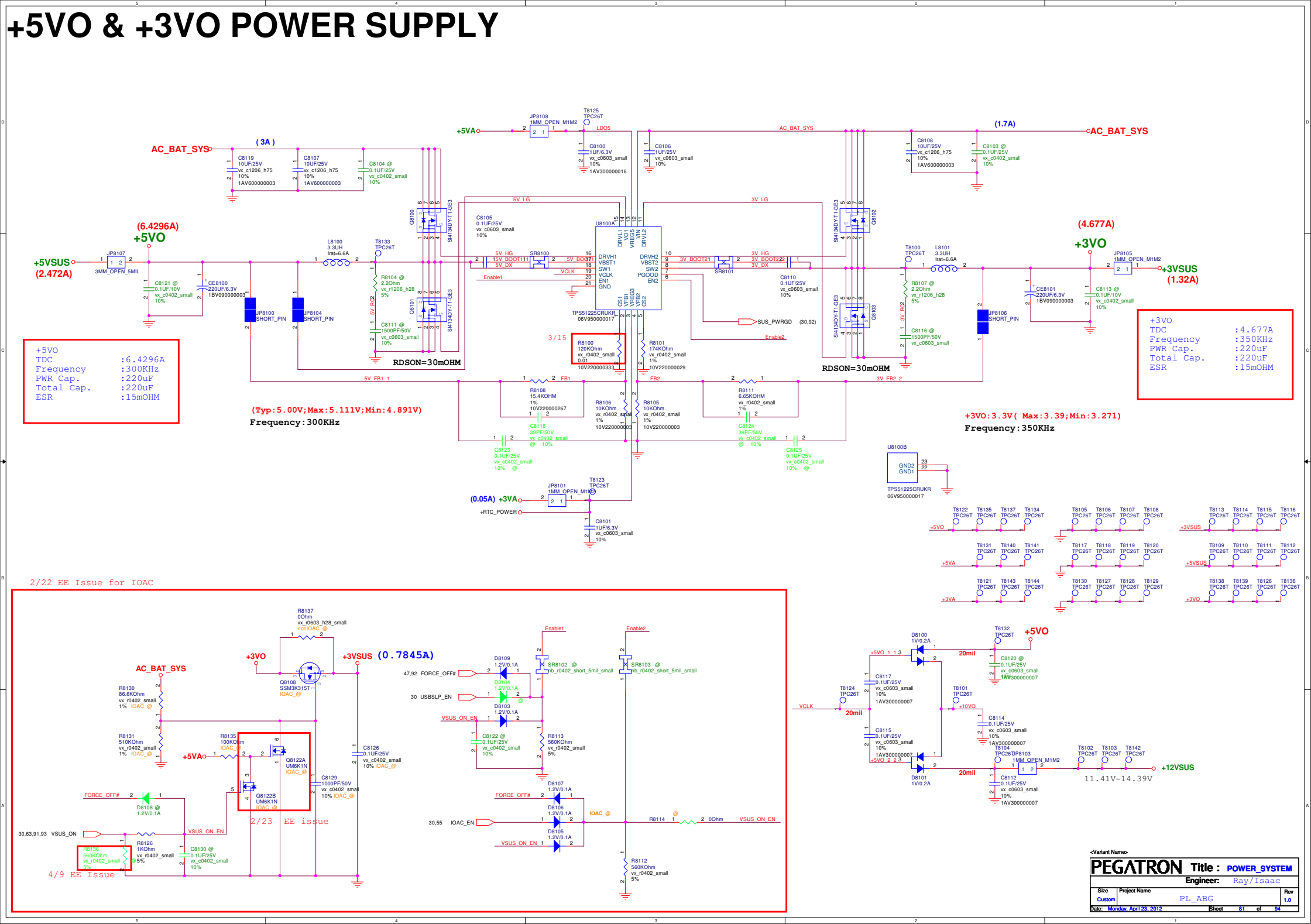
PEGATRON Title : POWER_VCORE

Engineer: Ray/Isaac

Size	Project Name	Rev
C		1.0

Date: Monday, April 23, 2012 Sheet 80 of 94

+5VO & +3VO POWER SUPPLY



2/22 EE Issue for IOAC

<Variant Name>

PEGATRON Title : POWER_SYSTEM

Engineer: Ray/Isaac

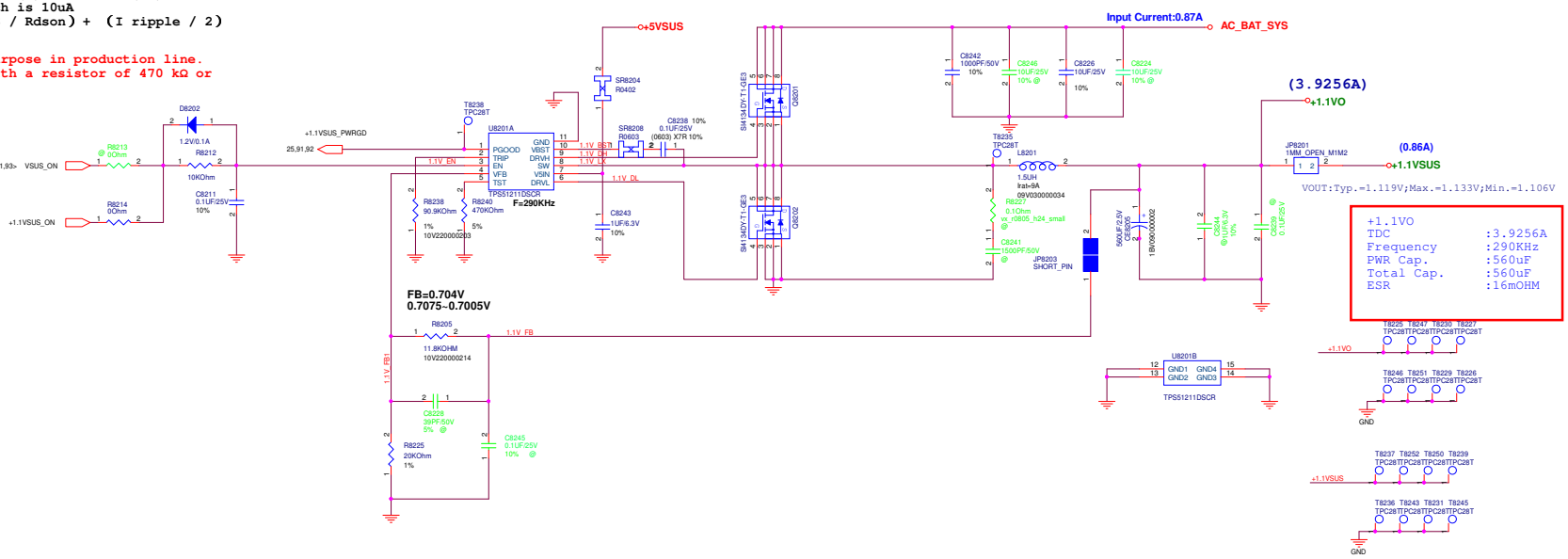
Size	Project Name	Rev
Custom	PL_ABG	1.0

Date: Monday, April 23, 2012 Sheet 81 of 94

+1.0VO&+1.1VO POWER SUPPLY

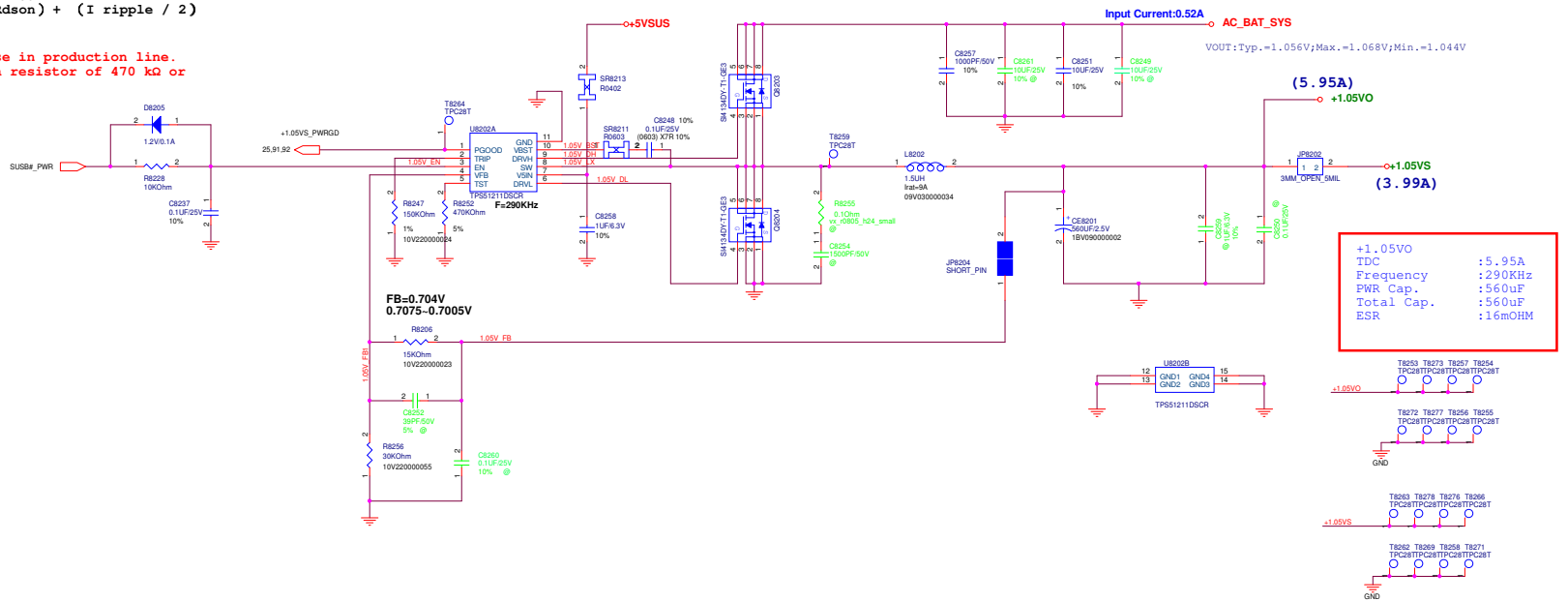
TRIP V (mV) = TRIP R (k) * TRIP I (mA)
TRIPI current, which is 10uA
VOCP = TRIP V / (8 / Rdson) + (I ripple / 2)

Used for testing purpose in production line.
Pull down to GND with a resistor of 470 kΩ or less



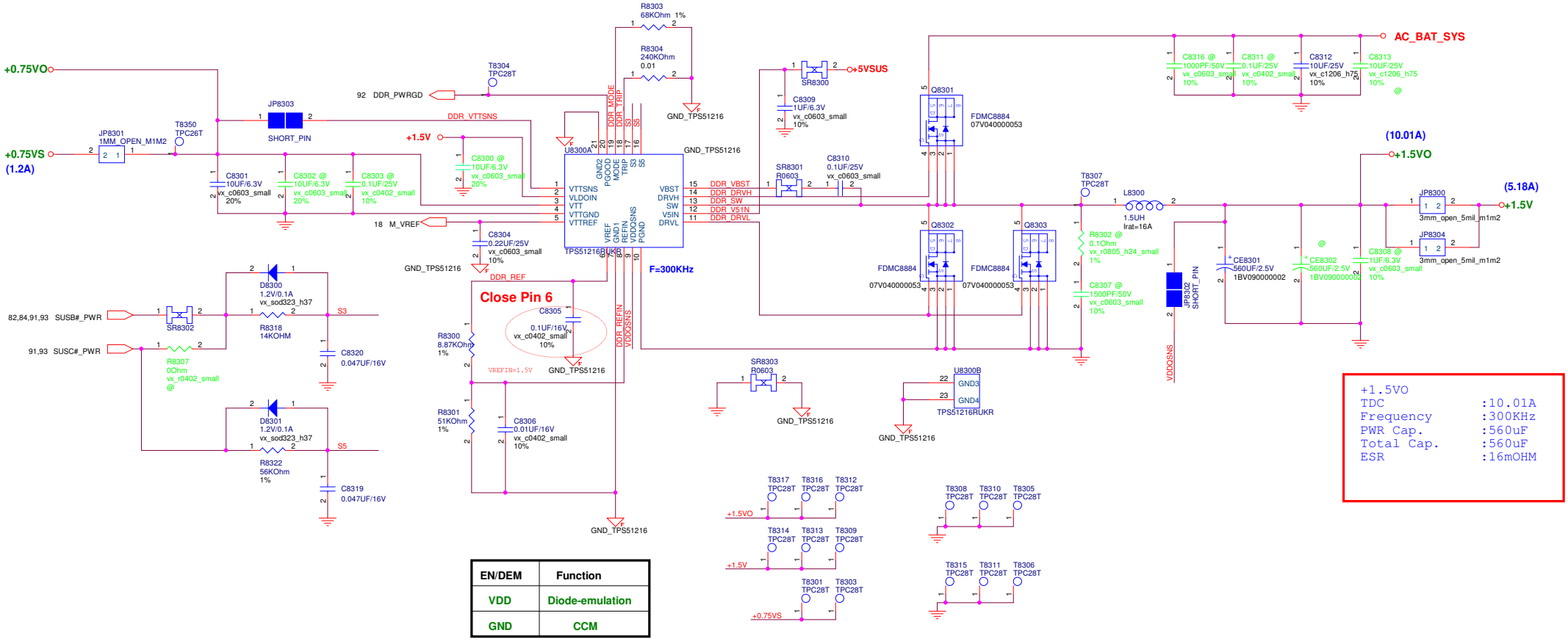
TRIP V (mV) = TRIP R (k) * TRIP I (mA)
TRIPI current, which is 10uA
VOCP = TRIP V / (8 / Rdson) + (I ripple / 2)

Used for testing purpose in production line.
Pull down to GND with a resistor of 470 kΩ or less



PEGATRON	Title : POWER_ +1.05V & +1.1V		
<OrgName>	Engineer: Ray/Isaac		
Size: Custom	Project Name		Rev: 1.0
Date: Monday, April 23, 2012	Sheet 82 of 88		

DDR & VTT POWER SUPPLY



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

+1.5VO	
TDC	:10.01A
Frequency	:300KHz
PWR Cap.	:560uF
Total Cap.	:560uF
ESR	:16mOHM

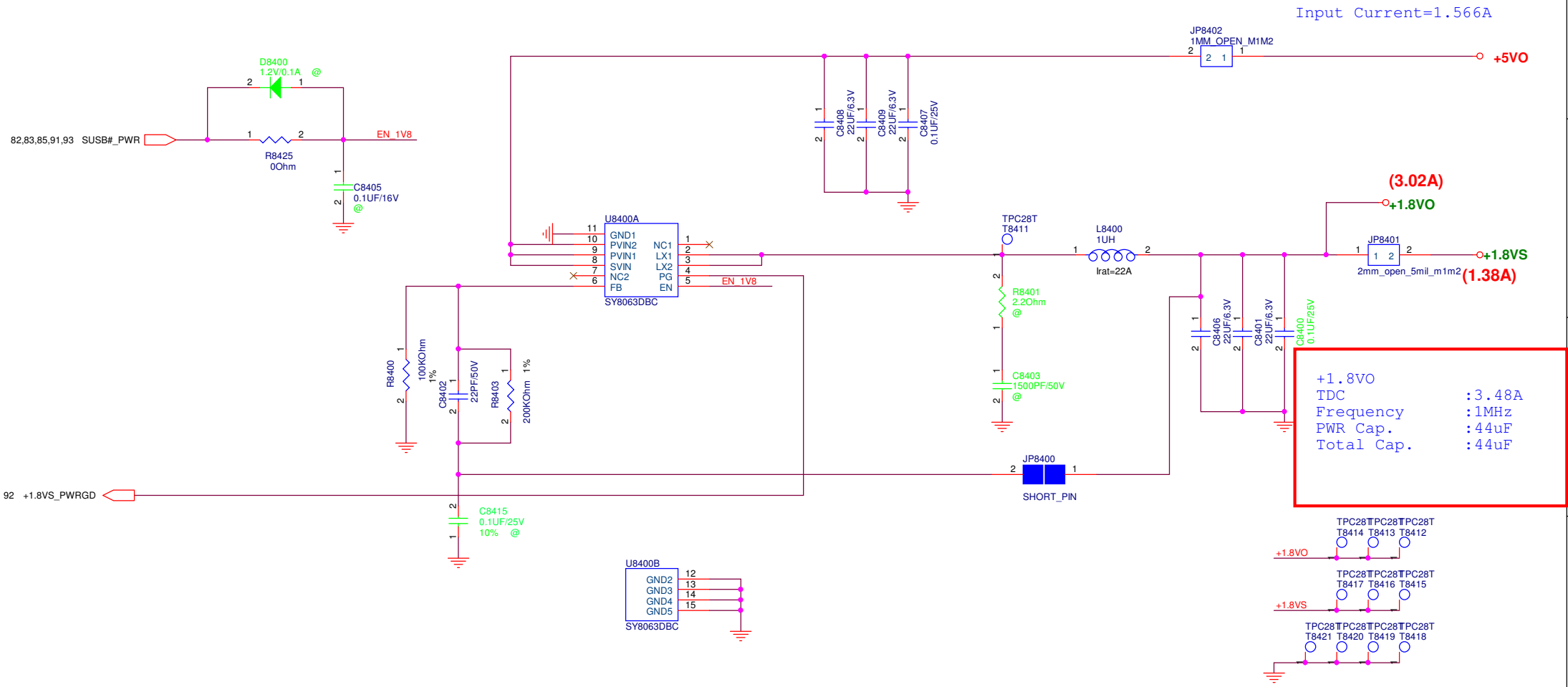
<Variant Name>

PEGATRON Title : POWER_DDR & VTT

Engineer: Ray/Isaac

Size	Project Name	Rev
Custom		1.0

Date: Monday, April 23, 2012 Sheet 83 of 94



<Variant Name>

PEGATRON Title :POWER_+1.8VS

Engineer: Ray/Isaac

Size	Project Name	Rev
B		1.0

Date: Monday, April 23, 2012 Sheet 84 of 94

PEGATRON Title : POWER_N/A

<OrgName> Engineer: Ray/Isaac

Size	Project Name	Rev
C		1.0

Date: Monday, April 23, 2012 Sheet 85 of 94

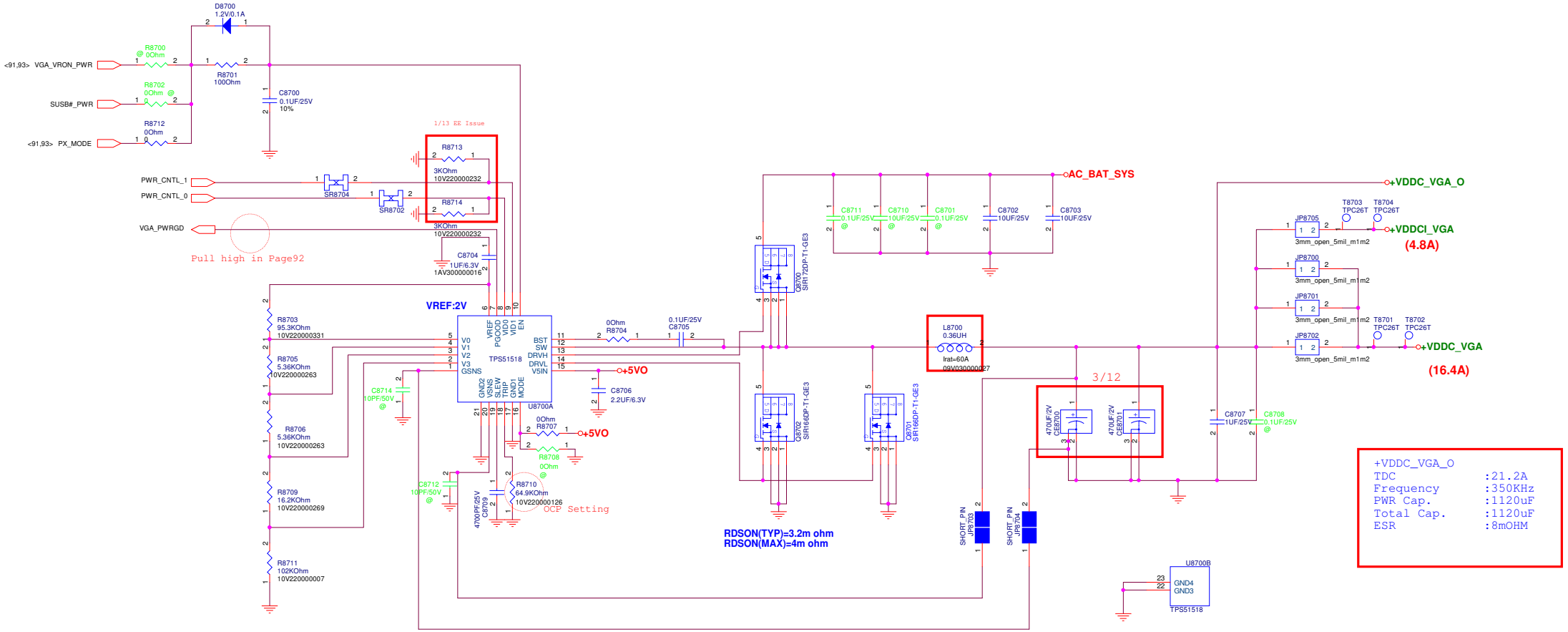
<variant_name><Variant Name></variant_name>

PEGATRON Title : POWER_N/A

Engineer: Ray/Isaac

Size	Project Name	Rev
Custom		1.0

Date: Monday, April 23, 2012 Sheet 86 of 94



VID1	VID0	Vo Formula
L	L	((R8705+R8706+R8709+R8711)/(R8703+R8705+R8706+R8709+R8711))*VREF
L	H	((R8706+R8709+R8711)/(R8703+R8705+R8706+R8709+R8711))*VREF
H	L	((R8709+R8711)/(R8703+R8705+R8706+R8709+R8711))*VREF
H	H	((R8711)/(R8703+R8705+R8706+R8709+R8711))*VREF

PWR_CNTL_1	PWR_CNTL_0	+VDDC_VGA
L	L	1.15V
L	H	1.1V
H	L	1.05V
H	H	0.9V

TPS51518 Pin16 (Mode)		
	Mode definition	Frequency
+5VO	DCAP2	350KHz
GND	DCAP	350KHz

IOCP=(R8710*10uA)/RDSON

<Variant Name>

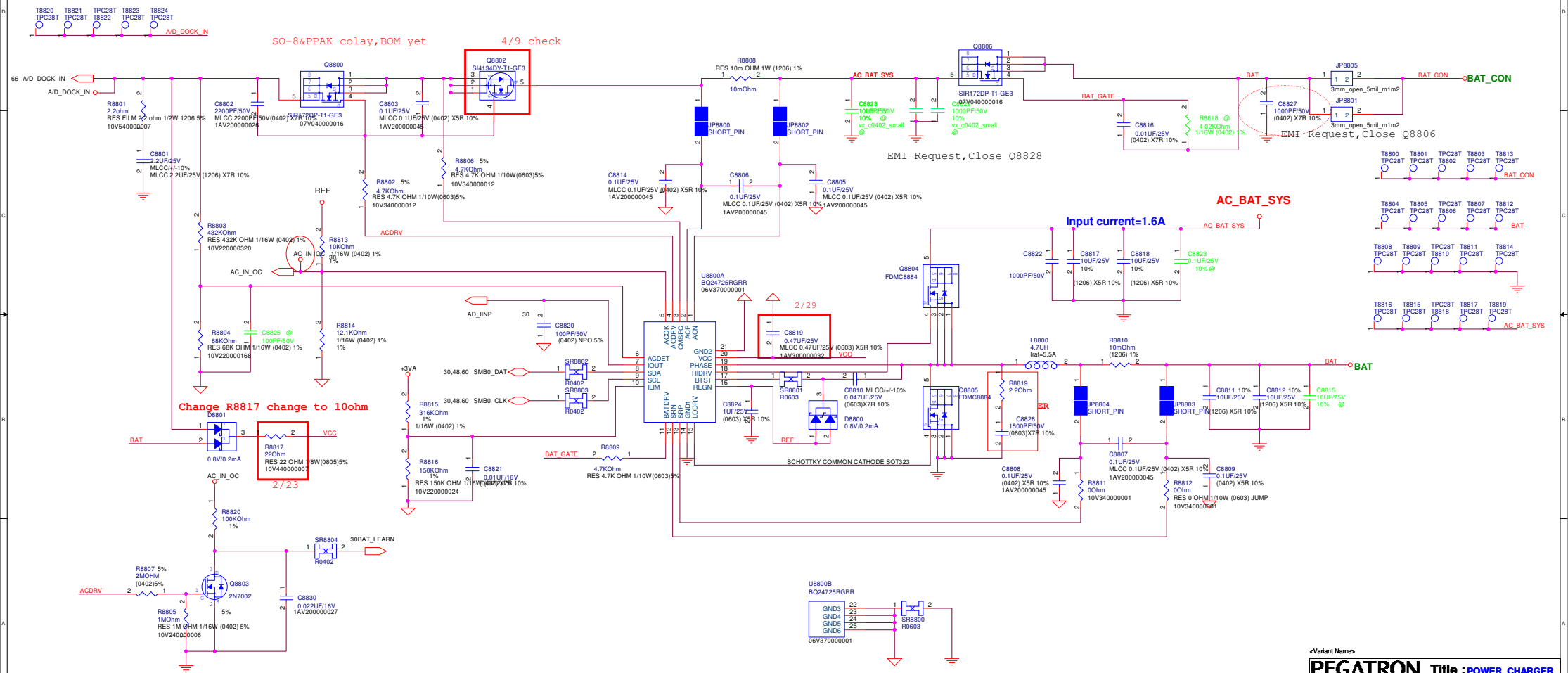
PEGATRON Title : POWER_+VGA_CORE

Engineer: Ray/Isaac

Size	Project Name	Rev
Custom		1.0

Date: Monday, April 23, 2012 Sheet 87 of 94

BATTERY CHARGER



<Variant Name>

PEGATRON Title : POWER_CHARGER

Engineer: Ray/Isaac

Size	Project Name	Rev
Custom		1.0

Date: Monday, April 23, 2012 Sheet 88 of 94

PEGATRON Title : POWER

<OrgName> Engineer: Ray/Isaac

Size	Project Name	Rev
B		1.0

Date: Monday, April 23, 2012 Sheet 89 of 94

BATTERY IN DETECT

<Variant Name>

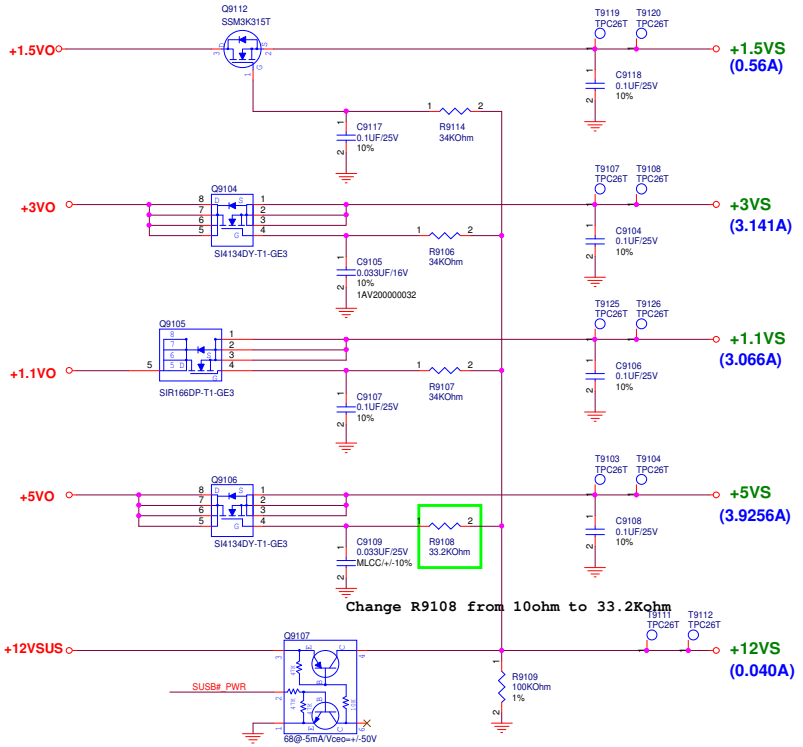
PEGATRON Title : POWER_DETECT

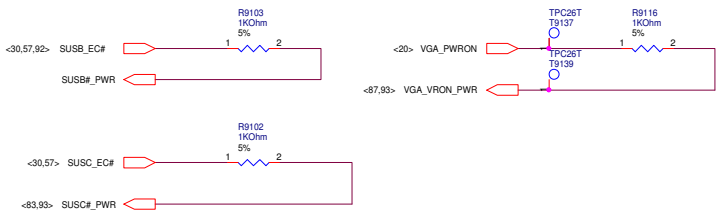
Engineer: Ray/Isaac

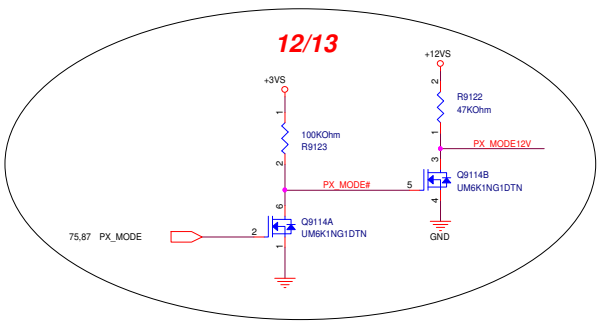
Size	Project Name	Rev
Custom	PL_ABG	1.0

Date: Monday, April 23, 2012 Sheet 90 of 94

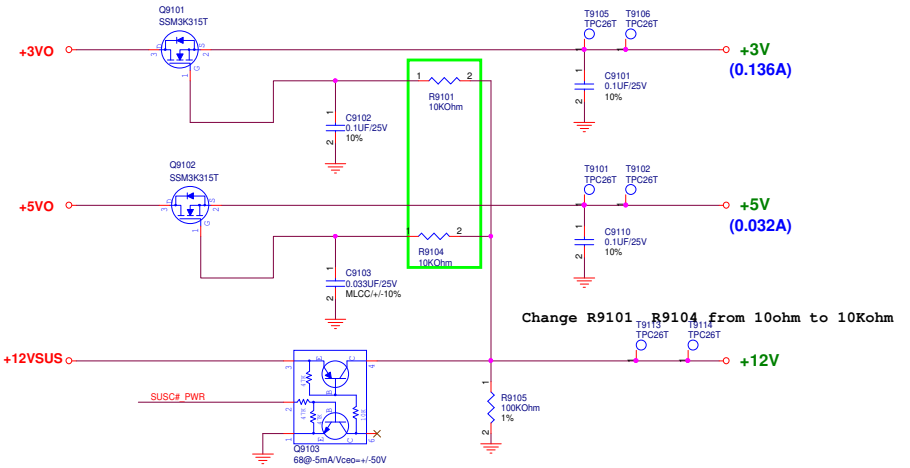
SUSB#_PWR POWER



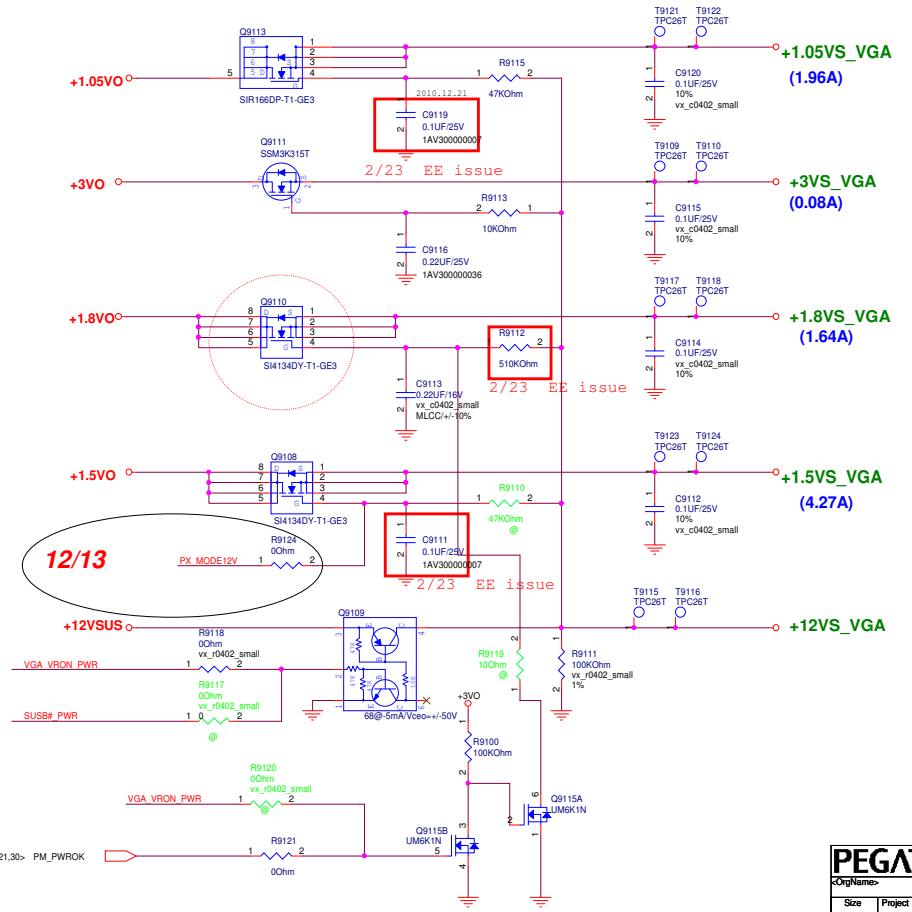




SUSC#_PWR POWER



VGA_VRON_PWR_PWR POWER



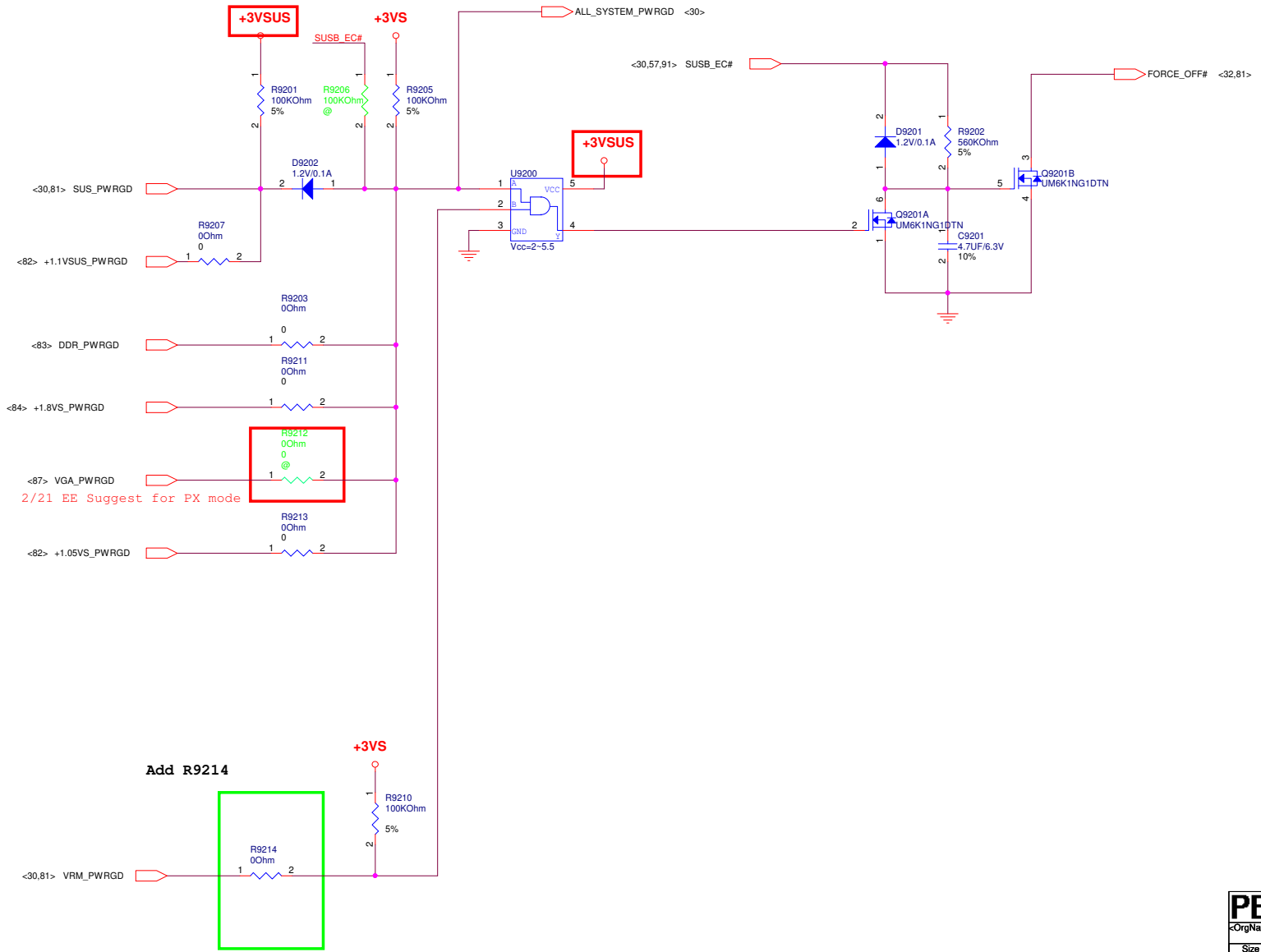
PEGATRON Title : POWER_LOAD SWITCH

<OrgName> Engineer: Ray/Isaac

Size	Project Name	Rev
C		1.0

Date: Monday, April 23, 2012 Sheet 91 of 94

POWER GOOD DETECTER



PEGATRON	Title : POWER_PROTECT	
<OrgName>	Engineer: Ray/Isaac	
Size: Custom	Project Name	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 92 of 94	

AC_BAT_SYS — AC_BAT_SYS <45,66,81,82,83,87,88>

+3VA — +3VA <20,22,30,52,56,57,81>
+RTC_POWER — +RTC_POWER <81>
+5VA — +5VA <52,56,81,87,88>

+5VO — +5VO <81,87,91>
+3VO — +3VO <81,87,91>
+3VSUS — +3VSUS <4,20,21,22,23,24,28,30,33,81,92>
+5VSUS — +5VSUS <51,52,56,66,81,82,83,84,87>

+12VSUS — +12VSUS <22,51,81,91>
+12V — +12V <91>
+12VS — +12VS <48,91>

+3V — +3V <30,40,44,45,53,57,91>
+3VS — +3VS <4,16,17,21,22,23,24,30,31,32,33,36,37,38,39,45,48,50,51,53,56,57,81,91,92>
+3VS_VGA — +3VS_VGA <57,70,71,74,75,91>
+5V — +5V <57,91>
+5VS — +5VS <30,31,36,38,45,46,48,50,51,56,57,81,91>
+1.1VO — +1.1VO <82,91>
+1.1VSUS — +1.1VSUS <21,23,82>
+1.05VS — +1.05VS <82,91>

+1.1VS — +1.1VS <82,91>

+1.8VS_VGA — +1.8VS_VGA <57,71,74,75,76,84>
+0.75VS — +0.75VS <16,17,57,83>
+0.75VO — +0.75VO <83>
+1.5VO — +1.5VO <83,87,91>
+1.5VS — +1.5VS <53,57,91>
+1.5V — +1.5V <3,4,5,16,17,45,57,83>
+1.5VS_VGA — +1.5VS_VGA <57,72,73,75,77,78,91>
+1.05VO — +1.05VO <82,91>
+1.05VS_VGA — +1.05VS_VGA <57,70,71,75,76,87>

+VCORE — +VCORE <5,81>

+VDDCR_NB — +VDDCR_NB <5,81>

+VDDC_VGA — +VDDC_VGA <75,87>
+VDDC_VGA_O — +VDDC_VGA_O <87>

BAT — BAT <88>
BAT_CON — BAT_CON <57,88>

FOR POWER TEST

+3VA

JP9300 — SGL_JUMP @ — 1 — 1 2 — 2 — CPU_VRON_PWR <81>

JP9301 — SGL_JUMP @ — 1 — 1 2 — 2 — SUSB#_PWR

JP9302 — SGL_JUMP @ — 1 — 1 2 — 2 — SUSC#_PWR <83,91>

JP9303 — SGL_JUMP @ — 1 — 1 2 — 2 — VSUS_ON <22,30,81,82>

JP9304 — SGL_JUMP @ — 1 — 1 2 — 2 — VGA_VRON_PWR <87,91>

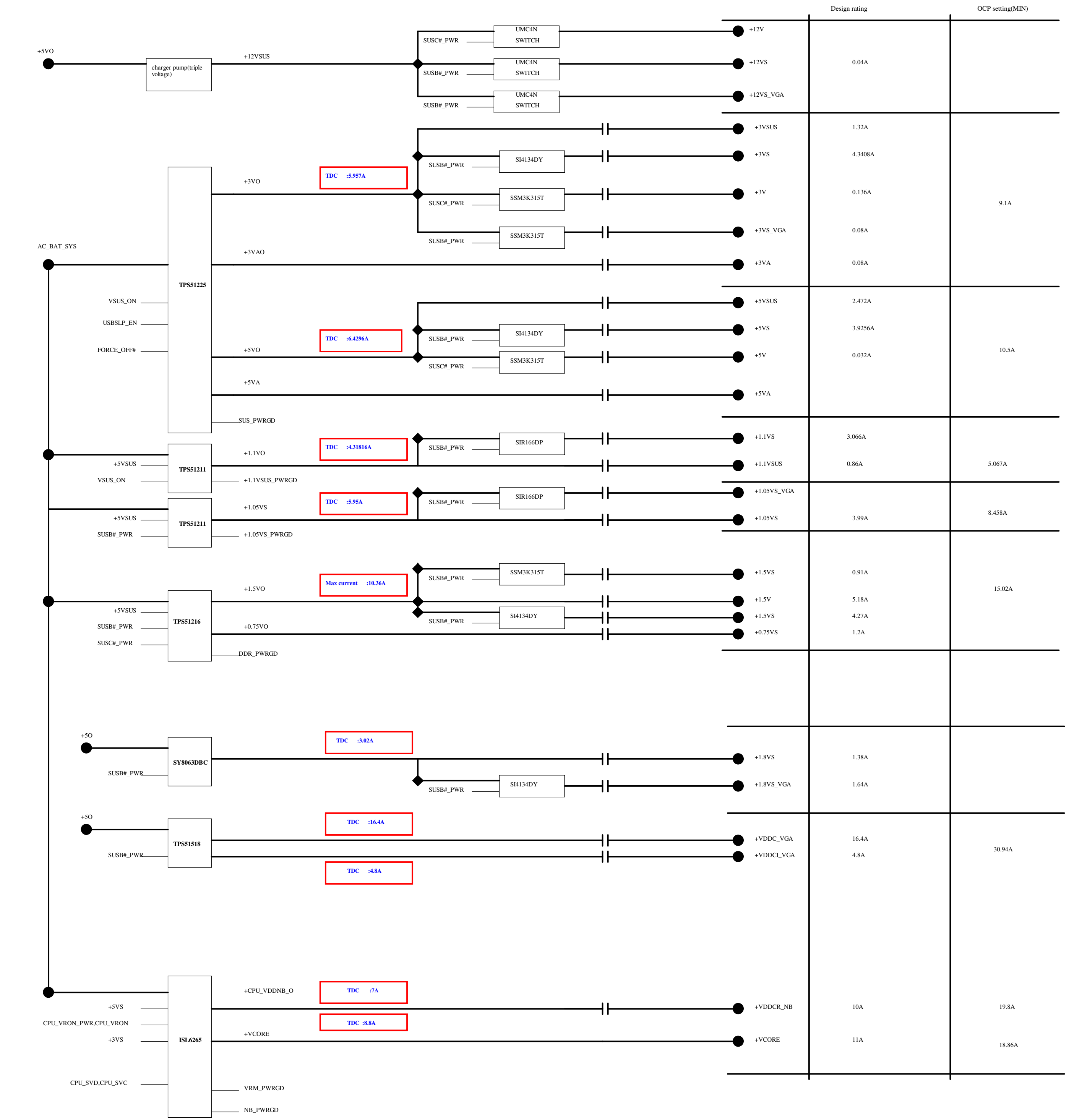
<Variant Name>

PEGATRON Title :POWER_SIGNAL

Engineer: Ray/Isaac

Size	Project Name	Rev
B		1.0

Date: Monday, April 23, 2012 Sheet 93 of 94



<Variant Name>

PEGATRON **Title : POWER_FLOWCHART**

Engineer: Ray/Isaac

Size	Project Name	Rev
Custom		1.0

Date: Monday, April 23, 2012 Sheet 94 of 94

Item	Date	Description
1	0202-12	mount R2036 and un-mount R2032 for judging the DSC sku
2	0202-12	mount D7001 and un-mount D7002 for the reset setting of GPU
3	0208-12	adding R2145 for reserving the pull-up (PCIE_WAKE# PIN)

Title	<Title>	
Size B	Document Number EG70	Rev <RevCode>
Date: Monday, April 23, 2012	Sheet 95 of 99	

Screw G x 1

Fix Hole H x 1

Fix Hole I x 1

PWR_H3
1
CT197D118N

delete the unnecessary screw hole /0118-13

PWR_H2
1
C276D110

PWR_GND

Screw F x 1

PWR_H1
1
2
NP_NC1
NP_NC2
GND1
GND2
5
4
3
DO142X118_DO189X110N
PWR_GND

change screw hole /0118-12

POWER Button LED

+5VSUS_PWR

PWR_C01
47PF/50V
PWR_GND

PWR_LED01
BLUE
07V130000054

change resister value from 300 to 1.5k ohm /0407-12

PWR_R02
1.5KOhm
10V220000022

PWRLED_ON#_PWR

R1.1 reverse PWR_CON01 and change pin 1~4 pin define 1024

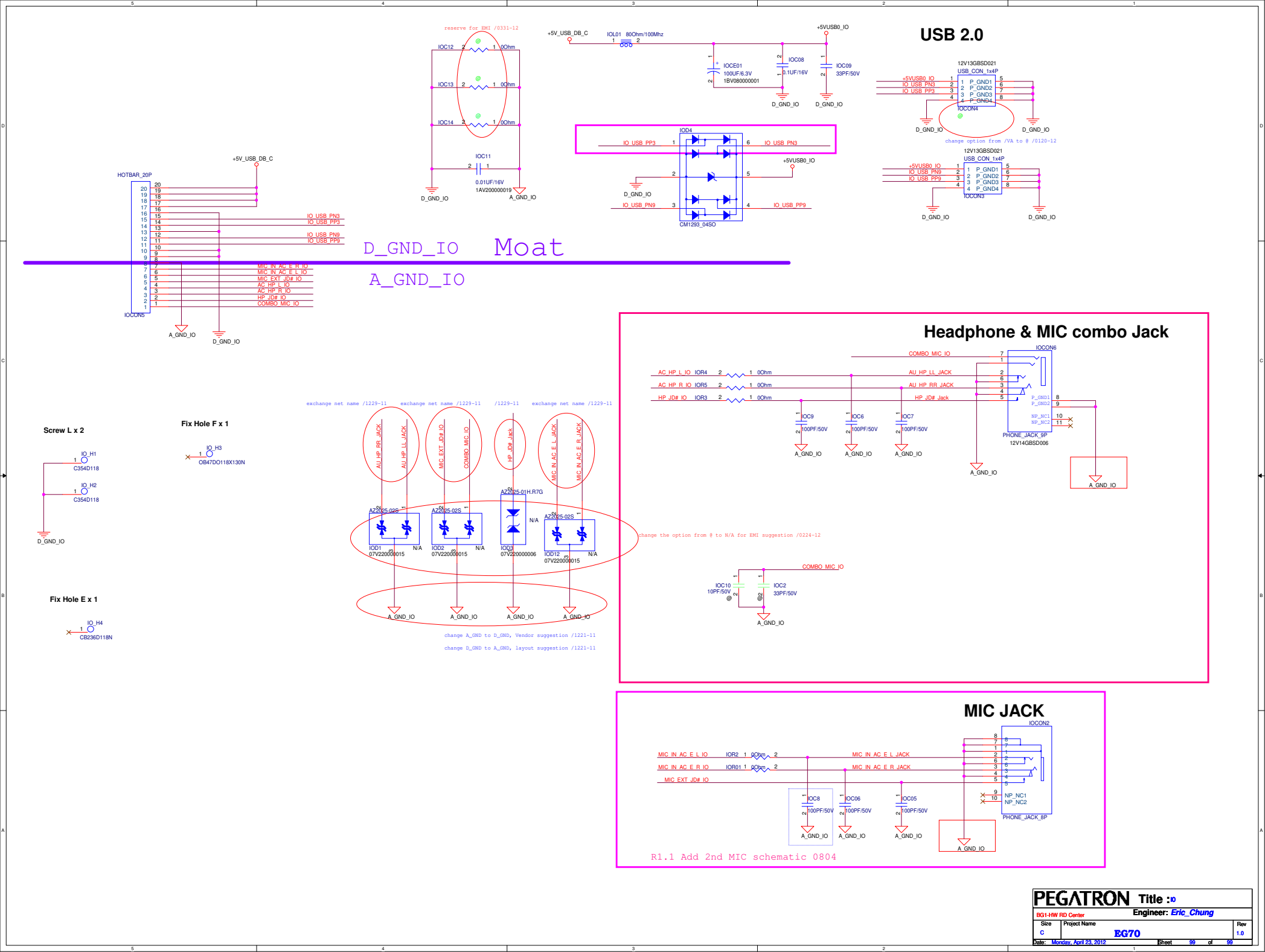
PWR_CON01
+3VA_PWR
+5VSUS_PWR
LID_SW#_PWR
PWRLED_ON#_PWR
PWR_SW#_PWR
HOTBAR_10P
PWR_GND

12V09SBSM032
TACT_SWITCH_4P
PWR_SW01
/0409-12
PWR_GND

LID Switch

+3VA_PWR
PWR_C02
0.1UF/16V
PWR_R05
100KOhm
AH180-WG-7
Vdd
GND
OUTPUT
LID_SW#_PWR
PWR_U01
PWR_GND

PEGATRON	Title : PWR BTN	
BG1-HW RD Center	Engineer: Eric_Chung	
Size: Custom	Project Name: EG70	Rev: 1.0
Date: Monday, April 23, 2012	Sheet 97 of 99	


USB 2.0
reserve for EMI /0331-12
IOC12 0Ohm
IOC13 0Ohm
IOC14 0Ohm
IOC11
0.01UF/16V
1AV200000019
D_GND_IO
A_GND_IO
+5V_USB_DB_C
IOL01 80Ohm/100Mhz
IOCE01
100UF/6.3V
1BV080000001
IOC08
0.1UF/16V
IOC09
33PF/50V
+5VUSB0_IO
12V13GBSD021
USB_CON_1x4P
IOCON4
IOCON3
change option from /VA to @ /0120-12
IOD4
CM1293_04SO
IO_USB_PP3
IO_USB_PN3
IO_USB_PN9
IO_USB_PP9
HOTBAR_20P
IOCON5
MIC_IN_AC_E_R_IO
MIC_IN_AC_E_L_IO
MIC_EXT_JD#_IO
AC_HP_L_IO
AC_HP_R_IO
HP_JD#_IO
COMBO_MIC_IO
D_GND_IO Moat
A_GND_IO
Headphone & MIC combo Jack
IOCON6
PHONE_JACK_9P
12V14GBSD006
AC_HP_L_IO IOR4 0Ohm
AC_HP_R_IO IOR5 0Ohm
HP_JD#_IO IOR3 0Ohm
AU_HP_LL_JACK
AU_HP_RR_JACK
HP_JD#_Jack
IOC9 100PF/50V
IOC6 100PF/50V
IOC7 100PF/50V
change the option from @ to N/A for EMI suggestion /0224-12
IOC10 10PF/50V
IOC2 33PF/50V
MIC JACK
IOCON2
PHONE_JACK_8P
MIC_IN_AC_E_L_IO
MIC_IN_AC_E_R_IO
MIC_EXT_JD#_IO
IOR2 0Ohm
IOR01 0Ohm
MIC_IN_AC_E_L_JACK
MIC_IN_AC_E_R_JACK
IOC8 100PF/50V
IOC06 100PF/50V
IOC05 100PF/50V
NP_NC1
NP_NC2
R1.1 Add 2nd MIC schematic 0804
exchange net name /1229-11
AZ2025-02S
AZ2025-01H.R7G
IOD1 07V220000015
IOD2 07V220000015
IOD3 07V220000006
IOD12 07V220000015
change A_GND to D_GND, Vendor suggestion /1221-11
change D_GND to A_GND, layout suggestion /1221-11
Screw L x 2
IO_H1
IO_H2
C354D118
Fix Hole F x 1
IO_H3
OB47DO118X130N
Fix Hole E x 1
IO_H4
CB236D118N
PEGATRON
Title :IO
Engineer: Eric_Chung
BG1-HW RD Center
Size C
Project Name EG70
Rev 1.0
Date: Monday, April 23, 2012
Sheet 99 of 99