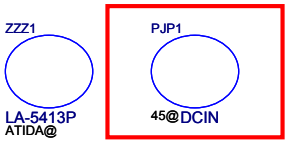


Compal Confidential

NBLB2 Schematics Document

Intel Clarksfield Processor with DDRIII + Ibex PM55

2009-11-17

REV:0.2

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics,Ltd.

Title: Cover Sheet

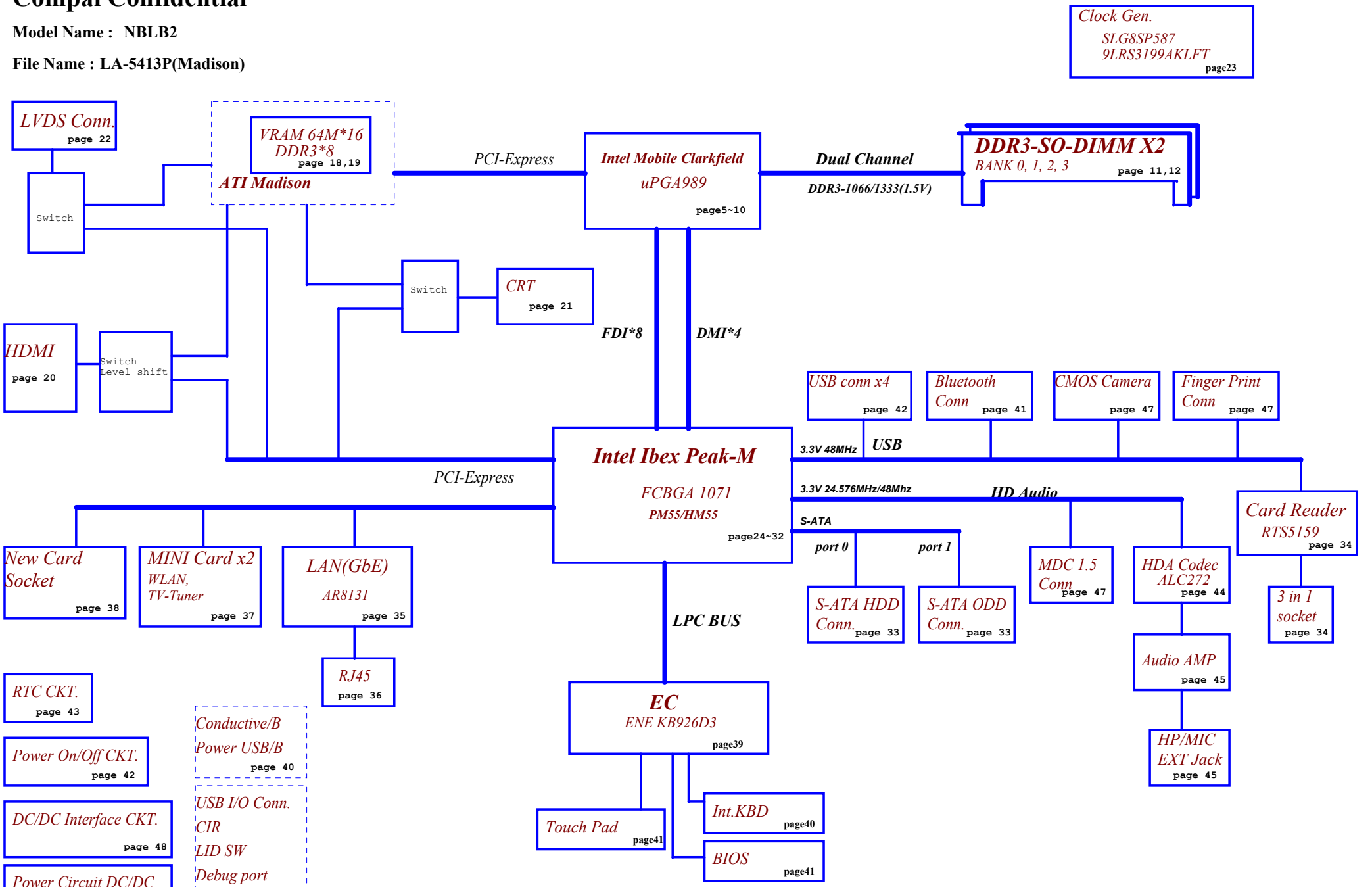
Size: Custom | Document Number: NBLB2 M/B LA-5413P Schematic | Rev: 0.1

Date: Thursday, November 19, 2009 | Sheet 1 of 61

Compal Confidential

Model Name : NBLB2

File Name : LA-5413P(Madison)



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/09/14

Compal Electronics,Ltd.

Title: MB Block Diagram

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Friday, November 13, 2009 | Sheet 2 of 61

DDR3 Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS +1.1VS_VTT +1.5VS_VRAM
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

GPIO PIN Define

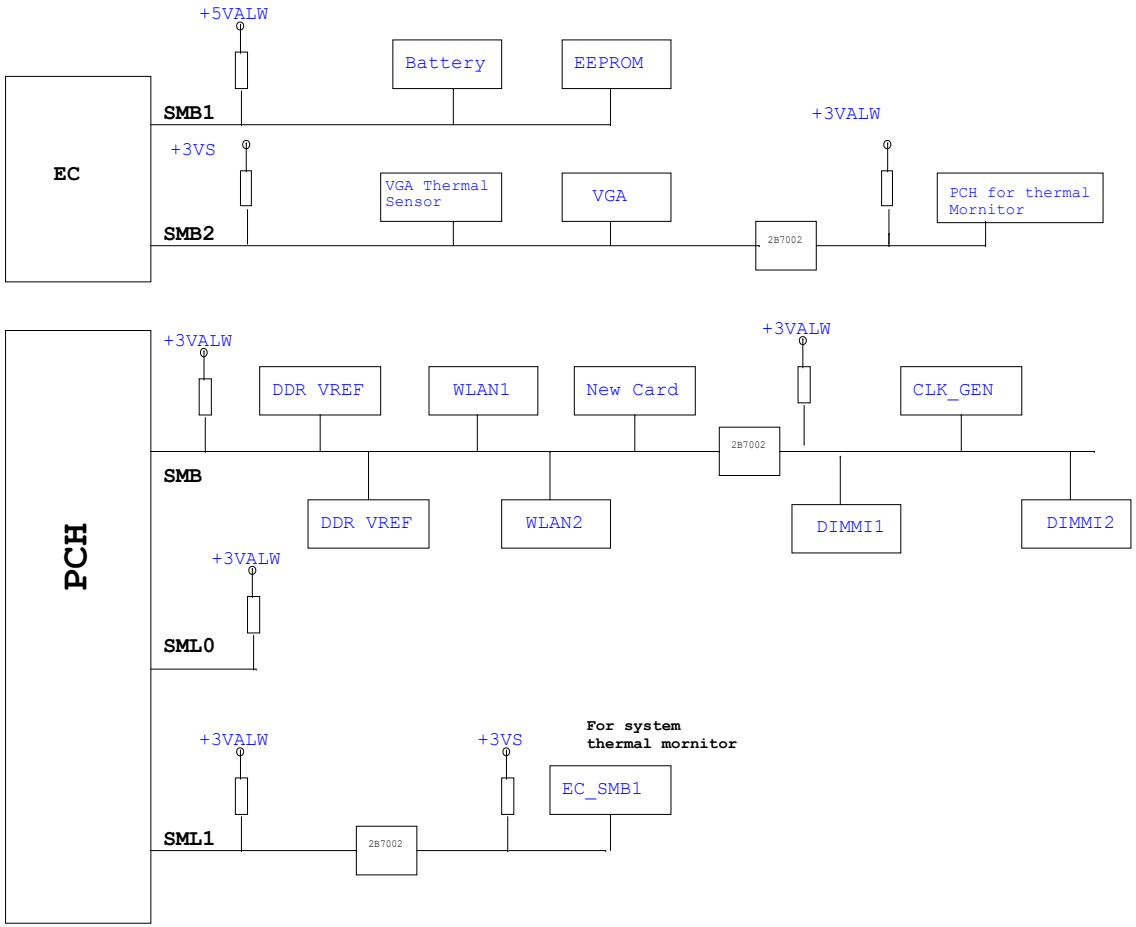
	ID3	ID2	ID1	ID0
NBLB2(1100)	R358	R361	R766	R765
Reserve (1101)	X	X	X	X
Reserve (1110)	X	X	X	X
Reserve (1111)	X	X	X	X
NBLB1 (0000)	R353	R350	R766	R765
Reserve(0001)	X	X	X	X
Reserve(0010)	X	X	X	X
Reserve(0011)	X	X	X	X
Reserve(0100)	X	X	X	X
Reserve(0101)	X	X	X	X
Reserve (0110)	X	X	X	X
Reserve (0111)	X	X	X	X
Reserve (1000)	X	X	X	X
Reserve (1001)	X	X	X	X
Reserve (1010)	X	X	X	X
Reserve (1011)	X	X	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
EMCI 1402	100_1100X b
NVIDIA N10P-GE1	



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: MB Notes List

Size: B | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Friday, November 13, 2009 | Sheet 3 of 61

VGA (Madison)

State \ power plane	+1.8VS +1.5VS_VRAM	+3VS_DELAY +VGA_CORE +1.1VS
S0	O	O
S1	O	O
S3	X	X
S5 S4/AC	X	X
S5 S4/ Battery only	X	X
S5 S4/AC & Battery don't exist	X	X

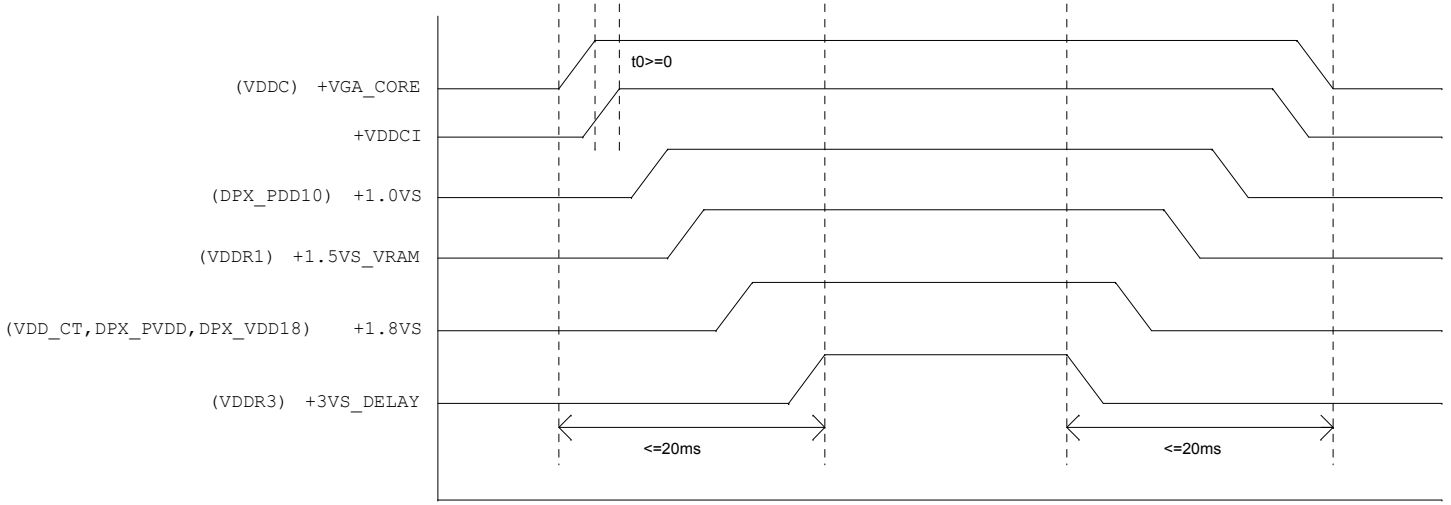
Ref:46039_m97_ds_nda_1.00

M97 sequence

M97 has the following requirements with regards to power supply sequencing to avoid damaging the ASIC.

- All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
- VDDC should ramp before or simultaneously with VDDCI.
- VDDCI should ramp before VDDR1.
- VDDC should ramp before VDDR4.
- VDDC should ramp before DPx_VDD18, DPx_VDD10, and DPx_PVDD.
- PWRGOOD must not be asserted, and must not exceed 300 mV, before all of VDDC, VDD_CT, and VDDR3 have ramped up. Asserting PWRGOOD only after all ASIC supplies have ramped up is preferred for forward compatibility.
- PWRGOOD must be de-asserted, and must be brought below 300 mV, before ramping down any of VDDC, VDD_CT, or VDDR3.
- DDC3DATA_DP3_AUXN, DDC4DATA_DP4_AUXN, DDC3CLK_DP3_AUXP, and DDC4CLK_DP4_AUXP must be pulled high either before or after both VDDC and VDD_CT have ramped up.
- For power down, reversing the ramp-up sequence is recommended.

POWER UP/DOWN Sequence



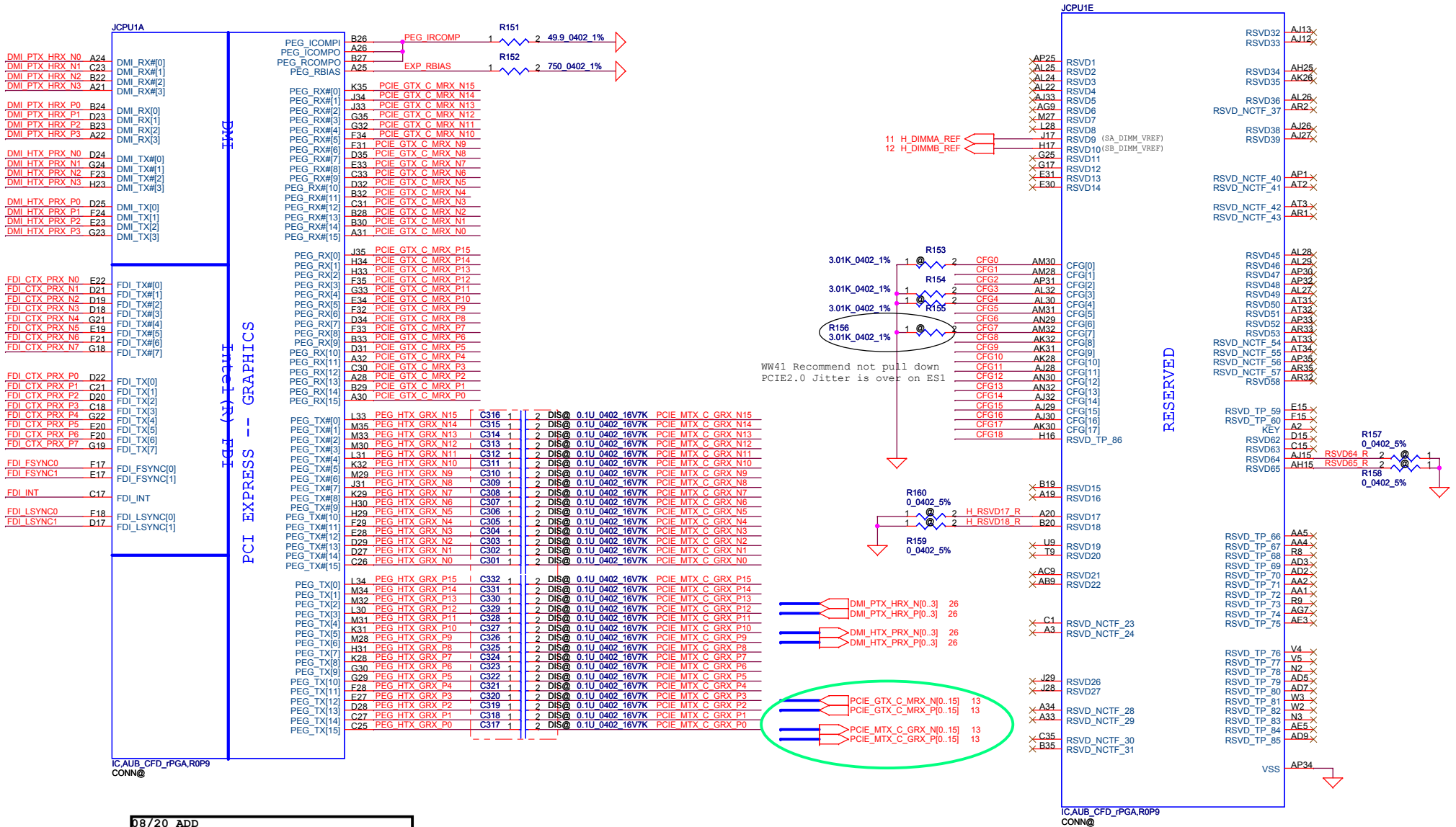
Security Classification	Compal Secret Data		
Issued Date	2009/02/24	Deciphered Date	2010/02/24

Compal Electronics, Inc.

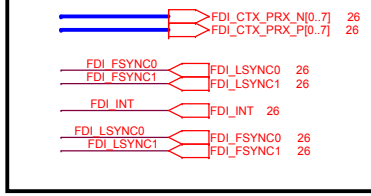
Title: VGA Notes List

Size	Document Number	Rev
B	NBLB2 M/B LA-5412P Schematic	0.2

Date: Friday, November 13, 2009 Sheet 4 of 61



08/20 ADD
FDI for SG



CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

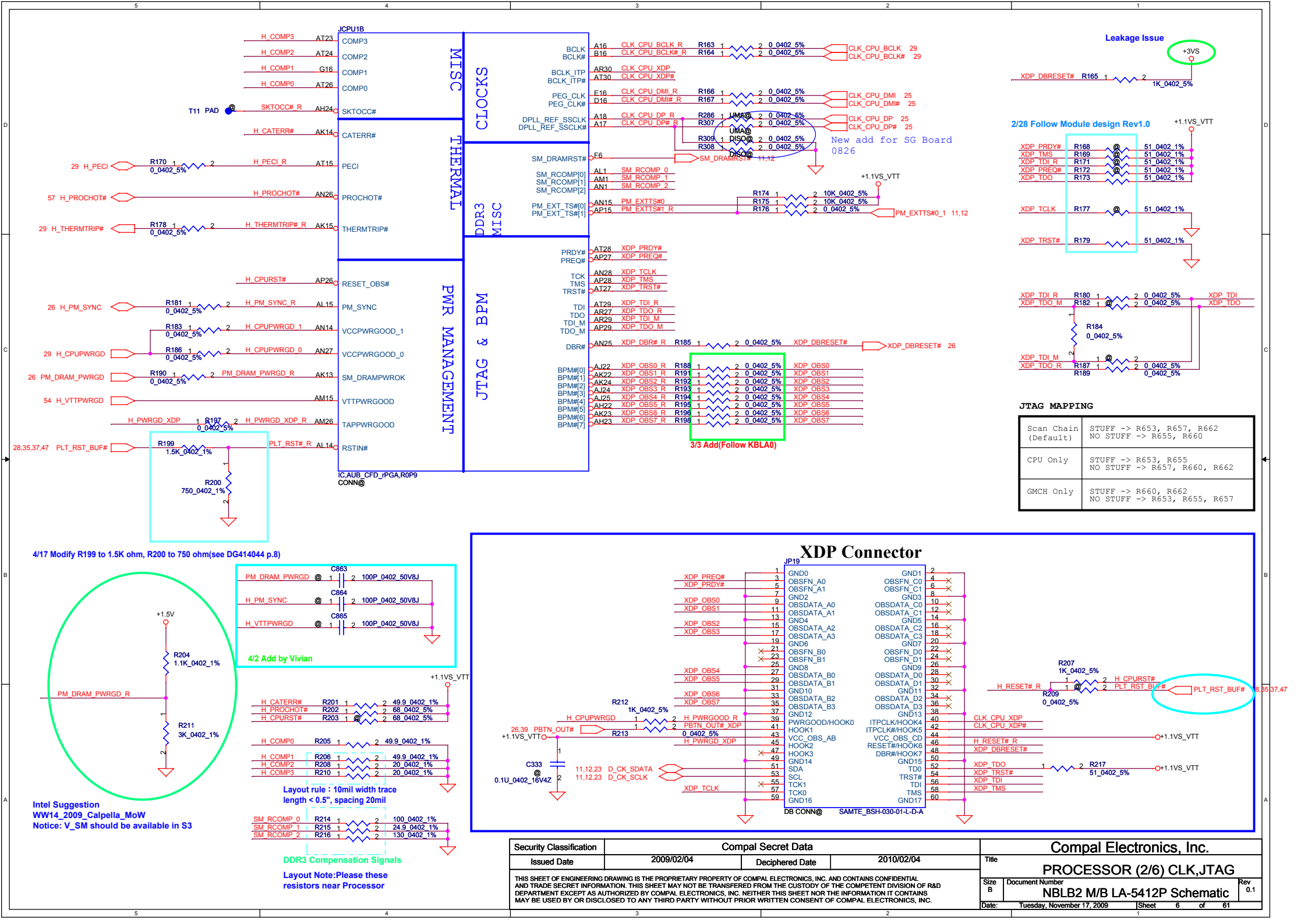
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: PROCESSOR (1/6) DMI,FDI,PEG

Size	Document Number	Rev
B	NBLB2 M/B LA-5412P Schematic	0.1

Date: Tuesday, November 17, 2009 | Sheet 5 of 61



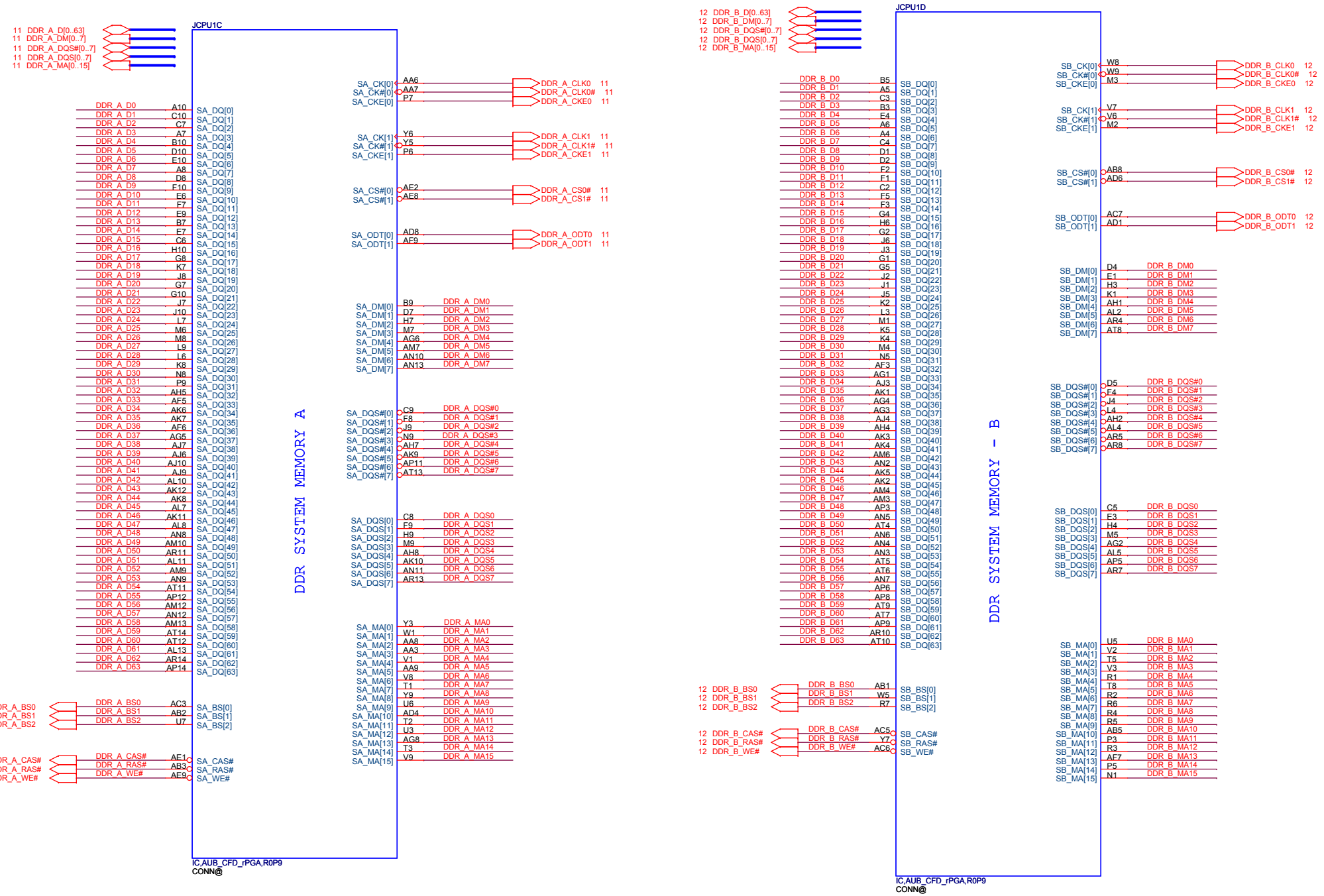
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: PROCESSOR (2/6) CLK,JTAG

Size	Document Number	Rev
B	NBLB2 M/B LA-5412P Schematic	0.1

Date: Tuesday, November 17, 2009 Sheet 6 of 61



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	NBLB2 M/B LA-5412P Schematic	0.1

Date: Tuesday, November 17, 2009 Sheet 7 of 61

JCPU1F

WW15 MOW
Peak 21A
Continuous 18A

48A

+CPU_CORE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

IC,AUB_CFD_rPGA,R0P9
CONN@

3/3 Follow Module design

3/3 Add

3/12 Follow Module design

3/12 Add

(Place these capacitors between inductor and socket on Bottom)

(Place these capacitors under CPU socket, top layer)

(Place these capacitors on CPU cavity, Bottom Layer)

CSC (Current Sense Configuration)
8/25

remove it from BOM, DVT

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

H_VTTVID1 = low, 1.1V
H_VTTVID1 = high, 1.05V

4 x 470uF(6mohm@100kHz; 4.0mohm@SRF)

TOP side (under inductor)

change to SGA00001Q80
DVT

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

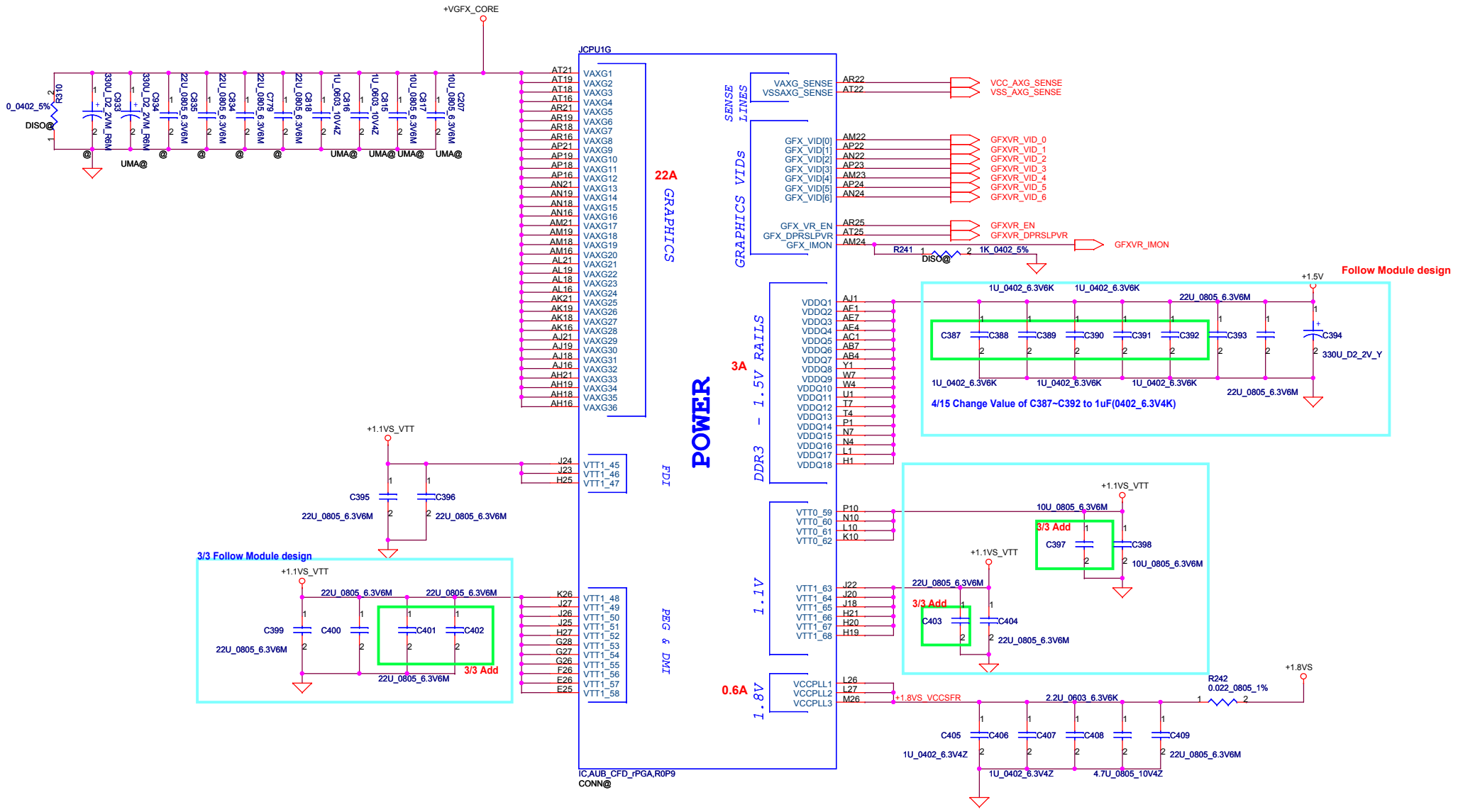
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 8 of 61



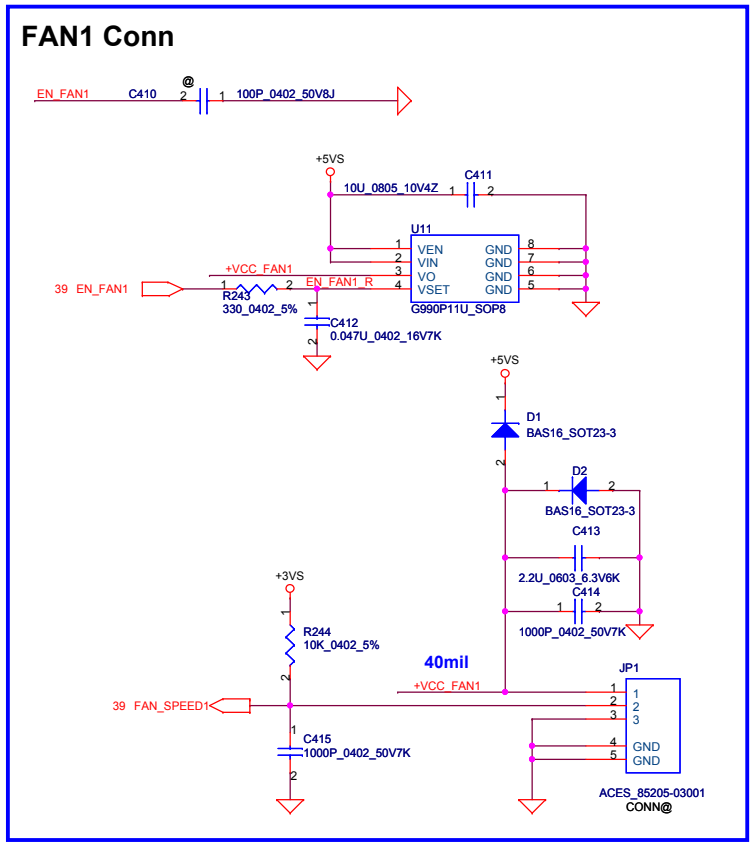
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

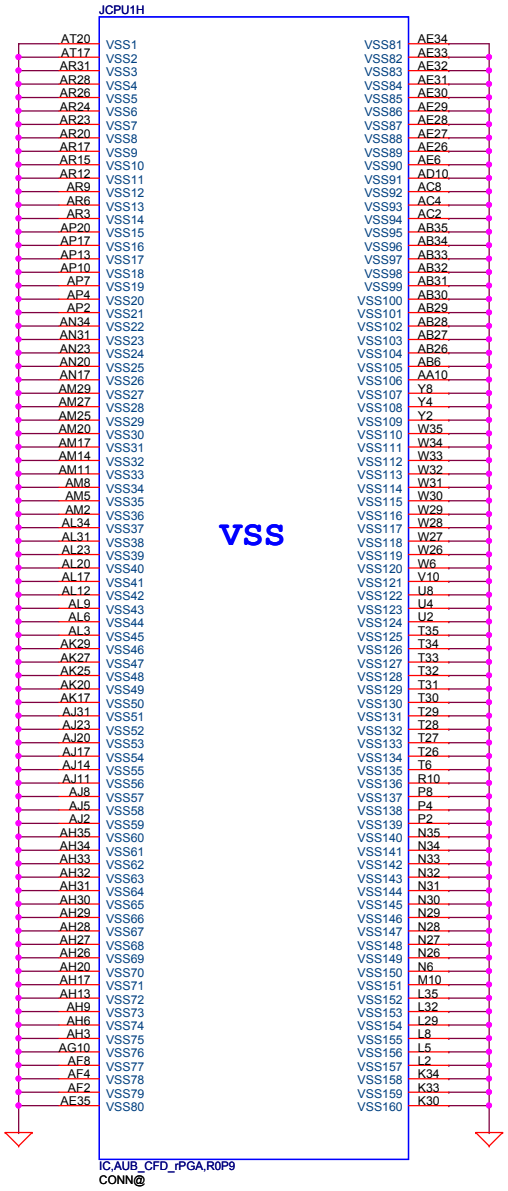
Compal Electronics, Inc.

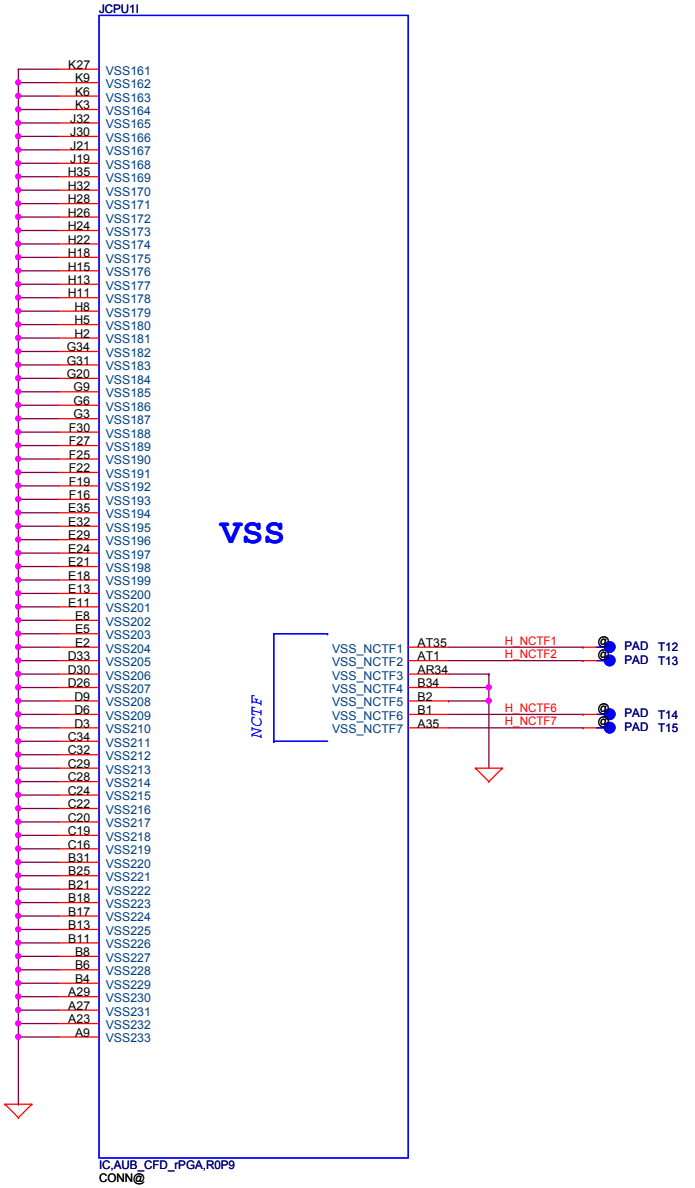
Title: PROCESSOR (5/6) PWR

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 9 of 61







Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS& FAN

Size	Document Number	Rev
Custom	NBLB2 M/B LA-5412P Schematic	0.1

Date: Tuesday, November 17, 2009 | Sheet 10 of 61

M1 Circuit

+1.5V

R246 1K_0402_1%

+V_DDR3_DIMM_REF

R249 1K_0402_1%

M3 Circuit

DISO@

R245 0_0402_5%

R247 0_0402_5%

5 H_DIMMA_REF

+V_DDR3_DIMM_REF

7 DDR_A_DQS#[0..7]
7 DDR_A_D[0..63]
7 DDR_A_DM[0..7]
7 DDR_A_DQS[0..7]
7 DDR_A_MA[0..15]

C417 0.1U_0402_16V4Z

C416 2.2U_0805_16V4Z

JP2

FOX_AS0A626-U2SN-7F_204P

CONN@

SM_DRAMRST# 6,12

2/28 Module design don't use pin78(NC),need double check it.

DDR_VREF_CA_DIMMA R256 0_0402_5%

C421 2.2U_0603_6.3V4Z

C422 0.1U_0402_16V4Z

R257 10K_0402_5%

C436 2.2U_0603_6.3V4Z

C437 0.1U_0402_16V4Z

R258 10K_0402_5%

PM_EXTTS#0_1 6,12
D_CK_SDATA 6,12,23
D_CK_SCLK 6,12,23

Layout Note:
Place near JP2

Follow Module design

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

10U_0603_6.3V6M: C423, C424, C425, C426, C427, C428, C434, C435

0.1U_0402_16V4Z: C429, C430, C431, C432

330U_D2_2V_Y: C433

3/3 Add(Follow Module design)

4/15 Change value of C423~C428 from 10uF(0805_6.3V6M) to 10uF(0603_6.3V6M)

Layout Note:
Place near JP2.203 & JP2.204

1U_0402_6.3V6K: C438, C439, C440, C441, C442

10U_0805_6.3V6M: C853

4/15 Change value of C438~C442 from 1uF(0603_10V4Z) to 1U(0402_6.3V6K)

Follow Module design

3/16 Add C853= 10uF(0805_6.3V6M)(Intel's comment)

DDR3 SO-DIMM A Standard Type

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 11 of 61

7 DDR_B_DQS#[0..7]
7 DDR_B_D[0..63]
7 DDR_B_DM[0..7]
7 DDR_B_DQS[0..7]
7 DDR_B_MA[0..15]

2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

M1 Circuit
M3 Circuit
DISO@
+V_DDR3_DIMM_REF
R259 1 2 0_0402_5%
VREF_DQB
5 H_DIMMB_REF
R261 1 2 0_0402_5%

3/3 Change value and symbol of C1833 to 2.2uF(0603_6.3V4Z)
C443 2.2U_0603_6.3V4Z
C444 0.1U_0402_16V4Z
Follow Module design

JP3
TYCO_2-2013310-1_204P
CONN@

2/28 Module design don't use pin78(NC),need double check it.

Layout Note:
Place near JP3

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA
+1.5V
10U_0603_6.3V6M
0.1U_0402_16V4Z
330U_D2_2V_Y
C449 C450 C451 C452 C453 C454 C455 C456 C457 C458 C459 C460 C461
3/3 Add(Follow Module design)

Layout Note:
Place near JP3.203 & JP3.204

4/15 Change value of C462~C465 from 1uF(0603_10V4Z) to 1U(0402_6.3V6K)
Follow Module design
+0.75VS
1U_0402_6.3V6K
C462 C463 C464 C465 C466 10U_0805_6.3V6M

+3VS
R267 1 2 10K_0402_5%
R268 1 2 10K_0402_5%
C467 2.2U_0603_6.3V4Z
C468 0.1U_0402_16V4Z

+V_DDR3_DIMM_REF
DDR_VREF_CA_DIMMB R266 1 2 0_0402_5%
C447 2.2U_0603_6.3V4Z
C448 0.1U_0402_16V4Z

DDR3 SO-DIMM B
Standard Type

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.
Title: DDRIII-SODIMM SLOT2
Size: | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1
Date: Tuesday, November 17, 2009 | Sheet 12 of 61

5 PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]
5 PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
5 PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
5 PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

U4A

PCI EXPRESS INTERFACE

T2 PAD	PCIE_MTX_C_GRX_P0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PCIE_GTX_MRX_P0	C58	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P0
T3 PAD	PCIE_MTX_C_GRX_N0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PCIE_GTX_MRX_N0	C66	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N0
	PCIE_MTX_C_GRX_P1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PCIE_GTX_MRX_P1	C68	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P1
	PCIE_MTX_C_GRX_N1	W36	PCIE_RX1N	PCIE_TX1N	W32	PCIE_GTX_MRX_N1	C79	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N1
	PCIE_MTX_C_GRX_P2	W38	PCIE_RX2P	PCIE_TX2P	U33	PCIE_GTX_MRX_P2	C83	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P2
	PCIE_MTX_C_GRX_N2	V37	PCIE_RX2N	PCIE_TX2N	U32	PCIE_GTX_MRX_N2	C86	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N2
	PCIE_MTX_C_GRX_P3	V35	PCIE_RX3P	PCIE_TX3P	U30	PCIE_GTX_MRX_P3	C87	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P3
	PCIE_MTX_C_GRX_N3	U36	PCIE_RX3N	PCIE_TX3N	U29	PCIE_GTX_MRX_N3	C94	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N3
	PCIE_MTX_C_GRX_P4	U38	PCIE_RX4P	PCIE_TX4P	T33	PCIE_GTX_MRX_P4	C95	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P4
	PCIE_MTX_C_GRX_N4	T37	PCIE_RX4N	PCIE_TX4N	T32	PCIE_GTX_MRX_N4	C104	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N4
	PCIE_MTX_C_GRX_P5	T35	PCIE_RX5P	PCIE_TX5P	T30	PCIE_GTX_MRX_P5	C105	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P5
	PCIE_MTX_C_GRX_N5	R36	PCIE_RX5N	PCIE_TX5N	T29	PCIE_GTX_MRX_N5	C108	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N5
	PCIE_MTX_C_GRX_P6	R38	PCIE_RX6P	PCIE_TX6P	P33	PCIE_GTX_MRX_P6	C109	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P6
	PCIE_MTX_C_GRX_N6	P37	PCIE_RX6N	PCIE_TX6N	P32	PCIE_GTX_MRX_N6	C116	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N6
T5 PAD	PCIE_MTX_C_GRX_P7	P35	PCIE_RX7P	PCIE_TX7P	P30	PCIE_GTX_MRX_P7	C117	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P7
T1 PAD	PCIE_MTX_C_GRX_N7	N36	PCIE_RX7N	PCIE_TX7N	P29	PCIE_GTX_MRX_N7	C122	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N7
	PCIE_MTX_C_GRX_P8	N38	PCIE_RX8P	PCIE_TX8P	N33	PCIE_GTX_MRX_P8	C124	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P8
	PCIE_MTX_C_GRX_N8	M37	PCIE_RX8N	PCIE_TX8N	N32	PCIE_GTX_MRX_N8	C128	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N8
	PCIE_MTX_C_GRX_P9	M35	PCIE_RX9P	PCIE_TX9P	N30	PCIE_GTX_MRX_P9	C130	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P9
	PCIE_MTX_C_GRX_N9	L36	PCIE_RX9N	PCIE_TX9N	N29	PCIE_GTX_MRX_N9	C135	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N9
	PCIE_MTX_C_GRX_P10	L38	PCIE_RX10P	PCIE_TX10P	L33	PCIE_GTX_MRX_P10	C139	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P10
	PCIE_MTX_C_GRX_N10	K37	PCIE_RX10N	PCIE_TX10N	L32	PCIE_GTX_MRX_N10	C144	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N10
	PCIE_MTX_C_GRX_P11	K35	PCIE_RX11P	PCIE_TX11P	L30	PCIE_GTX_MRX_P11	C146	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P11
	PCIE_MTX_C_GRX_N11	J36	PCIE_RX11N	PCIE_TX11N	L29	PCIE_GTX_MRX_N11	C149	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N11
	PCIE_MTX_C_GRX_P12	J38	PCIE_RX12P	PCIE_TX12P	K33	PCIE_GTX_MRX_P12	C150	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P12
	PCIE_MTX_C_GRX_N12	H37	PCIE_RX12N	PCIE_TX12N	K32	PCIE_GTX_MRX_N12	C157	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N12
	PCIE_MTX_C_GRX_P13	H35	PCIE_RX13P	PCIE_TX13P	J33	PCIE_GTX_MRX_P13	C158	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P13
	PCIE_MTX_C_GRX_N13	G36	PCIE_RX13N	PCIE_TX13N	J32	PCIE_GTX_MRX_N13	C162	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N13
	PCIE_MTX_C_GRX_P14	G38	PCIE_RX14P	PCIE_TX14P	K30	PCIE_GTX_MRX_P14	C163	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P14
	PCIE_MTX_C_GRX_N14	F37	PCIE_RX14N	PCIE_TX14N	K29	PCIE_GTX_MRX_N14	C165	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N14
T6 PAD	PCIE_MTX_C_GRX_P15	F35	PCIE_RX15P	PCIE_TX15P	H33	PCIE_GTX_MRX_P15	C166	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P15
T7 PAD	PCIE_MTX_C_GRX_N15	E37	PCIE_RX15N	PCIE_TX15N	H32	PCIE_GTX_MRX_N15	C168	1	2	PM@	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N15

CLOCK

25 CLK_PCIE_VGA — CLK_PCIE_VGA — AB35 — PCIE_REFCLKP
25 CLK_PCIE_VGA# — CLK_PCIE_VGA# — AA36 — PCIE_REFCLKN

AJ21 NC#1
AK21 NC#2
PWRGOOD_BUF — AH16 — NC_PWRGOOD

28 PLTRST_VGA# — PLTRST_VGA# — AA30 — PERSTB

R339 10K_0402_5% MAD@

CALIBRATION

PCIE_CALRP — Y30 — PCIE_CALRP — R44 1.27K_0402_1% PM@
PCIE_CALRN — Y29 — PCIE_CALRN — R43 2K_0402_1% PM@ — +1.1VS

DVT Rual: Change this power to +1.0VS! 06/09

216-0729042-00 A13 M96 BGA 962P 030
PM@

the same with M86

U4G

LVDS CONTROL

PM@ 10K_0402_5%
R161 2 1
VARY_BL — AK27 — VGA_PWM 22
DIGON — AJ27 — VGA_ENVDD 22
R162 2 1 PM@10K_0402_5%

TXCLK_UP_DPF3P	AK35	VGA_LVDS_BCLK	22
TXCLK_UN_DPF3N	AL36	VGA_LVDS_BCLK#	22
TXOUT_U0P_DPF2P	AJ38	VGA_LVDS_B0	22
TXOUT_U0N_DPF2N	AK37	VGA_LVDS_B0#	22
TXOUT_U1P_DPF1P	AH35	VGA_LVDS_B1	22
TXOUT_U1N_DPF1N	AJ36	VGA_LVDS_B1#	22
TXOUT_U2P_DPF0P	AG38	VGA_LVDS_B2	22
TXOUT_U2N_DPF0N	AH37	VGA_LVDS_B2#	22
TXOUT_U3P	AF35		
TXOUT_U3N	AG36		

LVTMDP

TXCLK_LP_DPE3P	AP34	VGA_LVDS_ACLK	22
TXCLK_LN_DPE3N	AR34	VGA_LVDS_ACLK#	22
TXOUT_L0P_DPE2P	AW37	VGA_LVDS_A0	22
TXOUT_L0N_DPE2N	AU35	VGA_LVDS_A0#	22
TXOUT_L1P_DPE1P	AR37	VGA_LVDS_A1	22
TXOUT_L1N_DPE1N	AU39	VGA_LVDS_A1#	22
TXOUT_L2P_DPE0P	AP35	VGA_LVDS_A2	22
TXOUT_L2N_DPE0N	AR35	VGA_LVDS_A2#	22
TXOUT_L3P	AN36		
TXOUT_L3N	AP37		

216-0729042-00 A13 M96 BGA 962P 030
PM@

Need check

+1.8VSDGPU — R115 2K_0402_1% M97@
+3VS_DELAY — R116 2K_0402_1% @
PWRGOOD_BUF — R117 M97@ 0_0402_5% — EC_VGAPWRGOOD 39
C251 M97@ 0.22U_0402_10V4Z
R118 2.37K_0402_1% @
item 02, Add M97@ 05/06

Security Classification	Compal Secret Data		
Issued Date	2009/02/24	Deciphered Date	2009/07/15

Compal Electronics,Ltd.

Title: M96- PCIE Interface

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 13 of 61

Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
	GPIO23 GPIO21	Reserved	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[2:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	1 1
	GENERICC H2SYNC	Reserved Reserved	0
VIP_DEVICE_STRAP_EN	V2SYNC		0

External VGA Thermal Sensor

+3VS_DELAY
R250 330_0402_5% PM@
C224 0.1U_0402_16V4Z PM@
U1 ADM1032ARMZ-2REEL_MSOP8 PM@
VDD SCLK SDATA D+ D- ALERT# THERM# GND
2200P_0402_50V7K C223 PM@
R817 4.7K_0402_5% PM@
R95 4.7K_0402_5% R94 4.7K_0402_5%
EC_SMB_CK2 25,39
EC_SMB_DA2 25,39
VGA_THERM# 39

03/06 Updated by Tock

Location / VRAM	MEM_ID0 (R110)	MEM_ID1 (R109)	MEM_ID2 (R108)	MEM_ID3 (R8)
Samsung	1	O	O	O
HYNIX	O	O	O	O

+3VS_DELAY

SI2301BDS_SOT23 Q1
06/09 DVT, soft start ice
C201 0.1U_0402_16V7K
R343 10K_0402_5%
R103 100K_0402_5%
R111 100K_0402_5%
C241 0.1U_0402_16V4Z
Q2 SSM3K7002FU_SC70-3
43,48,56,58 VGA_ON

PWR Sequence

+3VS_DELAY
VGA_CORE (VDDC)
+1.8VS

For ATI debug

GPIO24_TRSTB
GPIO25_TDI
GPIO26_TCK
GPIO27_TMS
GPIO28_TDO
CLK_VGA_27M 23
15 TESTEN
ATI Option 2 debug

4/2 Add by Vivian

C814 100P_0402_50V8J GPU_VID0

item 15, Add @ M96@ add L31 05/06
Rual Change to M96@!
DVT Rual: Change this power to +1.0S

4/24 ATI suggest

R101 2.2K_0402_5% PM@
R100 2.2K_0402_5% PM@
R10 10K_0402_5% PM@
R9 10K_0402_5% PM@

U4B
216-0729042-00 A13 M96 BGA 962P 030
PM@

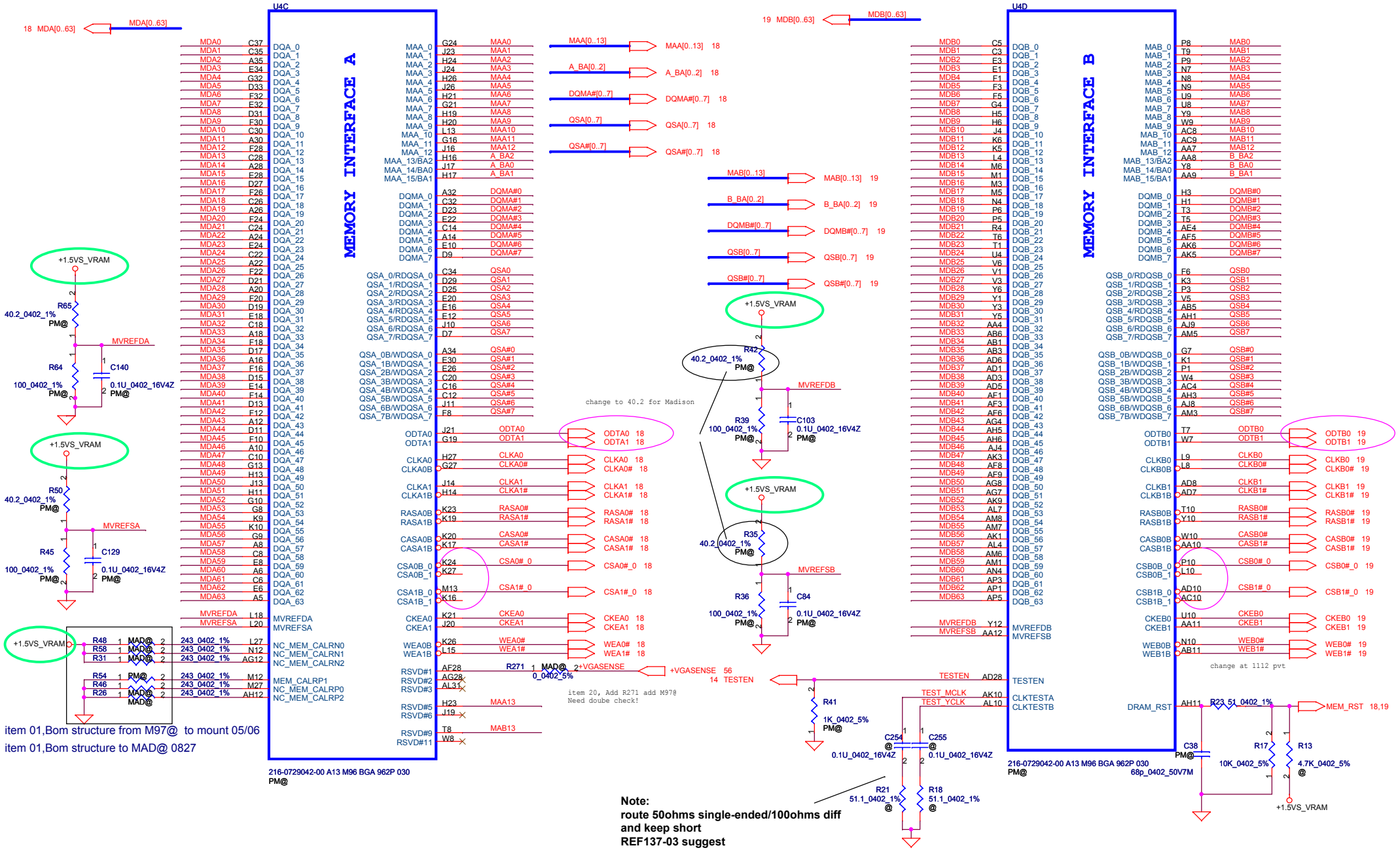
Security Classification	Compal Secret Data
Issued Date	2009/02/24
Deciphered Date	2010/02/24

Compal Electronics, Inc.

Title: M96 PCIE,LVDS,GPIO,CLK

Size: C | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 14 of 61



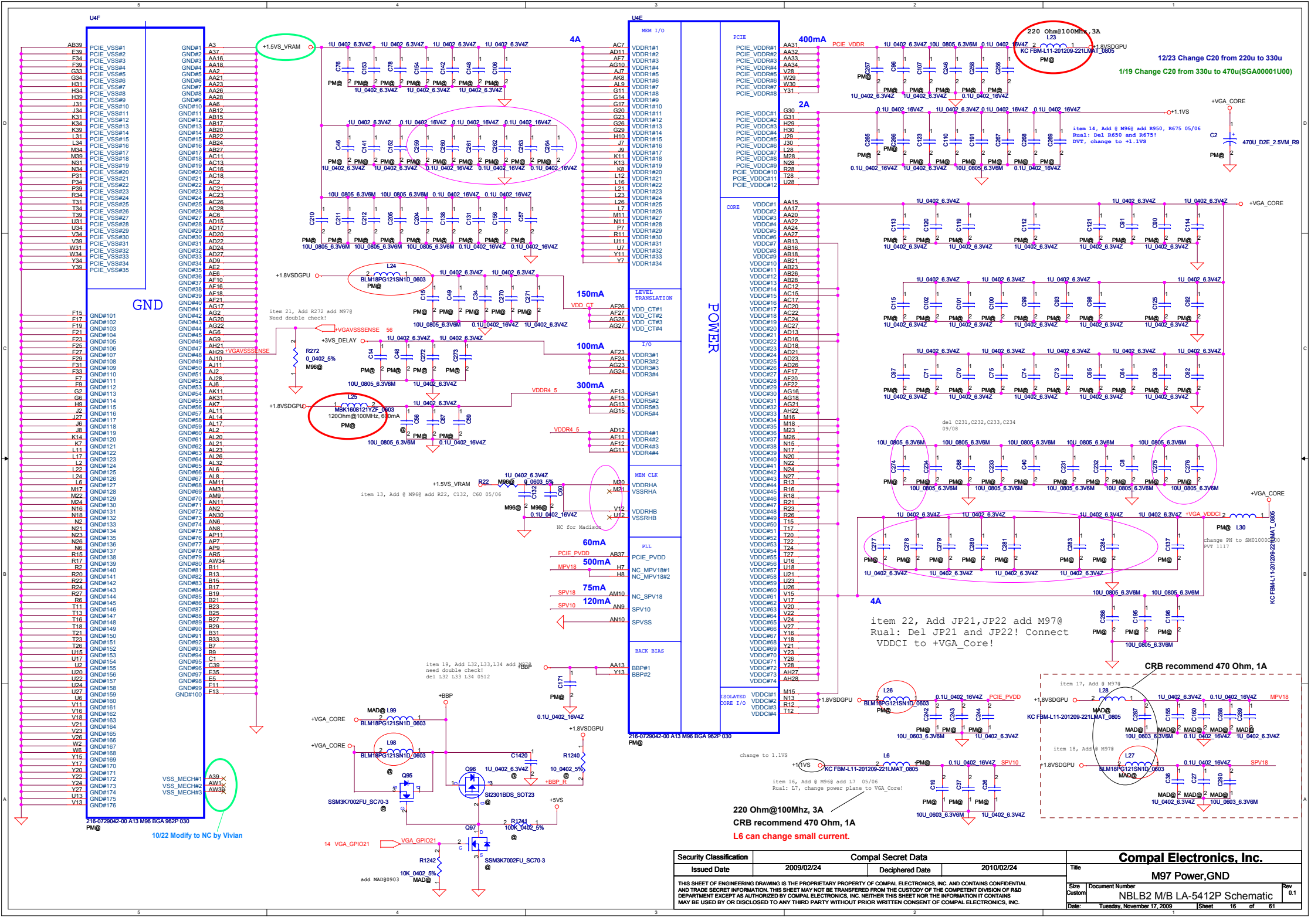
Security Classification	Compal Secret Data		
Issued Date	2009/02/24	Deciphered Date	2010/02/24

Compal Electronics, Inc.

Title: M96 Memory

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 15 of 61



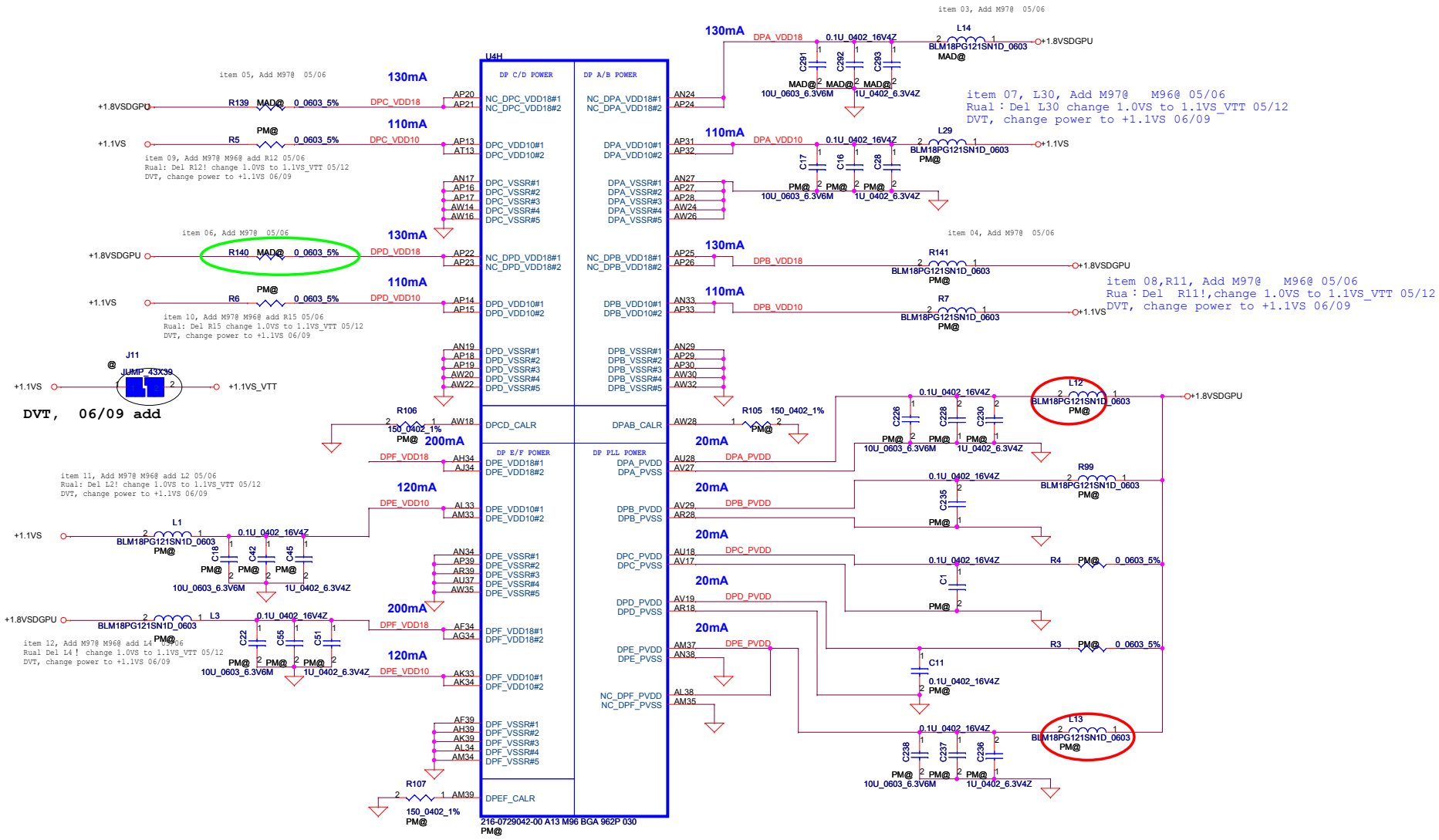
Security Classification	Compal Secret Data		
Issued Date	2009/02/24	Deciphered Date	2010/02/24

Compal Electronics, Inc.

Title: M97 Power,GND

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 16 of 61

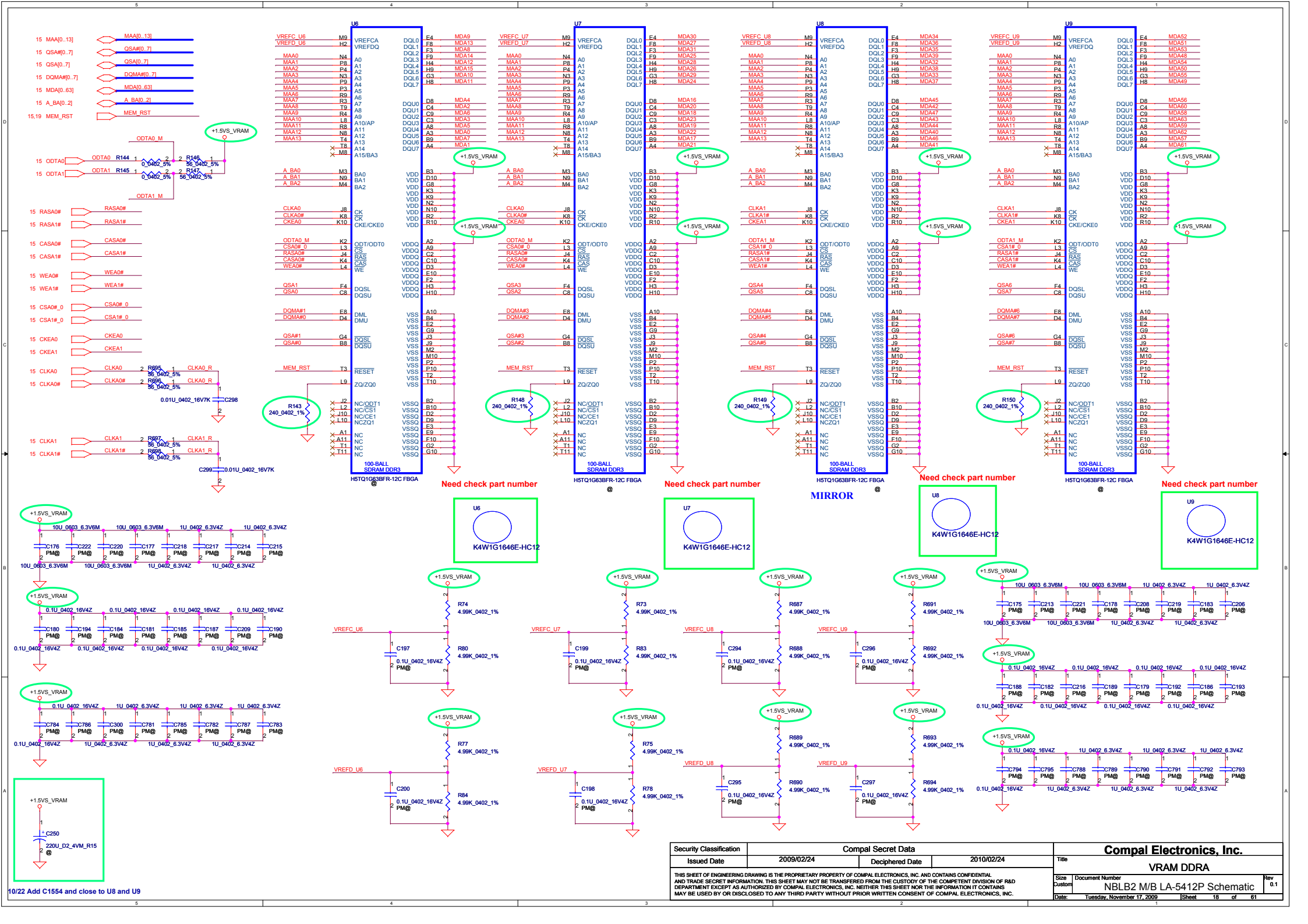


There is no use on DPB/DPC/DPD,DPB_VDD10, DPC_VDD10, DPD_VDD10, DPB_PVDD, DPC_PVDD and DPD_PVDD can be powered without filter

Security Classification	Compal Secret Data		
Issued Date	2009/02/24	Deciphered Date	2010/02/24

Compal Electronics,Ltd.

Title	M96	
Size: Custom	Document Number: NBLB2 M/B LA-5412P Schematic	Rev: 0.1
Date: Friday, November 13, 2009	Sheet 17 of 61	



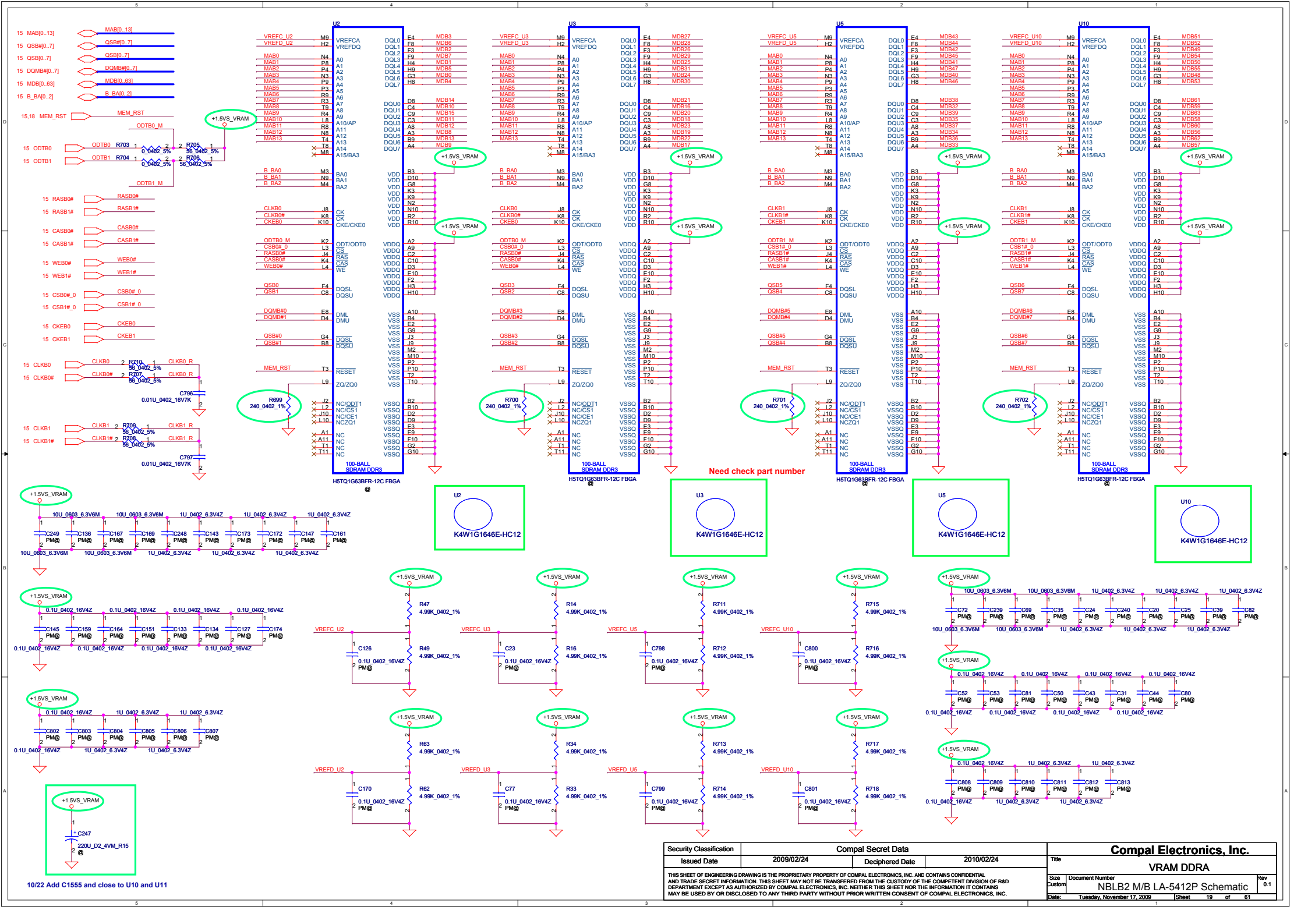
Security Classification	Compal Secret Data		
Issued Date	2009/02/24	Deciphered Date	2010/02/24

Compal Electronics, Inc.

Title: VRAM DDRA

Size	Document Number	Rev
Custom	NBLB2 M/B LA-5412P Schematic	0.1

Date: Tuesday, November 17, 2009 | Sheet 18 of 61



Security Classification	Compal Secret Data		
Issued Date	2009/02/24	Deciphered Date	2010/02/24

Compal Electronics, Inc.

Title: VRAM DDRA

Size	Document Number	Rev
Custom	NBLB2 M/B LA-5412P Schematic	0.1

Date: Tuesday, November 17, 2009 | Sheet 19 of 61

have the pull high on PCH/VGA side

DVT, change HDMI detec 06/09

TMDS pull down (500ohm) resistors G9x only

NEAR CONNECT

Same as Nvidia and ATI

DGPU_SELECT#
L: 0 -> Y(Madison)
H: 1 -> Y(PCH)

OE#--SEL1--SEL2--Result
1----X----X----Hi-Z
0----1----0----A active
0----0----1----B activve
0----0----0----B all port dis

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics,Ltd.

Title: HDMI Conn

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 20 of 61

CRT Connector

Checklist recommend: 2-pole filter on R/G/B signals
C - L - C - L - C
10p - 47 Ohm/100MHz - 22p - 47 Ohm/100MHz - 10p

12/15 Modified. Note L26~L30 are 0 Ohm resisters (IFTXX)

Change PCB footprint of L45/ L47/ L49 from L_0603 to R_0603

Change PCB footprint of L43 from L_0805 to R_0805

W=40mils

W=40mils

Place closed to chipset

Change PCB footprint of L50/L51 from L_0603 to R_0603

12/22 Change to SE071680J80 (IFTXX)

Add IFTXX
Andy_1102

L: 0 -> Y(PCH)
H: 1 -> Y(M96)

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

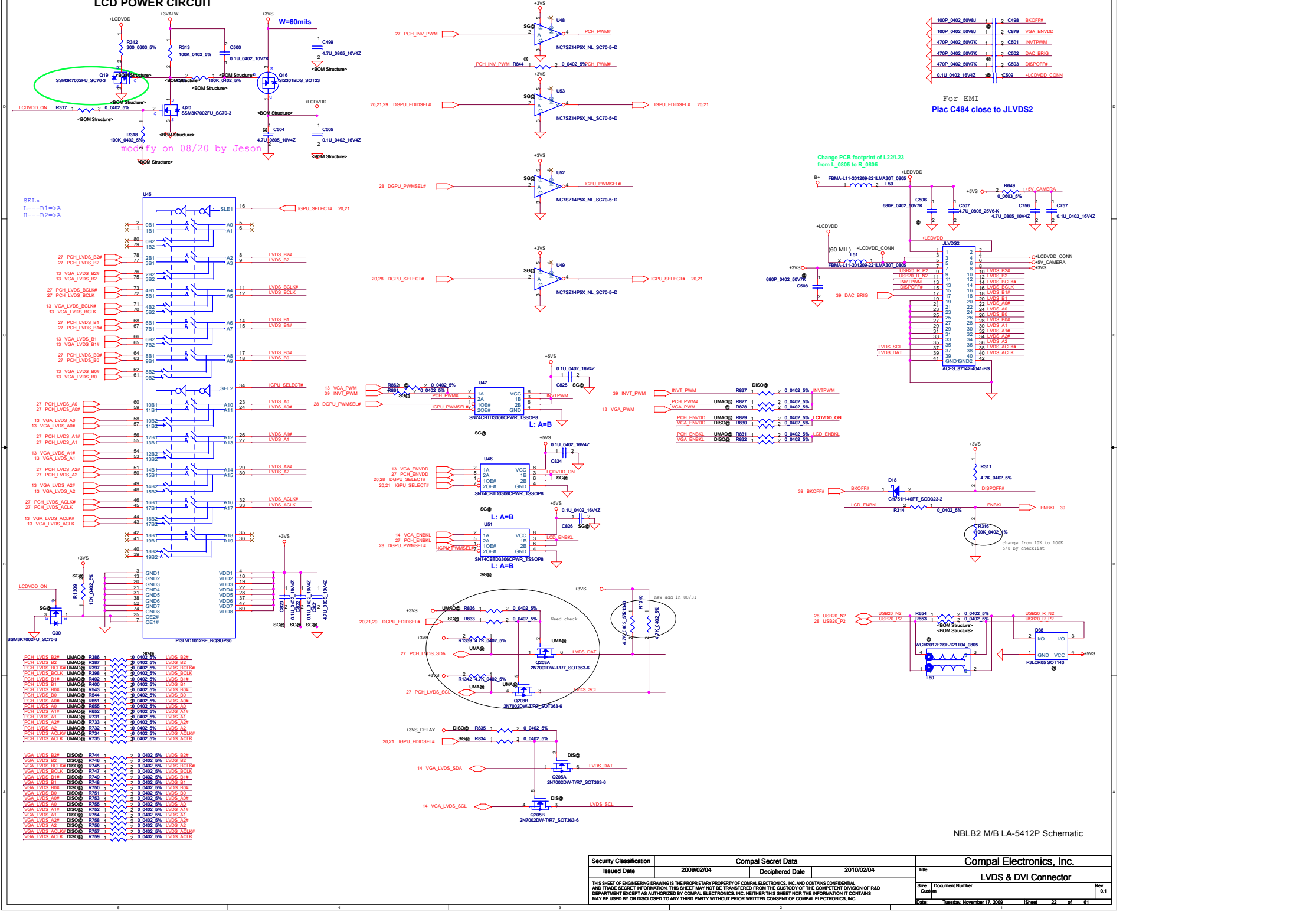
Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 21 of 61

LCD POWER CIRCUIT



Security Classification	Compal Secret Data		Compal Electronics, Inc.
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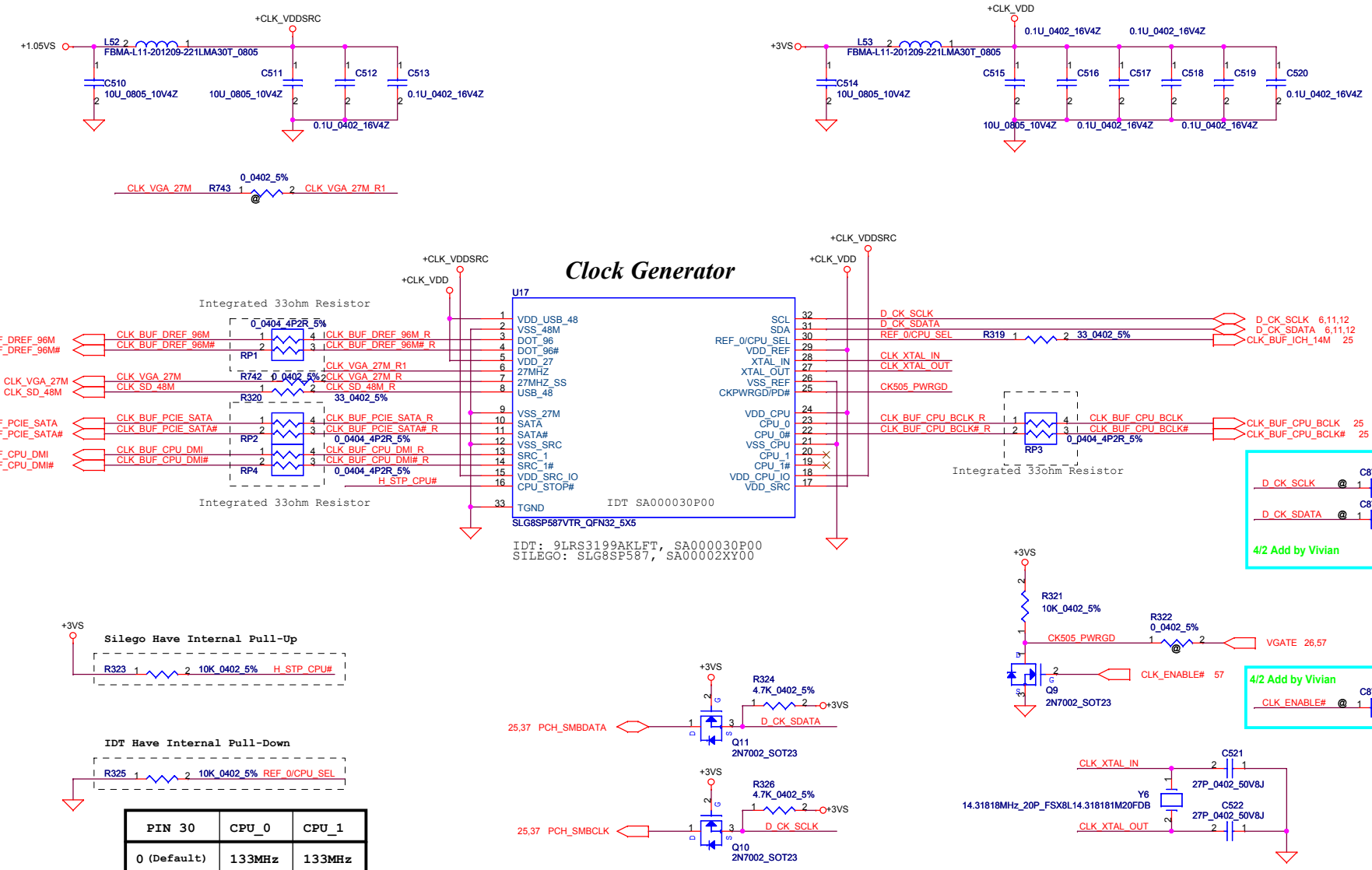
			Size: Custom; Document Number; Rev: 0.1
			Date: Tuesday, November 17, 2009; Sheet 22 of 61



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 23 of 61

DVT 06/09 ice add

RC Delay 18~25mS

close to RAM door

RC Delay 18~25mS

close to RAM door

2/26 Change R1519 to 330K

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

HDA for AUDIO

SATA for HDD1

SATA for ODD

12/26 SATA2/SATA3 Desktop Only

Have internal PD

3/16 Change to 0 ohm(Follow Intel's comment)

3/26 Add

EMI

3/20 Modify By Vivian

Project Port ID

2008 Intel MOW36/MOW50

TDO:
Reserved on ES1 Sample
Mount R369, R370 on ES2 Sample

MP mount R363, R368, R371, R374 and remove others

PCH_PIN	RefDes	PCH_JTAG		PCH_JTAG
		ES1	ES2	MP
PCH_JTAG_TDO	R369	No Install	200ohm	No Install
	R370	No Install	100ohm	No Install
PCH_JTAG_TMS	R364	200ohm	200ohm	No Install
	R366	100ohm	100ohm	No Install
PCH_JTAG_TDI	R372	200ohm	200ohm	No Install
	R373	100ohm	100ohm	No Install
PCH_JTAG_TCK	R380	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R376	20Kohm	20Kohm	No Install
	R378	10Kohm	10Kohm	No Install

enable iTPM: SPI_MOSI High

CRB 1.0 Change to 4.7K

Need double check

3/16 Change R380 to 51 ohm(follow Intel's comment)

3/20 Modify By Vivian

SPI ROM Footprint 150mil

11/18 SPI ROM Change to SA00002TO00
3/20 SPI ROM Change to SA00001KN10(Follow NIWBA)

Project ID table		
	ID1	ID0
DIS	0	0
SG	0	1
UMA	1	1

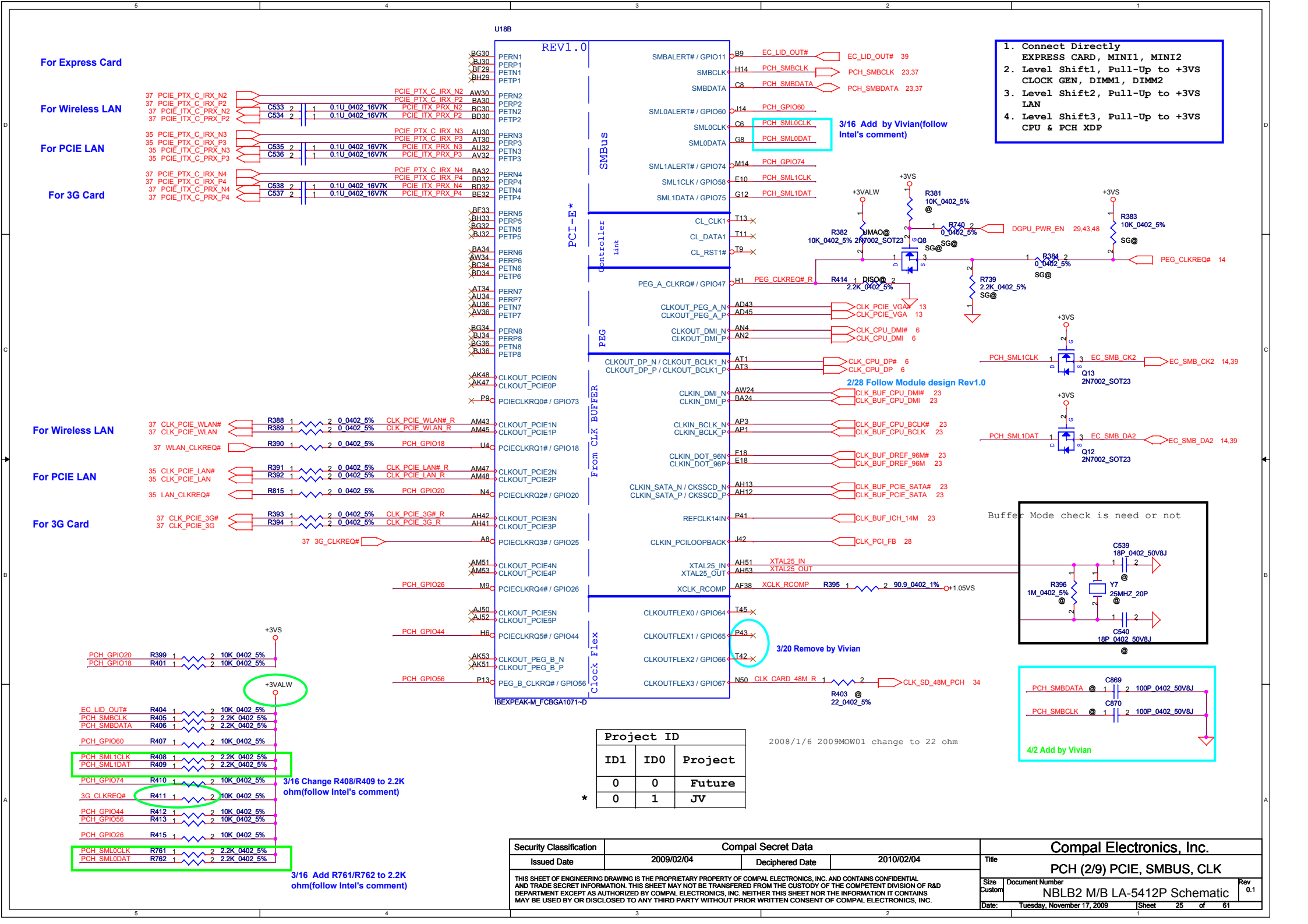
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 24 of 61



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

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Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 25 of 61

5 DMI_HTX_PRX_N[0..3] → DMI_HTX_PRX_N[0..3]
5 DMI_HTX_PRX_P[0..3] → DMI_HTX_PRX_P[0..3]
5 DMI_PTX_HRX_N[0..3] → DMI_PTX_HRX_N[0..3]
5 DMI_PTX_HRX_P[0..3] → DMI_PTX_HRX_P[0..3]

U18C

REV1.0

DMI_HTX_PRX_N0 BC24 DMI0RXN
DMI_HTX_PRX_N1 BJ22 DMI1RXN
DMI_HTX_PRX_N2 AW20 DMI2RXN
DMI_HTX_PRX_N3 BJ20 DMI3RXN
DMI_HTX_PRX_P0 BD24 DMI0RXP
DMI_HTX_PRX_P1 BG22 DMI1RXP
DMI_HTX_PRX_P2 BA20 DMI2RXP
DMI_HTX_PRX_P3 BG20 DMI3RXP
DMI_PTX_HRX_N0 BE22 DMI0TXN
DMI_PTX_HRX_N1 BF21 DMI1TXN
DMI_PTX_HRX_N2 BD20 DMI2TXN
DMI_PTX_HRX_N3 BE18 DMI3TXN
DMI_PTX_HRX_P0 BD22 DMI0TXP
DMI_PTX_HRX_P1 BH21 DMI1TXP
DMI_PTX_HRX_P2 BC20 DMI2TXP
DMI_PTX_HRX_P3 BD18 DMI3TXP
BH25 DMI_ZCOMP
DMI_COMP BF25 DMI_IRCOMP

DMI

FDI

FDI_RXN0 BA18 FDI_CTX_PRX_N0
FDI_RXN1 BH17 FDI_CTX_PRX_N1
FDI_RXN2 BD16 FDI_CTX_PRX_N2
FDI_RXN3 BJ16 FDI_CTX_PRX_N3
FDI_RXN4 BA16 FDI_CTX_PRX_N4
FDI_RXN5 BE14 FDI_CTX_PRX_N5
FDI_RXN6 BA14 FDI_CTX_PRX_N6
FDI_RXN7 BC12 FDI_CTX_PRX_N7
FDI_RXP0 BB18 FDI_CTX_PRX_P0
FDI_RXP1 BF17 FDI_CTX_PRX_P1
FDI_RXP2 BC16 FDI_CTX_PRX_P2
FDI_RXP3 BG16 FDI_CTX_PRX_P3
FDI_RXP4 AW16 FDI_CTX_PRX_P4
FDI_RXP5 BD14 FDI_CTX_PRX_P5
FDI_RXP6 BB14 FDI_CTX_PRX_P6
FDI_RXP7 BD12 FDI_CTX_PRX_P7
FDI_INT BJ14 FDI_INT → FDI_INT 5
FDI_FSYNC0 BF13 FDI_FSYNC0 → FDI_FSYNC0 5
FDI_FSYNC1 BH13 FDI_FSYNC1 → FDI_FSYNC1 5
FDI_LSYNC0 BJ12 FDI_LSYNC0 → FDI_LSYNC0 5
FDI_LSYNC1 BG14 FDI_LSYNC1 → FDI_LSYNC1 5

08/20 ADD
FDI for SG
FDI_CTX_PRX_N[0..7] 5
FDI_CTX_PRX_P[0..7] 5

+3VS
R416 1 2 8.2K_0402_5% PM_CLKRUN#
R417 1 @ 2 10K_0402_5% XDP_DBRESET#

+3VALW
R419 1 2 10K_0402_5% SUS_PWR_ACK
R421 1 2 8.2K_0402_5% PCH_GPIO72
R422 1 2 10K_0402_5% EC_SWI#
R423 1 2 1K_0402_5% PCH_PCIE_WAKE#
R425 1 @ 2 10K_0402_5% PM_SLP_LAN#

+1.05VS
R420 49.9_0402_1% 1 2 DMI_COMP

System Power Management

6 XDP_DBRESET# → XDP_DBRESET# T6 SYS_RESET#
SYS_PWROK R426 0_0402_5% SYS_PWROK_R M6 SYS_PWROK
VGATE R427 @ 0_0402_5%
SYS_PWROK → B17 PWROK
R767 0_0402_5% MEPWROK K5 MEPWROK
3/24 Add
LAN_RST# A10 LAN_RST#
6 PM_DRAM_PWRGD → D9 DRAMPWROK
PCH_RSMRST# C16 RSMRST#
39 SUS_PWR_ACK → SUS_PWR_ACK M1 SUS_PWR_DN_ACK / GPIO30
10/2 Intel suggestion change to 10K
+3VALW R428 10K_0402_5% 6,39 PBTN_OUT# → PBTN_OUT# P5 PWRBTN#
39 EC_ACIN D19 CH751H-40PT_SOD323-2 PCH_ACIN P7 ACPRESENT / GPIO31
PCH_GPIO72 A6 BATLOW# / GPIO72
39 EC_SWI# → EC_SWI# F14 RI#

WAKE# J12 PCH_PCIE_WAKE# → PCH_PCIE_WAKE# 35,37
CLKRUN# / GPIO32 Y1 PM_CLKRUN# → PM_CLKRUN# 39,47
SUS_STAT# / GPIO61 P8 SUS_STAT# → SUS_STAT# 47
SUSCLK / GPIO62 F3 PCH_GPIO62 @ PAD T18
SLP_S5# / GPIO63 E4 PM_SLP_S5# 39
SLP_S4# H7 PM_SLP_S4# 39
SLP_S3# P12 PM_SLP_S3# 39
SLP_M# K8 PM_SLP_M# @ PAD T19
TP23 N2 PM_SLP_DSW# @ PAD T20
PMSYNCH BJ10 H_PM_SYNC 6
SLP_LAN# / GPIO29 F6 PM_SLP_LAN#

IBEXPEAK-M_FCBGA1071~D

R429 2 @ 1 0_0402_5%
Q15 MMBT3906_SOT23-3
PCH_RSMRST# → EC_RSMRST# 39
R430 10K_0402_5%
R431 4.7K_0402_5% +3VALW
D20A BAV99DW-7_SOT363
D20B BAV99DW-7_SOT363
R433 2.2K_0402_5%

R432 @ 0_0402_5%
+3VS
U21
SYS_PWROK → ICH_PWROK → ICH_PWROK 39
VGATE → VGATE 23,57
NC7SZ08P5X_NL_SC70-5

R725 @ 0_0402_5%
+3VS
U41
57 VR_ON → VR_ON_EC 39
PWR_GD 43
NC7SZ08P5X_NL_SC70-5

4/2 Add by Vivian
VGATE @ C866 100P_0402_50V8J
H_PM_SYNC @ C867 100P_0402_50V8J
PBTN_OUT# @ C868 100P_0402_50V8J
VR_ON @ C862 100P_0402_50V8J

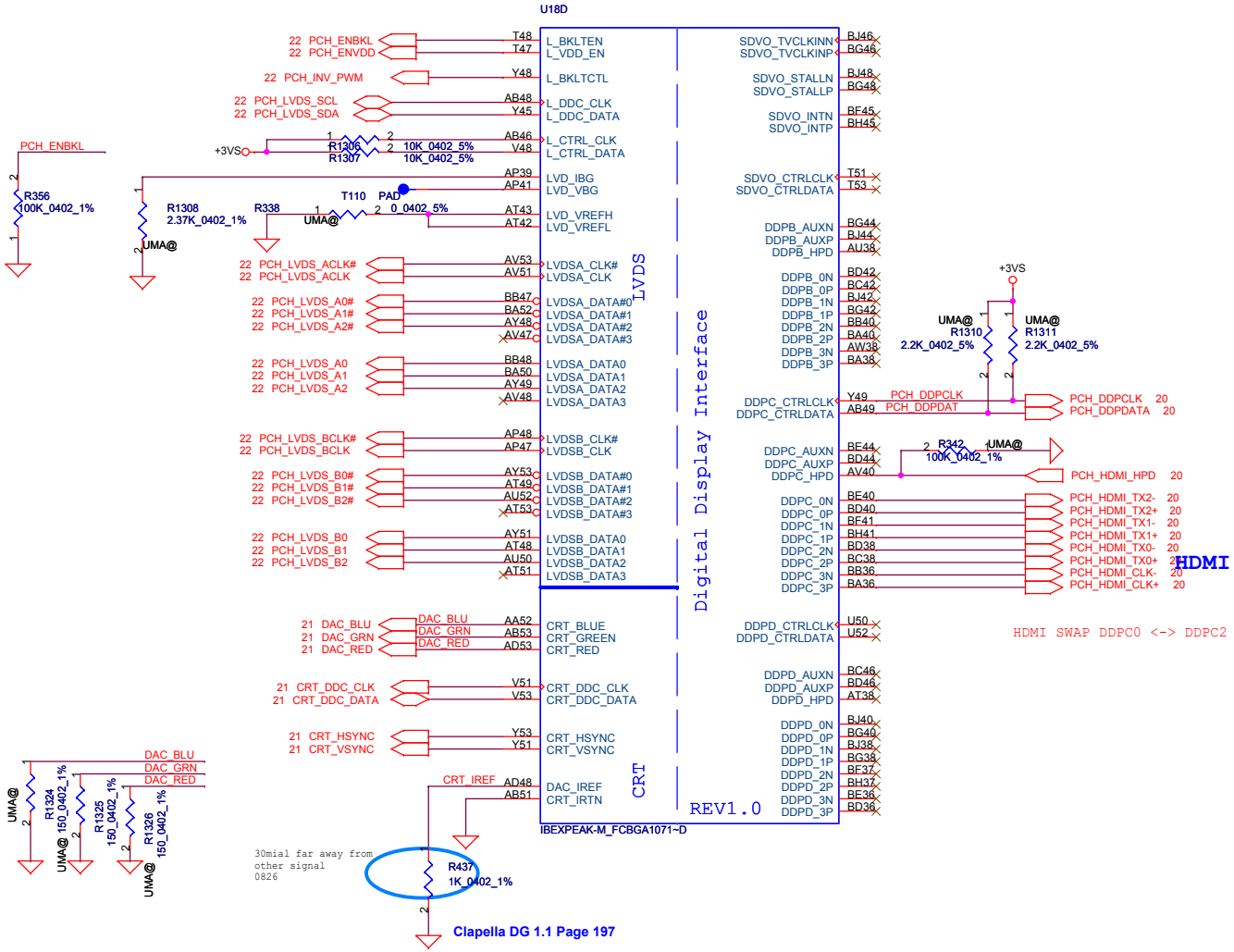
SYS_PWROK R434 10K_0402_5%
ICH_PWROK R435 10K_0402_5%
LAN_RST# R436 10K_0402_5%
No used Integrated LAN,
connecting LAN_RST# to GND

Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

Size	Document Number	Rev
Custom	NBLB2 M/B LA-5412P Schematic	0.1

Date: Tuesday, November 17, 2009 Sheet 26 of 61



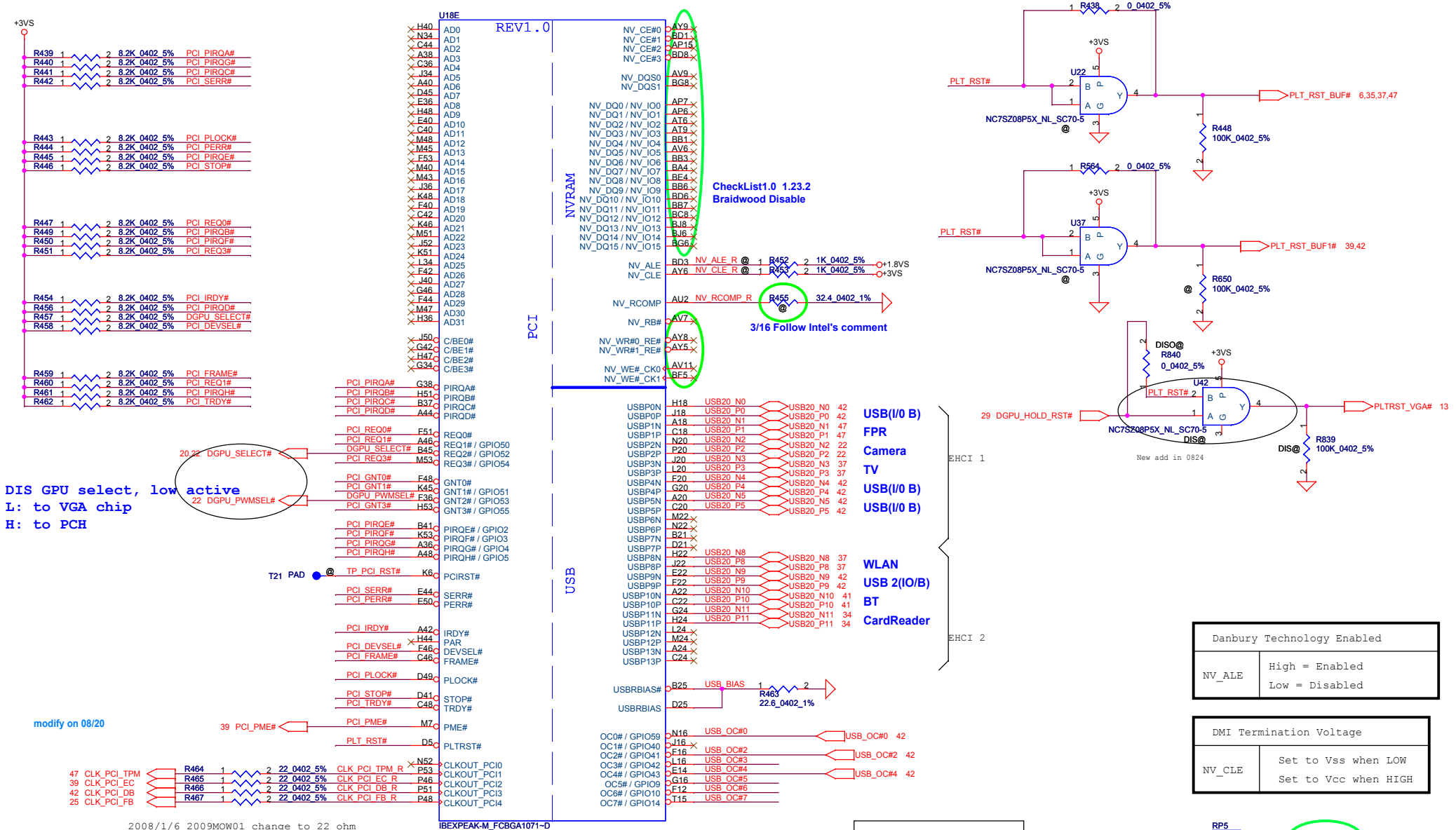
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 27 of 61



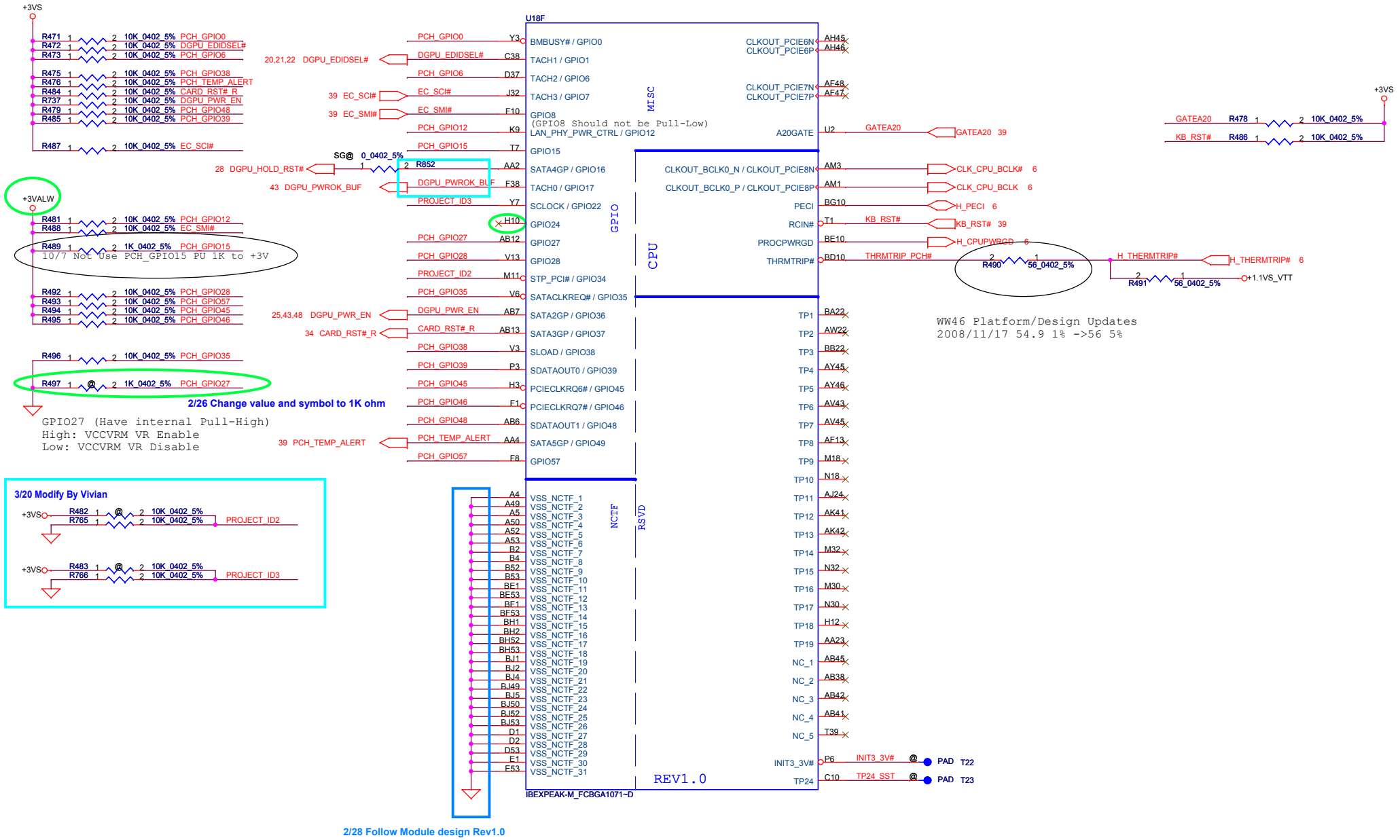
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 28 of 61



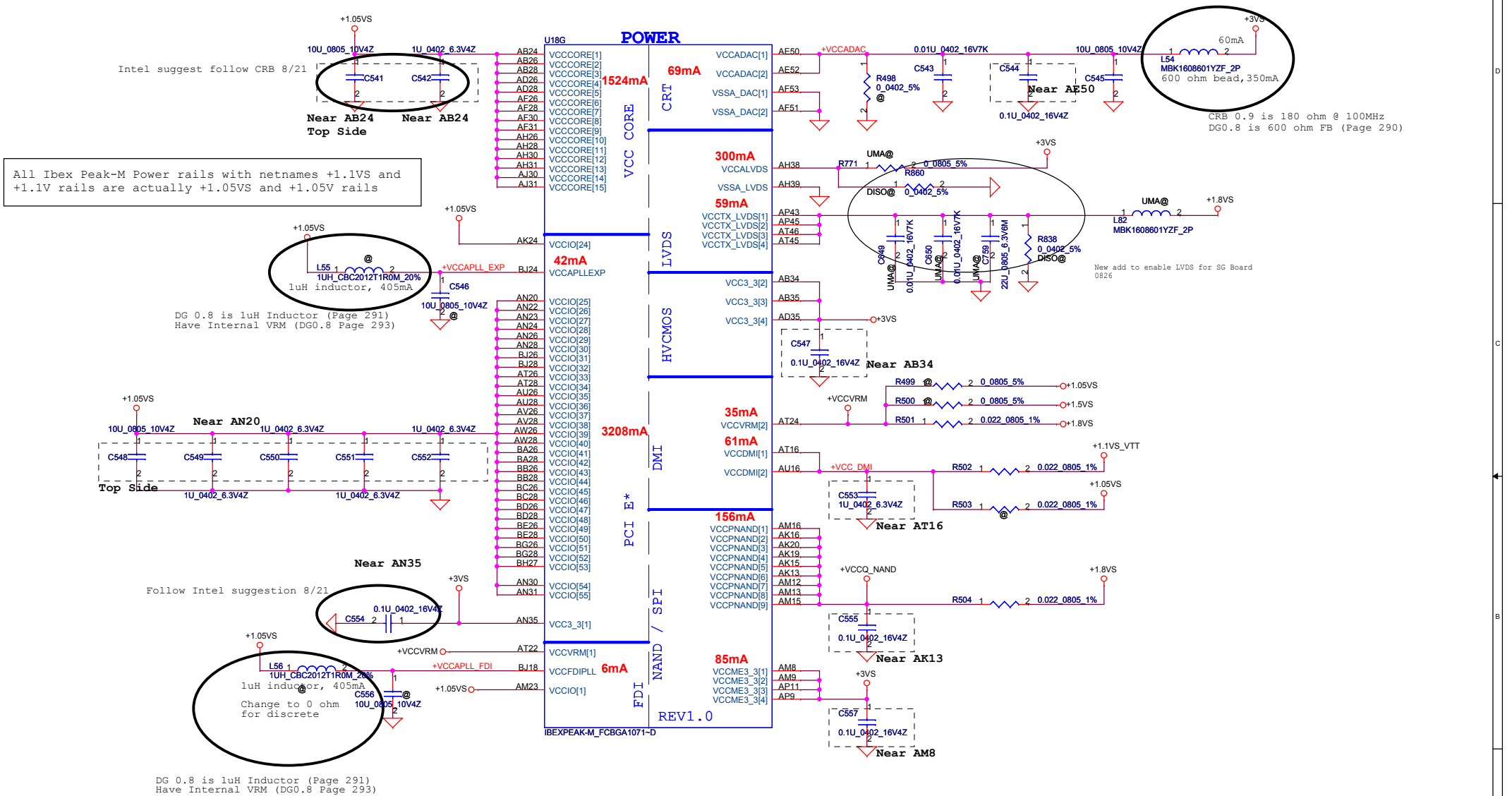
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 29 of 61



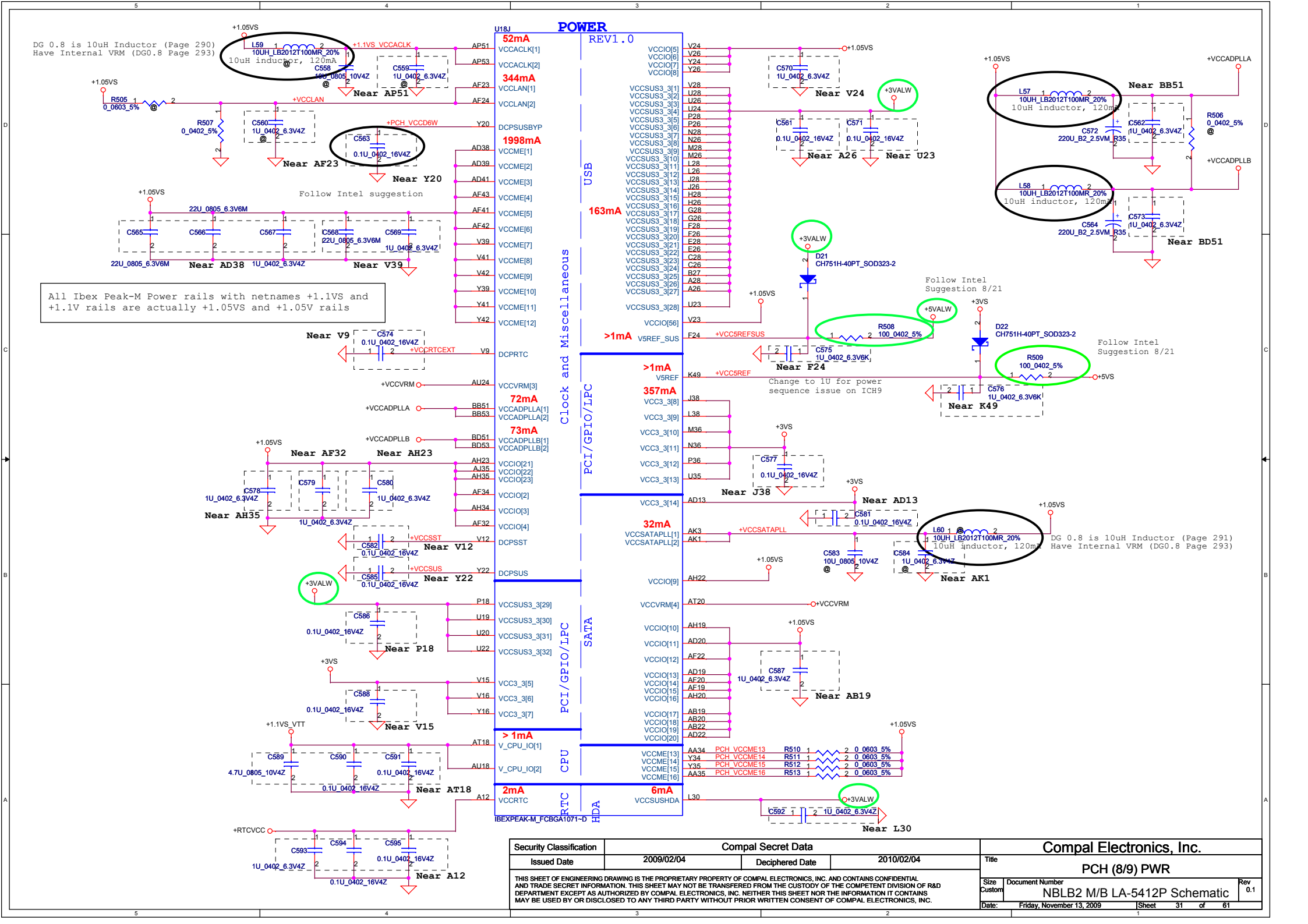
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size	Document Number	Rev
Custom	NBLB2 M/B LA-5412P Schematic	0.1

Date: Friday, November 13, 2009 Sheet 30 of 61



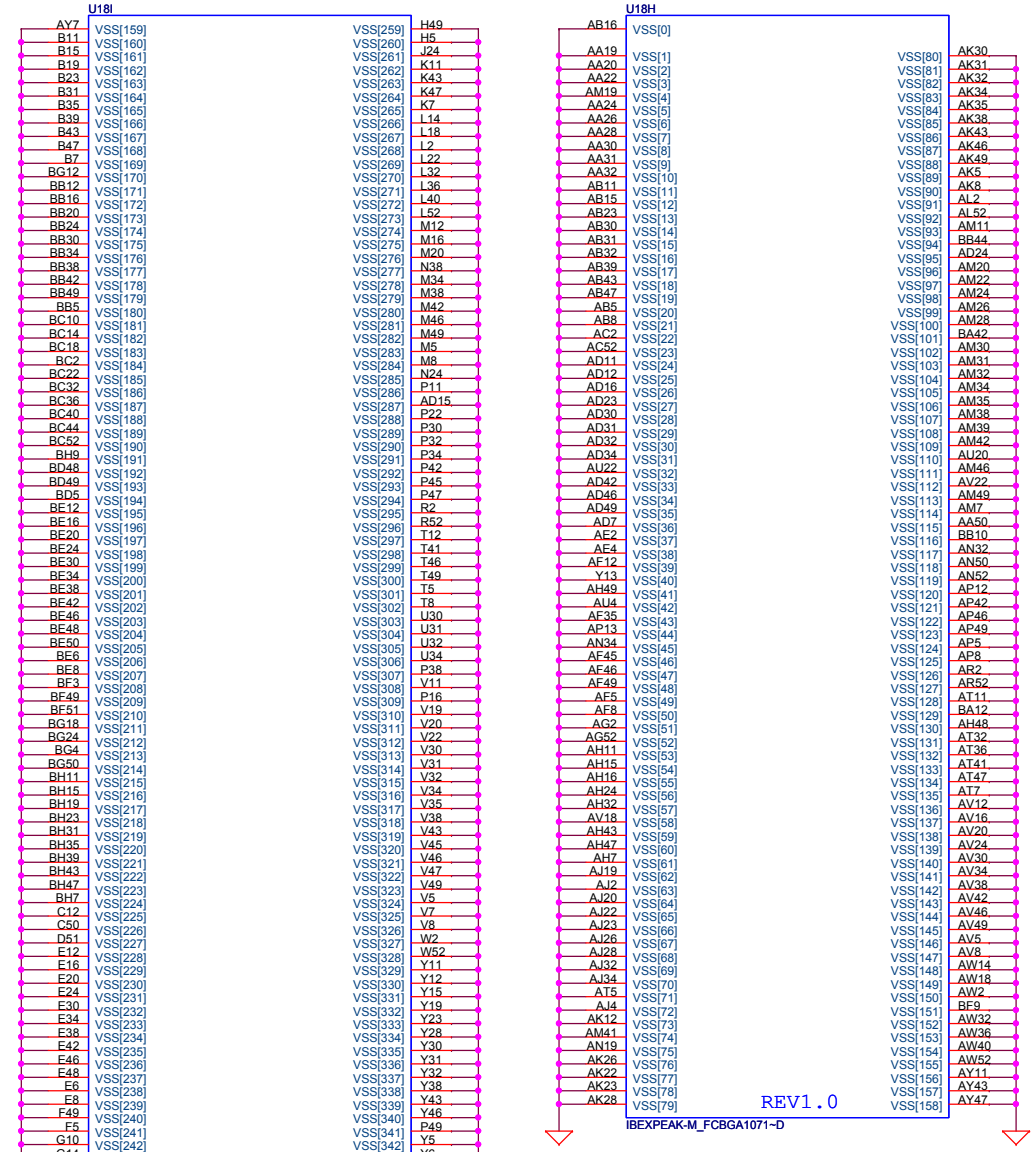
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size	Document Number	Rev
Custom	NBLB2 M/B LA-5412P Schematic	0.1

Date: Friday, November 13, 2009 | Sheet 31 of 61



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

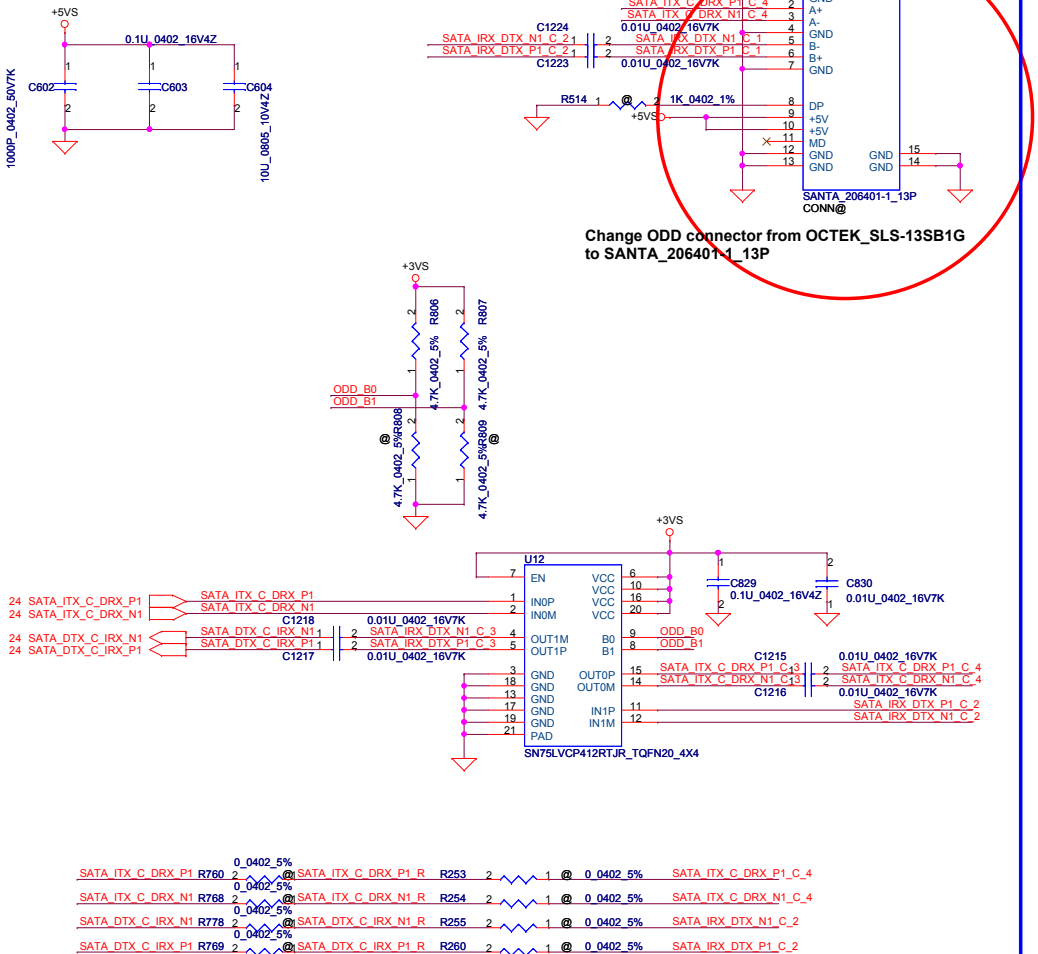
Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

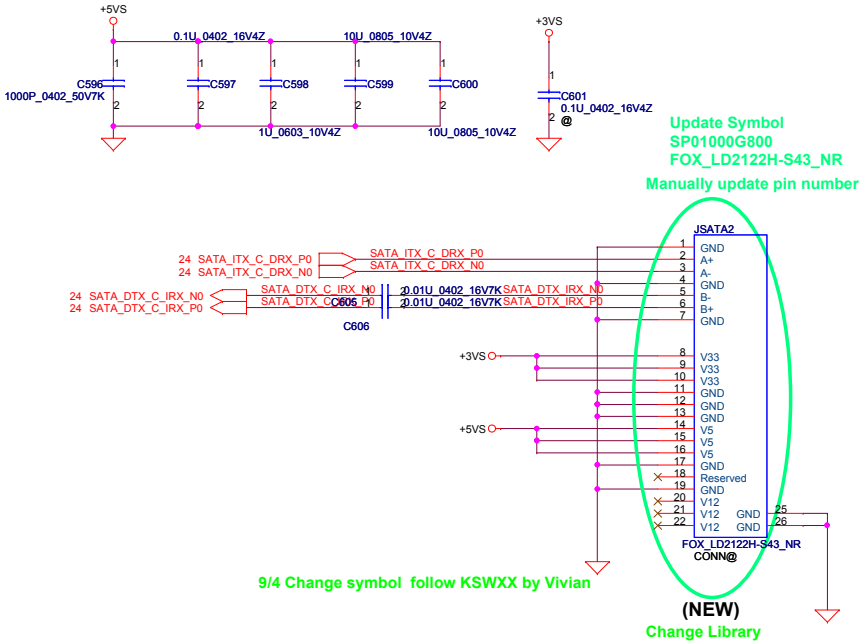
Size	Document Number	Rev
Custom	NBLB2 M/B LA-5412P Schematic	0.1

Date: Friday, November 13, 2009 Sheet 32 of 61

SATA ODD Conn.



SATA HDD Conn.



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: B | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

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SD,MMC,MS muti-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
SP1			
SP2	SDWP#		
SP3	SDCD#		
SP4	SDCDAT1		MSWR
SP5			MSBS
SP6			MSCDAT1
SP7	SDCDAT0		MSCDAT0
SP8	SDCDAT7		MSCDAT2
SP9			MS_INS#
SP10	SDCDAT6		MSCDAT3
SP11	SDCCLK		MSCCLK
SP12	SDCDAT5		MSCDAT6
SP13	SDCDAT4		MSCDAT7
SP14			
SP15	SDCDAT3		
SP16	SDCDAT2		
SP17			
SP18			
SP19			

Realtek Recommend

MODE_SEL C609 @ 47P_0402_50V8J R516 0_0402_5%

MS_CLK R515 @ 10_0402_5% C610 @ 10P_0402_50V8J

SD_CLK R517 @ 10_0402_5% C611 @ 10P_0402_50V8J

+3VS_CR_VCC C612 1U_0603_10V4Z C613 0.1U_0402_16V4Z C614 0.1U_0402_16V4Z

0.1U_0402_16V4Z C615 1U_0603_10V4Z C616 0.1U_0402_16V4Z AV_PLL +VCC_OUT

U23

AV_PLL 20mil (+1.8V internal regulator)

AV_PLL, NC, NC, CARD_3V3, D3V3, D3V3

+3VS_CR_VCC R518 0_0603_5% +3VALW R520 @ 0_0603_5% C617 4.7U_0805_10V4Z C618 0.1U_0402_16V4Z

29 CARD_RST#_R R519 @ 0_0402_5%

+3V3_IN, CARD_RST#, MODE_SEL, CARD_XTLO, CARD_XTLI

28 USB20_N11 28 USB20_P11

3V3_IN, RST#, MODE_SEL, XTLO, XTLI, DM, DP, GPIO0

VREG, MS_D4, NC

XD_CLE_SP19, XD_CE#_SP18, XD_ALE_SP17, SD_DAT2/XD_RE#_SP16, SD_DAT3/XD_WE#_SP15, XD_RDY_SP14, SD_DAT4/XD_WP#/MS_D7_SP13, SD_DAT5/XD_D0/MS_D6_SP12, SD_CLK/XD_D1/MS_CLK_SP11, SD_DAT6/XD_D7/MS_D3_SP10, MS_INS#_SP9, SD_DAT7/XD_D2/MS_D2_SP8, SD_DAT0/XD_D6/MS_D0_SP7, SD_DAT1/XD_D3/MS_D1_SP6, XD_D5_SP5, XD_D4/SD_DAT1_SP4, SD_CD#_SP3, SD_WP_SP2, XD_CD#_SP1, EEDI

SDDAT2_XDRE#, SDDAT3_XDWE#, SDCLK_MSCLK, SDDAT6_MSD3, MS_INS#, SDDAT7_MSD2, SDDAT0_MSD0, SP6, MS_BS, XDD4_SDDAT1, SD_CD#, SD_WP, CARD_EEDI

XTAL_CTR, MS_D5, EEDO, EECS, EESK, SD_CMD

CARD_EEDO, CARD_EECS, CARD_EESK, SD_CMD

R522 0_0402_5% SD_CLK, R523 0_0402_5% MS_CLK

+3VS_CR_VCC R526 0_0402_5%

+3VS_CR_VCC R521 @ 100K_0402_5% Internal 200K pull up

R524 0_0603_5% CARD_RST# C619 1U_0603_10V4Z R525 @ 499K_0402_1%

R527 6.19K_0402_1% R530 0_0402_5% AGND1

RREF, DGND, DGND, AGND, AGND

23 CLK_SD_48M R528 0_0402_5% CARD_XTLI Y8 @ 12MHZ_16P_6X12000012 CARD_XTLO

25 CLK_SD_48M_PCH R529 @ 0_0402_5% R531 @ 270K_0402_5%

C621 @ 6P_0402_50V8J C622 @ 6P_0402_50V8J

S IC RTS5159-GR LQFP 48P CARD READER

2/17 Change Part number of U25 from SA00001NK10 to SA00002YP00

+3VS_CR_VCC C620 @ 0.1U_0402_16V4Z U24 AT93C46-10SI-2.7_SO8 @

VCC, NC, NC, GND, CS, SK, DI, DO

CARD_EECS, CARD_EESK, CARD_EEDO, CARD_EEDI

4/2 Add by Vivian C878 100P_0402_50V8J @ CLK_SD_48M

+VCC_3IN1 JREAD1

SDDAT0_MSD0, XDD4_SDDAT1, SDDAT2_XDRE#, SDDAT3_XDWE#, SD_CLK, SD_WP, SD_CMD, SD_CD#

VDD_SD, DAT0_SD, DAT1_SD, DAT2_SD, CD/DAT3_SD, CLK_SD, WP_SD, CMD_SD, CD_SD, VSS_SD, VSS_SD

SP6, MS_CLK, MS_INS#, SDDAT0_MSD0, MS_BS, SDDAT6_MSD3, SDDAT7_MSD2

VCC_MS, VCC_MS, SCLK_MS, INS_MS, SDIO_MS, BS_MS, RESERVED_MS, RESERVED_MS, VSS_MS, VSS_MS, GND, GND

PROCO_MDR019-C0-1202 CONN@

+VCC_3IN1 +VCC_OUT R532 0_0603_5% 40mil

C623 4.7U_0805_10V4Z 10U_0805_10V4Z C624 @ C625 0.1U_0402_16V4Z

Add C822 4.7u and reserve C808 10u for cost down Michael 2008/5/30

+3VS W=40mils C626 @ 0.1U_0402_16V4Z C627 @ 1U_0603_10V4Z R533 0_0805_5%

39 CR_ON# R534 @ 100K_0402_5% Q17 SI2301BDS_SOT23 @ W=40mils +3VS_CR_VCC

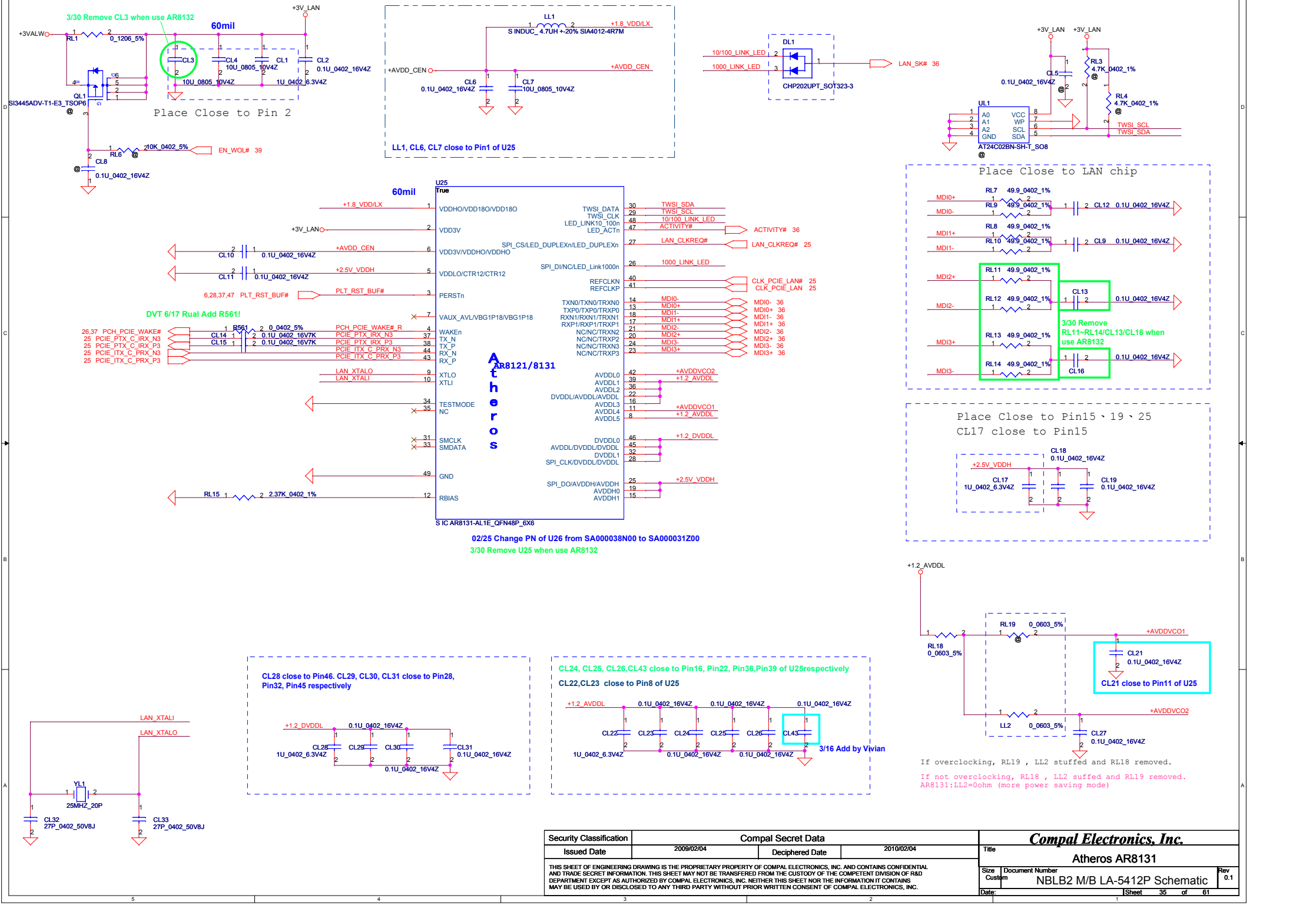
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: RTS5159 Cardreader

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 34 of 61



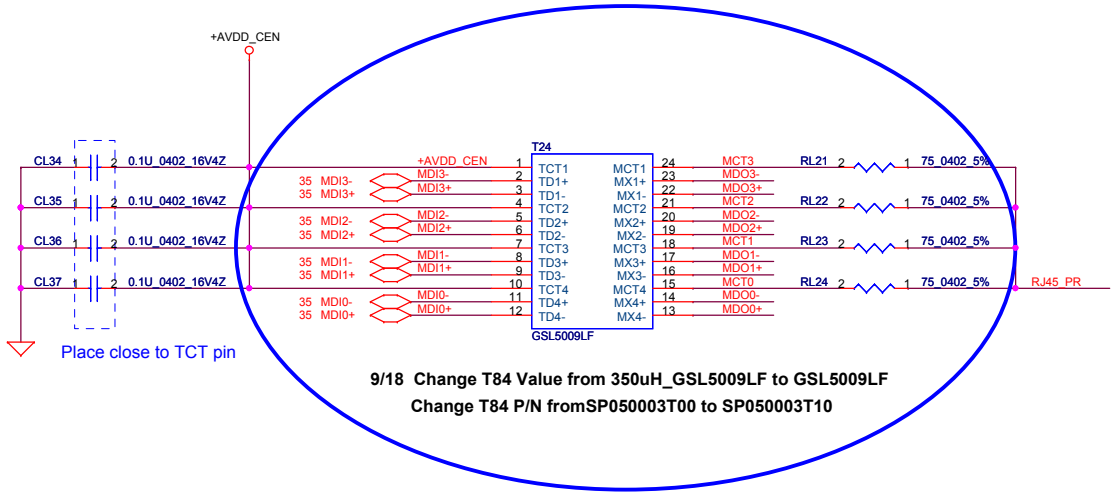
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

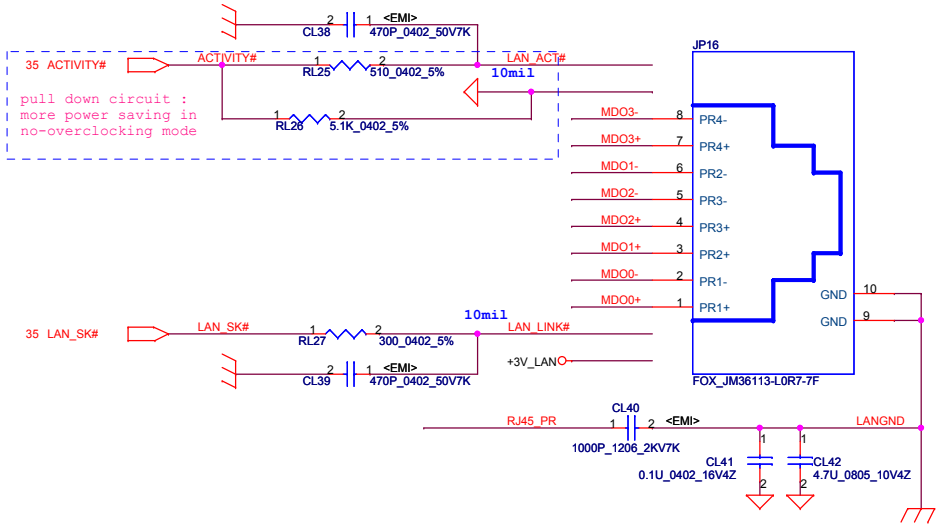
Title: Atheros AR8131

Size	Document Number	Rev
Custom	NBLB2 M/B LA-5412P Schematic	0.1

Date: | Sheet 35 of 61



Lan Conn.



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: LAN CONNECTOR

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

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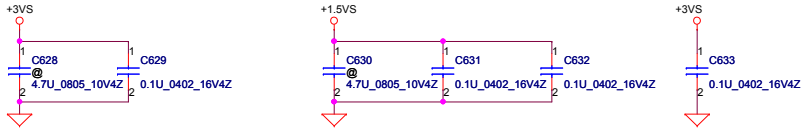
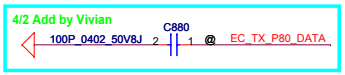
Mini-Express Card for TV Tuner

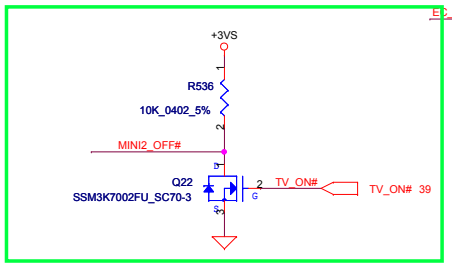


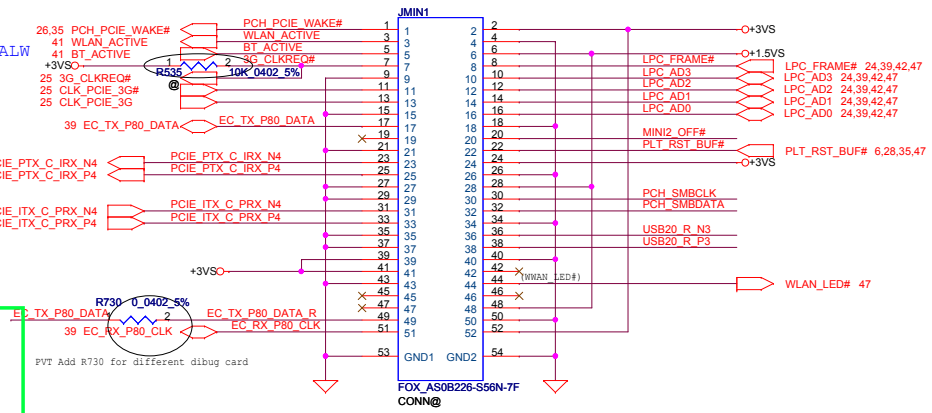
there is a pull high at +3V_ALW
05/19

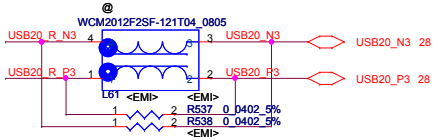
4/2 Add by Vivian



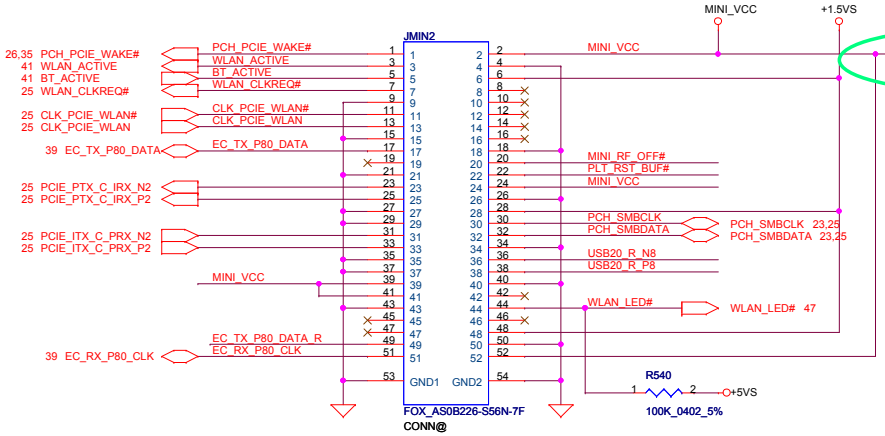
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



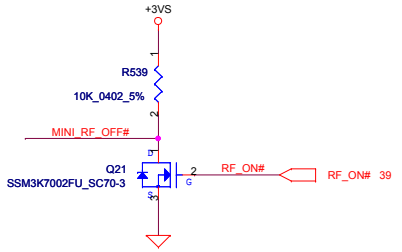


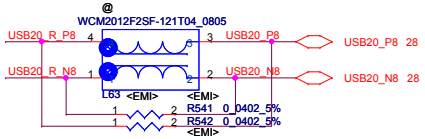


Mini-Express Card for WLAN

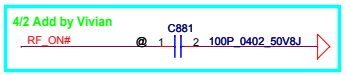


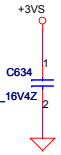
Change PCB footprint of L59 from L_0805 to R_0805

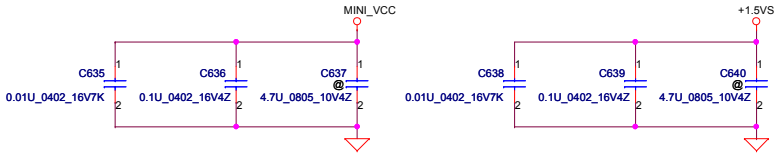




4/2 Add by Vivian







Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: Mini-Card/Kill SWITCH

Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

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Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: NEW CARD

Size	Document Number	Rev
B	NBLB2 M/B LA-5412P Schematic	0.1

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Board ID table, in EVT and EVT2 phase, it is NA 09-03

	MB2_ID	MB1_ID
DVT	0	1
DVT_R	0	0
PVT	1	0
MP	1	1

U27

KB926QFD3 LQFP 128P

1/15 Use KB926D3

KB926 SPI STRAP PIN
No stuff when use KB926C0

2/26 Copy KFT(avoid for LED random turn off issue)

06/09 DVT ice add

2/26 Add by Vivian(for LED random turn off issue)

add this for EC suggestion DVT,0625

4/2 Add by Vivian

3/26 Change color of LED1 from Blue to Amber
4/1 Change color of LED1 from Amber to Blue

change C871 to 18p

change to SN100003F00 PVT 1022

06/25 DVT ice add

EC DEBUG PORT

Security Classification	Compal Secret Data
Issued Date	2009/02/04
Deciphered Date	2010/02/04

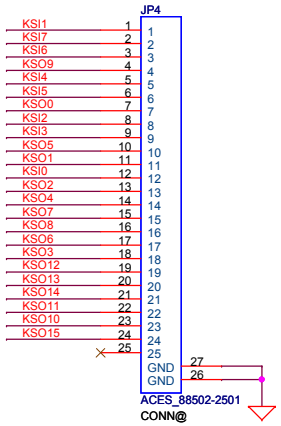
Compal Electronics, Inc.

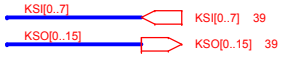
Title: ENE-KB926

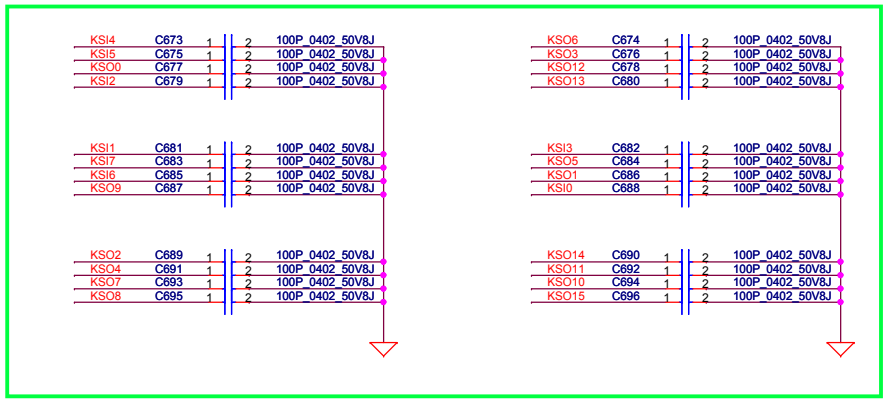
Size: Custom | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 39 of 61

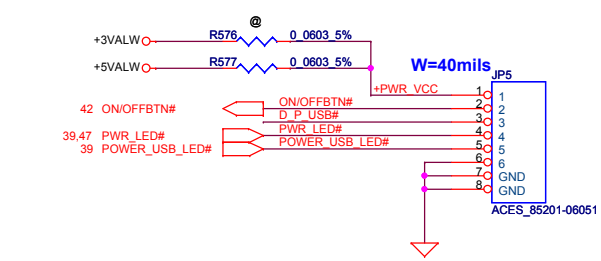
INT_KBD Conn.

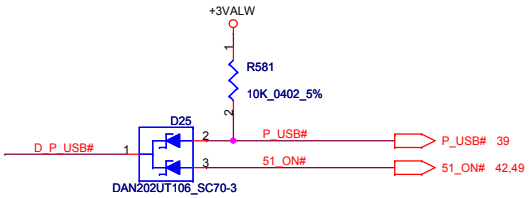




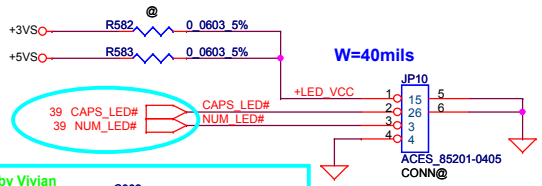


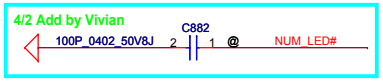
Power USB Board Conn



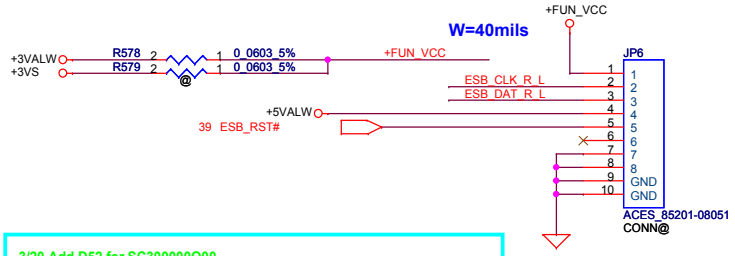


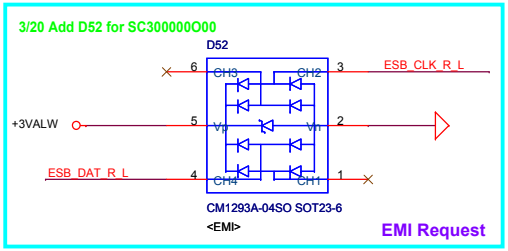
LED Board Conn

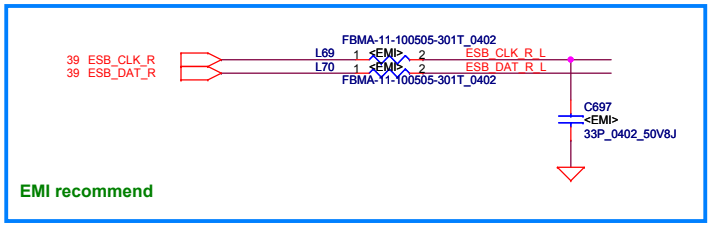




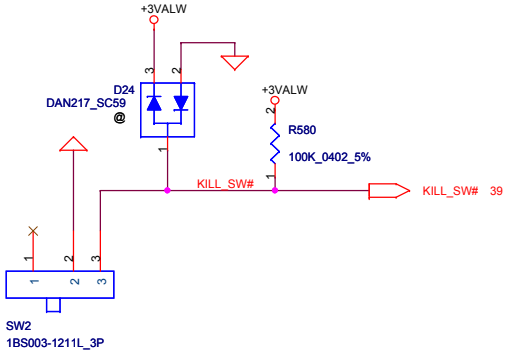
Conductive board conn







Kill SWITCH



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.			
Title	KB/SW/PW/Fun Conn		
Size B	Document Number NBLB2 M/B LA-5412P Schematic		Rev 0.1
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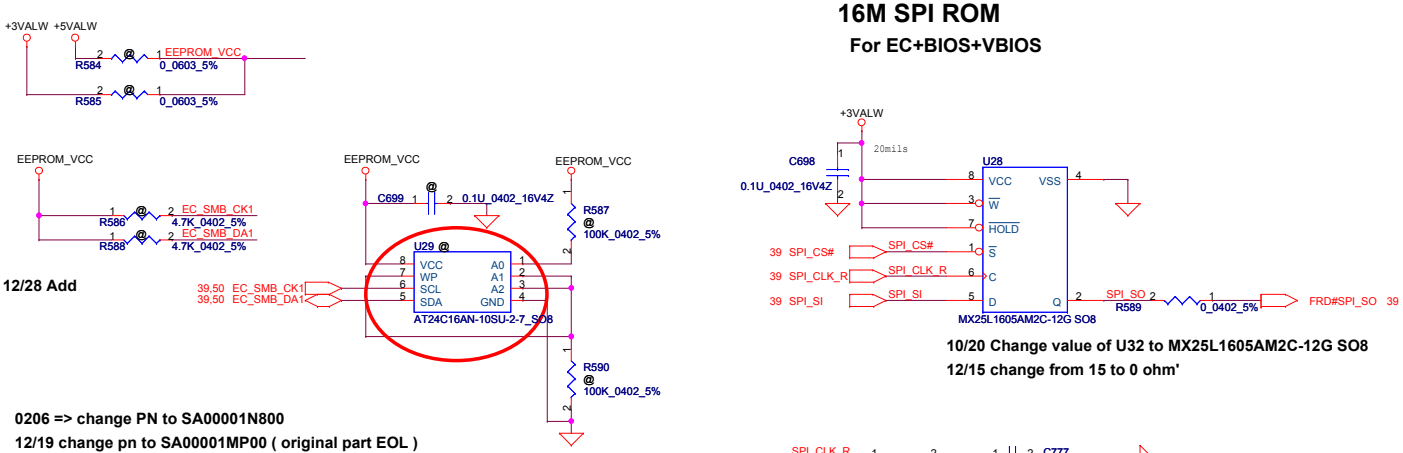
16M SPI ROM

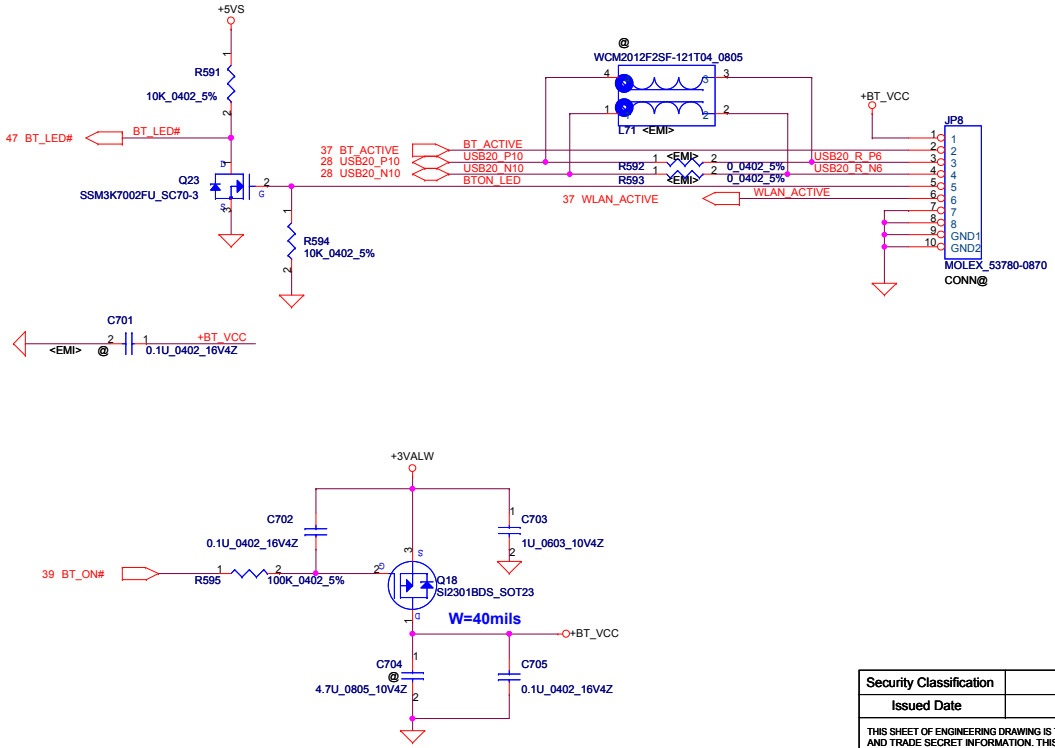
For EC+BIOS+VBIOS



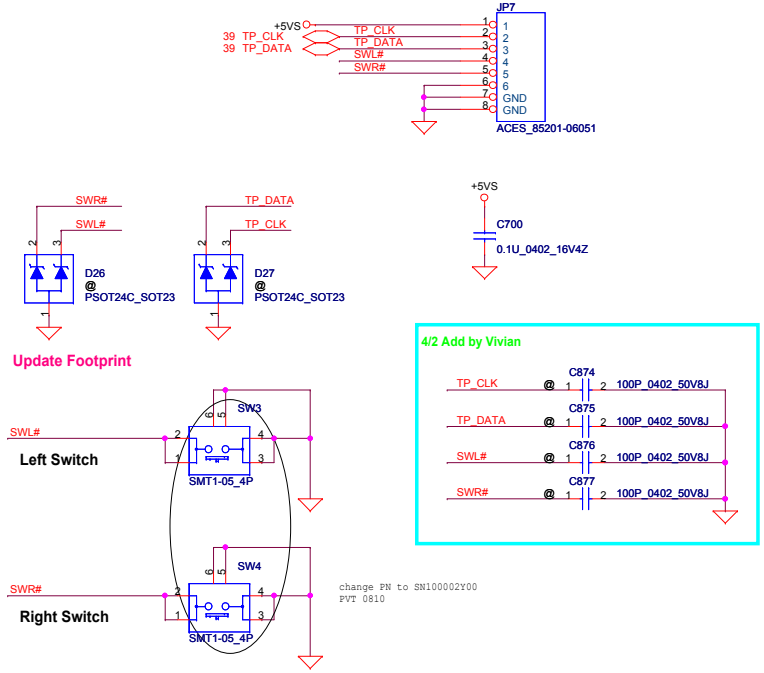
Bluetooth Conn.

Need to check BT pin definition again!

9/20 modified this block



To TP/B Conn.



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: BIOS, TP & BT Connector

Size	Document Number	Rev
B	NBLB2 M/B LA-5412P Schematic	0.1

Date: Tuesday, November 17, 2009 Sheet 41 of 61

ON/OFF switch

TOP Side

J3 @JOPEN

J4 @JOPEN

Bottom Side

+3VALW

R596 100K_0402_5%

40 ON/OFFBTN# — ON/OFFBTN# — D28 DAN202UT106_SC70-3 — ON/OFF# — ON/OFF# 39

51_ON# — 51_ON# 40,49

Power Button

SMT1-05_4P SW5

SMT1-05_4P SW6

ON/OFFBTN#

10/09 add for debug

3/3 Add

C708 1000P_0402_50V7K

D29 RLZ20A_LL34

39 EC_ON — EC_ON — Q24 SSM3K7002FU_SC70-3

R598 10K_0402_5%

FOR LPC DEBUG PORT

+3VS

JP9 ACES_85201-1005N DB CONN@

CLK_PCI_DB — CLK_PCI_DB 28

LPC_AD0 — LPC_AD0 24,37,39,47

LPC_AD1 — LPC_AD1 24,37,39,47

LPC_AD2 — LPC_AD2 24,37,39,47

LPC_AD3 — LPC_AD3 24,37,39,47

LPC_FRAME# — LPC_FRAME# 24,37,39,47

PLT_RST_BUF1# — PLT_RST_BUF1# 28,39

C709 @ 0.1U_0402_16V4Z

USB IO 2 Conn.

DVT 6/24 Rual Add C480 for EMI! DVT

+USB_VCCA

C480 @ 0.01U_0402_25V7K

JP18 ACES_88266-04001 CONN@

28 USB20_N9

28 USB20_P9

+USB_VCCA W=40mils

C706 470P_0402_50V7K

C707 10U_0805_10V4Z

10/27 Remove C1640 by Vivian

DVT 6/25 Add C778 for EMI! DVT ice

+5VALW

C778 @ 0.01U_0402_25V7K

U30 G528P1UF_SOP8

C710 4.7U_0805_10V4Z

39 USB2_ON#

+USB_VCCA

+3VALW

R597 10K_0402_5%

R598 0_0402_5%

USB_OC#4 28

C711 @ 0.1U_0402_16V4Z

CIR

11/03 Modify symbol to SCR00000H00 by Vivian

3/30 Change part number of IR1 from SCR00000H00 to SCR00000E00

39 RCIRRX — RCIRRX — C713 1000P_0402_50V7K @

IR1 FM-2136SC-5CN(REV)_4P CIR@ W=20mils

+CIR_VCC

R600 100_0402_5% CIR@ — +3VALW

C714 4.7U_0603_6.3V6K CIR@

39 CIR_DET# — R601 0_0402_5% CIR@

USB IO Conn.

150u

ESR 0.9 ohm

Package(L*W*H)7.3*4.3*2.9

Rating 6.3V

+USB_VCCC

JP11 ACES_85201-20051

28 USB20_N0 — USB20_N0 — USB20_P0 — 28 USB20_P0

28 USB20_N5 — USB20_N5 — USB20_P5 — 28 USB20_P5

28 USB20_N4 — USB20_N4 — USB20_P4 — 28 USB20_P4

USB2_ON# C712 100P_0402_50V8J

+USB_VCCC W=80mils

C716 470P_0402_50V7K

C715 10U_0805_10V4Z

11/29 change this symbol's footprint as ADT7421ARMZ-REEL_MSOP8

+5VALW

+USB_VCCC

+3VALW

copy LM75CIMMX-3_MSOP8 footprint

U31 G545A2P8U MSOP 8P

C718 4.7U_0805_10V4Z

39 USB2_ON#

R604 10K_0402_5%

R605 0_0402_5%

USB_OC#0 28

USB_OC#2 28

C720 @ 0.1U_0402_16V4Z

USB2_ON# C721 100P_0402_50V8J

Lid Switch

+3VALW — R602 0_0402_5% — +VCC_LID — R603 100K_0402_5%

U32 A3212ELHLT-T_SOT23W-3 (VDD, OUTPUT, GND)

C717 0.1U_0402_16V4Z

C719 10P_0402_50V8J

LID_SW# 39

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

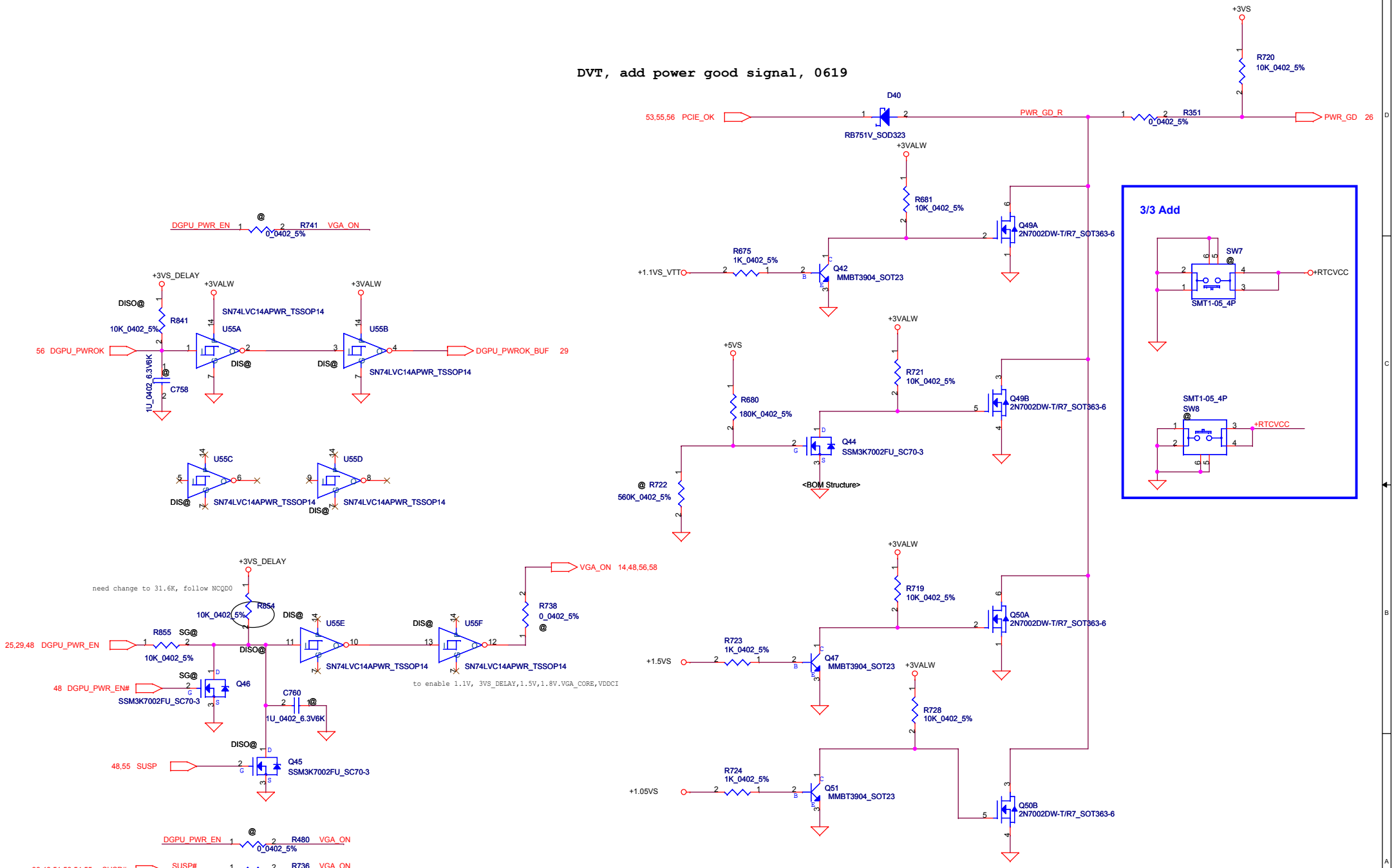
Compal Electronics, Inc.

Title: Power OK/Lid/Front,IO,DB Conn

Size: B | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 42 of 61

DVT, add power good signal, 0619



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: RTC

Size	Document Number	Rev
Custom	NBLB2 M/B LA-5412P Schematic	0.1

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Copy KFTOO

EC Beep

39 BEEP# — R607 10K_0402_5% — MONO_IN_1 — C726 0.1U_0402_16V4Z — MONO_IN

24 PCH_SPKR — R608 10K_0402_5%

C722 0.1U_0402_16V4Z

PCI Beep

R609 10K_0402_5%

+5VS — L72 FBMA-L11-201209-221LMA30T_0805 — L73 FBMA-L11-201209-221LMA30T_0805 — +5VAMP

C723 0.1U_0402_16V4Z — C724 0.1U_0402_16V4Z

2/18 Change from GNDA to DGND of vendor suggest

R606 0_0805_5%

60mil — U33 G9191-475T1U_SOT23-5 (IN, GND, SHDN, OUT, BYP) — 40mil

+VDDA 4.75V

C725 0.01U_0402_25V7K @

(output = 300 mA)

HD Audio Codec

2/20 Change value and symbol of R1107 and R1111 from 2.2K ohmto 4.7K ohm(of Vendor suggest)

+VDDA — L74 FBMA-L11-160808-800LMT_0603 — 0.1U_0402_16V4Z — 40mil — +AVDD_HDA

C727 10U_0805_10V4Z — C728 — C729 — 0.1U_0402_16V4Z

10mil — 0.1U_0402_16V4Z — +3VS_DVDD — L75 MBK1608121YZF_0603 — +3VS

C730 — C731 — C732 10U_0805_10V4Z — 0.1U_0402_16V4Z

U34 (ALC272-VA2-GR LQFP_48P)

AVDD1, AVDD2, DVDD, DVDD_IO

MIC2_VREFO — R610 0_0402_5% @ — D30 RLS4148_LL34-2 DUAL@ — R613 4.7K_0402_5% DUAL@

R614 0_0402_5% SINGLE@ — D31 RLS4148_LL34-2 DUAL@ — R615 4.7K_0402_5%

2/11 Modify Schematic

45 MIC2_L — MIC2_L R611 1K_0402_1% — MIC2_R_L — C733 — MIC2_C_L 4.7U_0805_6.3V6K — LINE2_L / MIC2_L

45 MIC2_R — MIC2_R R612 1K_0402_1% — MIC2_R_R — C734 — MIC2_C_R 4.7U_0805_6.3V6K — LINE2_R / MIC2_R

2/11 Remove LINE-IN Schematic

LINE1_L, LINE1_R, LINE1_VREFO, LINE2_VREFO, MIC2_VREFO

45 MIC1_L — MIC1_L R616 — MIC1_C_L 4.7U_0805_6.3V6K — MIC1_L

45 MIC1_R — MIC1_R R617 — MIC1_C_R 4.7U_0805_6.3V6K — MIC1_R

C737 — C738 @ 100P_0402_50V8J — MONO_IN — PCBEEP_IN

2/11 Remove Digital MIC Schematic

24 HDA_RST_AUDIO# — RESET#

24 HDA_SYNC_AUDIO — SYNC

24 HDA_SDOUT_AUDIO — SDATA_OUT

GPIO0/DMIC_DATA1/2, GPIO1/DMIC_DATA3/4

45 MIC_PLUG# — R618 20K_0402_1%

45 HP_PLUG# — R619 5.1K_0402_1%

SENSE_A, SENSE_B

45 MUTE# — R620 0_0402_5% — EAPD

3/3 Follow HW2 schematic(NSKAA)

SPDIFO1

2/11 Remove SPDIF Schematic

DVSS1, DVSS2

LINE2_L — LOUT1_L — AMP_LEFT — AMP_LEFT 45

LINE2_R — LOUT_R — AMP_RIGHT — AMP_RIGHT 45

LOUT2_L, LOUT2_R

SPDIFO2, DMIC_CLK1/2

2/11 Remove Digital MIC Schematic

NC, DMIC_CLK3/4

R616 33_0402_5% — C735 33P_0402_50V8J

DVT For EMI add 6/23

BITCLK — HDA_BITCLK_AUDIO 24

SDATA_IN — HDA_SDIN0_AUDIO — R617 33_0402_5% — HDA_SDIN0 24

MONO_OUT

2/11 Remove SUB WOOFER Schematic

CBP — 2.2U_0402_6.3VM

CPVEE — C739 — 10mil

MIC1_VREFO — MIC1_VREFO

HPOUT_R — HP_R — HP_R 45

C740 2.2U_0402_6.3VM

CBN

10mil

VREF — CODEC_VREF — C741 0.1U_0402_16V4Z — C742 10U_0805_10V4Z

JDREF — R621 20K_0402_1%

HPOUT_L — HP_L — HP_L 45

AVSS1, AVSS2

DGND GNDA

2/26 Change PN of U61 from SA00002CI20 to SA00002CI10

R622 0_0805_5% — R624 0_0805_5% — R626 0_0805_5% — GND GNDA

R623 0_0805_5% — R625 0_0805_5% — R627 0_0805_5% — GND GNDA

ESD

3/20 Copy KHLBX

+3VS +5VS

R763 4.7K_0402_5% @ — R764 4.7K_0402_5% @ — HDA_RST_AUDIO#

C854 0.01U_0402_16V7K @

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

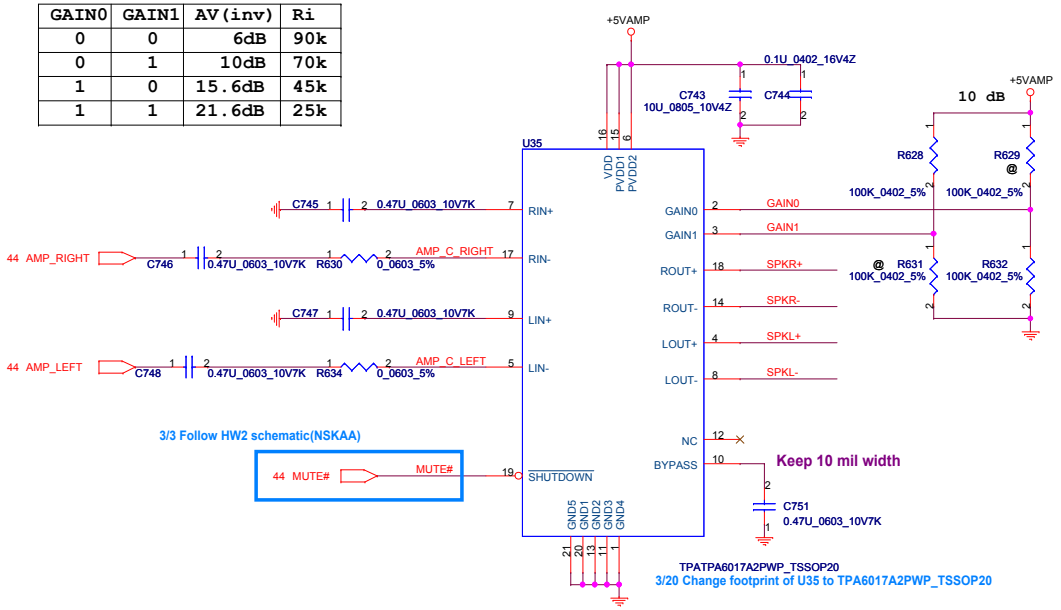
Compal Electronics, Inc.

Title: HD Audio Codec ALC272

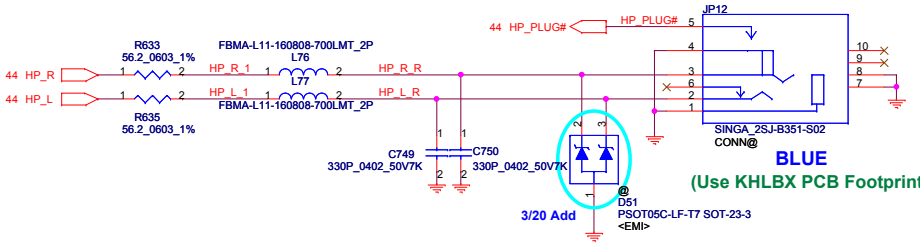
Size: B | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 44 of 61

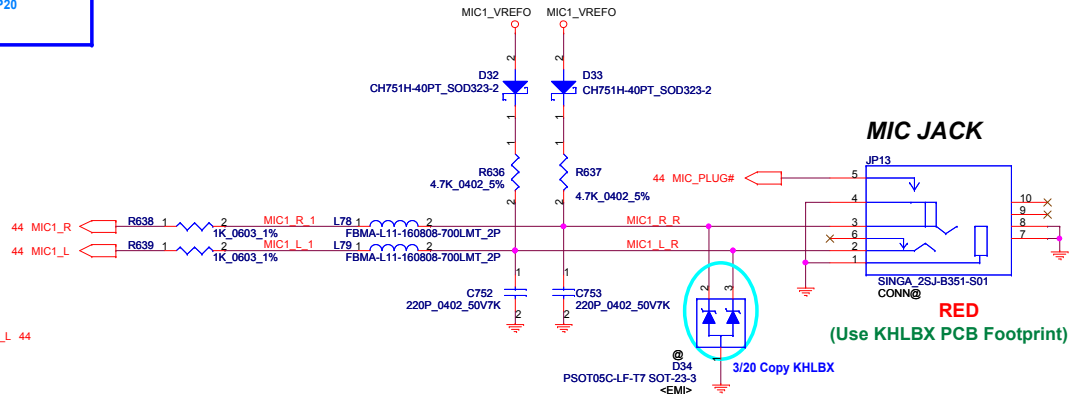
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

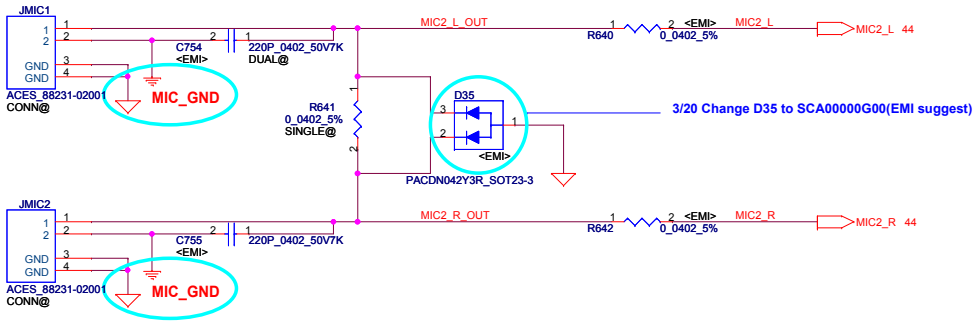


HP JACK

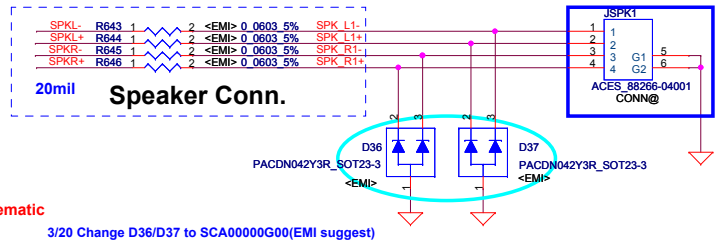


MIC JACK





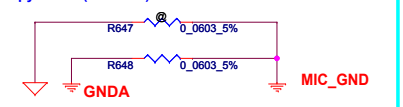
Int. Speaker Conn.



Copy KHLBX schematic

3/20 Change D36/D37 to SCA00000G00(EMI suggest)

Copy KFT00(2/20 add)



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

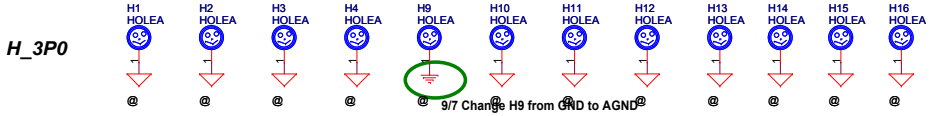
Compal Electronics, Inc.

Title: MIC & Amplifier & Audio Jack

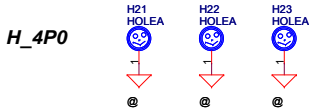
Size: B | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

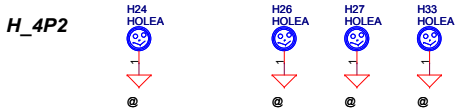
Date: Tuesday, November 17, 2009 | Sheet 45 of 61

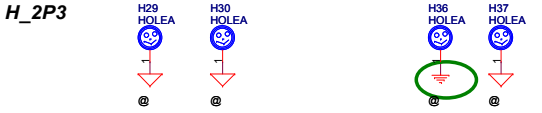
11/27 Add screw for layout request

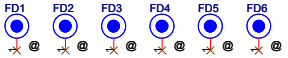


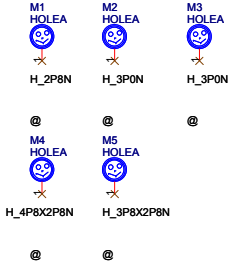
Del modem holea (H17 and H18) H34,H35
2009/09/02











11/27 Add screw for layout request

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

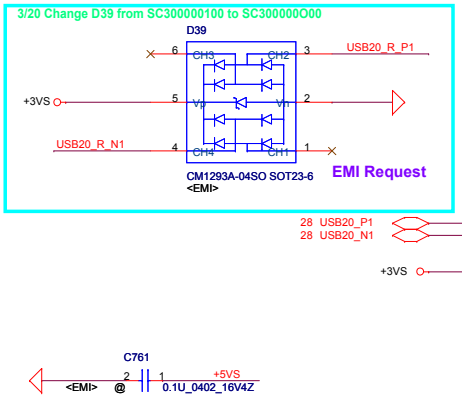
Compal Electronics, Inc.

Title: Screw

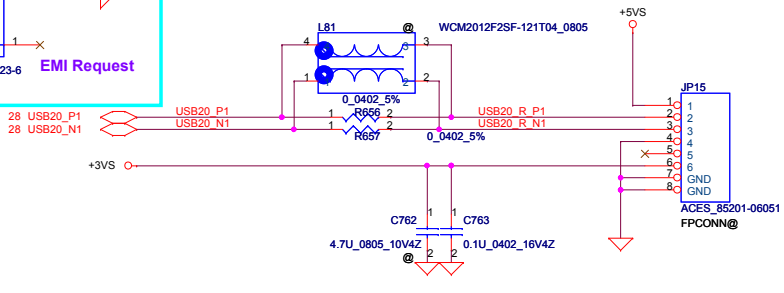
Size: Custom | Document Number: NBLB1 M/B LA-5411P Schematic | Rev: 0.1

Date: Friday, November 13, 2009 | Sheet 46 of 61

Camera Conn



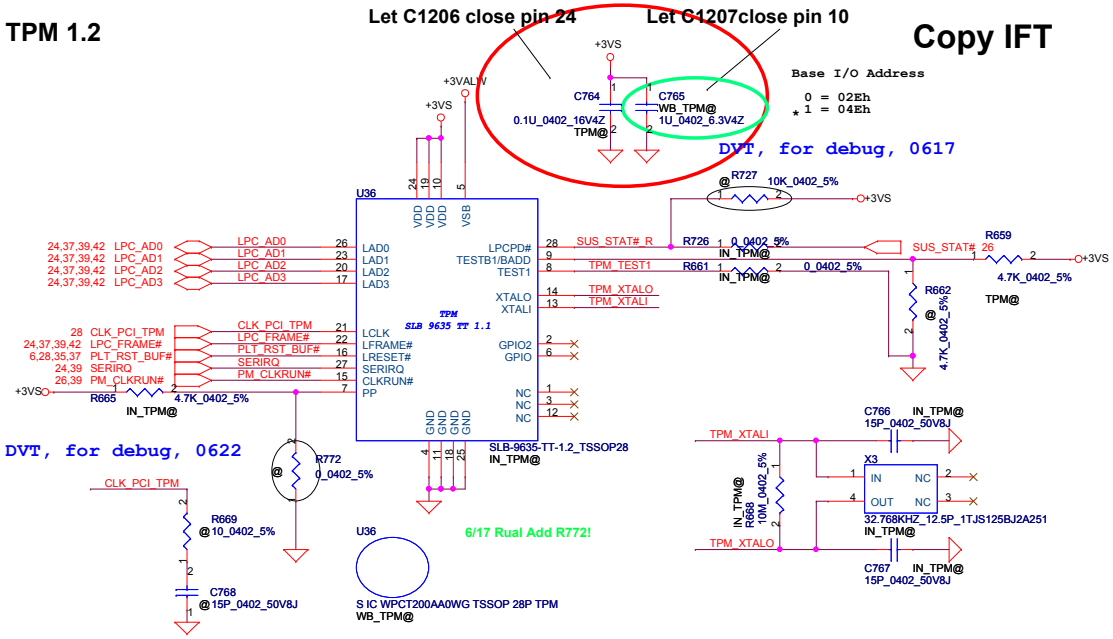
Finger Print board



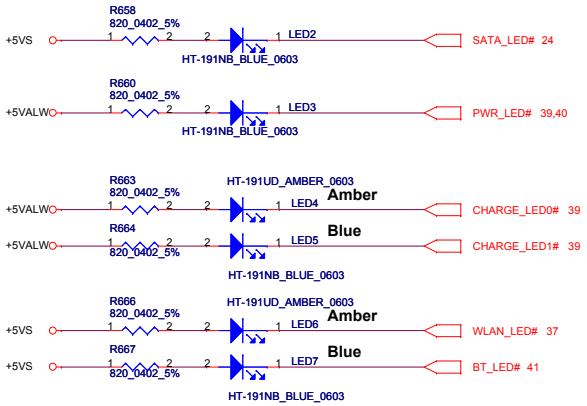
TPM X76 Information

X76 P/N	Vendor	Location	Bom Structure
X7611630L07	Infineon	C717,C718,R698,R702,R703,U32,X3	IN_TPM@
X7611630L08	Winbond	C724,U32	WB_TPM@

TPM 1.2



LED



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

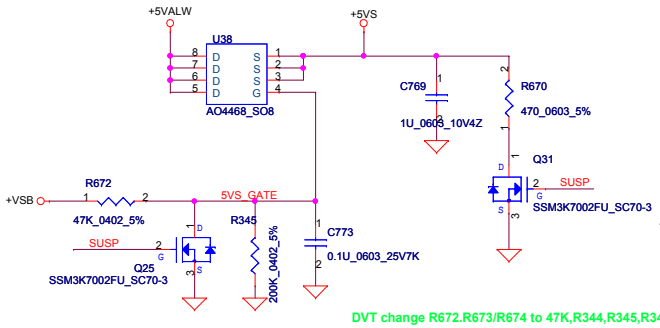
Compal Electronics, Inc.

Title: MDC/LED/Camera/FP

Size: B | Document Number: NBLB2 M/B LA-5412P Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 47 of 61

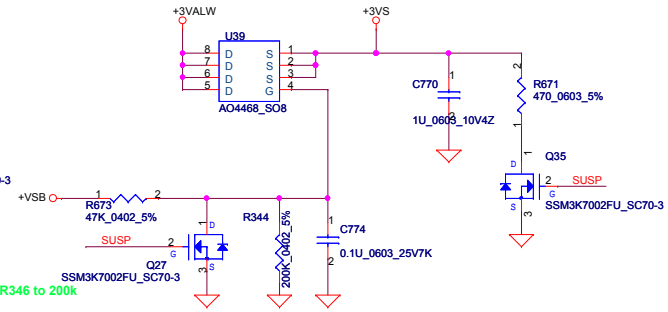
+5VALW TO +5VS



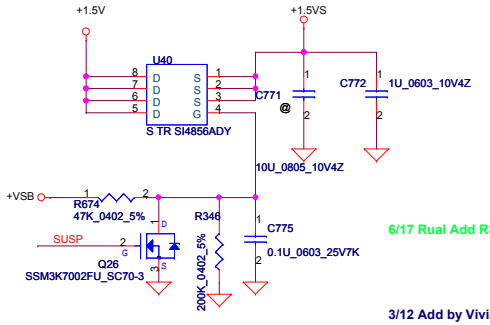
DVT change R672.R673/R674 to 47K,R344,R345,R346 to 200k

6/17 Rual Add R345!

+3VALW TO +3VS

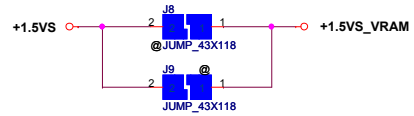


+1.5V TO +1.5VS

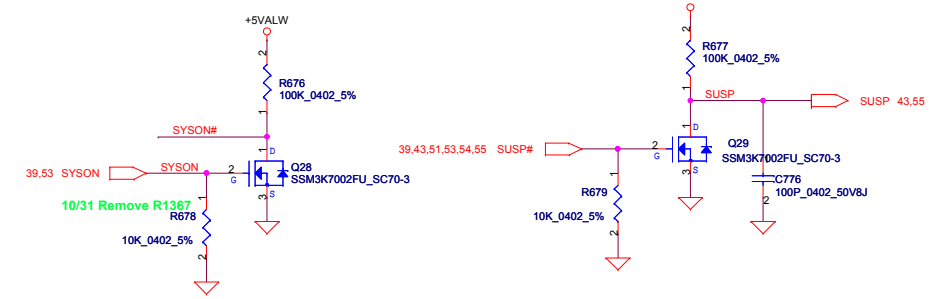


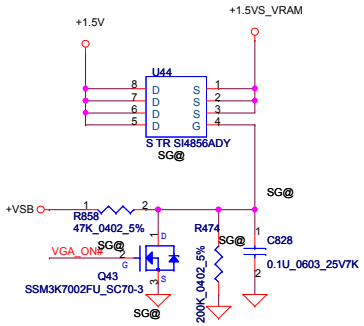
6/17 Rual Add R346!

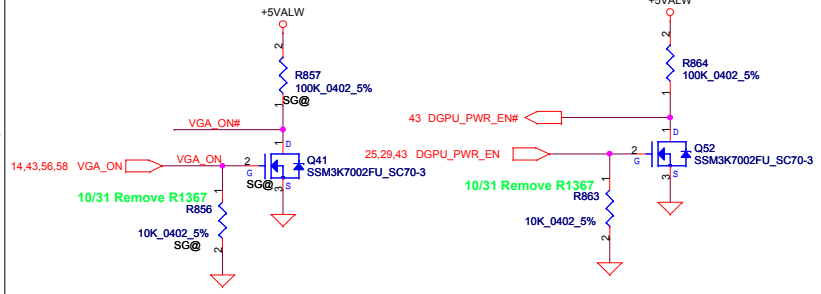
3/12 Add by Vivian



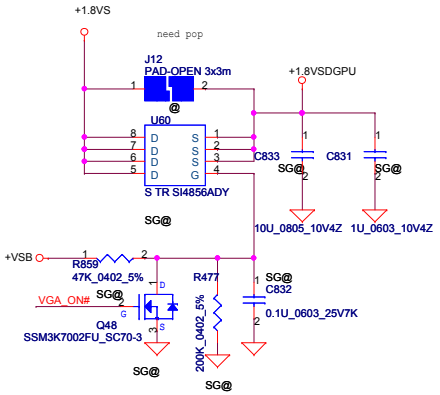
need pop

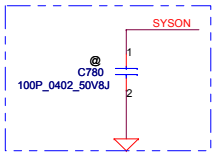




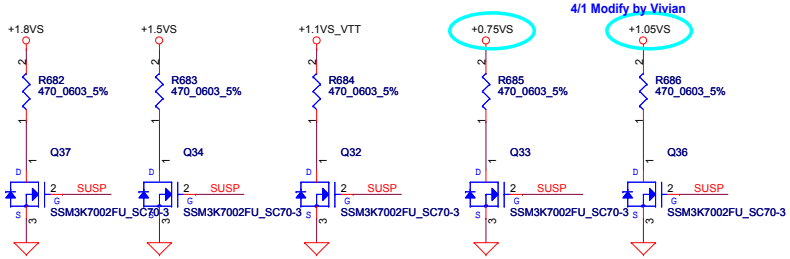


need pop





4/1 Modify by Vivian



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

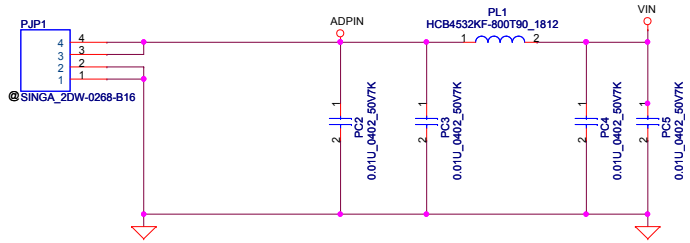
Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	NBLB2 M/B LA-5412P Schematic	0.1

Date: Tuesday, November 17, 2009 Sheet 48 of 61

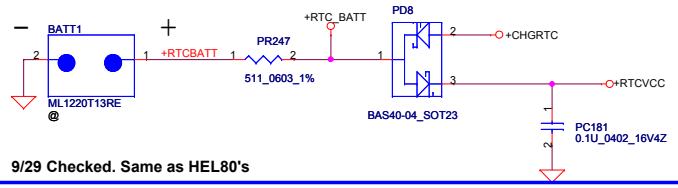
DC301001Y00



RTC Battery

Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

9/29 modified to follow ISKAA



9/29 Checked. Same as HEL80's

Reserve another location

06/24 Rual remove BATT2!

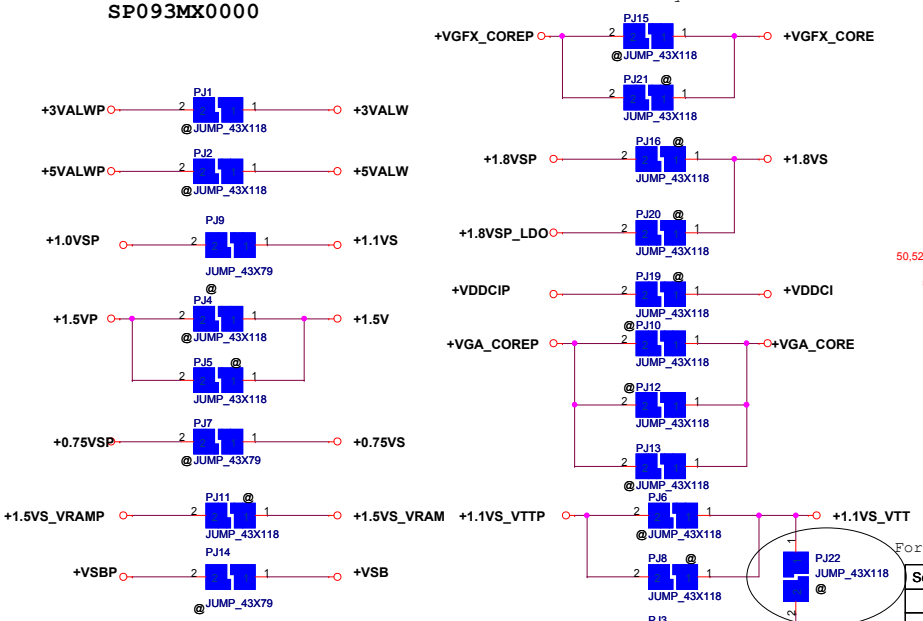
SP093MX0000

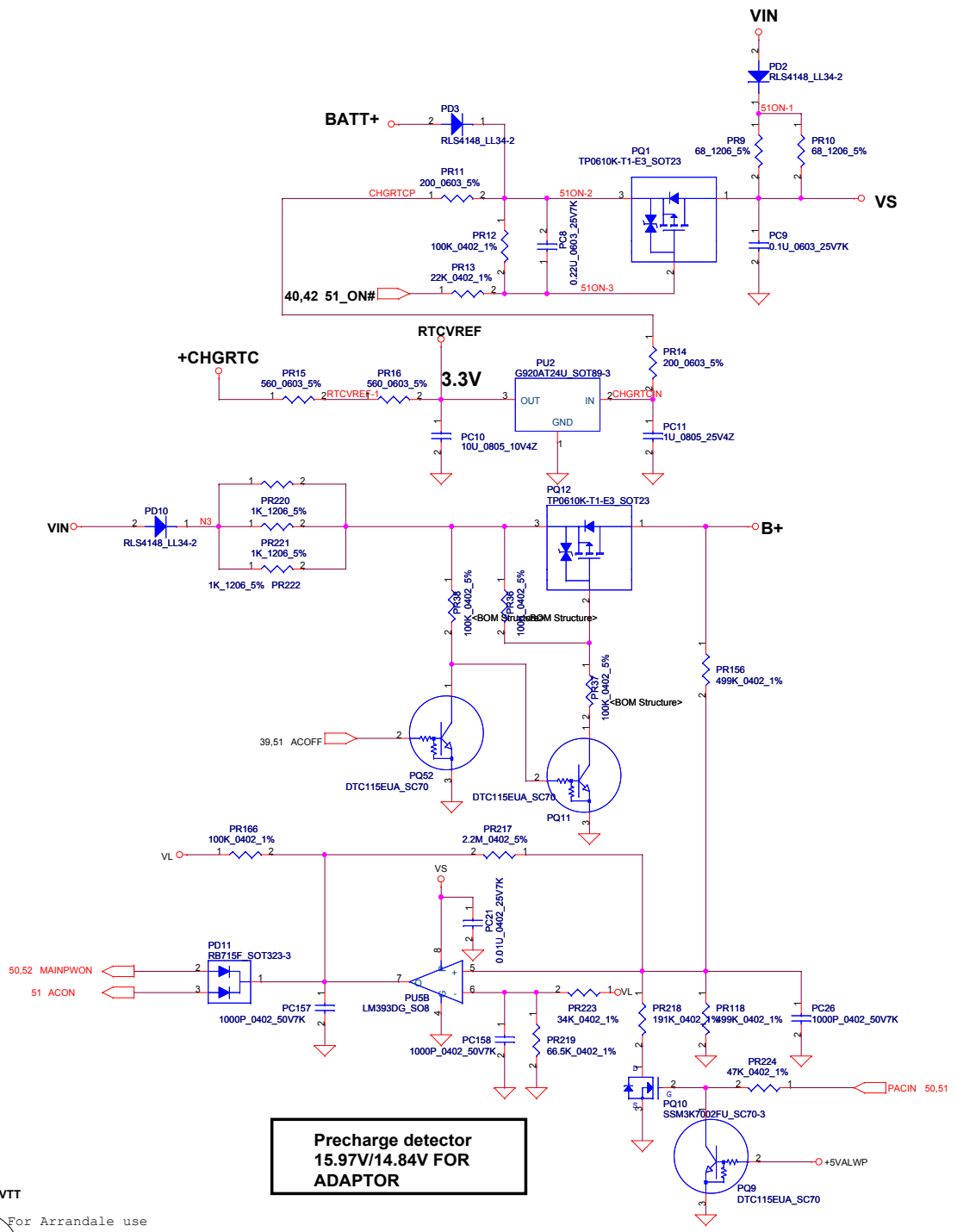
BOM structure comment

@ ==>unpop

NV@==>Nvidia sku only

M97@==>ATI sku only





Precharge detector 15.97V/14.84V FOR ADAPTOR

For Arrandale use

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

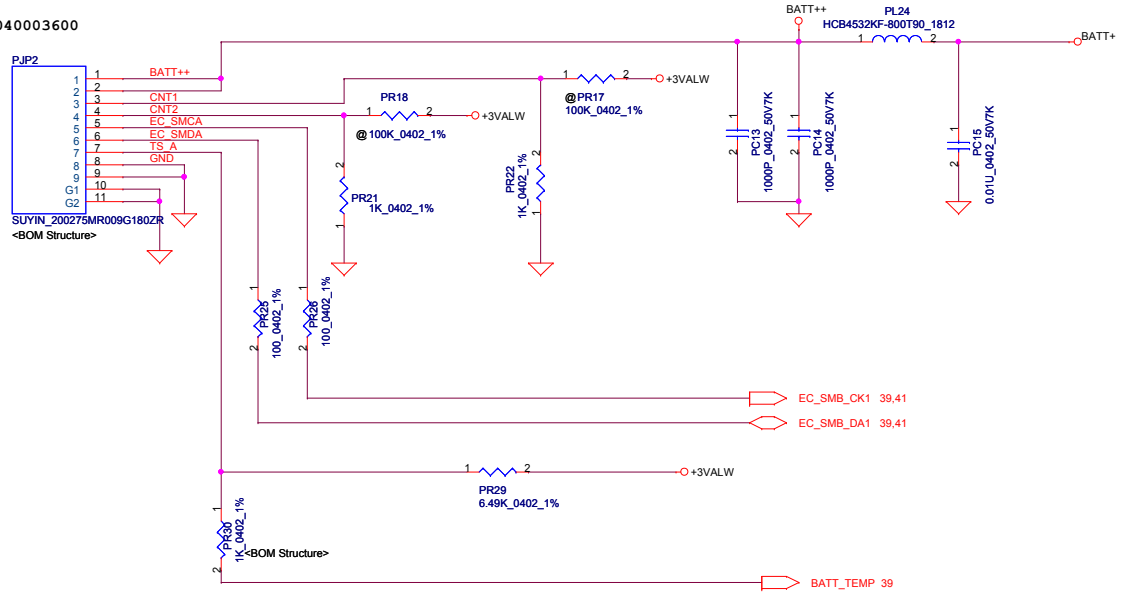
Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size: Custom | Document Number: MB Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 49 of 61

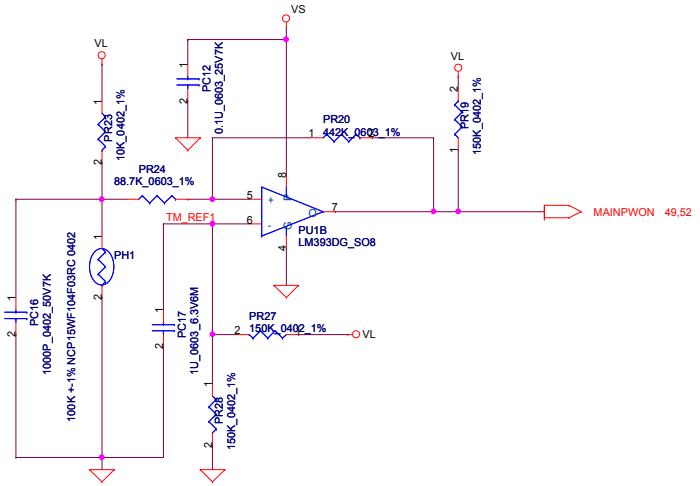
DC040003600

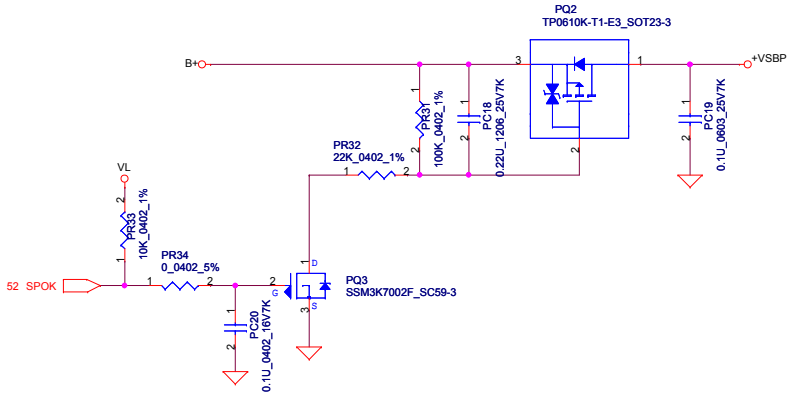


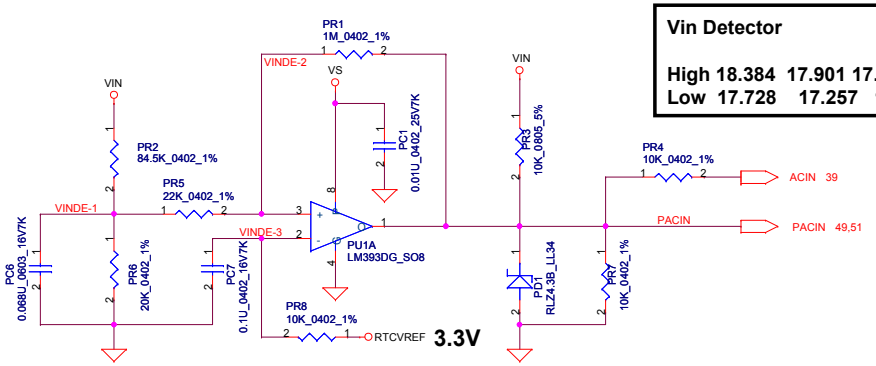
PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 70 degree C





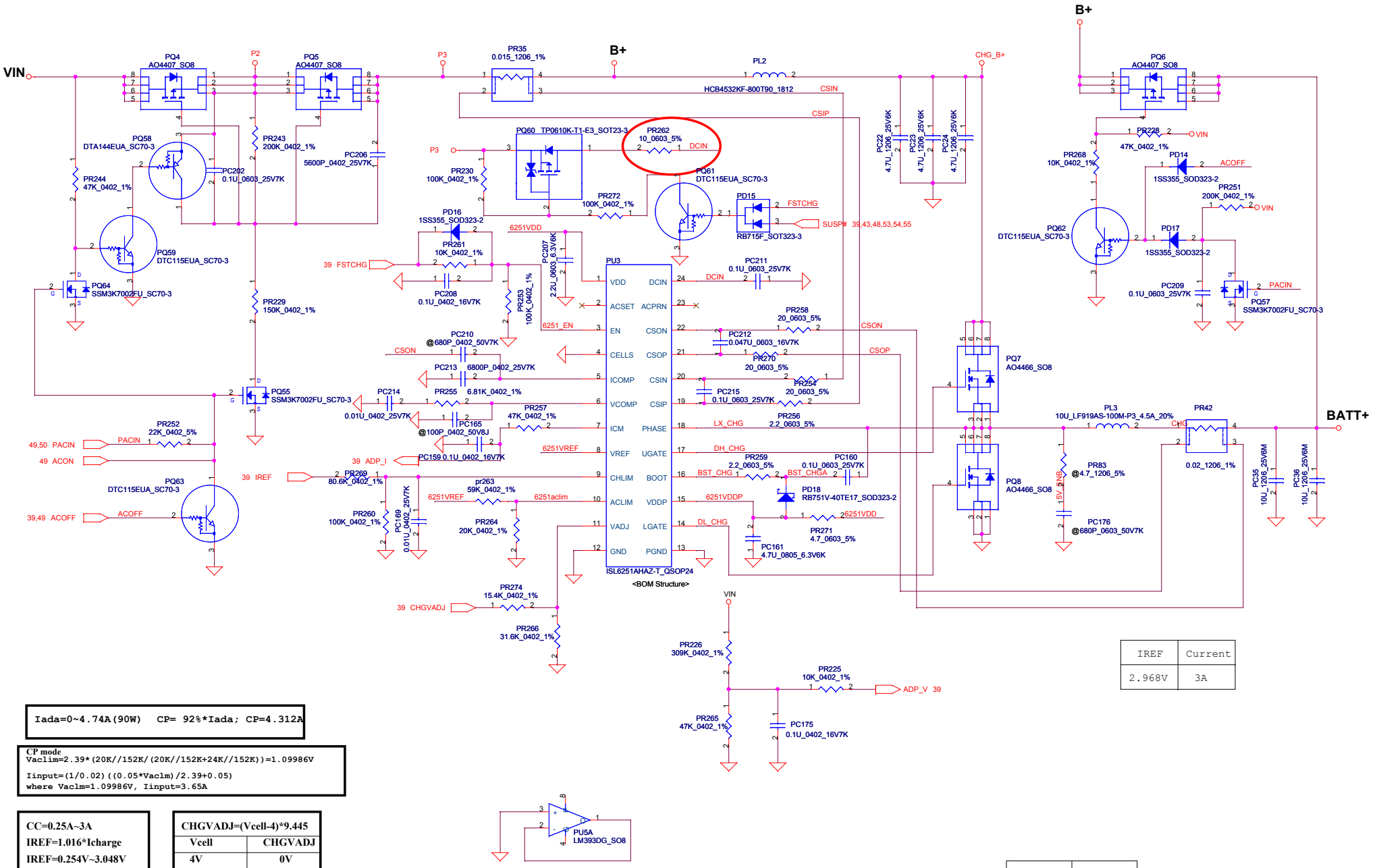


Vin Detector

High 18.384 17.901 17.430
Low 17.728 17.257 16.976

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.			
Title: BATTERY CONN / OTP			
Size: Custom	Document Number: MB Schematic		Rev: 0.1
Date: Tuesday, November 17, 2009	Sheet 50 of 61		



IREF	Current
2.968V	3A

Iada=0~4.74A(90W) CP= 92%*Iada; CP=4.312A

CP mode
Vaclm=2.39*(20K//152K/(20K//152K+24K//152K))=1.09986V

Iinput=(1/0.02)((0.05*Vaclm)/2.39+0.05)
where Vaclm=1.09986V, Iinput=3.65A

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445

Vcell	CHGVADJ
4V	0V
4.2V	1.898V
4.35V	3.315V

CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

CELLS	VDD	GND	Float
CELL number	4	3	2

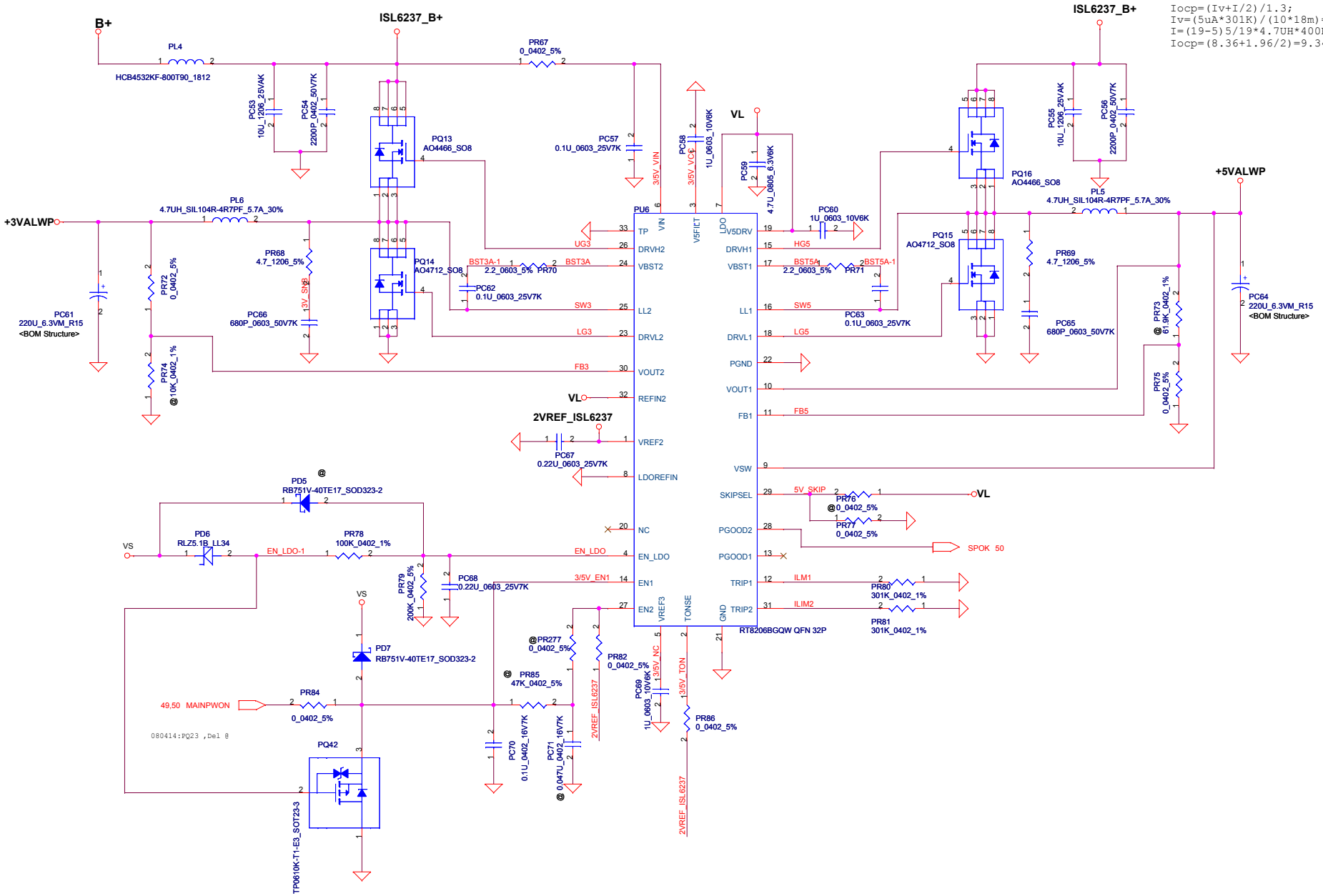
"CHGVADJ" connect to EC DA pin

LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+

Title	<Title>
Size: Custom	Document Number: <Doc>
Rev	<RevCode>
Date: Tuesday, November 17, 2009	Sheet 51 of 61

Iocp=Iv+I/2; Iv=(5uA*301K)/(10*18m)=8.36A
I=(19-3.3)3.3/19*4.7UH*300K=1.93AIocp=8.36+1.93/2=9.32A

Iocp=(Iv+I/2)/1.3;
Iv=(5uA*301K)/(10*18m)=8.36A ;
I=(19-5)5/19*4.7UH*400K=1.96A;
Iocp=(8.36+1.96/2)=9.34A



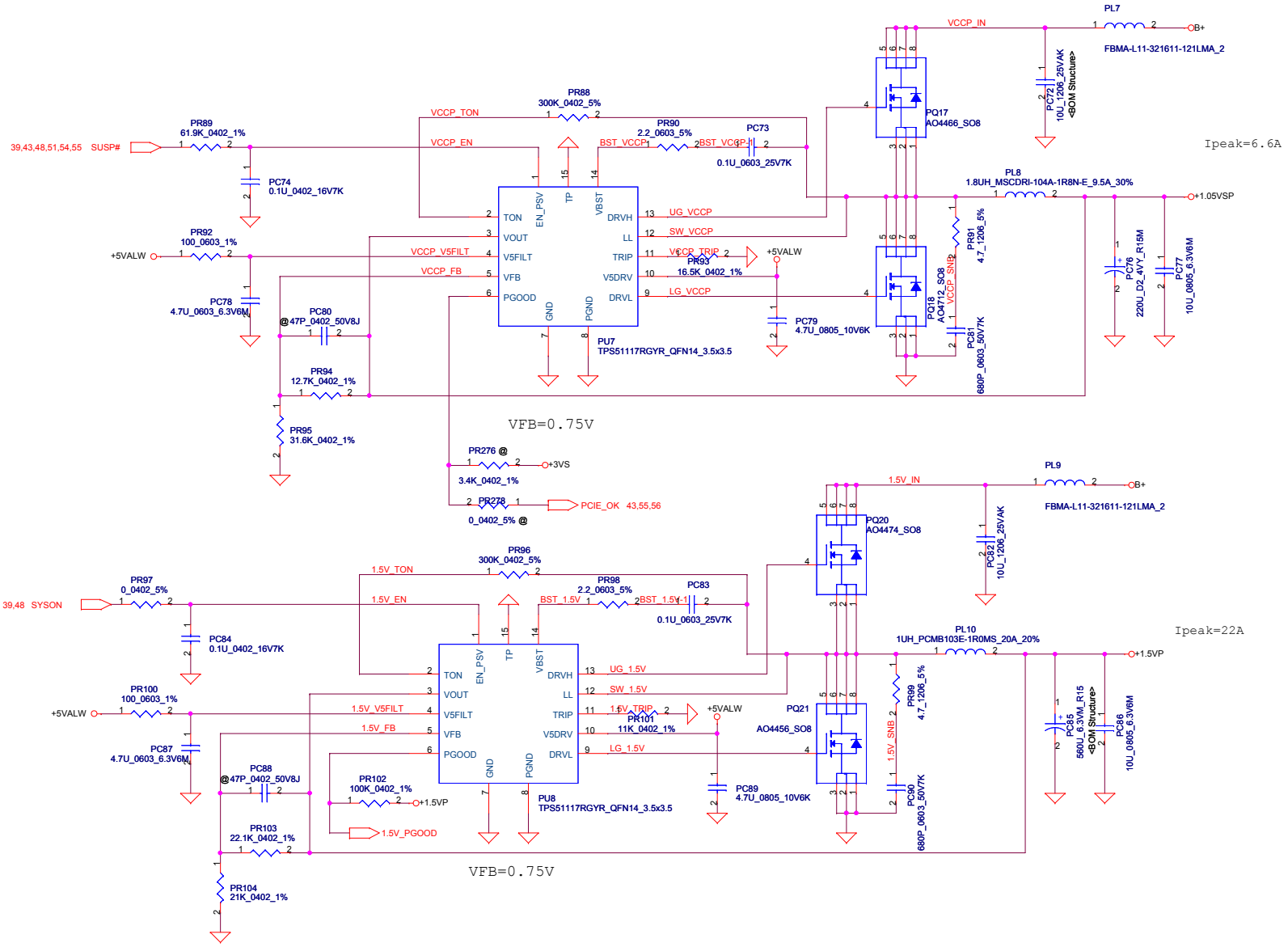
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: *3VALW/5VALW*

Size: Custom | Document Number: *MB Schematic* | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 52 of 61



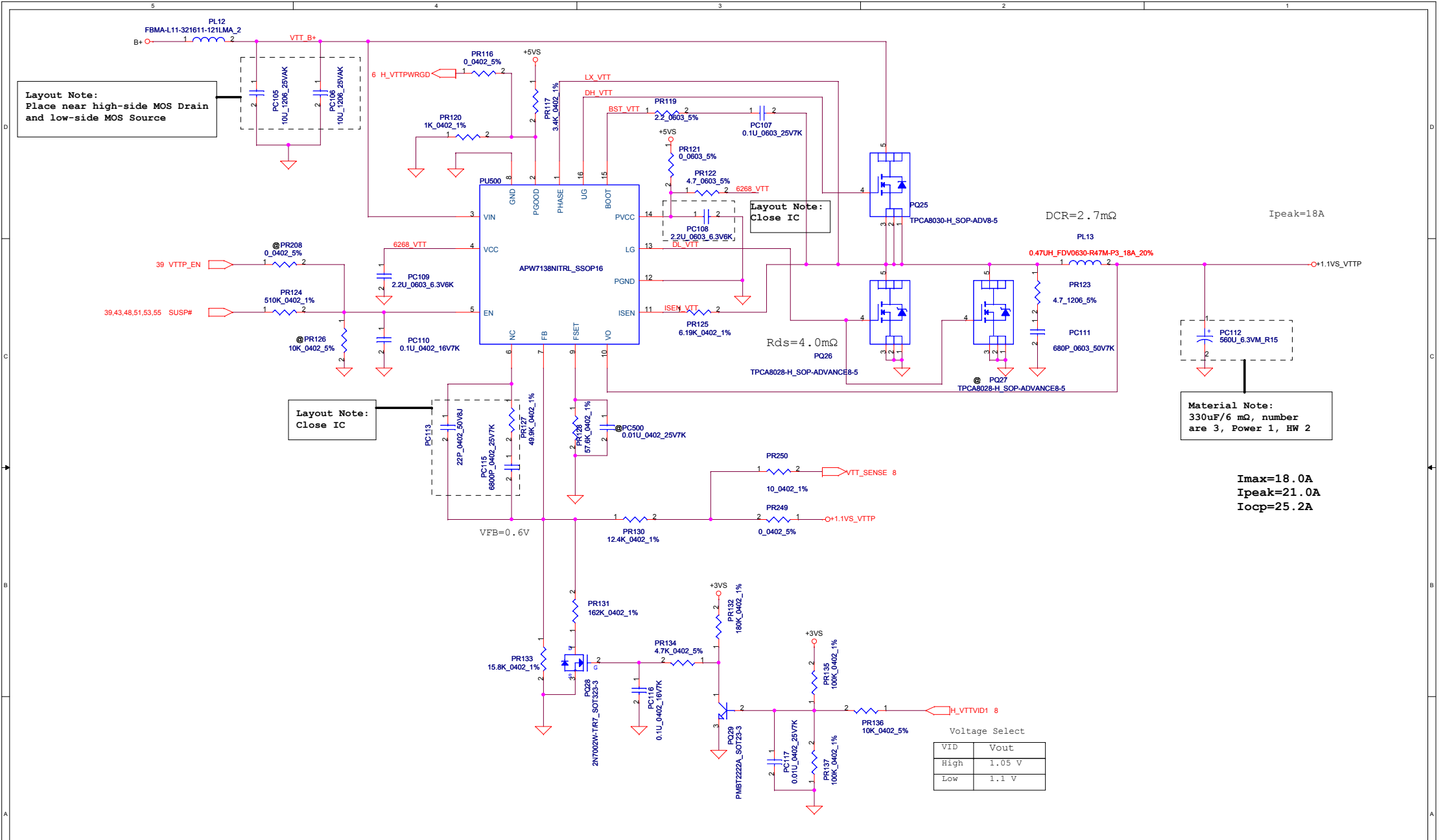
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: **1.5V/VCCP/0.75V**

Size	Document Number	Rev
Custom	MB Schematic	0.1

Date: Tuesday, November 17, 2009 | Sheet 53 of 61



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: **+1.1VS_VTT**

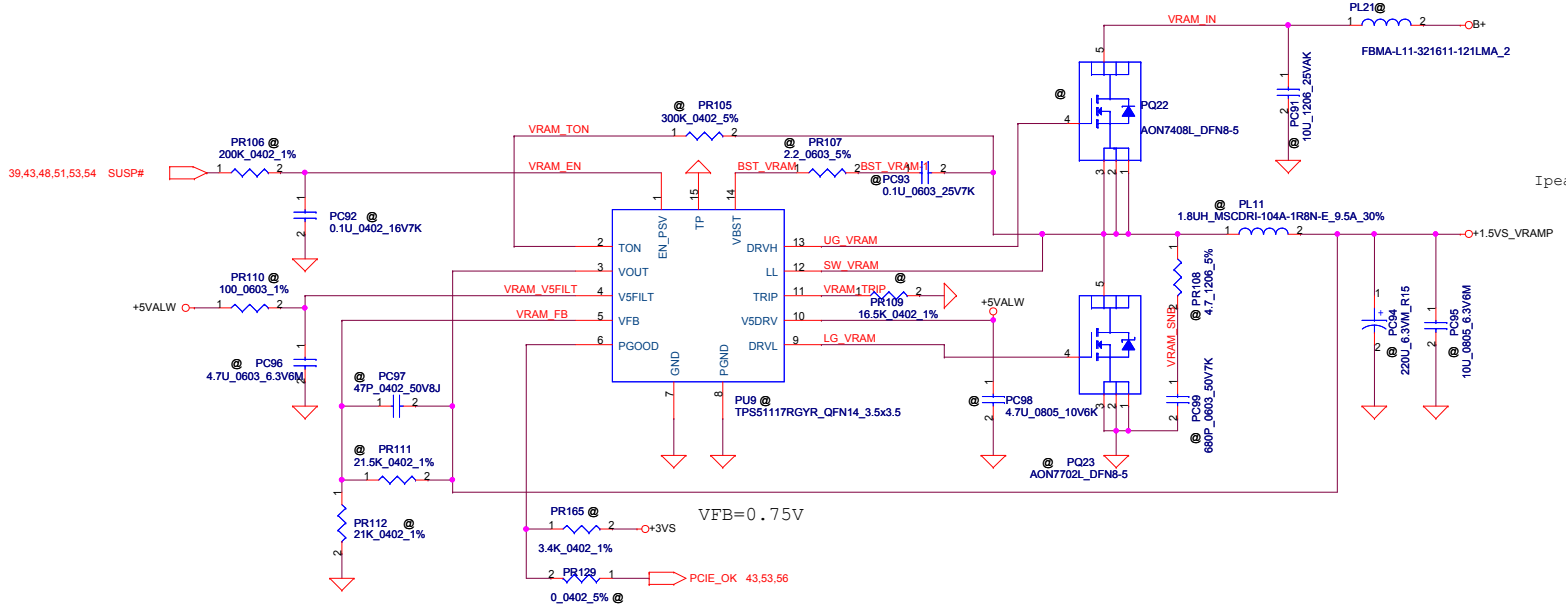
Size: Custom | Document Number: **MB Schematic** | Rev: 0.1

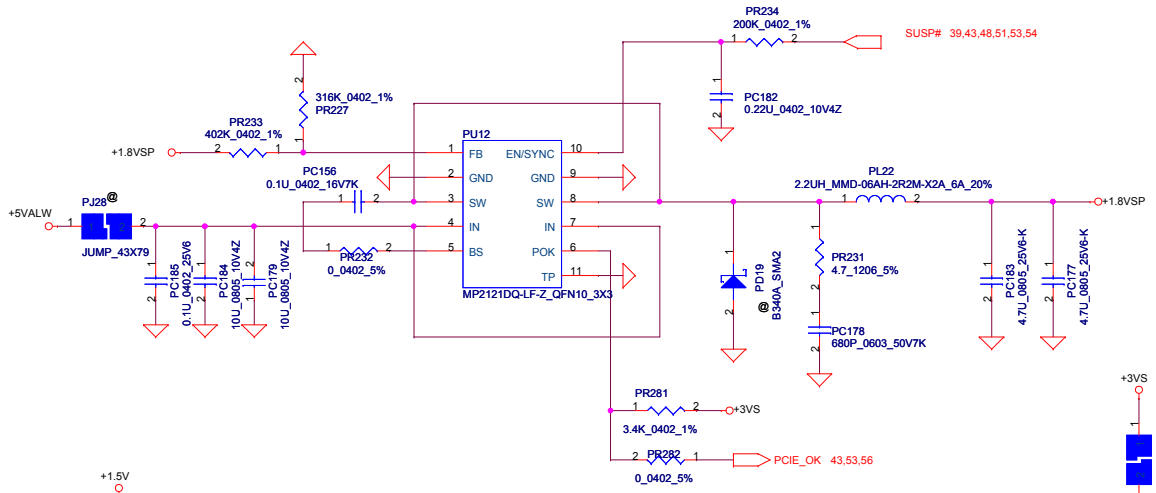
Date: Tuesday, November 17, 2009 | Sheet 54 of 61

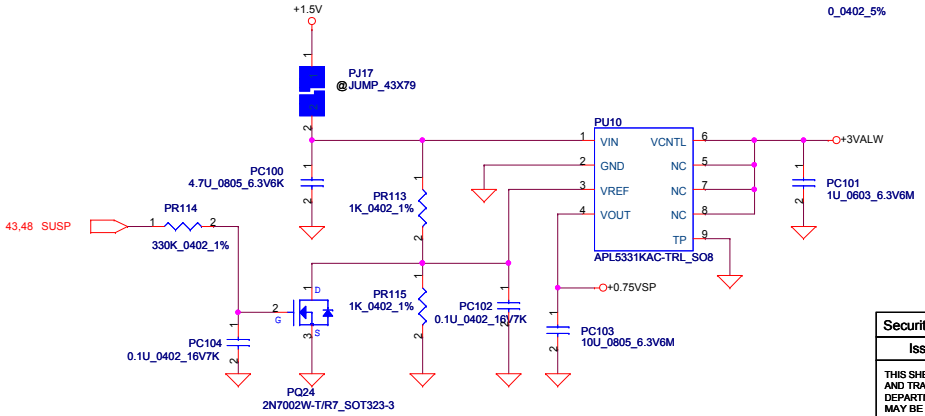
Iocp=RTEIP*ITRIP/RDS(ON)+1/2 I=13k*9u/15m+1/2*2.7=9.15A

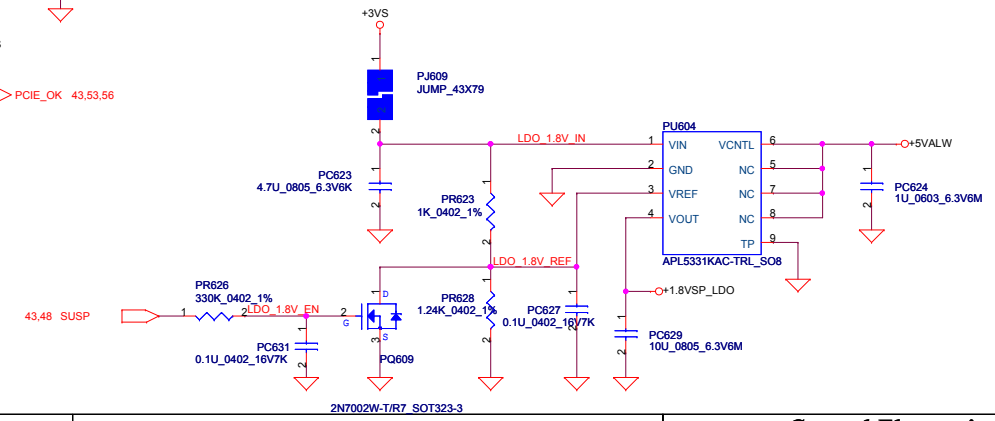
Ipeak=8A

VFB=0.75V









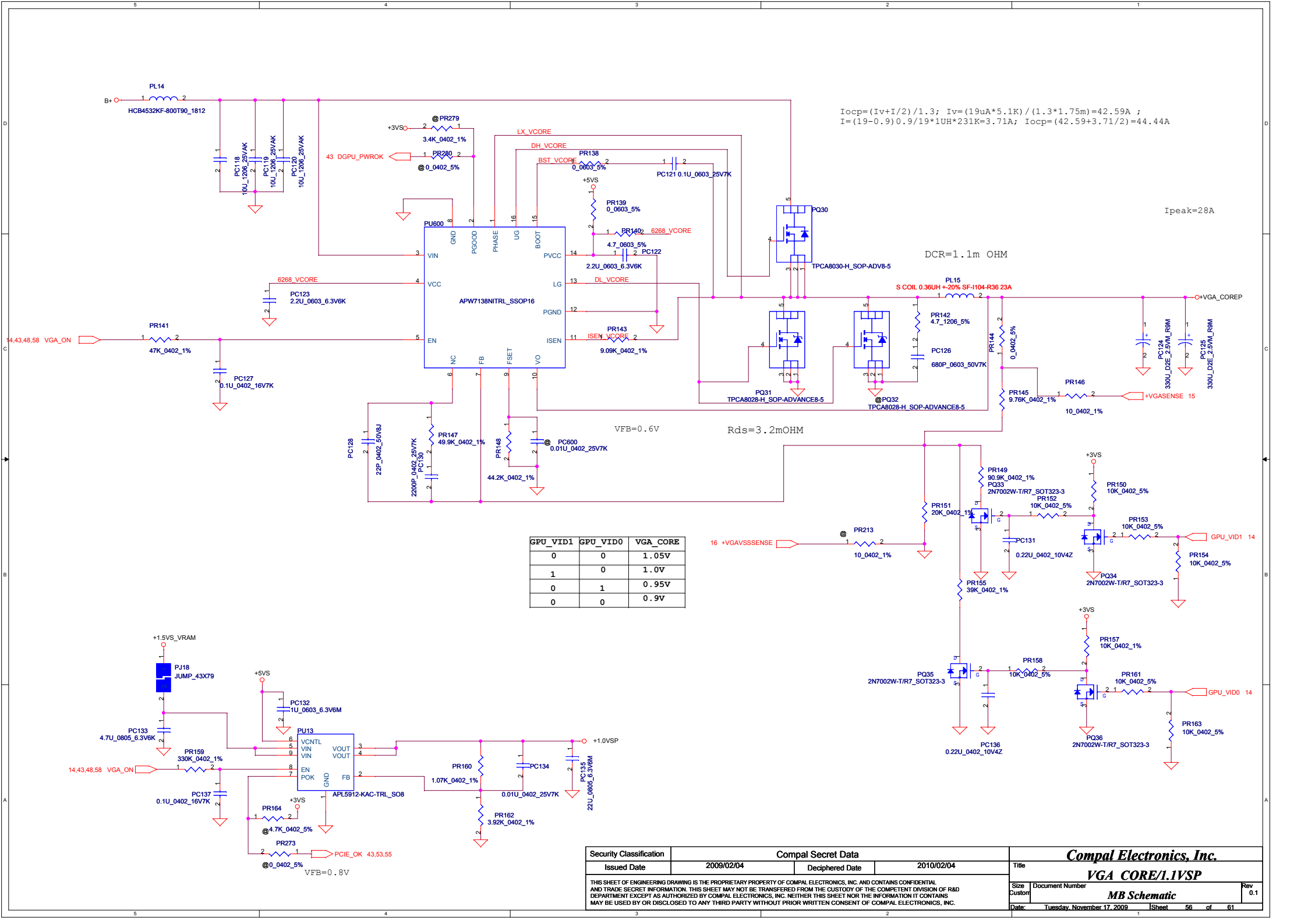
Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: **VGA_CORE/1.8V/1.1V**

Size: Custom | Document Number: MB Schematic | Rev: 0.1

Date: Tuesday, November 17, 2009 | Sheet 55 of 61



GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
0	0	0.9V

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

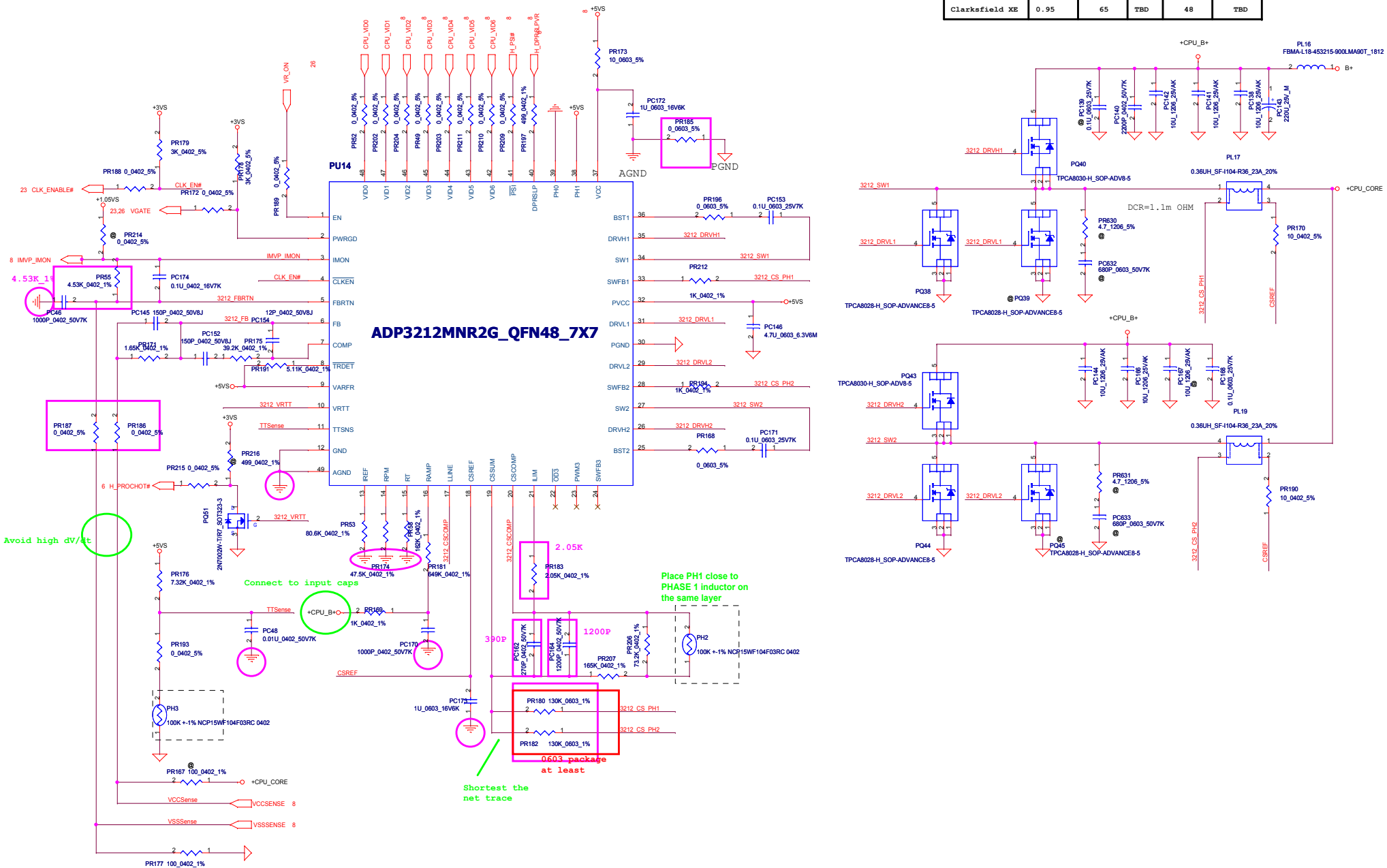
Title: **VGA_CORE/1.1VSP**

Size	Document Number	Rev
Custom	MB Schematic	0.1

Date: Tuesday, November 17, 2009 | Sheet 56 of 61

PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
C	MB Schematic	0.1

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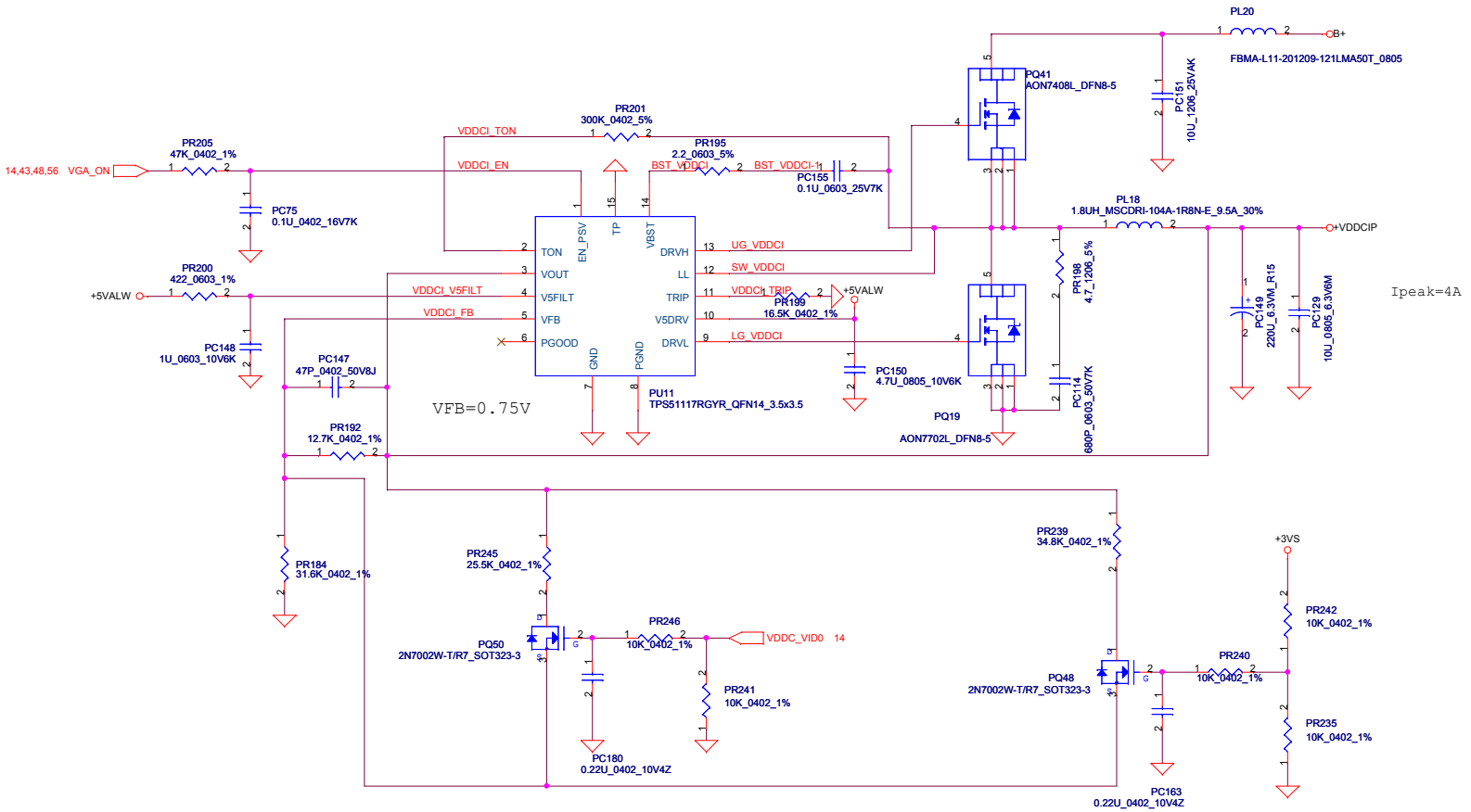
Iocp=RTEIP*ITRIP/RDS(ON)+1/2 I=16.5K*9u/15m+1.64/2= 10.72A

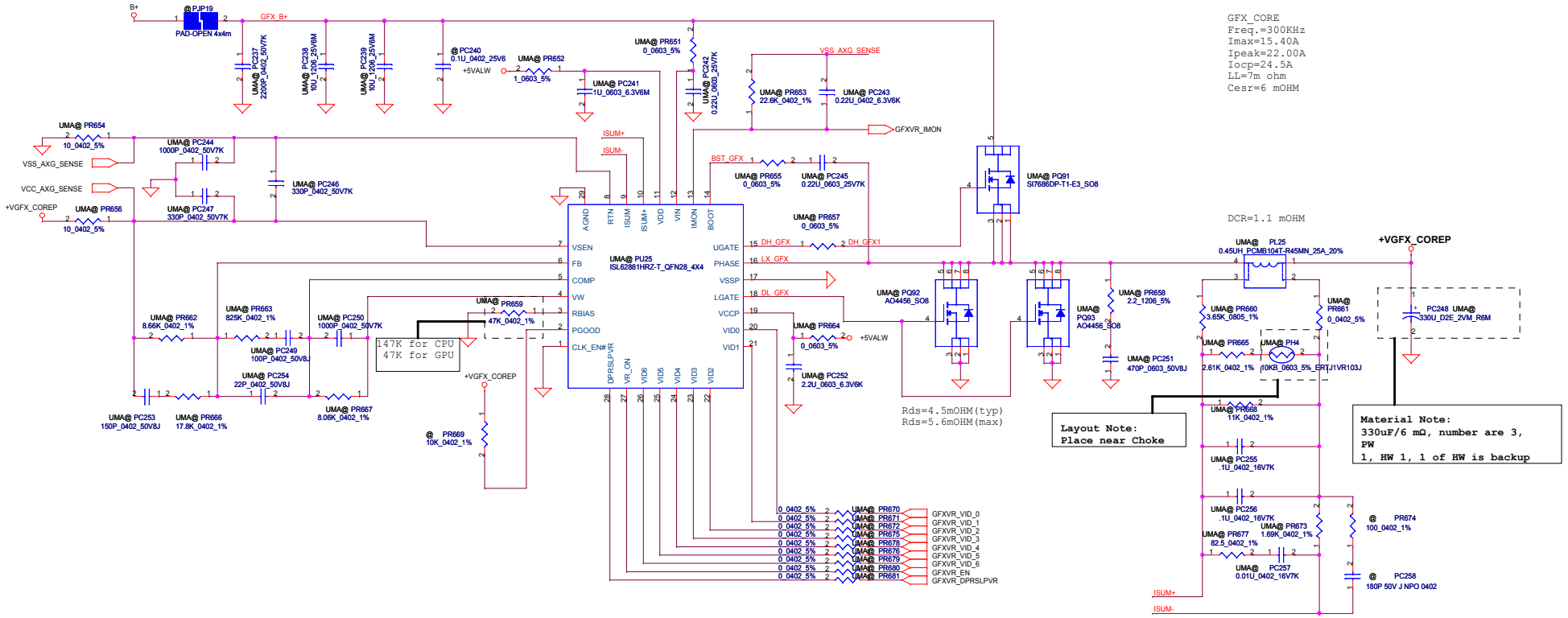


VID1	VID0(GPIO6)	VDDC
0	0	1.12V
		1.07V
0	1	
1	0	1.05V
1	1	0.95V

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title	ATI VDDC	
Size: Custom	Document Number: MB Schematic	Rev: 0.1
Date: Tuesday, November 17, 2009	Sheet 58 of 61	



Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: **CPU_CORE**

Size	Document Number	Rev
Custom	MB Schematic	0.1

Date: Tuesday, November 17, 2009 | Sheet 59 of 61

Version change list (P.I.R. List)

for HW

Item	Category	Modify List	Requestor	PG#	Date	Comment	Phase
1	Change VGA chip from M97 to M96 as sourcer request		sourcer		2009/05/6		EVT2
2	connect EC RST to PLT_RST	Add U37,R564,R560 and connect the BUF_RST1#	ice		2009/05/11		EVT2
3	change the footprint of C381~C386	Change from C_D2 to C_D2T	power		2009/05/12		EVT2
4	Remove R768 R769 from BOM	we do not use the Camer connector(JP14) so remove it.	ice_liu		2009/05/19		EVT2
5	3VS leakage issue(0.1V)	Remove R535 from BOM	TPE		2009/05/19		EVT2
6	Confirm the DDR_VREF schematic		TPE		2009/05/19		EVT2
7	Add soft start for +3vs_delay	add C201, R343	ice_liu	P14	2009/06/09		DVT
8	Add RST# for Cap board	add net of ESB_RST#	ice_liu	P39	2009/06/09		DVT
9	Add PCH CMOS clear	change J5,J6 to PCH_RST#	ice_liu	P24	2009/06/09		DVT
10	Add +1.1VS option power for M96	Add J11	ice_liu		2009/06/09		DVT
11	change HDMI_DET for ATI suggestion	add R770,R771,Q40,Del R287,R285,R286,L38,C480	ice_liu	P20	2009/06/09		DVT
12	add option R for TPM PP pin	add R772	ice_liu	P47	2009/06/17		DVT
13	Add option R for PCIE_WAKE#for debug	Add R561	ice_liu	P35	2009/06/17		DVT
14	add division R for DC/DC MOS gate	change R672.R673/R674 to 47K,R344,R345,R346 to 200k	ice_liu	P48	2009/06/19		DVT
15	Add HAD_BITCLK_AUDIO termination	Add R616(33ohm)C735 (33pf) in BOM	EMI	P44	2009/06/19		DVT
16	Add option R on SUS_STAT# for debug	Add R727,R726	ice_liu	P47	2009/06/22		DVT
17	Add power good schematic	Add R720,R351,R681,R721,R722,R719,R728,R723,R724,R680,R770,R675, D40,Q42,Q44,(need modify to sot23 FP)Q47,Q51,Q48,Q50,u41	ice_liu	P43	2009/06/23		DVT
18	Add PCH_SPI_R termination	Add R729, C777	EMI	P41	2009/06/23		DVT
19	Add 0.01 uf C for EMI request	Add C480 SE068103K80 S CER CAP 0.01UF 25V K X7R 0402	EMI	P42	2009/06/24		DVT
20	Add C861 as EC sugesstion	add C861 in to BOM	EC	P39	2009/06/25		DVT
21	Add C778 close to U30.2 for EMI	Add C788	EMI	P42	2009/06/25		DVT
22	Change Crystal C for vendor suggestion	change C671 C672 from 15pf to 22 pf	Vendor	P39	2009/06/25		DVT
23	Board ID	Add R547 R547, Board ID is 01	ice_liu	P39	2009/06/26		DVT
24	CPU_CORE	Remove C377，C365，C366，C367 from BOM and change C381,C382,C383,C384 to SGA00001Q80	power	P39	2009/06/27		DVT
25	add discharge in BOM	Add R682,R683,R684,R685,R686,Q37,Q34,Q32,Q33,Q36 in BOM	ice_liu	P8	2009/07/03		DVT

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: MB Schematic | Rev: 0.1

Date: Friday, November 13, 2009 | Sheet 60 of 61

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
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19							
20							
21							
22							
23							

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: MB Schematic | Rev: 0.1

Date: Friday, November 13, 2009 | Sheet 61 of 61