

A close-up photograph of a green printed circuit board (PCB). A large, square, black integrated circuit (IC) is the central focus, with numerous gold-plated pins visible along its edges. To the left of the IC, there are several smaller components, including capacitors labeled C108, C107, C113, and C112. A pink ribbon cable is connected to the top left of the board. The background is blurred, showing other parts of the board and components.

MB62 TFT IDTV SERVICE MANUAL

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Features:	36
• Complete interface between LNB and I ² C bus.....	36
• Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.5 A).....	36
• Selectable output current limit by external resistor.....	36
• Compliant with main satellite receivers output voltage specification.....	36
• Auxiliary modulation input (EXTM pin) facilitates DiSEqC™ 1.X encoding.....	36
• Accurate built-in 22 kHz tone generator suits widely accepted standards.....	36
• Low-drop post regulator and high efficiency step-up PWM with integrated power NMOS allow low power losses	36
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1. INTRODUCTION

17MB62 mainboard is driven by MStar SOC. This IC is capable of handling Video and audio processing, Scaling-Display processing, 3D comb filter, OSD and text processing, LVDS transmitting, channel and MPEG2/4 decoding, integrated DVB-T/C demodulator and media center functionality.

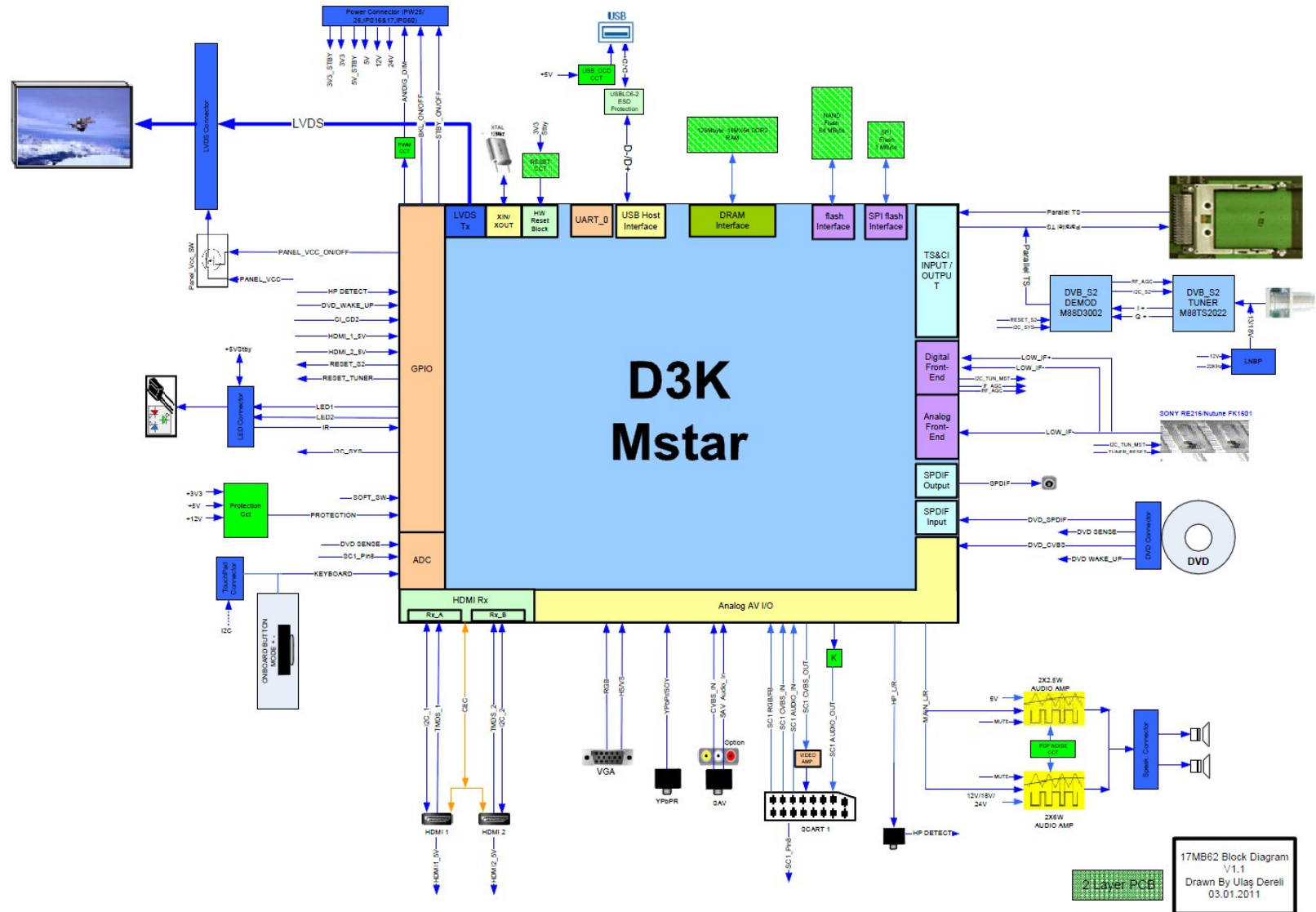
TV supports PAL, SECAM, NTSC colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo. Also DVB T, DVB-C are supported internal demodulators of Mstar IC and DVB-S/S2 is supported with external demodulator.

Sound system output is supplying max. 2x2,5W (less 10%THD at max output) with 4Ω speakers or 2x6W for stereo 8Ω speakers.

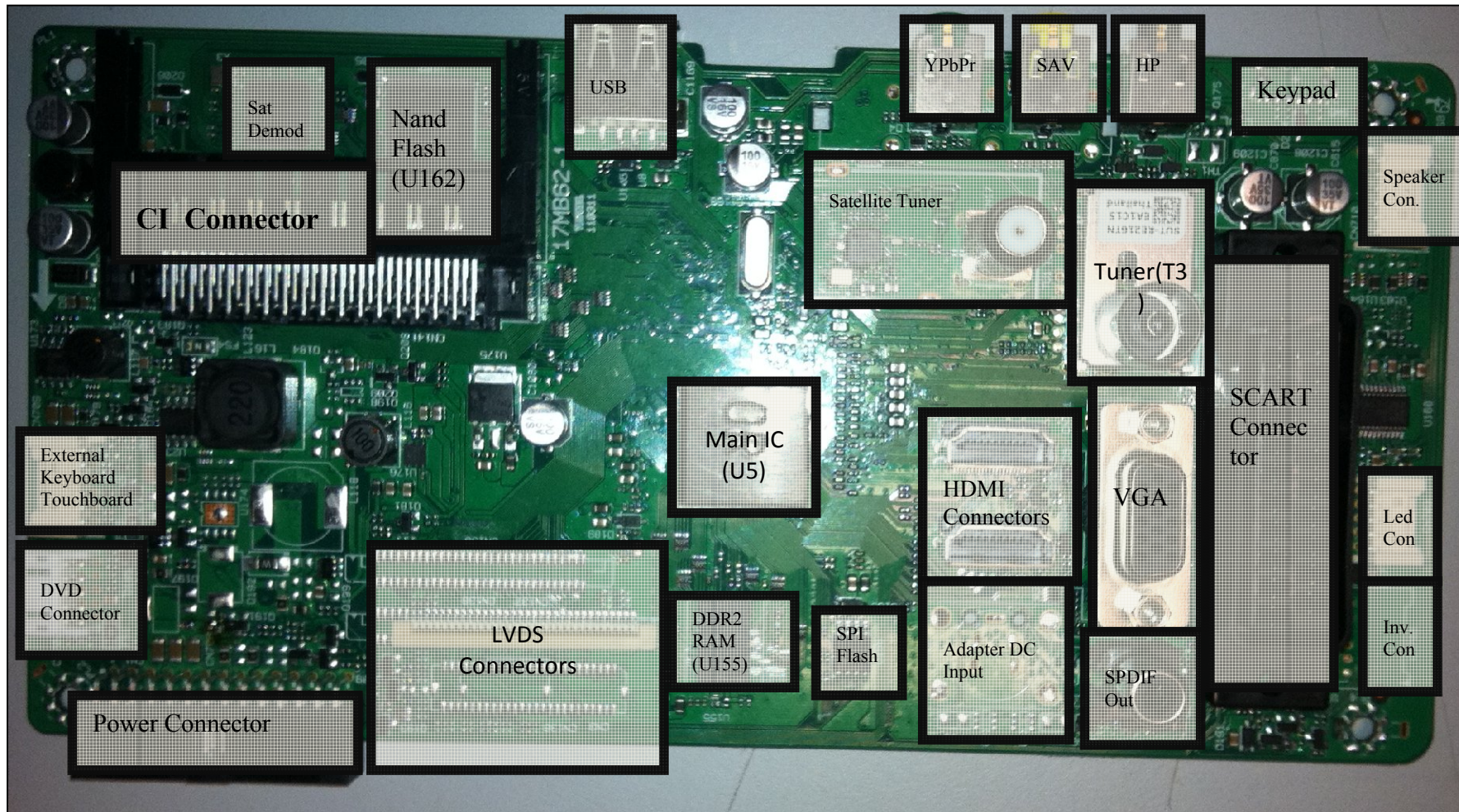
Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF @ 75Ohm(Common)
- 1 Side AV (CVBS, R/L_Audio)
- 1 SCART socket(Common)
- 1 YPbPr (Optional)
- 1 PC input(Common)
- 2 HDMI 1.3 input(1 HDMI input is common, 1 input is optional)
- 1 S/PDIF output(Optional)
- 1 Headphone(Optional)
- 1 Common interface(Common)
- 1 USB(Common)
- 1 DVD(Optional)
- 1 On-board Keypad(Optional)
- 1 External Keypad(Optional)
- 1 External TouchPad(Optional)

1.1. General Block Diagram



1.2.MB62 Placement of Blocks

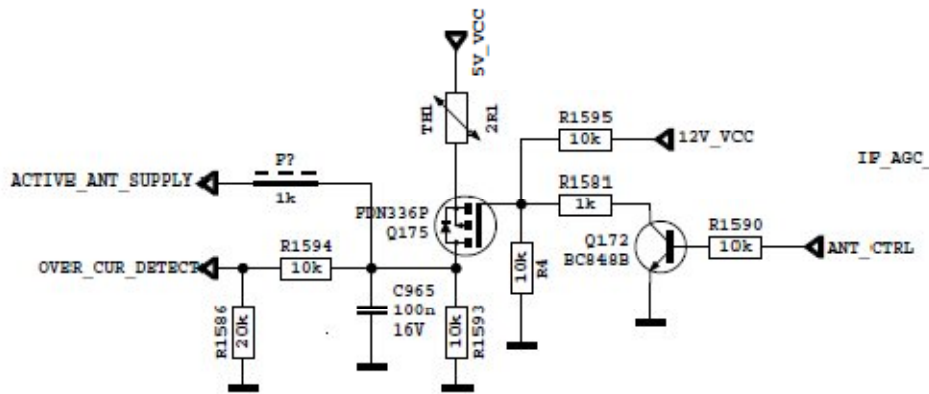


1. TUNER(TU3)

A horizontal mounted and Digital Half-Nim tuner is used in the product, which covers 3 Bands(From 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). The tuning is available through the digitally controlled I2C bus (PLL). Below you will find info about the tuner.

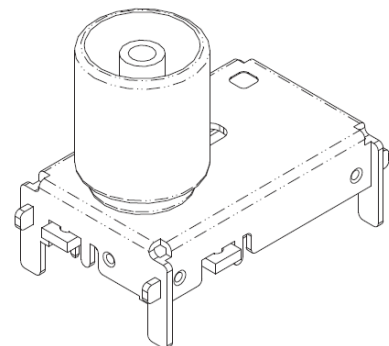
In active antenna option, the following circuit are used. ANT_CTRL pin is controlled by microcontroller. If ANT_CTRL is low, ANT_PWR will be low. If ANT_CTRL is high, ANT_PWR will be high.

OVER_CUR_DETECT pin is a monitor for short circuit in antenna. OVER_CUR_DETECT is low, ANT_CTRL will be low, so ANT_PWR will be low. Finally, short circuit protection is done by circuits and microcontroller.



1.1. General description of Sony RE216:

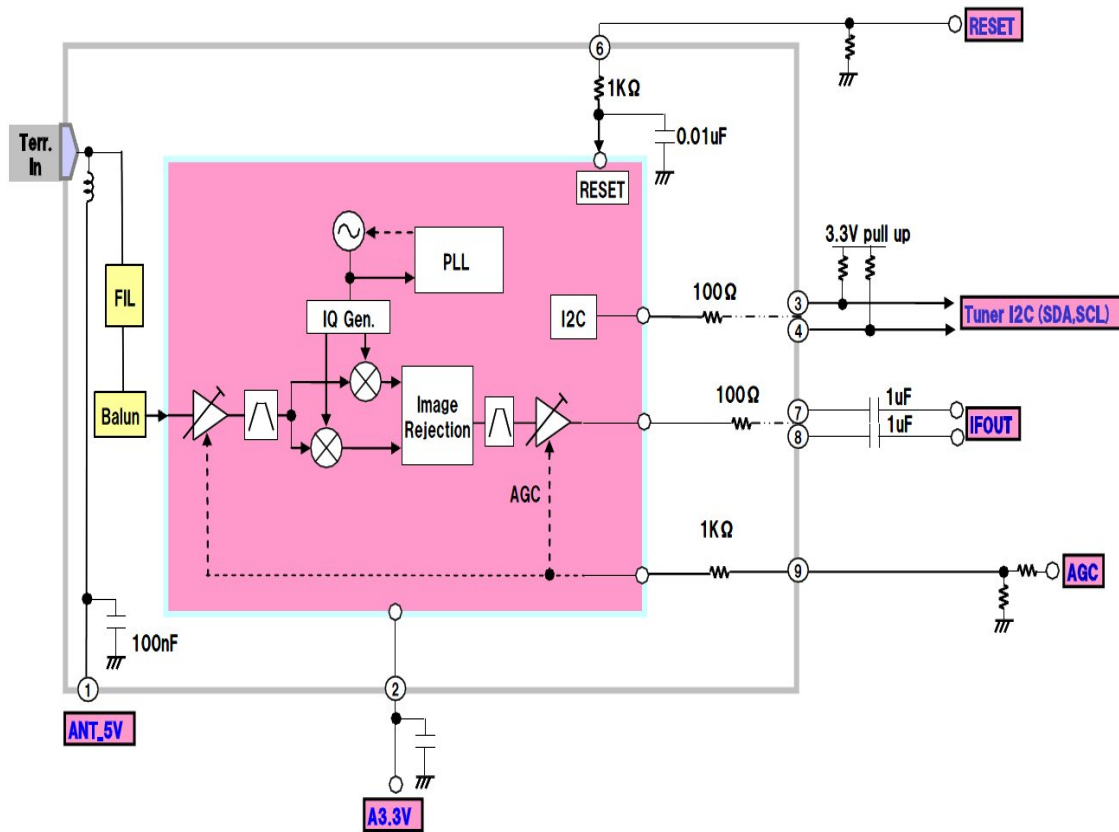
The SUT-RE216 is designed for terrestrial TV (digital & analog) and digital cable reception. It includes a full band tuner and a channel filtering for digital signals. It provides a low IF output after channel filtering to drive a channel demodulator. Tuning, band switching and initialization are made via an I2C bus interface. The module is built on a low-loss printed circuit board carrying all the components in a metal housing frame with top and rear covers. The single aerial connector is mounted on one frame side and all other connections are made via pins at the bottom.



Features:

- ✓ Full frequency range from 47 to 870 Mhz
- ✓ Digital Platform (DVB-T/T2, DVB-C, ISDB-T & ATSC)
- ✓ Analog platforms (PAL B/G/I/D/K, NTSC M & SECAM L/L')
- ✓ Low IF tuner concept

- ✓ Programmable channel Filter bandwidth
- ✓ Fully I2C bus controlled
- ✓ For Hybrid TV applications



---Pinning Table

No	Item	Description
1	ANT_5V	5V supply to an external amplifier via antenna connector. Maximum current is 200mA. If this function is not required in customer's application, it should be connected with GND.
2	A3.3V	3.3V power supply for RF IC. The power supply is recommended to use series regulator etc. in order to reduce ripple component.
3	I2C_SCL	I2C serial clock (0/3.3V, fast mode)
4	I2C_SDA	I2C serial data (0/3.3V, fast mode)
5	GND	-
6	RESET	RF IC system reset (0/3.3V). Low: RESET, High: Normal operation RESET must be kept "Low" when the status is power on.
7	IF_N	Low IF output for external demodulator.
8	IF_P	Low IF output for external demodulator.
9	AGC	IF AGC input from external demodulator

and Application Block Diagram of Tuner---

2. AUDIO AMPLIFIER STAGE WITH AZAD2102(U163, U164)

2.1. General Description

17MB62 uses two 2.5W Class D Mono Audio Amplifiers for from 16" to 24" TVs. AZAD2102B is a 2.9 Watts (max. can offer 3.0 Watts @ Load = 3Ω, THD=10%, AVdd=DVdd=5.5V) with high efficiency filter-free class-D audio power amplifier in a 1613 mm x 1613 mm wafer chip scale package (WCSP). AZAD2102B uses Current-switch technology to achieve high performance class-d amplifier that features 0.03% THD, 85% efficiency, -70 dB PSRR, to improve RF-rectification immunity.

AZAD2102B provide a Vibration-Spectrum modulation clock for PWM Output. This vibration frequency is around 10KHZ shift (+/- 5KHZ of Fpwm).

The advantage of the small size package (WCSP) makes AZAD2102B very suitable for mobile phone and PDA device application. And the Class-D amplifier structure let AZAD2102B to have highly efficiency power consumption than Class-AB amplifier. AZAD2102B can shrink the application board, reduce system cost, and external components.

ESD level protection I/O embedded in AZAD2102B. For general applications, doesn't need to add extra ESD protection device (like Varistors) in application system for AZAD2102B's I/O.

2.2. Features

- CMOS Technology
- High Efficiency 85%
- High PSRR 70dB at 217Hz
- Differential OP-amp Input
- AZAD2102B provides Vibration-Spectrum Modulation clock for reduce EMI
- Provide Mute function(set Mute_B to GND will go into Mute status)
- For the input stage AZAD2102B built-in a 10Kohm resistors (Gain setting=29.5dB)
- Maximum Battery Life and Minimum Heat
- Efficiency With an 8- Ω Speaker:
 - 3.5 mA Quiescent Current
 - Output Power at 10% THD
 - 2.85Watts at AVdd=DVdd=5.0Volt, Rload=4 Ω
 - 1.45Watts at AVdd=DVdd=3.6Volt, Rload=4 Ω
 - 0.30Watts at AVdd=DVdd=3.0Volt, Rload=4 Ω
 - 1.75Watts at AVdd=DVdd=5.5Volt, Rload=8 Ω
 - 0.87Watts at AVdd=DVdd=3.6Volt, Rload=8 Ω
 - 0.41Watts at AVdd=DVdd=3.0Volt, Rload=8 Ω
- Eliminate Power on and Power-off “Pop” noise
- A Fewer External Components
- Optimized PWM Output Stage Eliminates LC Output Filter
- Internally generate 290 kHz Switching Frequency to eliminate Capacitor and Resistor
- Improve PSRR (–70 dB) and Wide Supply Voltage (3.0 V to 5.5 V)
- Fully Differential Design Reduces RF Rectification
- This chip has been built-in a very strong ESD protection.
- System level ESD 4KV (IEC 61000-4-2 ESD Contact Level)
- Wafer Chip Scale Package (WCSP)
- TSSOP Package with Exposed Pad

2.3. Absolute Ratings

2.3.1. Electrical Characteristics

VDD=AVdd=DVdd , VSS=AVss=DVss=Ground

TA = 25°C, Filter Bandwidth = 20 ~20KHz

PARAMETER	Symbol	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	Vop	AVdd=DVdd to AVss=DVss	3.0	5	5.5	V
Output offset voltage	VOS	VDD = 5.5 V, VI = 0 V, AV = 6 V/V		4.5	6.5	mV
		VDD = 3.6 V, VI = 0 V, AV = 6 V/V		2.1	4.0	
		VDD = 3.0 V, VI = 0 V, AV = 6 V/V		1.2	3.0	
Power supply rejection ratio	PSRR	VDD = 3.0 V to 5.5 V, AV = 2 V/V input ac grounded with Ci=2.2uF,Vripple=200mVpp, RL=8Ω,f=217Hz		-68		dB
Common mode rejection ratio	CMRR	VDD = 3.0 V to 5.5 V , Vi c = VDD/2 to 0.5 V, Vi c = VDD/2 to 0.5 VDD -0.8 V,		-65		dB
High level Input current	IIH	VDD= 5.5V, Vi=5.8V		25		uA
Low level Input current	IIL	VDD= 5.5V, Vi=-0.3V		1		uA
Operation current	Iop	VDD = 5.5 V, no load		3.6	5.0	mA
		VDD = 3.6 V, no load		3.0	4.2	
		VDD = 3.0 V, no load		2.5	3.5	
Output switching frequency	Fpwm	VDD = 5.5 V, no load		290		KHz
		VDD = 3.6 V, no load		300		
		VDD = 3.0 V, no load		315		
Vibration-Spectrum Modulation clock Range	Fvs	VDD = 5.0 V, no load		+/-5	+/-10	KHz
Under Voltage Protection	UVP	Vin+ and Vin- connect to GND, no load		2.0	2.5	V
Mute_B pin Impedance	RMuB	Mute_B to Ground		270		KΩ
Gain	Gain	VDD=5.0V,Ri=5KΩ+10KΩ (Av=20V/V)	18	20	22	V/V

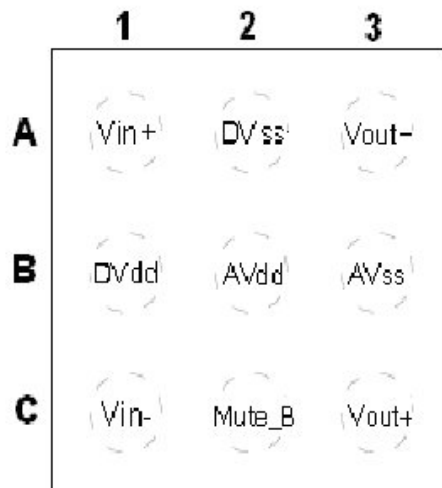
2.3.2. Operating Specifications

T_A = 25°C, Gain = 20 V/V,

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P _w	Output power	THD + N = 10%, f = 1 kHz, R _L = 4 Ω	VDD = 5.0 V		2.85		W
			VDD = 3.6 V		1.45		
			VDD = 3.0 V		0.77		
		THD + N = 1%, f = 1 kHz, R _L = 4 Ω	VDD = 5.0 V		2.25		W
			VDD = 3.6 V		1.15		
			VDD = 3.0 V		0.60		
		THD + N = 10%, f = 1 kHz, R _L = 8 Ω	VDD = 5.0 V		1.75		W
			VDD = 3.6 V		0.87		
			VDD = 3.0 V		0.47		
		THD + N = 1%, f = 1 kHz, R _L = 8 Ω	VDD = 5.0 V		1.39		W
			VDD = 3.6 V		0.70		
			VDD = 3.0 V		0.36		
THD+N	Total harmonic distortion plus noise	VDD = 5.0 V, P _O = 1 W, R _L = 8 Ω, f = 1 kHz			0.15		%
		VDD = 3.6 V, P _O = 0.5 W, R _L = 8 Ω, f = 1 kHz			0.12		
		VDD = 3.0 V, P _O = 200 mW, R _L = 8 Ω, f = 1 kHz			0.09		
PSRR	Supply ripple rejection ratio	VDD = 3.6 V, A _v =20V/V, Inputs connect to grounded with C _i = 1.0μF	F = 217 Hz, V _{Ripple} = 200 mVpp		-67		dB
SNR	Signal-to-noise ratio	VDD = 5 V, P _O = 1 W, R _L = 8 Ω			95		dB
V _{noise}	Output noise level	VDD = 3.6 V, f = 20 Hz to 20 kHz, Inputs ac-grounded with C _i = 1.0μF	No weighting		45		μVRMS
			A weighting		40		
CMRR	Common mode rejection ratio	VDD = 3.6 V, V _{in} = 100mVpp	f = 217 Hz		-72		dB
Z _I	Input impedance			8	10	12	kΩ
Z _F	Feedback resistor			120	150	180	kΩ

2.4. Pinning

Top View



Pad Location	Pad Name	I/O	Function
A1	Vin+	I	Non-inverting Input
B1	DVdd		Supply Voltage for control circuit
C1	Vin-	I	Inverting Input
A2	DVss		Ground pad for control circuit
B2	AVdd		Supply Voltage for Power MOS
C2	Mute_B	I	Mute control pin
A3	Vout-	O	Negative Output
B3	AVss		Ground pad for Power MOS
C3	Vout+	O	Positive Output

3. AUDIO AMPLIFIER STAGE WITH TPA3113(U168)

3.1. General Description

17MB62 uses a 6W Class D Mono Audio Amplifiers for from 26" to 32" TVs. The TPA3113D2 is a 6-W (per channel) efficient, Class-D audio power amplifier for driving bridged-tied stereo speakers. Advanced EMI Suppression Technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. SpeakerGuard™ speaker protection circuitry includes an adjustable power limiter and a DC detection circuit. The adjustable power limiter allows the user to set a "virtual" voltage rail lower than the chip supply to limit the amount of current through the speaker. The DC detect circuit measures the frequency and amplitude of the PWM signal and shuts off the output stage if the input capacitors are damaged or shorts exist on the inputs.

The TPA3113D2 can drive stereo speakers as low as 4 Ω. The high efficiency of the TPA3113D2, 87%, eliminates the need for an external heat sink when playing music.

The outputs are also fully protected against shorts to GND, VCC, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

3.2. Features

- 6-W/ch into an 8- Ω Loads at 10% THD+N From a 10-V Supply
- 12-W into a 4- Ω Mono Load at 10% THD+N From a 10-V Supply
- 87% Efficient Class-D Operation Eliminates Need for Heat Sinks
- Wide Supply Voltage Range Allows Operation from 8 V to 26 V
- Filter-Free Operation
- SpeakerGuard™ Speaker Protection Includes Adjustable Power Limiter plus DC Protection
- Flow Through Pin Out Facilitates Easy Board Layout
- Robust Pin-to-Pin Short Circuit Protection and Thermal Protection with Auto Recovery Option
- Excellent THD+N / Pop-Free Performance
- Four Selectable, Fixed Gain Settings
- Differential inputs

3.3. Absolute Ratings

3.3.1. Electrical Characteristics

DC CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$, $R_L = 8\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V _{OS}	Class-D output offset voltage (measured differentially)	V _I = 0 V, Gain = 36 dB			1.5	15	mV	
I _{CC}	Quiescent supply current	SD = 2 V, no load, PV _{CC} = 12V			20	35	mA	
I _{CC(SD)}	Quiescent supply current in shutdown mode	SD = 0.8 V, no load, PV _{CC} = 12V			200		μA	
r _{DS(on)}	Drain-source on-state resistance	V _{CC} = 12 V, I _O = 500 mA, T _J = 25°C	High Side		400		mΩ	
			Low side		400			
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB	
			GAIN0 = 2 V	25	26	27		
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB	
			GAIN0 = 2 V	35	36	37		
t _{ON}	Turn-on time	SD = 2 V			14		ms	
t _{OFF}	Turn-off time	SD = 0.8 V			2		μs	
GVDD	Gate Drive Supply	I _{GVDD} = 2mA			6.4	6.9	7.4	V
V _O	Output Voltage maximum under PLIMIT control	V _(PLIMIT) = 2 V; V _I = 1V rms			6.75	7.90	8.75	V

3.3.2. Operating Specifications

AC CHARACTERISTICS

$T_A = 25^{\circ}\text{C}$, $V_{CC} = 12\text{ V}$, $R_L = 8\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	200 mV _{pp} ripple from 20 Hz–1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		–70		dB
THD+N	Total harmonic distortion + noise	$R_L = 8\ \Omega$, $f = 1\text{ kHz}$, $P_O = 3\text{ W}$ (half-power)		0.06		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		μV
				–80		dBV
	Crosstalk	$P_O = 1\text{ W}$, Gain = 20 dB, $f = 1\text{ kHz}$		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, $f = 1\text{ kHz}$, Gain = 20 dB, A-weighted		102		dB
f_{osc}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		$^{\circ}\text{C}$
	Thermal hysteresis			15		$^{\circ}\text{C}$

3.4. Pinning

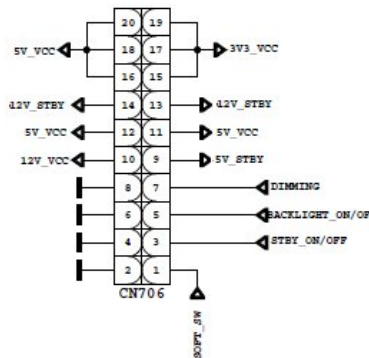
PIN		I/O/P	DESCRIPTION
NAME	Pin Number		
$\overline{\text{SD}}$	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
$\overline{\text{FAULT}}$	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULT pin to SD pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
LINP	3	I	Positive audio input for left channel. Biased at 3V.
LINN	4	I	Negative audio input for left channel. Biased at 3V.
GAIN0	5	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	6	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
AVCC	7	P	Analog supply
AGND	8		Analog signal ground. Connect to the thermal pad.
GVDD	9	O	High-side FET gate drive supply. Nominal voltage is 7V. Also should be used as supply for PLIMIT function
PLIMIT	10	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
RINN	11	I	Negative audio input for right channel. Biased at 3V.
RINP	12	I	Positive audio input for right channel. Biased at 3V.
NC	13		Not connected
PBTL	14	I	Parallel BTL mode switch
PVCCR	15	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
PVCCR	16	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally.
BSPR	17	I	Bootstrap I/O for right channel, positive high-side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
PGND	19		Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	I	Bootstrap I/O for right channel, negative high-side FET.
BSNL	22	I	Bootstrap I/O for left channel, negative high-side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.
PGND	24		Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	I	Bootstrap I/O for left channel, positive high-side FET.
PVCCL	27	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.
PVCCL	28	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.

4. POWER STAGE

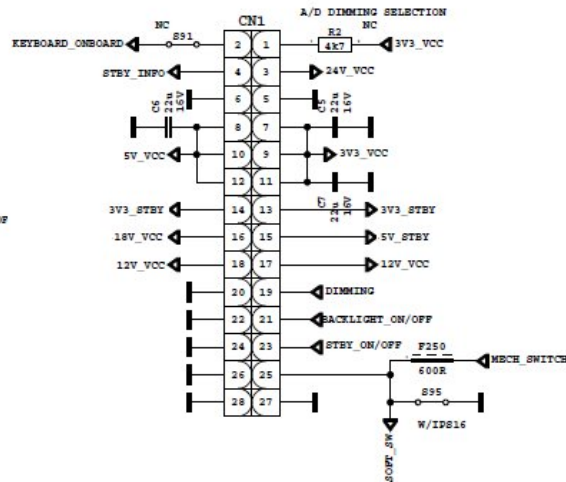
The DC voltages required at various parts of the chassis and panel are provided by a main power supply unit. MB62 chassis can operate with IPS60, IPS16, IPS17, PW26, PW27 as main power supply and also with 12V adaptor.

CN706 is used for IPS60, IPS16 and IPS17 and CN1 is used for PW26 and PW27.

16" to 24" POWER SOCKET

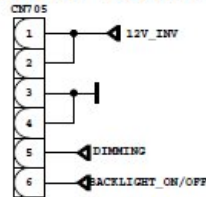


26" to 32" POWER SOCKET

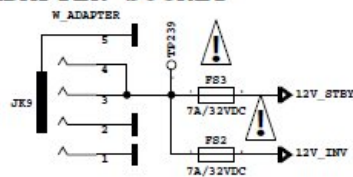


JK9 is used for the adapter option and also CN705 inverter socket or DB32 chassis with CN706 is used to supply backlight.

INVERTER SOCKET W/ADAPTER

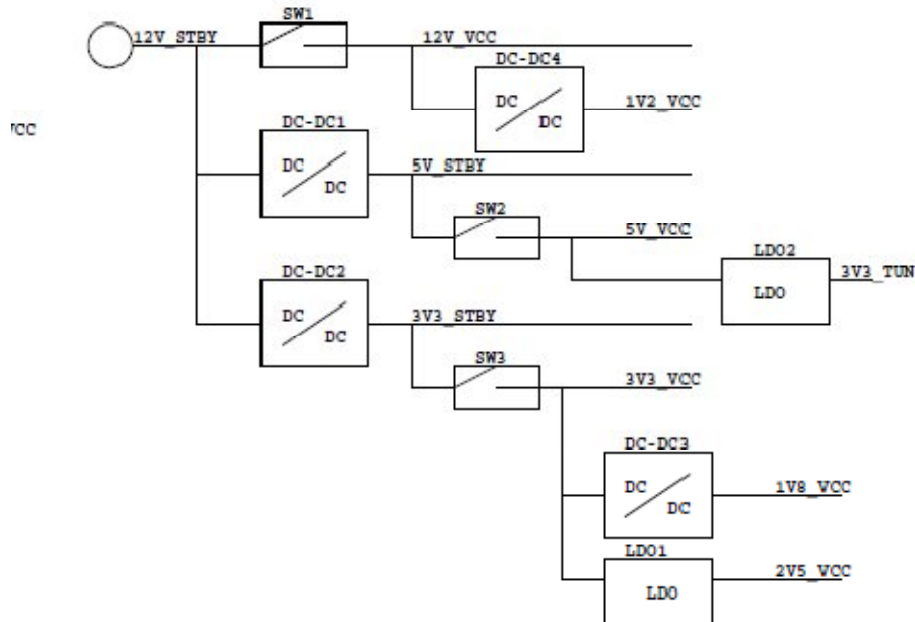


ADAPTER SOCKET

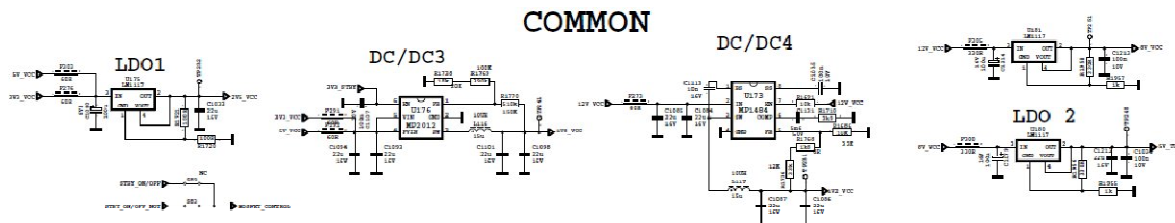


The power supplies generate 18V, 12V, 5V, 3,3V and 12V, 5V, stand by mode DC voltages. Power stage which is on-chassis generates 5V, 3V3 stand by voltage and 12V, 8V, 5V, 3V3, 2.5V, 1,8V and 1,2V supplies for other different parts of the chassis. Chassis block diagram is indicated below.

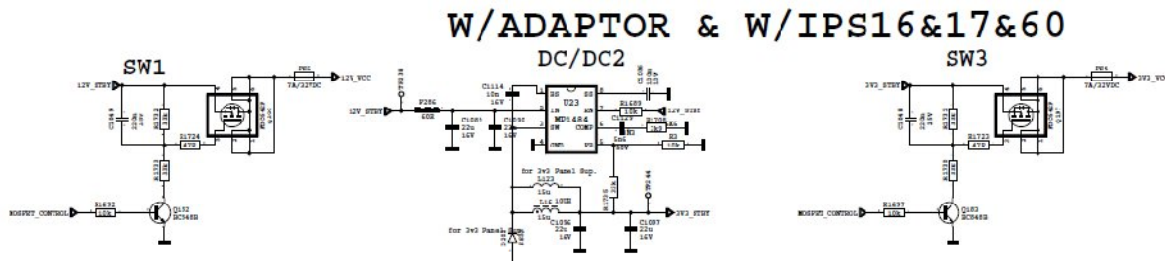
POWER BLOCK DIAGRAM



The blocks on power block diagram is using dependent to main supply. For PW26 and PW27 just common blocks are enough for proper operation.

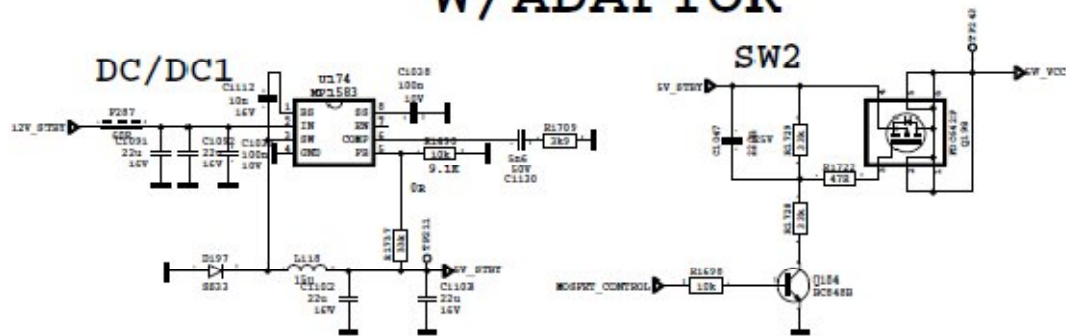


For IPS16, IPS17, IPS60 below blocks must work properly.



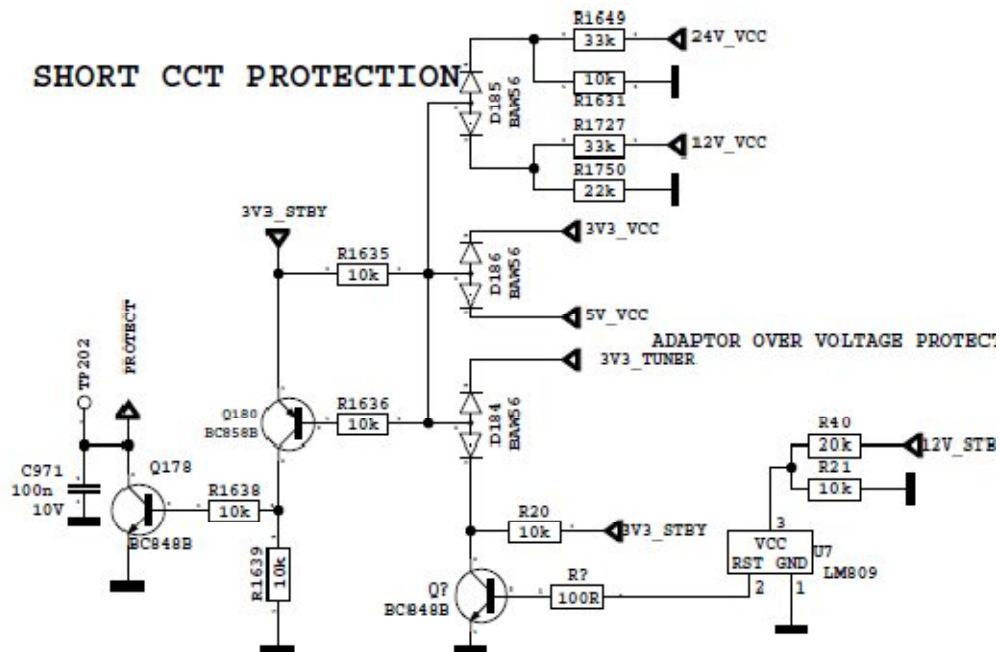
For adopter case also below blocks are necessary.

W/ADAPTOR

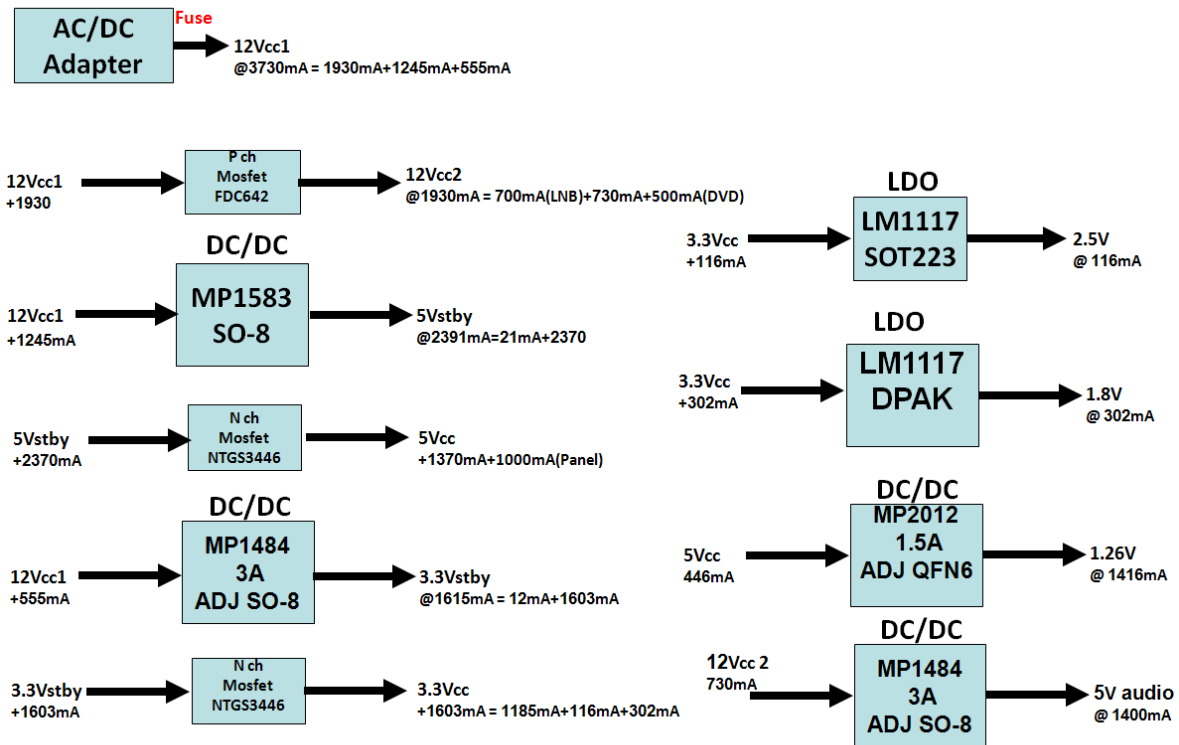


Short CCT Protection Circuit

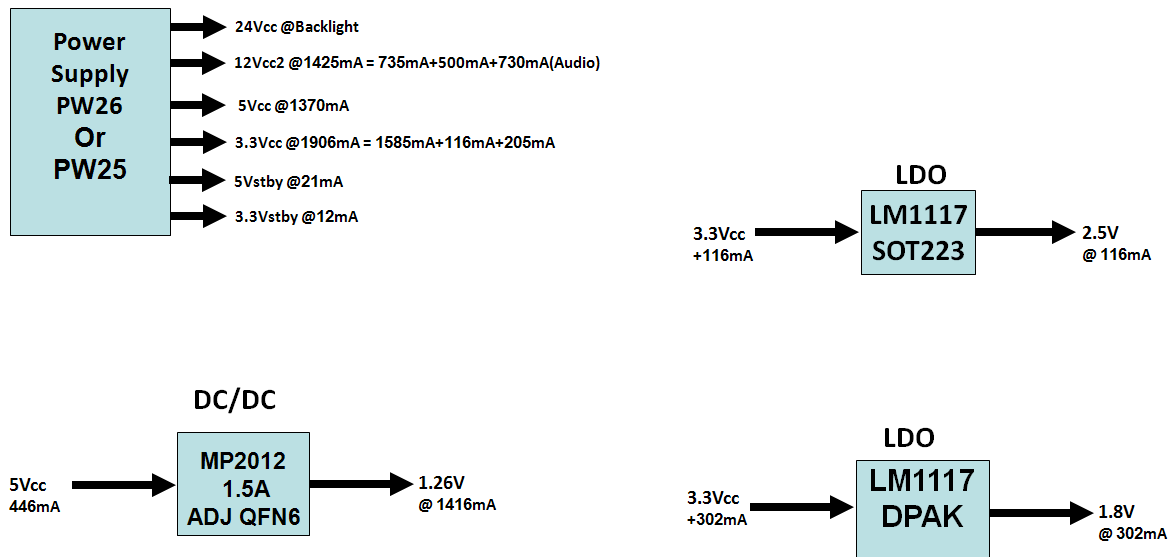
Short circuit protection is necessary for protecting chassis and main IC against damages when any Vcc supply shorts to ground. Protect pin should be logic high while normal operation. When there is a short circuit protect pin should be logic low. After any short detection, SW forces LEDs on LED card to blink.



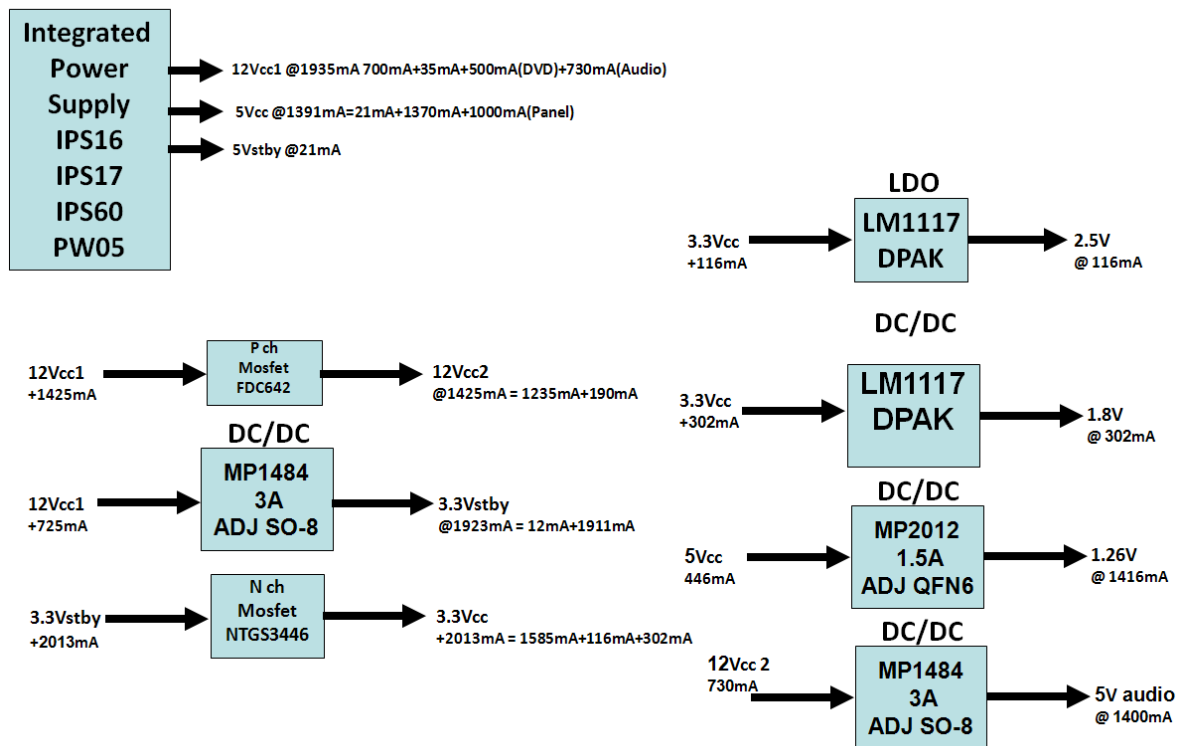
4.1. Power Management



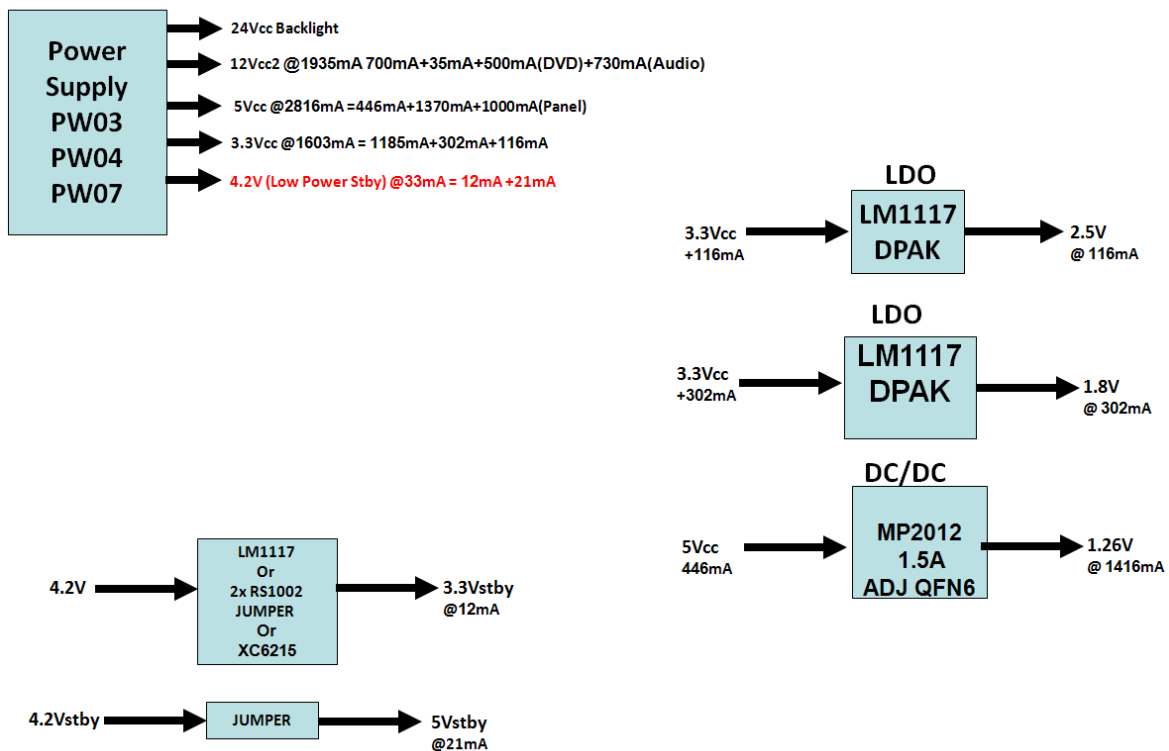
---MB62 Power Management with Adaptor---



---MB62 Power Management with PW25/ PW26---



---MB62 Power Management with IPS16/IPS17/IPS60/PW05---



---MB62 Power Management with PW03/PW04/PW07---

5. MICROCONTROLLER – MSTAR(U5)

5.1. Description

MSD9WB9PT-2 (Main IC) (U5)

The MSD9WB9PT-2 is MStar's most up-to-date system-on-chip solution for flat panel integrated digital television products. Building on the success of MStar's preceding SOC series, the MSD9WB9PT-2 provides most cost-effective solution for DTV application with creative and attractive features exclusively presented by MStar.

The MSD9WB9PT-2 integrates DTV/multi-media all-purpose AV decoder, DVB-T demodulator, VIF demodulator, and Sound/Video processor into a single device. This allows the overall BOM to be reduced significantly making the MSD9WB9PT-2 a very competitive multi-media DTV solution. For ATV users, the MSD9WB9PT-2 provides multi-standard analog TV support with adaptive 3D video decoding and VBI data extraction. The build-in audio decoder is capable of decoding FM, AM, NICAM, A2, BTSC and EIA-J sound standards. The MSD9WB9PT-2 supplies all the necessary A/V inputs and outputs to complete a receiver design including a multi-port HDMI receiver and component video ADC. All input selection multiplexed for video and audio are integrated, including full SCART support with CVBS output. The equipped MStar MACE-5 color engine is the latest masterpiece from

MStar famous color engine series providing excellent video and picture quality in Full-HD and large-scale displaying system.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MSD9WB9PT-2 has an ultra low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

The MSD9WB9PT-2 is composed of several modules:

- ☐ High Performance Micro-processor
 - Ultra high speed/performance 32-bit RISC CPU
 - One full duplex UARTs
 - Supports USB and ISP programming
 - DMA Engine
- ☐ Transport Stream De-multiplexer
 - Supports parallel and serial TS interface, with or without sync signal
 - Supports TS input and output for external CI module
 - Maximum TS data rate is 104 Mb/sec for serial or 16 MB/sec for parallel
 - 32 general purpose PID filters and section filters for each transport stream de-multiplexer
 - Supports additional audio/video/PCR filters
 - Supports TS DMA channel for time-shift
 - Supports 3DES/DES and AES encryption/decryption
- ☐ MPEG-2 Video Decoder
 - ISO/IEC 13818-2 MPEG-2 video MP@HL
 - Automatic frame rate conversion
 - Supports resolution up to HDTV (1080i, 720p) and SDTV

□ MPEG-4 Video Decoder

- ISO/IEC 14496-2 MPEG-4 ASP video decoding
- Supports resolutions up to HDTV (1080p@30fps)
- Supports DivX1 Home Theater & HD profiles **Optional**
- Supports VC-1 **Optional**, FLV video format decoding

□ Hardware JPEG

- Supports sequential mode, single scan
- Supports both color and grayscale pictures
- Following the file header scan the hardware decoder fully handles the decode process
- Supports programmable Region of Interest (ROI)
- Supports formats: 422/411/420/444/422T
- Supports scaling down ratios: 1/2, 1/4, 1/8
- Supports picture rotation

□ NTSC/PAL/SECAM Video Decoder

- Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
- Automatic standard detection
- Motion adaptive 3D comb filter
- Five configurable CVBS & Y/C S-video inputs
- Supports Teletext, Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), V-chip and SCTE

□ Multi-Standard TV Sound Processor

- SIF audio decoding
- Supports BTSC/A2/EIA-J demodulation
- Supports NICAM/FM/AM demodulation
- Supports MTS Mode Mono/Stereo/SAP in BTSC/ EIA-J mode
- Supports Mono/Stereo/Dual in A2/NICAM mode
- Built-in audio sampling rate conversion (SRC)
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
- Advanced sound processing options available, for example: SRS1, BBE2, QSound3, Audyssey4
- Supports digital audio format decoding:
 - ~ MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3), AAC-LC
 - ~ Supports **Optional** Dolby Digital Plus, Dolby mPulse, and MS10 multistream decoder, including Dolby Digital Encoder for transcoding streams to Dolby Digital 5.1 (DDCO)
- Supports MPEG Audio, Dolby Digital, Dolby Digital Plus format AD (Audio Description)
- Supports PVR and time-shifting

□ Audio Interface

- One SIF audio input interface with minimal external saw filters
- Four L/R audio line-inputs
- Two L/R outputs for main speakers and additional line-outputs
- Supports stereo headphone driver

- I2S digital audio input & output
- S/PDIF digital audio output
- HDMI audio channel processing
- Programmable delay for audio/video synchronization
- Analog RGB Compliant Input Port
 - Three analog ports support up to 1080P
 - Supports PC RGB input up to SXGA@75Hz
 - Supports HDTV RGB/YPbPr/YCbCr
 - Supports Composite Sync and SOG Sync-on-Green
 - Automatic color calibration
 - AV-link support
- Analogue RGB Auto-Configuration & Detection
 - Auto input signal format and mode detection
 - Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
 - Sync Detection for H/V Sync
- DVI/HDCP/HDMI Compliant Input Port
 - Two HDMI/DVI Input ports
 - HDMI 1.3 Compliant
 - HDCP 1.1 Compliant
 - 225MHz @ 1080P 60Hz input with 12-bit Deep-color support
 - CEC support
 - Single link DVI 1.0 compliant
 - Robust receiver with excellent long-cable support
- MStar Advanced Color Engine (MStarACE-5)
 - 10/12-bit internal data processing
 - Fully programmable multi-function scaling engine
 - ~ Nonlinear video scaling supports various modes including Panorama
 - ~ Supports dynamic scaling for VC-1
 - High-Quality DTV video processor
 - ~ 3D motion video deinterlacer with motion object stabilizer
 - ~ Edge-oriented deinterlacer with edge and artifact smoother
 - ~ Automatic 3:2/2:2/M:N pull-down detection and recovery
 - ~ 3D multi-purpose noise reduction for DTV or lousy air/cable input
 - ~ MPEG artifact removal including de-blocking and mosquito noise reduction
 - ~ Arbitrary frame rate conversion
 - MStar Professional Picture Enhancement:
 - ~ Dynamic brilliant and fresh color
 - ~ Dynamic Blue Stretch
 - ~ Intensified contrast and details
 - ~ Dynamic Vivid Skin
 - ~ Dynamic sharpened Luma/Chroma edges
 - ~ Global and local dynamic depth of field perception
 - ~ Accurate and independent color control
 - ~ Supports sRGB and xvYCC color processing
 - ~ Supports HDMI 1.3 deep color format
 - Programmable 12-bit RGB gamma CLUT

□ Output Interface

- Single/dual link 8/10-bit LVDS output
- Supports panel resolution up to Full-HD (1920x1080) @ 60Hz
- Supports TH/TI format
- Supports dithering options to 6/8-bit output
- Spread spectrum output for EMI suppression

□ CVBS Video Encoder

- Supports all NTSC/PAL TV Standard
- Stand-alone scaling engine
- Programmable Hue, Contrast, Brightness
- Supports TTX/CC/WSS output

□ CVBS Video Output

- Allows CVBS output of all source inputs

□ 2D Graphics Engine

- Hardware Graphics Engine for responsive
- Interactive applications
- Supports point draw, line draw, rectangle draw/fill, text draw and trapezoid draw
- BitBlit, stretch BitBlit, trapezoid BitBlit, mirror BitBlit and rotate BitBlit
- Raster Operation (ROP)
- Support Porter-Duff

□ VIF Demodulator

- Compliant with NTSC M/N, PAL B, G/H, I, D/K,
- SECAM L/L' standards
- Audio/Video dual-path processor
- Stepped-gain PGA with 25 dB tuning range and 1 dB tuning resolution
- Maximum IF gain of 37 dB
- Programmable TOP to accommodate different tuner gain and SAW filter insertion loss to optimize noise and linearity performance
- Multi-standard processing with single SAW
- Supports silicon tuner low IF output architecture

□ DVB-T Demodulator

- Digital carrier frequency offset correction: $\pm 500\text{KHz}$
- Optimised for SFN channels with pre/post-cursive echoes inside/outside the guard
- Acquisition range $\pm 857\text{kHz}$ includes up to $3 \times \pm 1/6\text{ MHz}$ transmitter offset
- Meets Nordig Unified 1.0.3, D-Book 5.0, EICTA E-Book/C-Book test requirement
- $\pm 400\text{kHz}$ internal carrier offset recovery range
- 6.8 μs echo cancellation at 7 Msym/s
- Supports IF, low-IF, zero-IF inputs
- Ultra-fast automatic blind UHF/VHF channel scan (constellations and symbol rate)

□ Connectivity

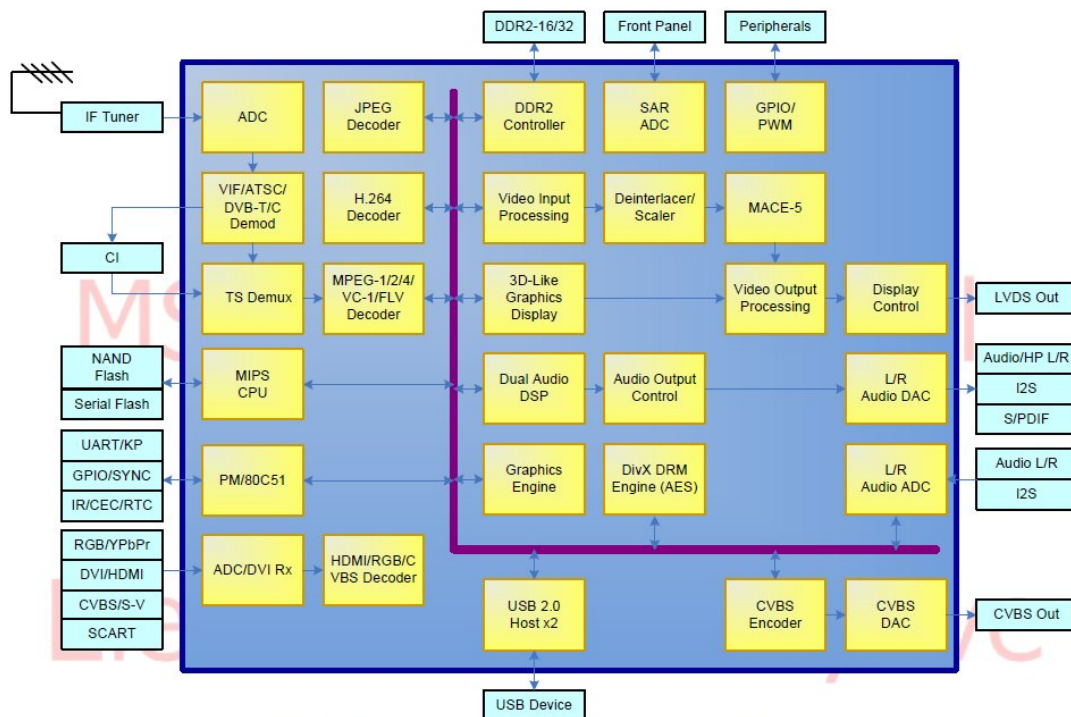
- Two USB 2.0 host ports

- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting

□ Miscellaneous

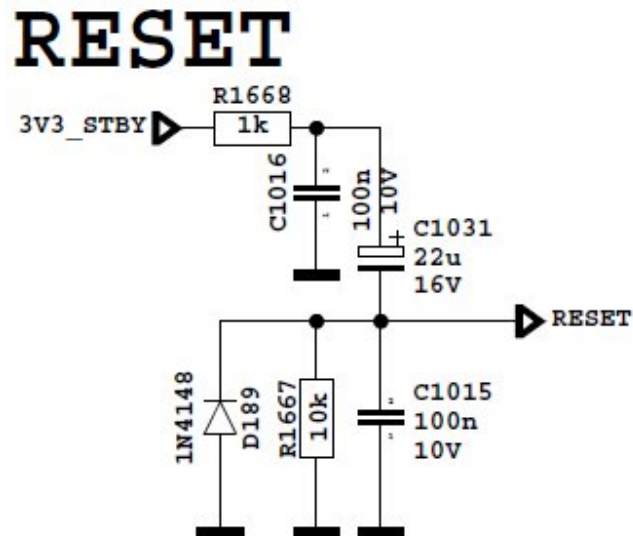
- DRAM interface supporting one 16-bit DDR2 @1066MHz
- Supports PVR
- Supports Common Interface for conditional access support
- Bootable SPI interface with serial flash support
- Parallel interface for external NAND flash support
- Power control module with ultra low power MCU available in standby mode
- 380-ball LFBGA package
- Operating Voltages: 1.26V (core), 1.8V (DDR2), 2.5V and 3.3V (I/O and analog)

5.2. MSTAR Block Diagram



5.3. Reset Circuit

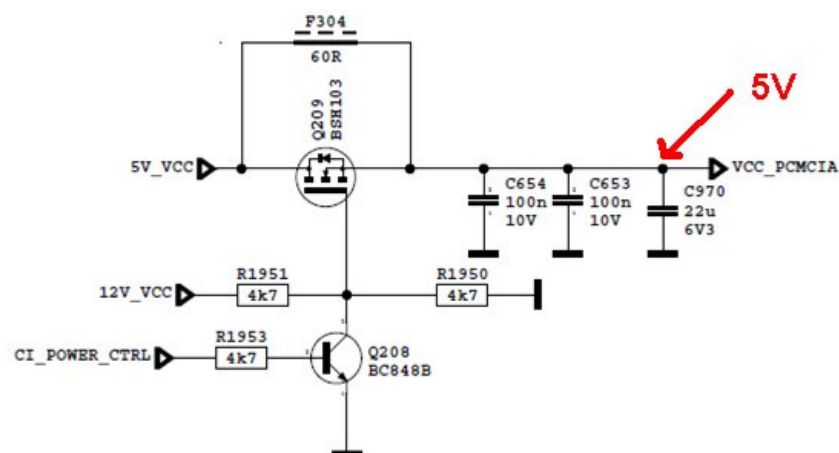
Reset circuit using for initializing main Mstar IC. Reset condition is high and normal working condition is low for RESET pin.



6. CI INTERFACE

CI Interface Power Switch:

It is used for CI module supply, when Module is inserted (it means CI detect is low) This circuit is opened or closed by CI_POWER_CTRL port of main uController

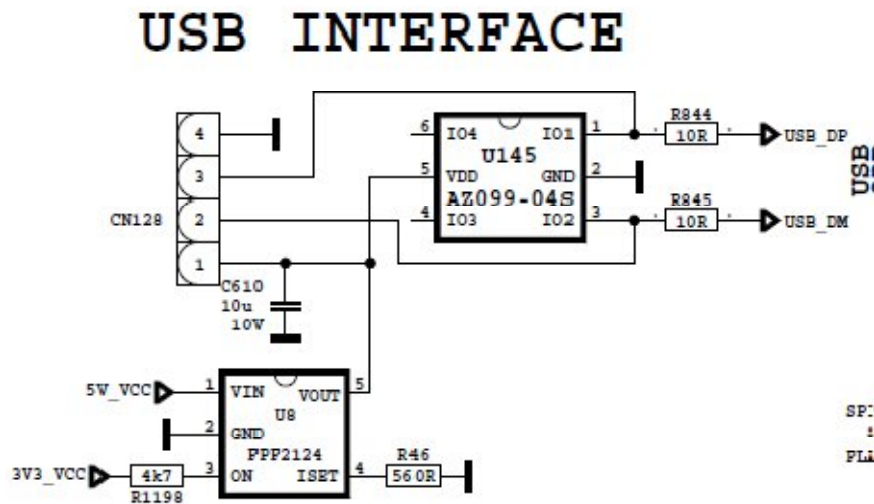


7. USB INTERFACE

Main Concept IC has integrated 2 USB 2.0 interface. One of them is used for ethernet function, the other one is used for USB connectivity for last user. Last user can play video, picture and audio files. Also digital channels can be record to external storage device by this interface. All SW files can be updated with interface.

USB circuit has 3 main parts

- Integrated USB 2.0 Host interface of D3K (U5)
- Protection IC (U145)
- Over Current Protection IC (U8)



8. DDR2 SDRAM K4T1G164QF (U155)

Description:

The 1Gb DDR2 SDRAM is organized as a 16Mbit x 8 I/Os x 8 banks, 8Mbit x 16 I/Os x 8 banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 1066Mb/sec/pin (DDR2-1066) for general applications. The chip is designed to comply with the following key DDR2 SDRAM features such as posted CAS with additive latency, write latency = read latency - 1, Off-Chip Driver(OCD) impedance adjustment and On Die Termination. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a RAS/CAS multiplexing style. For example, 1Gb(x8) device receive 14/10/3 addressing. The 1Gb DDR2 device operates with a single $1.8V \pm 0.1V$ power supply and $1.8V \pm 0.1V$ VDDQ. The 1Gb DDR2 device is available in 60ball FBGA(x8) and 84ball FBGA(x16).

Features:

- JEDEC standard VDD = $1.8V \pm 0.1V$ Power Supply
- VDDQ = $1.8V \pm 0.1V$
- 533MHz fCK for 1066Mb/sec/pin
- 8 Banks
- Posted CAS
- Programmable CAS Latency: 4, 5, 6, 7
- Programmable Additive Latency: 3, 4, 5, 6
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4, 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Special Function Support - PASR(Partial Array Self Refresh) - 50ohm ODT - High Temperature Self-Refresh rate enable
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE < 95°C
- All of products are Lead-free, Halogen-free, and RoHS compliant

Pinning:

1	2	3	4	5	6	7	8	9
---	---	---	---	---	---	---	---	---

A	V _{DD}	NC	V _{SS}
B	DQ14	V _{SSQ}	UDM
C	V _{DDQ}	DQ9	V _{DDQ}
D	DQ12	V _{SSQ}	DQ11
E	V _{DD}	NC	V _{SS}
F	DQ6	V _{SSQ}	LDM
G	V _{DDQ}	DQ1	V _{DDQ}
H	DQ4	V _{SSQ}	DQ3
J	V _{DDL}	V _{REF}	V _{SS}
K		CKE	$\overline{\text{WE}}$
L	BA2	BA0	BA1
M		A10/AP	A1
N	V _{SS}	A3	A5
P		A7	A9
R	V _{DD}	A12	NC

V _{SSQ}	$\overline{\text{UDQS}}$	V _{DDQ}
UDQS	V _{SSQ}	DQ15
V _{DDQ}	DQ8	V _{DDQ}
DQ10	V _{SSQ}	DQ13
V _{SSQ}	$\overline{\text{LDQS}}$	V _{DDQ}
LDQS	V _{SSQ}	DQ7
V _{DDQ}	DQ0	V _{DDQ}
DQ2	V _{SSQ}	DQ5
V _{SSDL}	CK	V _{DD}
$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
A2	A0	V _{DD}
A6	A4	
A11	A8	V _{SS}
NC	NC	

Ball Locations (x16)

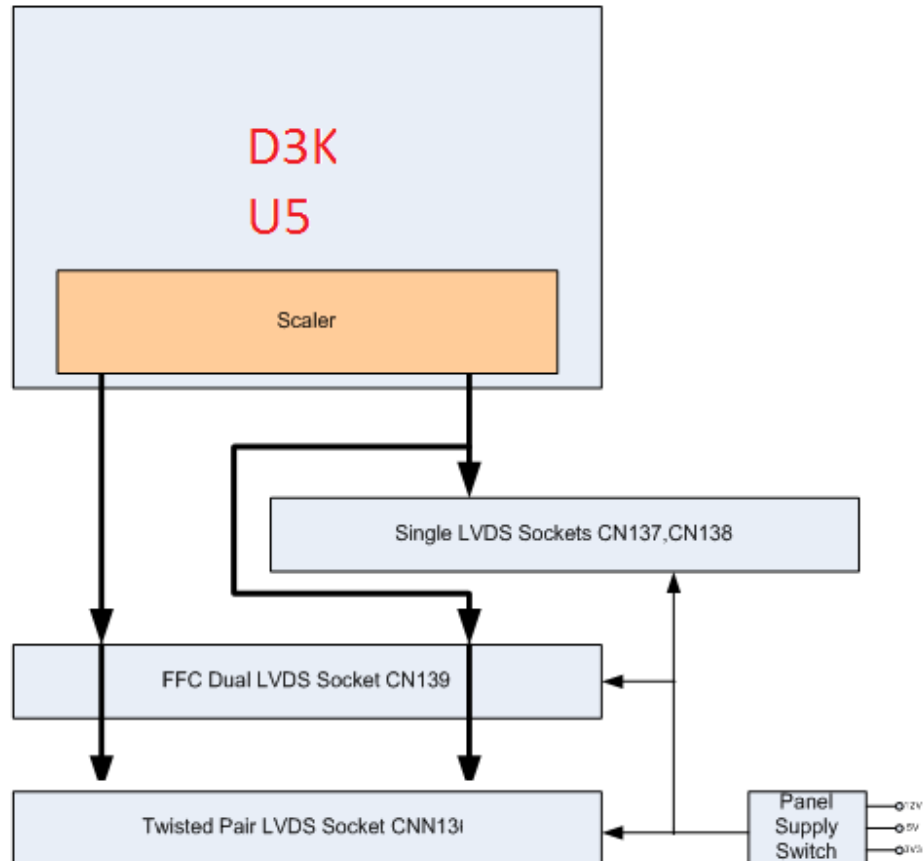
- Populated ball
- + Ball not populated

Top view
(See the balls through package)

	1	2	3	4	5	6	7	8	9
A	●	●	●	+	+	+	●	●	●
B	●	●	●	+	+	+	●	●	●
C	●	●	●	+	+	+	●	●	●
D	●	●	●	+	+	+	●	●	●
E	●	●	●	+	+	+	●	●	●
F	●	●	●	+	+	+	●	●	●
G	●	●	●	+	+	+	●	●	●
H	●	●	●	+	+	+	●	●	●
J	●	●	●	+	+	+	●	●	●
K	+	●	●	+	+	+	●	●	●
L	●	●	●	+	+	+	●	●	+
M	+	●	●	+	+	+	●	●	●
N	●	●	●	+	+	+	●	●	+
P	+	●	●	+	+	+	●	●	●
R	●	●	●	+	+	+	●	●	+

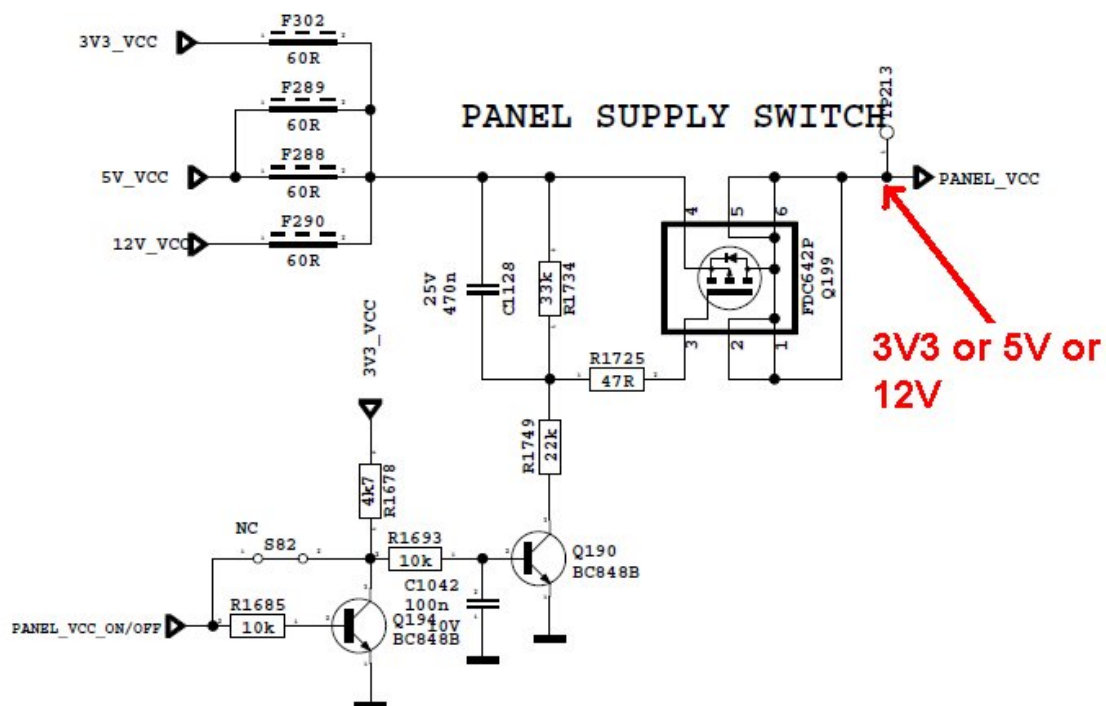
9. SCALER AND LVDS SOCKETS

9.1. LVDS sockets Block Diagram



9.2. Panel Supply Switch Circuit

This switch is used to open and close panel supply of TCON. It is controlled by port of main ucontroller. Also with this circuit panel sequency could be adjusted correctly. 3 panel suplys are connected to this circuit. All of them are optional according to panels.



10. SPI FLASH MEMORY - MX25L1005 (U158)

10.1. General Description

MX25L1005 is a CMOS 1,048,576 bit serial Flash memory, which is configured as 131,072 x 8 internally. The MX25L1005 feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by CS# input. The MX25L1005 provide sequential read operation on whole chip. After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on page (256 bytes) basis, and erase command is executes on chip or sector(4K-bytes) or block(64K-bytes). To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit. When the device is not in operation and CS# is high, it is put in standby mode and draws less than 10uA DC current. The MX25L1005 utilize MXIC's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

10.2. Features

- Serial Peripheral Interface (SPI) compatible -- Mode 0 and Mode 3
- 1,048,576 x 1 bit structure
- 32 Equal Sectors with 4K byte each, Any Sector can be erased individually
- 2 Equal Blocks with 64K byte each, Any Block can be erased individually
- Single Power Supply Operation

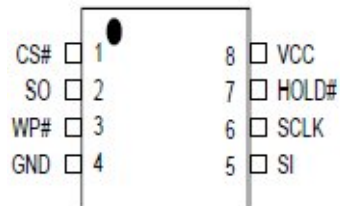
- 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V

10.3. Absolute Maximum Ratings

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 125°C
Applied Input Voltage	-0.5v to 4.6v
Applied Output Voltage	-0.5v to 4.6v
VCC to Ground Potential	-0.5v to 4.6v

10.4. Pinning

8-PIN SOP (150mil)



SYMBOL	DESCRIPTION
CS#	Chip select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
HOLD#	Hold, to pause the device without deselecting the device
VCC	+3.3v Power Supply
GND	Ground

11. NAND FLASH MEMORY – NAND512XXA2C (U162)

11.1. General Description

The NAND flash 528-byte/ 264-word page is a family of non-volatile flash memories that uses the single level cell (SLC) NAND technology. It is referred to as the small page family.

The NAND512R3A2C, NAND512R4A2C, and NAND512W3A2C have a density of 512 Mbits and operate with either a 1.8 V or 3 V voltage supply. The size of a page is either 528 bytes (512 + 16 spare) or 264 words (256 + 8 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 or x16 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

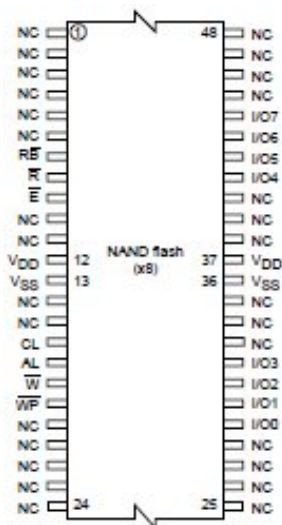
To extend the lifetime of NAND flash devices it is strongly recommended to implement an error correction code (ECC). The use of ECC correction allows to achieve up to 100,000 program/erase cycles for each block. A write protect pin is available to give a hardware protection against program and erase operations.

11.2. Features

- High density NAND flash memories
 - 512-Mbit memory array
 - Cost effective solutions for mass storage applications
- NAND interface
 - x8 or x16 bus width
 - Multiplexed address/ data
- Supply voltage: 1.8 V, 3 V
- Page size
 - x8 device: (512 + 16 spare) bytes
 - x16 device: (256 + 8 spare) words
- Block size
 - x8 device: (16K + 512 spare) bytes
 - x16 device: (8K + 256 spare) words
- Page read/program
 - Random access: 12 μ s (3 V)/15 μ s (1.8 V) (max)
 - Sequential access: 30 ns (3 V)/50 ns (1.8 V) (min)
 - Page program time: 200 μ s (typ)
- Copy back program mode
- Fast block erase: 2 ms (typ)

- Status register
- Electronic signature
- Chip Enable 'don't care'
- Security features
 - OTP area
- Serial number (unique ID) option
- Hardware data protection
 - Program/erase locked during power transitions
- Data integrity
 - 100,000 program/erase cycles (with ECC)
 - 10 years data retention
- RoHS compliant packages
- Development tools
 - Error correction code models
 - Bad blocks management and wear leveling algorithms

11.3. Pinning



12. LNBH23L (U6)

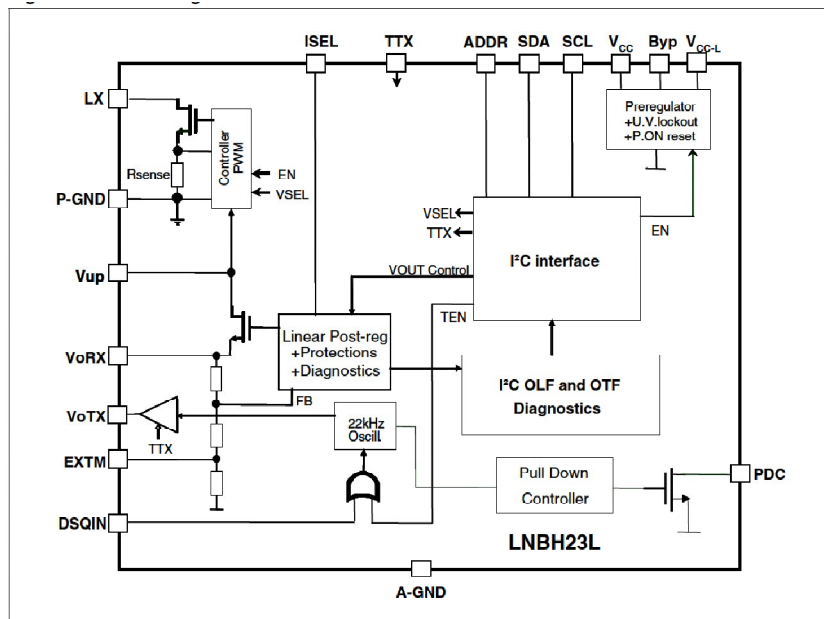
Description:

Intended for analog and digital satellite receivers, the LNBH23L is a monolithic voltage regulator and interface IC, assembled in QFN32 5 x 5 specifically designed to provide the 13 / 18 V power supply and the 22 kHz tone signalling to the LNB down-converter in the antenna dish or to the multi-switch box. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with simple design and I²C standard interfacing.

Features:

- Complete interface between LNB and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.5 A)
- Selectable output current limit by external resistor
- Compliant with main satellite receivers output voltage specification
- Auxiliary modulation input (EXTM pin) facilitates DiSEqC™ 1.X encoding
- Accurate built-in 22 kHz tone generator suits widely accepted standards
- Low-drop post regulator and high efficiency step-up PWM with integrated power NMOS allow low power losses
- Overload and over-temperature internal protections with I²C diagnostic bits
- LNB short circuit dynamic protection
- +/- 4 kV ESD tolerant on output power pins

Block Diagram:



13. Advanced DVB-S/S2 Demodulator M88DS3002 (U3)

Description:

The M88DS3002 is an advanced single-chip demodulator for digital satellite television broadcasting. It is fully compliant with the DVB-S/S2 standard and can support QPSK, 8PSK, 16APSK and 32APSK demodulation schemes. The chip provides a fast, easy-to-apply and cost-effective front-end solution for digital satellite receiver.

The M88DS3002 accepts baseband differential or singleended I and Q signals from a tuner, then digitizes, demodulates and decodes the signals, and finally outputs an MPEG transport stream.

The M88DS3002 supports symbol rate from 1 Msps up to 45 Msps, and code rate from 1/4 to 9/10. Its features cover blind scan, fade detection, timing and carrier recovery, performance monitoring, co-channel interference cancellation, command interface, and DiSEqC™ 2.X interface, etc. The device is controlled via a 2-wire serial bus. The M88DS3002 works properly with 1.25 V and 3.3 V voltage supplies. Typically, the power consumption is around 390 mW. The chip is available in a 64-pin QFN package and is RoHS compliant.

Features:

• Multi-standard demodulation

- ✓ Compliant with DVB-S/S2 specification
- ✓ QPSK, 8PSK, 16APSK and 32APSK demodulation schemes
- ✓ Maximum channel bit rate is 130 Mbps
- ✓ Maximum symbol rates are: 45 Msps for QPSK and 8PSK; 36 Msps for 16APSK and 28 Msps for 32APSK

- **DSP features**

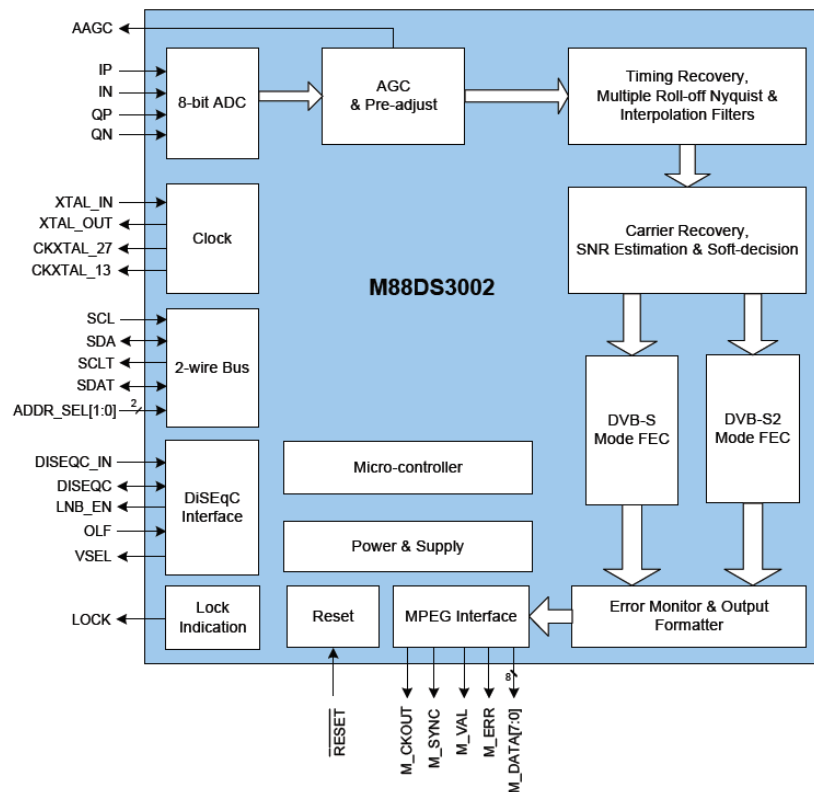
- ✓ Symbol rate sweeping
- ✓ I/Q impairment cancellation
- ✓ Automatic spectrum inversion
- ✓ Adaptive equalizer for RF reflection removal
- ✓ Roll-off factor automatic identification
- ✓ Blind scan for programming search
- ✓ High performance on-chip micro-controller
- ✓ Multi-error monitor
- ✓ Accurate SNR estimation
- ✓ Multi-lock indicators
- ✓ Clipping rate reporter
- ✓ DC removal
- ✓ Automatic frequency correction (AFC)
- ✓ Fast timing loop acquisition
- ✓ Robust frame synchronization scheme
- ✓ Phase noise indicator
- ✓ Fast system recovery from fading or other abnormal conditions
- ✓ Co-channel interference cancellation
- ✓ Constellation monitor

- **Interface**

- ✓ DVB-S/S2 common, parallel and serial MPEG output interface compliant
- ✓ 2-wire serial bus to configure the device
- ✓ 2-wire bus repeater for tuner configuration
- ✓ DiSEqC™ 2.X compliant interface
- ✓ General purpose output (GPO)
- ✓ Dedicated reference clocks (13.5MHz / 27MHz) generation

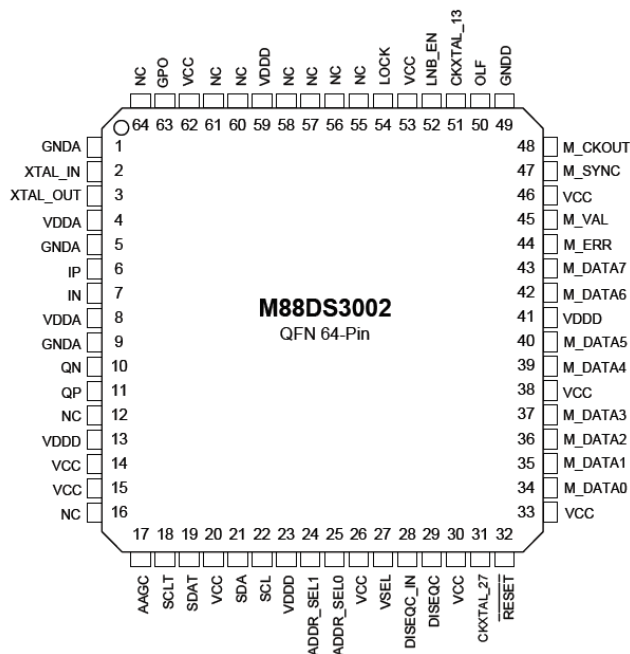
- **System**

- ✓ On-chip 8-bit ADC
- ✓ On-chip PLL for master clock from a 27 MHz external clock or quartz crystal
- ✓ Sleep mode supported



---Block Diagram of M88DS3002---

Pin Assignment:



14. LM1117(U175, U180, U181)

14.1. General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within $\pm 1\%$. The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10 μ F tantalum capacitor is required at the output to improve the transient response and stability.

14.2. Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
- LM1117 0°C to 125°C
- LM1117I -40°C to 125°C

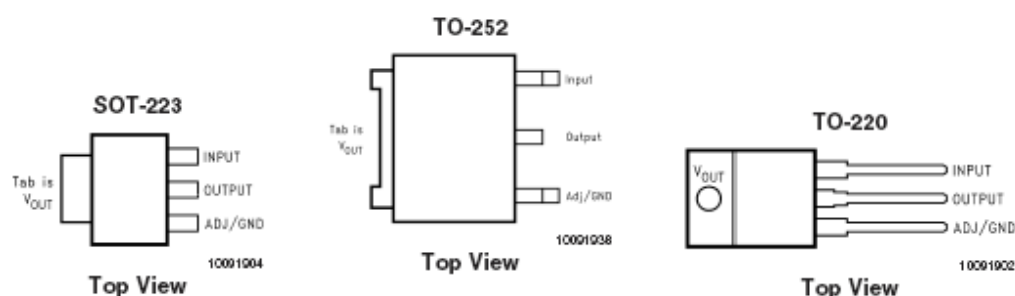
14.3. Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators 15
- 32" TFT TV Service Manual 10/01/2005
- Battery Charger
- Battery Powered Instrumentation

14.4. Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
DC Input Voltage	V_{IN}		7	V
Lead Temperature (Soldering, 5 Seconds)	T_{SOL}		260	°C
Storage Temperature Range	T_{STG}	-65	150	°C
Operating Junction Temperature Range	T_{OPR}	0	125	°C

14.5. Pinning



15. MP2012 (U176)

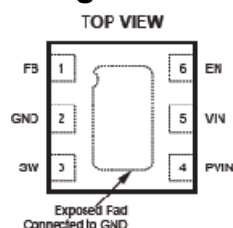
15.1. General Description

The MP2012 is a fully integrated, internally compensated 1.2MHz fixed frequency PWM step-down converter. It is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) Battery, with an input range from 2.7V to 6V. The MP2012 can provide up to 1.5A of load current with output voltage as low as 0.8V. It can also operate at 100% duty cycle for low dropout applications. With peak current mode control and internal compensation, the MP2012 is stable with ceramic capacitors and small inductors. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

15.2. Features

- 2.7-6V Input Operation Range
- Output Adjustable from 0.8V to V_{IN}
- 1 μ A Max Shutdown Current.
- Up to 95% Efficiency
- 100% Duty Cycle for Low Dropout
- Applications
- 1.2MHz Fixed Switching Frequency
- Stable with Low ESR Output Ceramic Capacitors
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Short Circuit Protection
- Available in 6-pin 3x3mm QFN

15.3. Pinning



Pin #	Name	Description
1	FB	Feedback input. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage.
2	GND, Exposed Pad	Ground pin. Connect exposed pad to ground plane for proper thermal performance.
3	SW	Switch node to the inductor.
4	PVIN	Input supply pin for power FET.
5	VIN	Input Supply pin for controller. Put small decoupling ceramic near this pin.
6	EN	Enable input, “High” enables MP2012. EN is pulled to GND with 1Meg internal resistor.

16. RTA8283A (U23, U173)

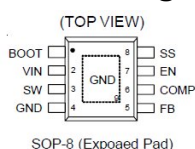
16.1. General Description

The RT8283A is a high-efficiency, monolithic synchronous step-down DC/DC converter that can deliver up to 3A output current from a 4.5V to 23V input supply. The RT8283A's current mode architecture and external compensation allow the transient response to be optimized over a wide range of loads and output capacitors. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RT8283A also provides output under voltage protection and thermal shutdown protection. The low current (<3 μ A) shutdown mode provides output disconnect, enabling easy power management in battery-powered systems. The RT8283A is available in a SOP-8 package.

16.2. Features

- $\pm 1.5\%$ High Accuracy Feedback Voltage
- Integrated N-MOSFET Switches
- Current Mode Control
- Fixed Frequency Operation : 340kHz
- Output Adjustable from 0.8V to 20V
- Up to 95% Efficiency
- Thermal Shutdown Protection

16.3. Pinning



Pin No.	Pin Name	Description
1	BOOT	Bootstrap for high-side gate driver. Connect a 0.1 μ F or greater ceramic capacitor from BOOT to SW pins.
2	VIN	Input Supply 4.5V to 23V. Must bypass with a suitably large ceramic capacitor.
3	SW	Phase Node--Connect to external L-C filter..
4, 9 (Exposed Pad)	GND	Ground.
5	FB	Feedback Input pin is connected to the converter output. It is used to set the output of the converter to regulate to the desired value via an internal res divider. For an adjustable output, an external res divider is connected to this pin.
6	COMP	Compensation Node. COMP is used to compensate the regulation Control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required.
7	EN	Enable Input Pin. Logic high enables the converter; a logic low forces the RT8253A into shutdown mode. Attach this pin to VIN with a 100k Ω pull up resistor for automatic startup.
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1 μ F capacitor sets the soft-start period to 13.5ms.

17. MP1583 (U174)

17.1. General Description

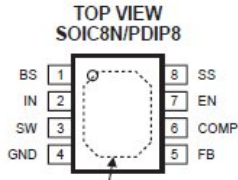
The MP1583 is a step-down regulator with a built-in internal Power MOSFET. It achieves 3A of continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. An adjustable soft-start reduces the stress on the input source at start-up. The MP1583 requires a minimum number of external components, providing a compact solution.

17.2. Features

- 3A Output Current
- Programmable Soft-Start
- 100m Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20 μ A Shutdown Mode
- Fixed 385KHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection

- Wide 4.75V to 23V Operating Input Range
- Output Adjustable from 1.22V to 21V
- Under-Voltage Lockout

17.3. Pinning



Pin No.	Pin Name	Description
1	BOOT	High-Side Gate Drive Bootstrap Input. BS supplies the drive for the high-side N-Channel MOSFET switch.
2	IN	Power Input. Drive IN with a 4.75V to 23V power source.
3	SW	Power Switching Out is the switching node that supplies power to the output
4	GND	Ground.
5	FB	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider from the output voltage. FB threshold is 1.222V.
6	COMP	Compensation Node is used to compensate the regulation control loop.
7	EN	Enable/UVLO. A voltage greater than 2.71V enables operation. For complete low current shutdown the EN pin voltage needs to be at less than 900mV. When the voltage on EN exceeds 1.2V, the internal regulator will be enabled and the soft-start capacitor will begin to charge. The MP1583 will start switching after the EN pin voltage reaches 2.71V.
8	SS	Soft-Start Control Input. SS controls the soft-start period.

18. FDC642

18.1. General Description

This P-Channel 2.5V specified MOSFET is produced using Fairchild's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

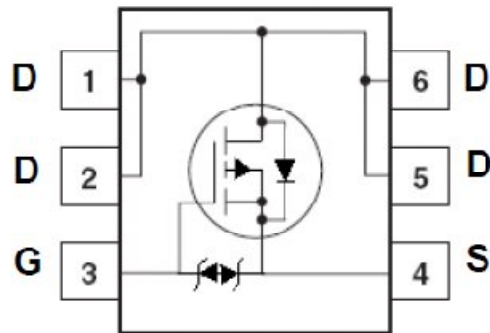
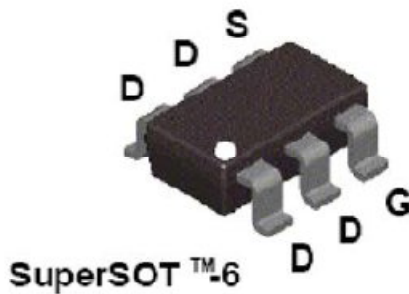
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the larger packages are impractical.

18.2. Features

- Max $r_{DS(on)}$ = 65 mΩ at $V_{GS} = -4.5$ V, $I_D = -4.0$ A
- Max $r_{DS(on)}$ = 100 mΩ at $V_{GS} = -2.5$ V, $I_D = -3.2$ A
- Fast switching speed
- Low gate charge (11nC typical)

- High performance trench technology for extremely low $r_{DS(on)}$
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1 mm thick)
- Termination is Lead-free and RoHS Compliant

18.3. Pinning



19. FDC604P

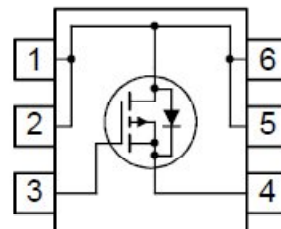
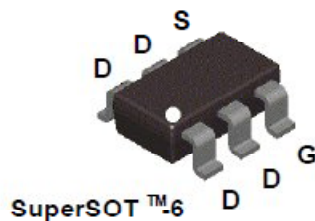
19.1. General Description

This P-Channel 1.8V specified MOSFET uses Fairchild's low voltage PowerTrench process. It has been optimized for battery power management applications.

19.2. Features

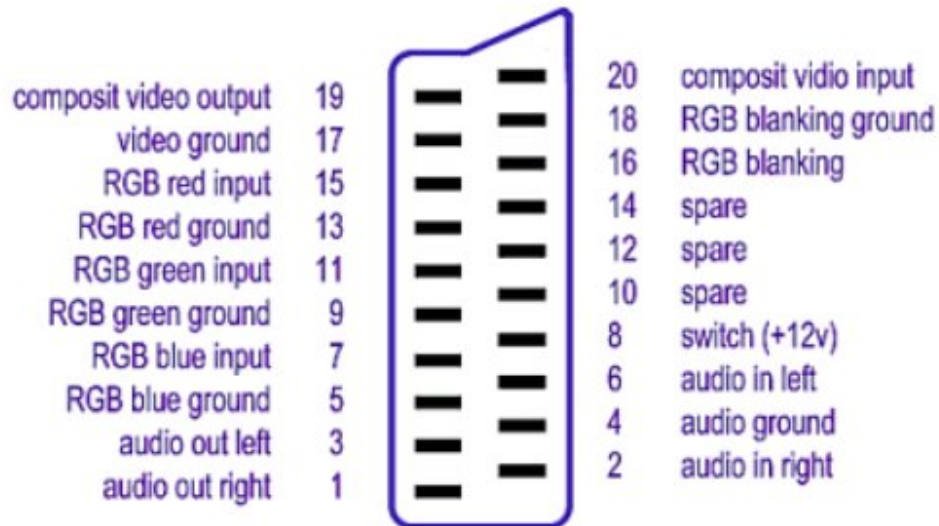
- -5.5 A , -20 V . $R_{DS(ON)} = 33\text{ m}\Omega$ @ $V_{GS} = -4.5\text{ V}$
- $R_{DS(ON)} = 43\text{ m}\Omega$ @ $V_{GS} = -2.5\text{ V}$
- $R_{DS(ON)} = 60\text{ m}\Omega$ @ $V_{GS} = -1.8\text{ V}$
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(ON)}$ (S)

19.3. Pinning

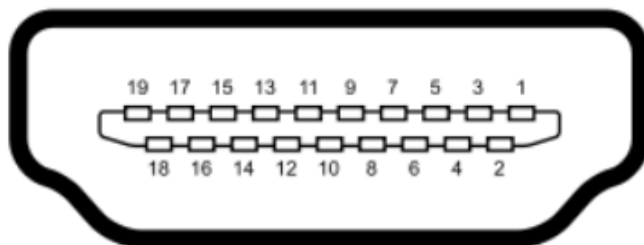


20. CONNECTORS

20.1. SCART (SC1)

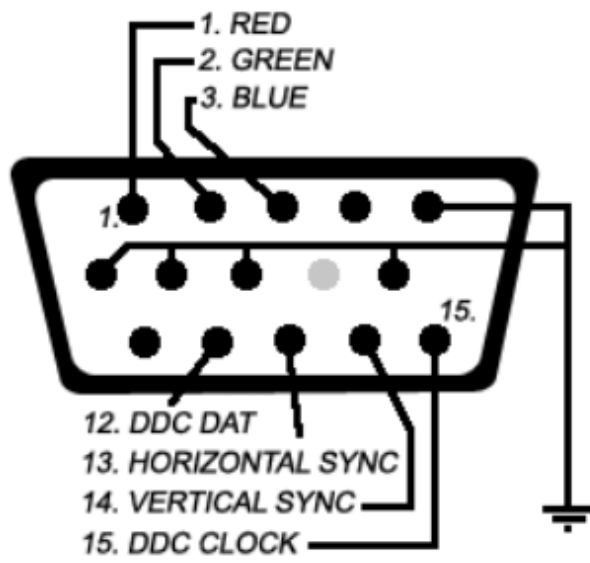


20.2. HDMI (CN707,CN708)



Pin Number	Signal Name	Pin Number	Signal Name
1	TMDS Data 2+	20	SHELL
2	TMDS Data 2 Shield	19	Hot Plug Detect
3	TMDS Data 2-	18	+5V Power
4	TMDS Data 1+	17	Ground
5	TMDS Data 1 Shield	16	DDC Data
6	TMDS Data 1-	15	DDC Clock
7	TMDS Data 0+	14	No Connect
8	TMDS Data 0 Shield	13	CEC
9	TMDS Data 0-	12	TMDS Clock-
10	TMDS Clock+	11	TMDS Clock Shield

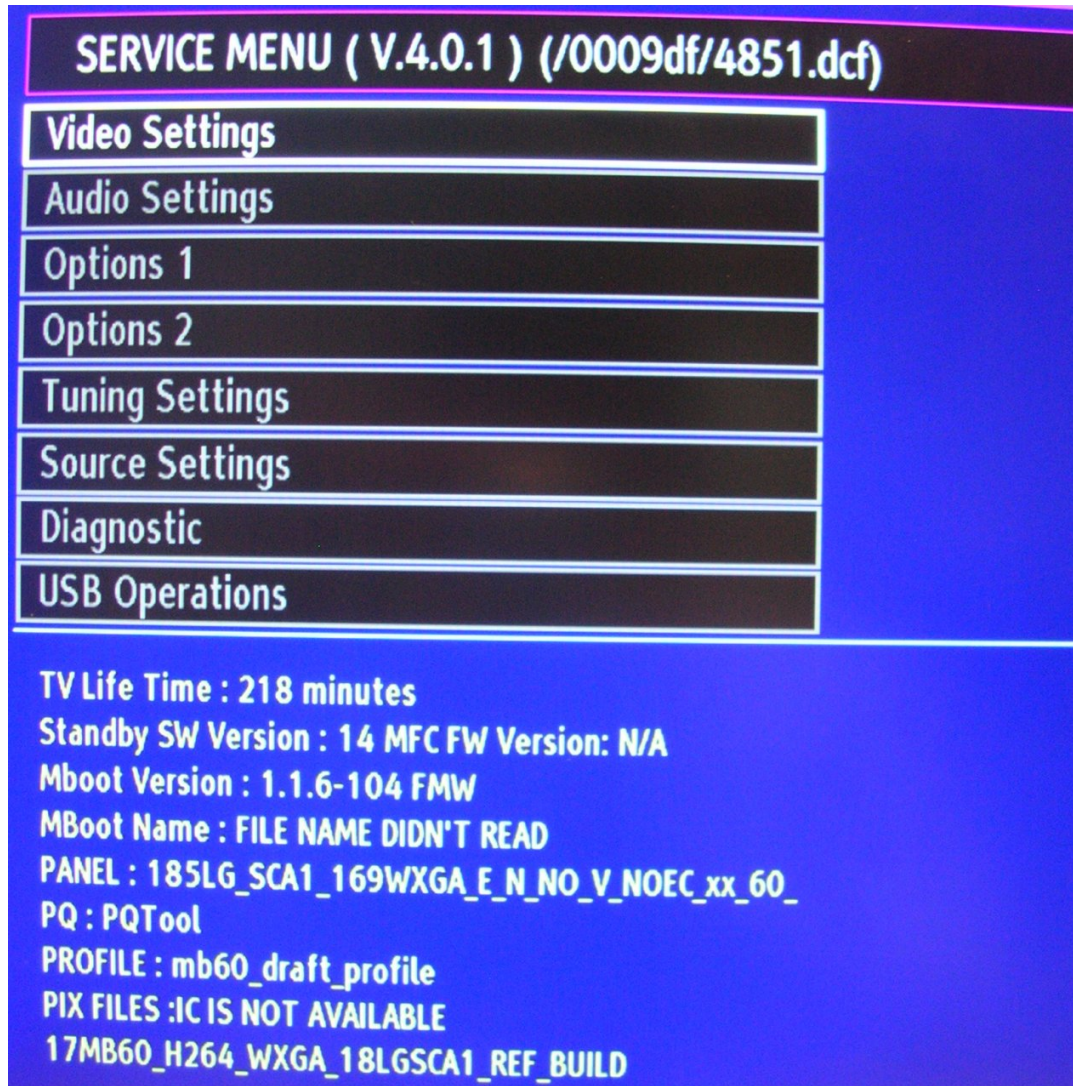
20.3. VGA (CN711)



21. SERVICE MENU SETTINGS

In order to reach service menu, First Press **"MENU"** Then press the remote control code two times, which is **"4725"**.

In first screen following items can be seen:



21.1. Video Settings

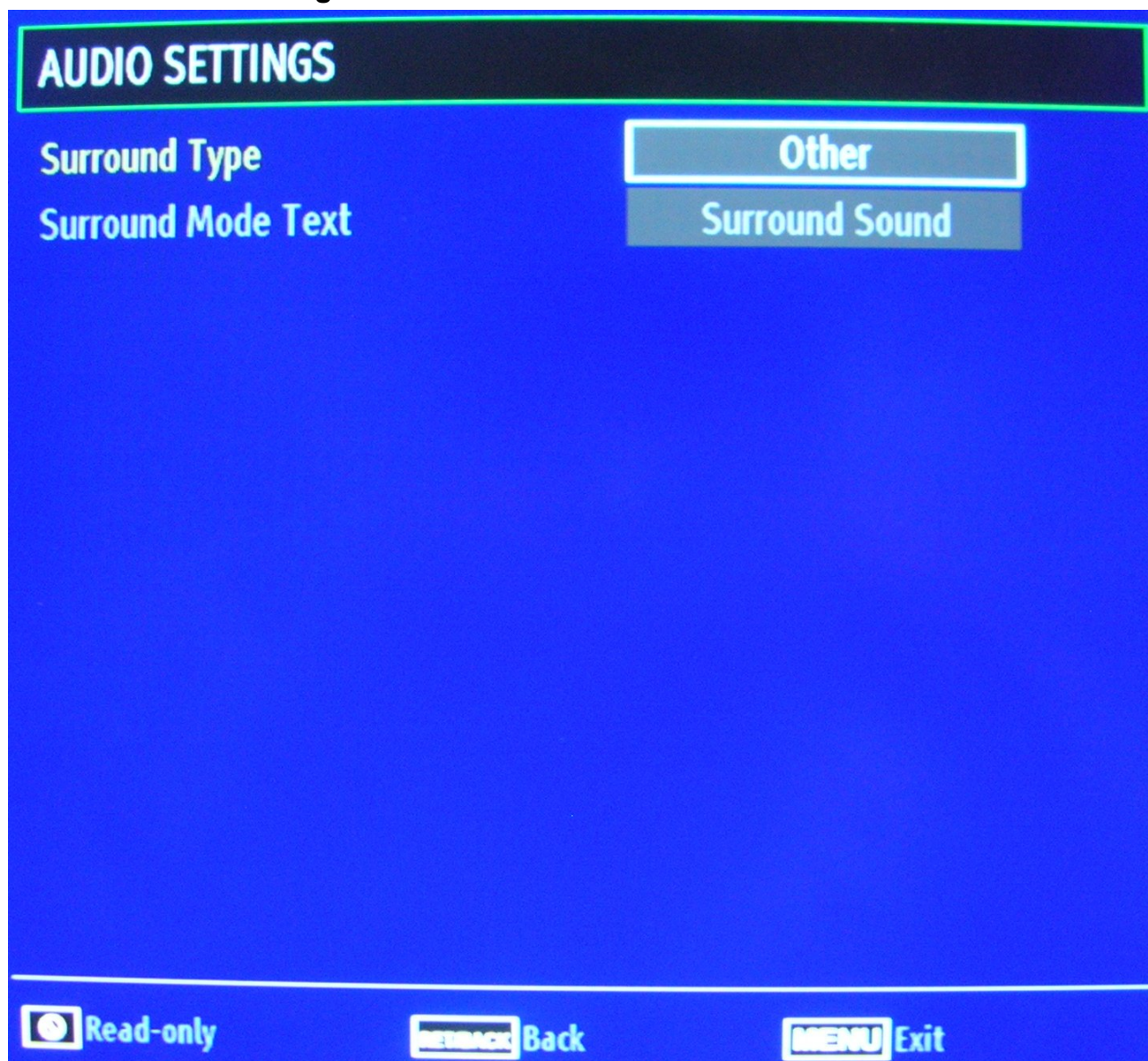
VIDEO SETTINGS		
RF AGC SECAM	<input type="range"/>	3
RF AGC NEIGHBOUR NO IMAGE NO	<input type="range"/>	3
RF AGC NEIGHBOUR NO IMAGE YES	<input type="range"/>	3
RF AGC NEIGHBOUR YES IMAGE NO	<input type="range"/>	6
RF AGC NEIGHBOUR YES IMAGE YES	<input type="range"/>	6
RF AGC TEST	<input type="range"/>	3
ADC Calibration Source	EXT-1	
ADC Calibration R Gain	<input type="range"/>	82
ADC Calibration G Gain	<input type="range"/>	82
ADC Calibration B Gain	<input type="range"/>	81
ADC Calibration R Offset	<input type="range"/>	0
ADC Calibration G Offset	<input type="range"/>	0
ADC Calibration B Offset	<input type="range"/>	0

  Change Value

 Back

 Exit

21.2. Audio Settings



21.3. Options

Options-1

OPTIONS 1	
Auto TV OFF	4 h
Power Up Mode	Last State
BacklightTrick Mode	Yes
Cable Support	No
EPG Type	2
Hotel Mode	Yes
LCN	No
PC Standby	Yes
Stby Search	Yes
Test Tool	Yes
Local Key	KeyPad
Volume Level	15

 Read-only

 Back

 Exit

Options-2

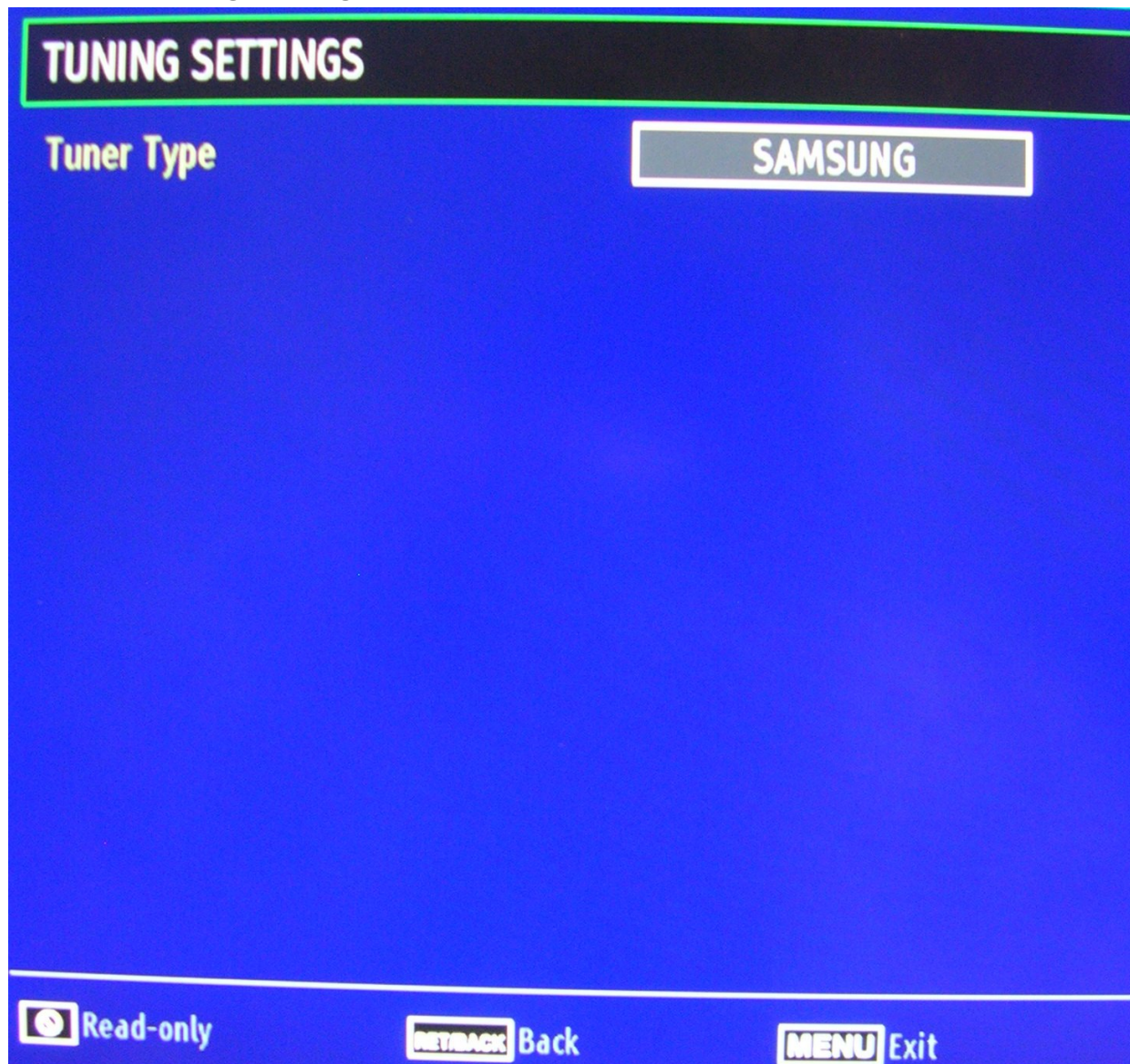
OPTIONS 2	
Aps Sorting	Enabled
Dynamic Menu	Disabled
EPG Menus	Enabled
Transparent Text	Enabled
HDMI Number	2
HDMI Auto Switch	Enabled
Rc Type	Rc3900
DCF ID	4851.dcf
Touchpad Sw Version	0

 Read-only

 Back

 Exit

21.4. Tuning Settings



21.5. Source Settings

SOURCE SETTINGS	
SCART	Yes
SCART2	No
SCART2-S	No
SIDE AV	Yes
SCART-S	Yes
HDMI1	Yes
HDMI2	Yes
HDMI3	No
HDMI4	No
YPbPr	Yes
VGA/PC	Yes
BluRay	No

 Read-only

 Back

 Exit

21.6. Diagnostic

DIAGNOSTIC	
Remote control test	OK
UHF test	OK
VHF test	OK
Factory reset	OK
Tuner I2C	OK
IF I2C	OK
HDMI I2C	NOK
Ethernet	NOK
EDID status	NOK
HDCP status	NOK
DDR Settings	NOK
CI+ credentials	NOK
MAC address	ff:ff:ff:ff:ff:ff

Press any key to test

RETRYBACK Back **MENU** Exit

21.7. USB Operations

USB operations option can not be used directly. It can be used for updating panel tool, hw congiguration etc.

22. SOFTWARE UPDATE

In MB62 project there is only one software. From following steps software update procedure can be seen:

1. MB62_en.bin, mboot.bin and usb_auto_update_T4.txt documents should copy directly inside of a flash memory(not in a folder).
2. Put flash memory to the tv when tv is powered off.
3. Power on the and wait when the tv is opened.
4. If First Time Installation screen comes, it means software update procedure is successful.

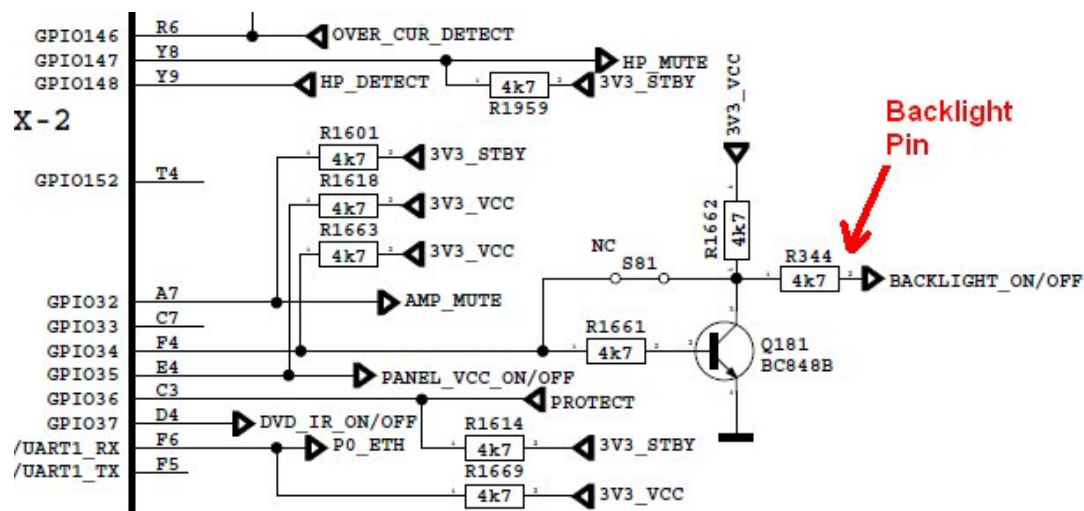
23. TROUBLESHOOTING

23.1. No Backlight Problem

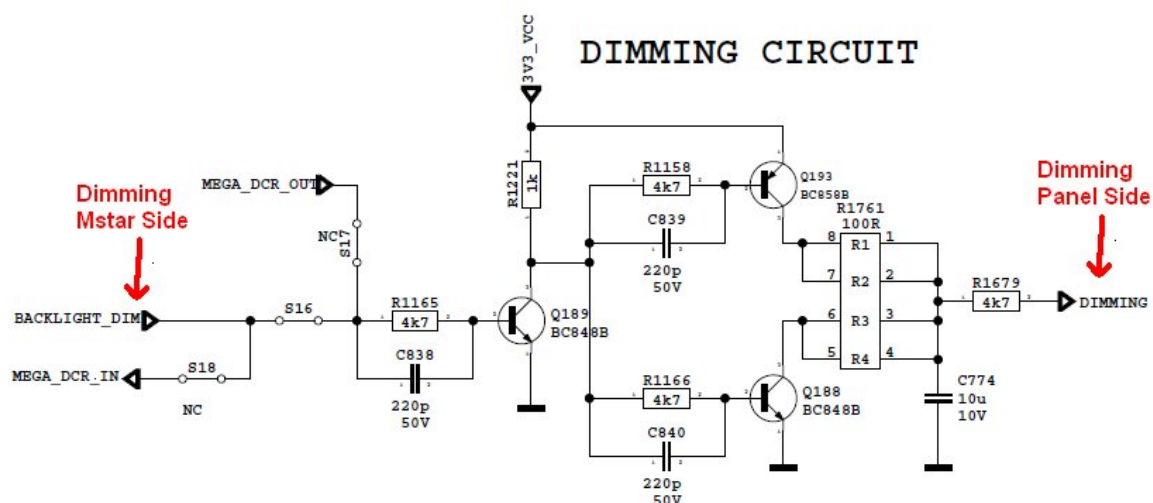
Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply, stby on/off pin

Backlight pin should be high in open position. If it is low, please check Q181 and panel cables.

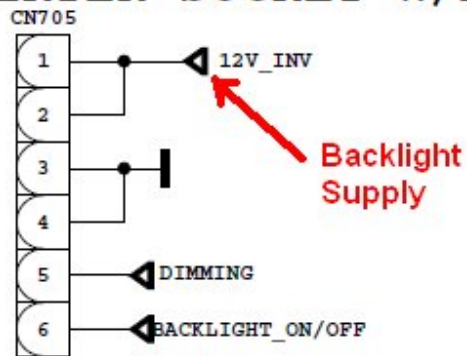


Dimming pin should be high or square wave in open position. If it is low, please check S16 for Mstar side and panel or power cables, connectors.

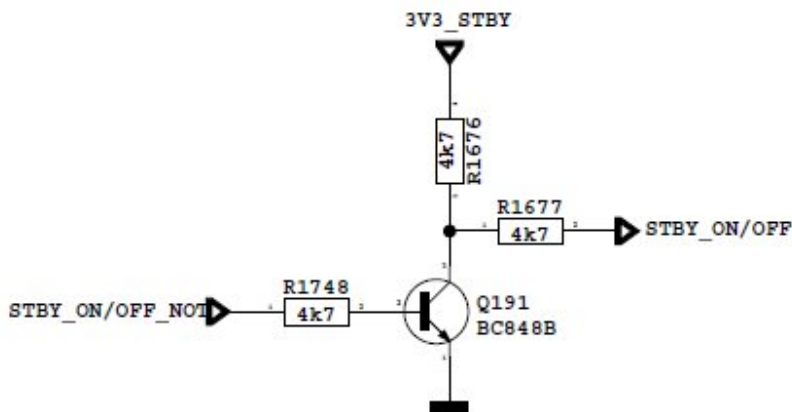


Backlight power supply should be in panel specs. Please check CN705 for MB62, related connectors for power supply cards.

INVERTER SOCKET W/ADAPTER



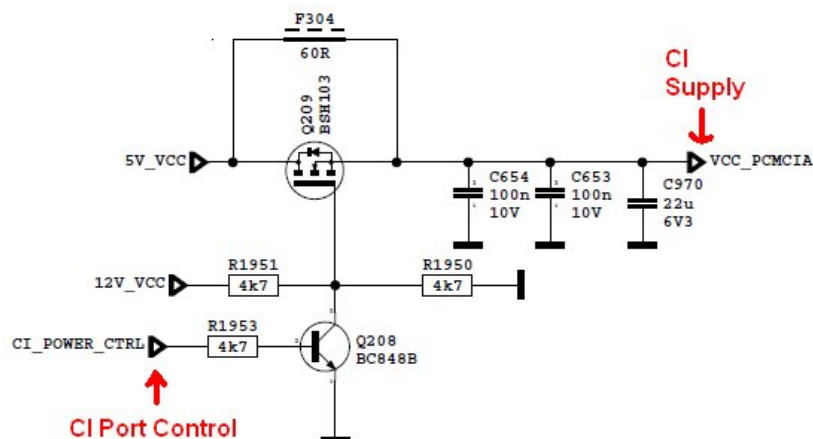
STBY_ON/OFF should be low for standby on condition, please check R1677.



23.2. CI Module Problem

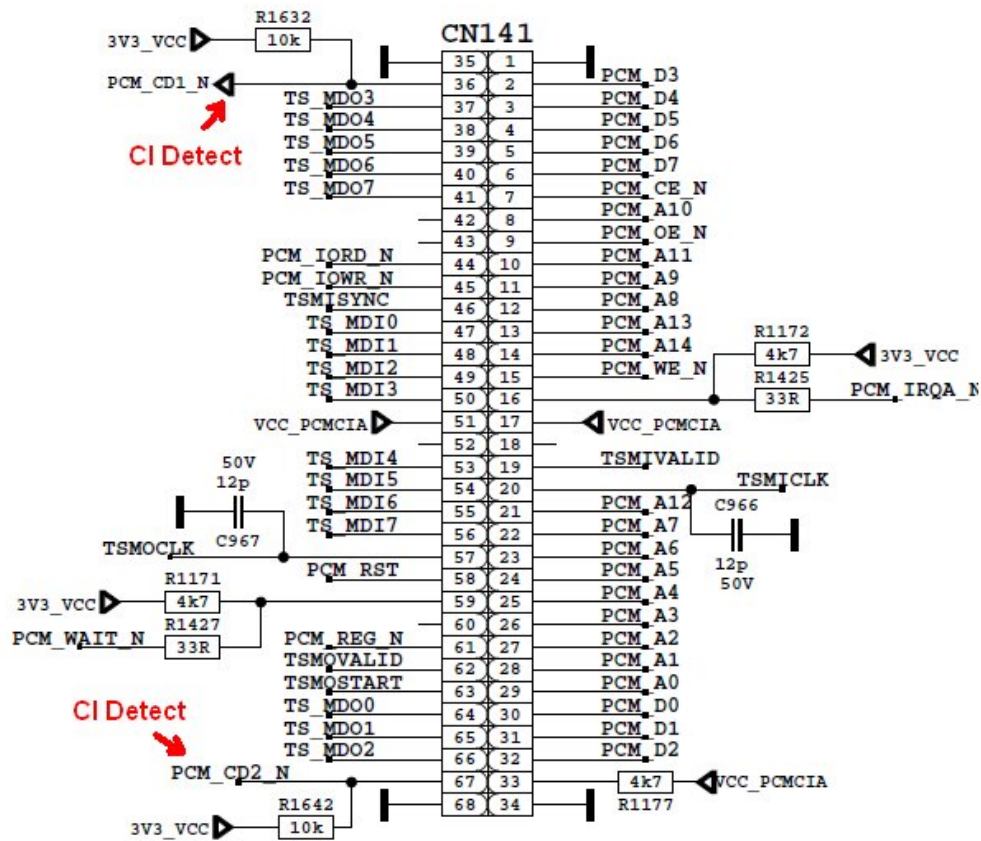
Problem: CI is not working when CI module inserted.

Possible causes: Supply, supply control pin, detect pins, mechanical positions of pins
CI supply should be 5V when CI module inserted. If it is not 5V please check
CI_POWER_CTRL, this pin should be low.



Please check mechanical positions of CI module.

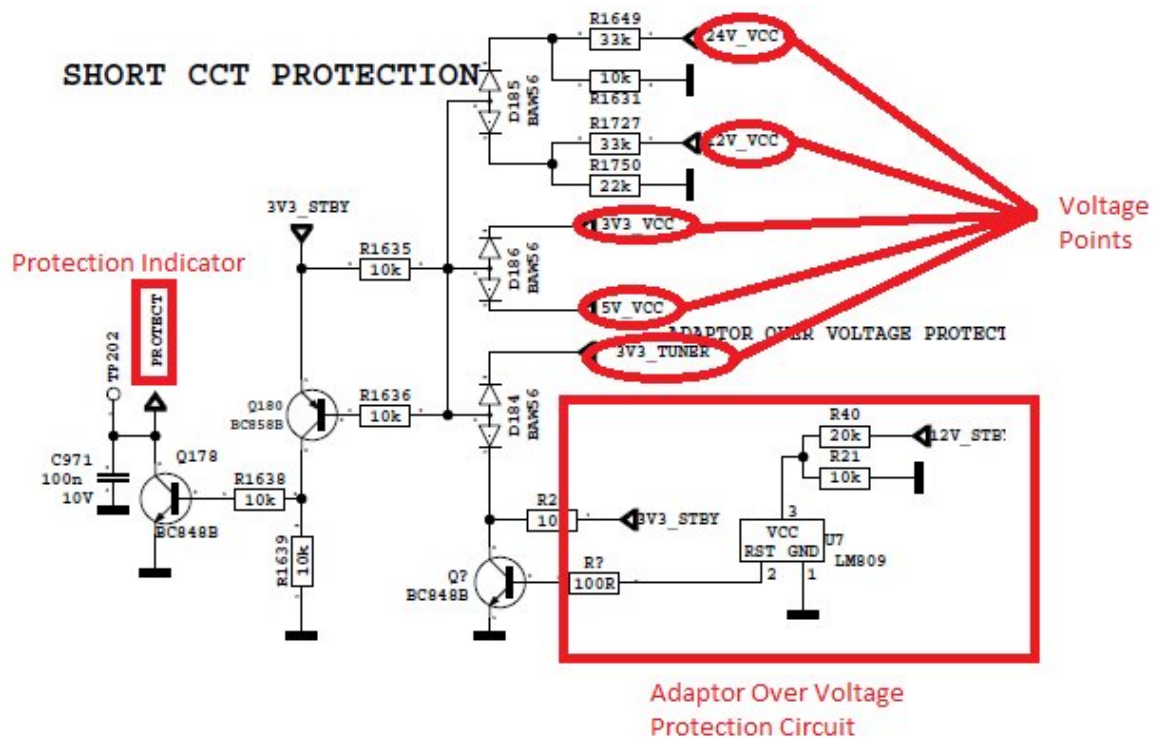
Detect ports should be low. If it is not low please check CI connector pins, CI module pins and 3V3_VCC on MB62.



23.3. Led Blinking Problem

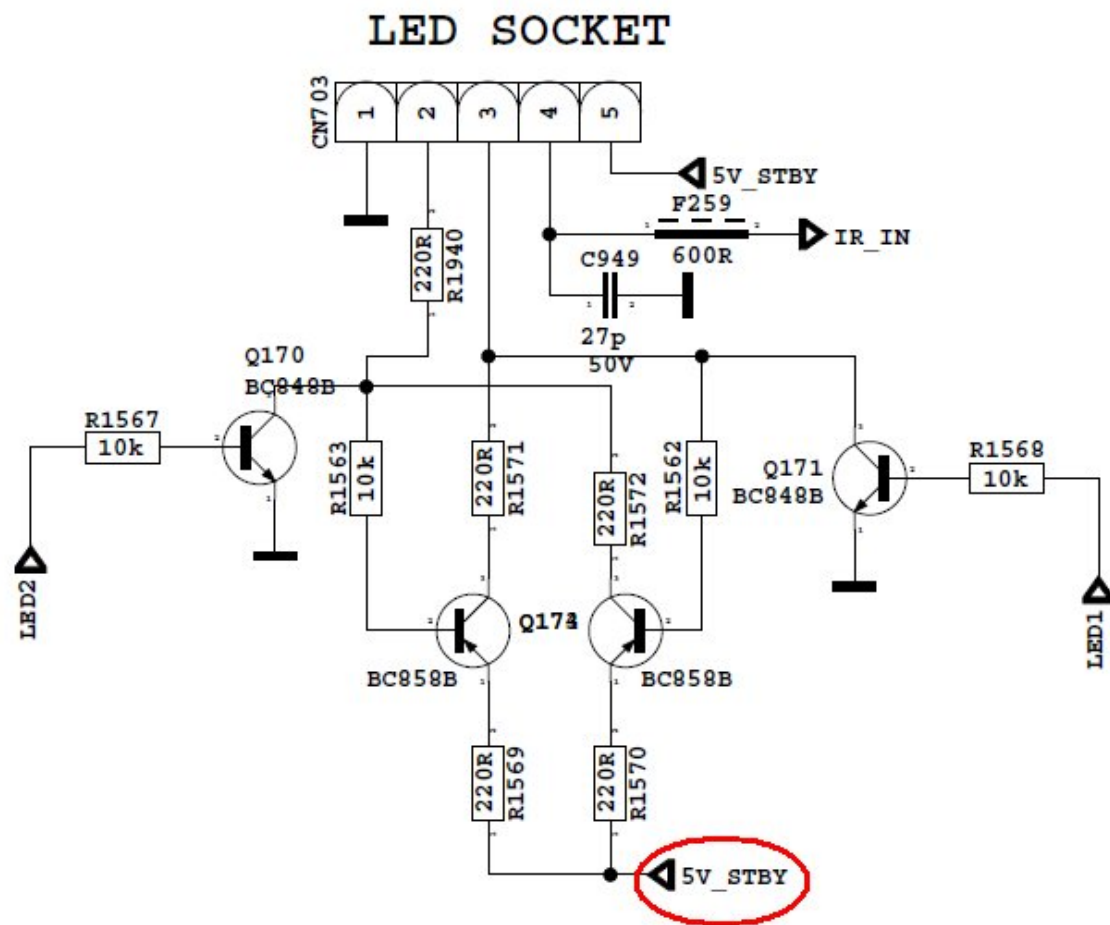
Problem: LED blinking, no other operation

This problem indicates a short on Vcc voltages. Protect pin should be logic high while normal operation. When there is a short circuit protect pin will be logic low. If you detect logic low on protect pin, unplug the TV set and control voltage points with a multimeter to find the shorted voltage to ground.



23.4. IR Problem

Problem: LED or IR not working
Check LED card supply on MB62 chasis.

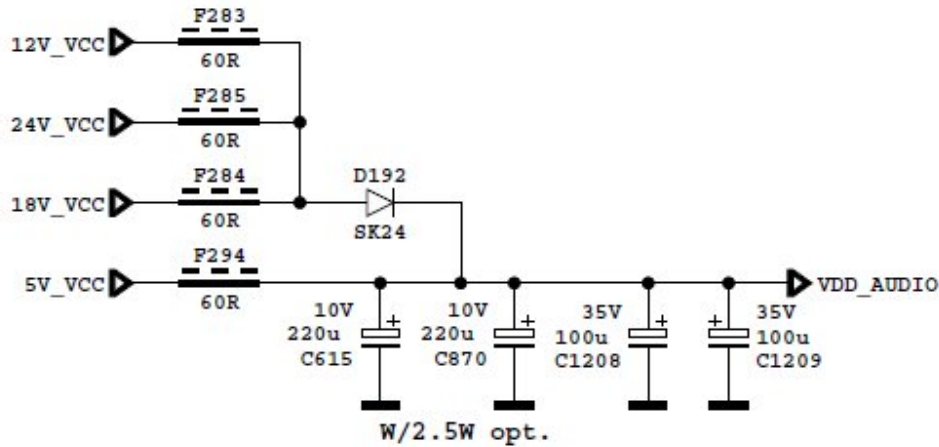


23.5. Keypad Touchpad Problems

Problem: Keypad or Touchpad is not working

Check keypad supply and KEYBOARD pin on MB62.

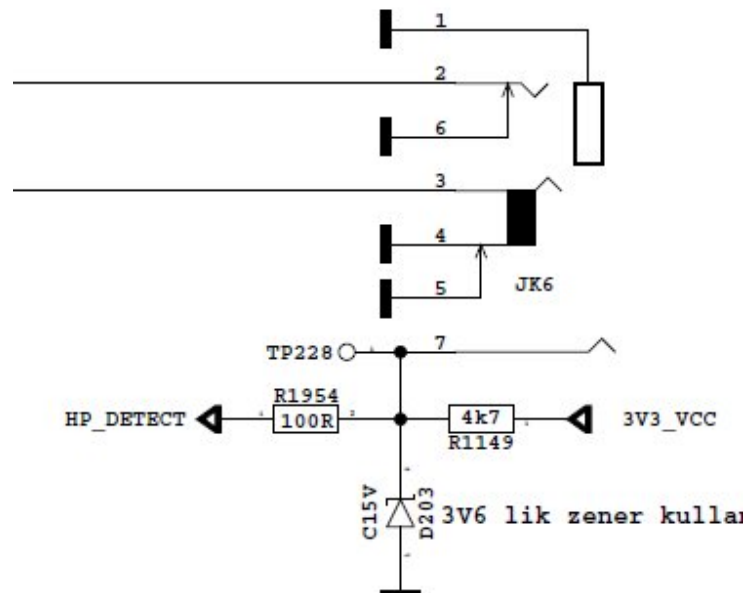
Check supply voltages of VDD_AUDIO, 5V_VCC and 3V3_VCC with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.



23.8. No Sound Problem at Headphone

Problem: No audio at headphone output.

Check HP detect pin, when headphone is. Check 5V_VCC and 3V3_VCC with a voltage-meter.



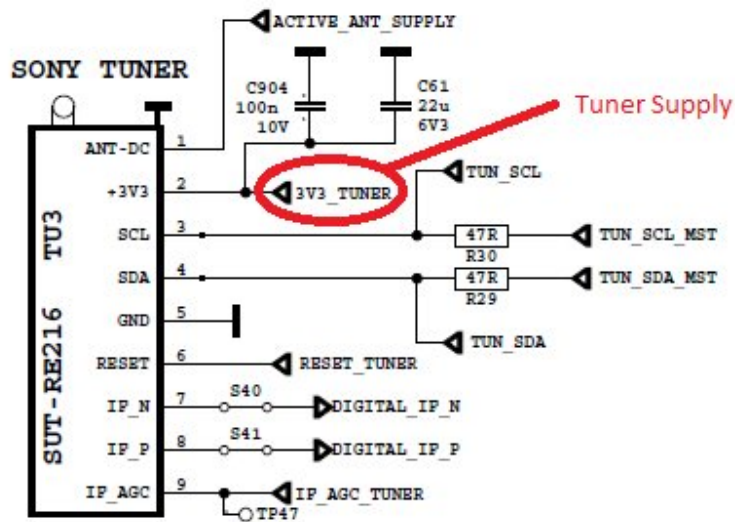
23.9. Standby On/Off Problem

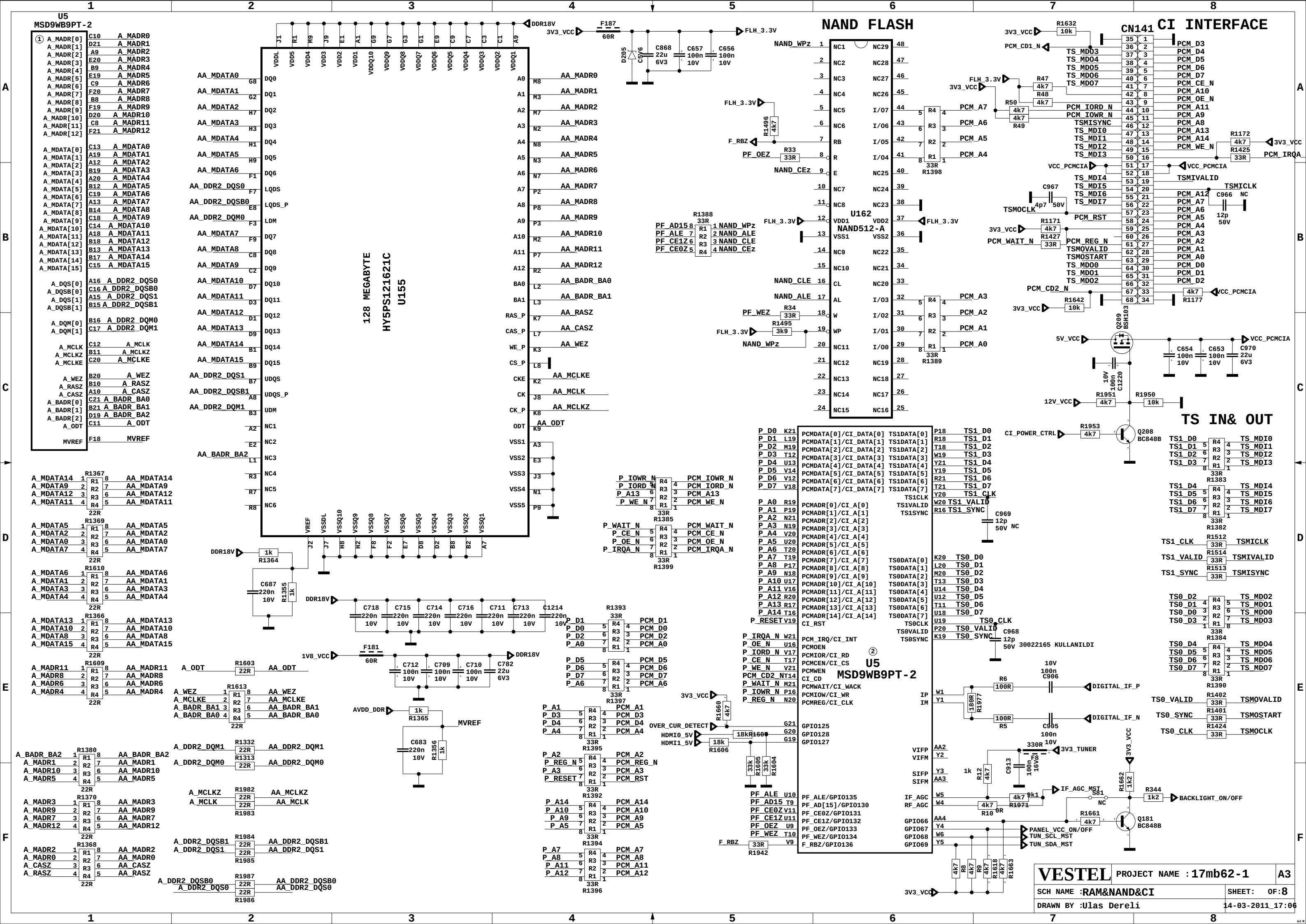
Problem:
Device cannot boot, TV hangs in standby mode.

23.10. No Signal Problem

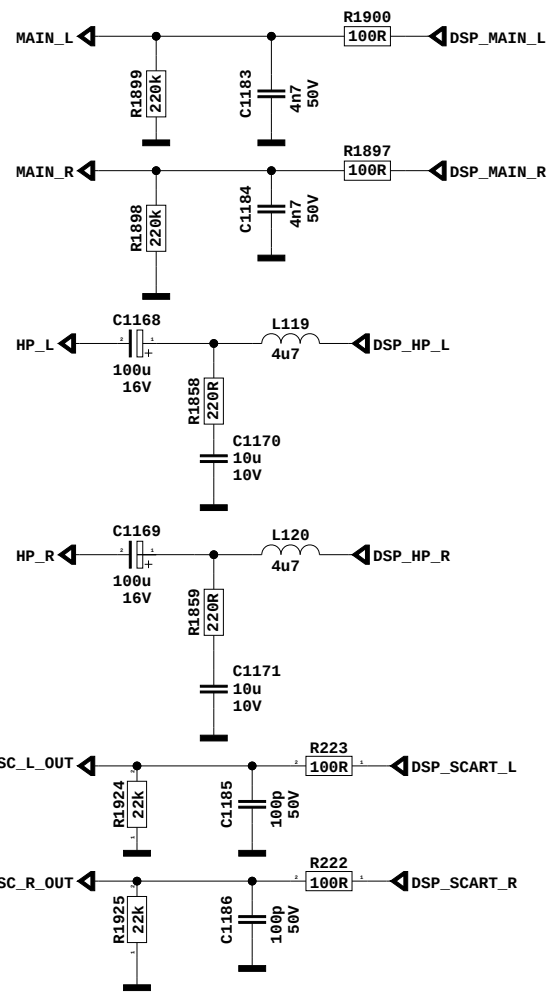
Problem: No signal in TV mode.

Check tuner supply voltage; 3V3_TUN. Check tuner options are correctly set in Service menu. Check AGC voltage at IF_AGC pin of tuner.

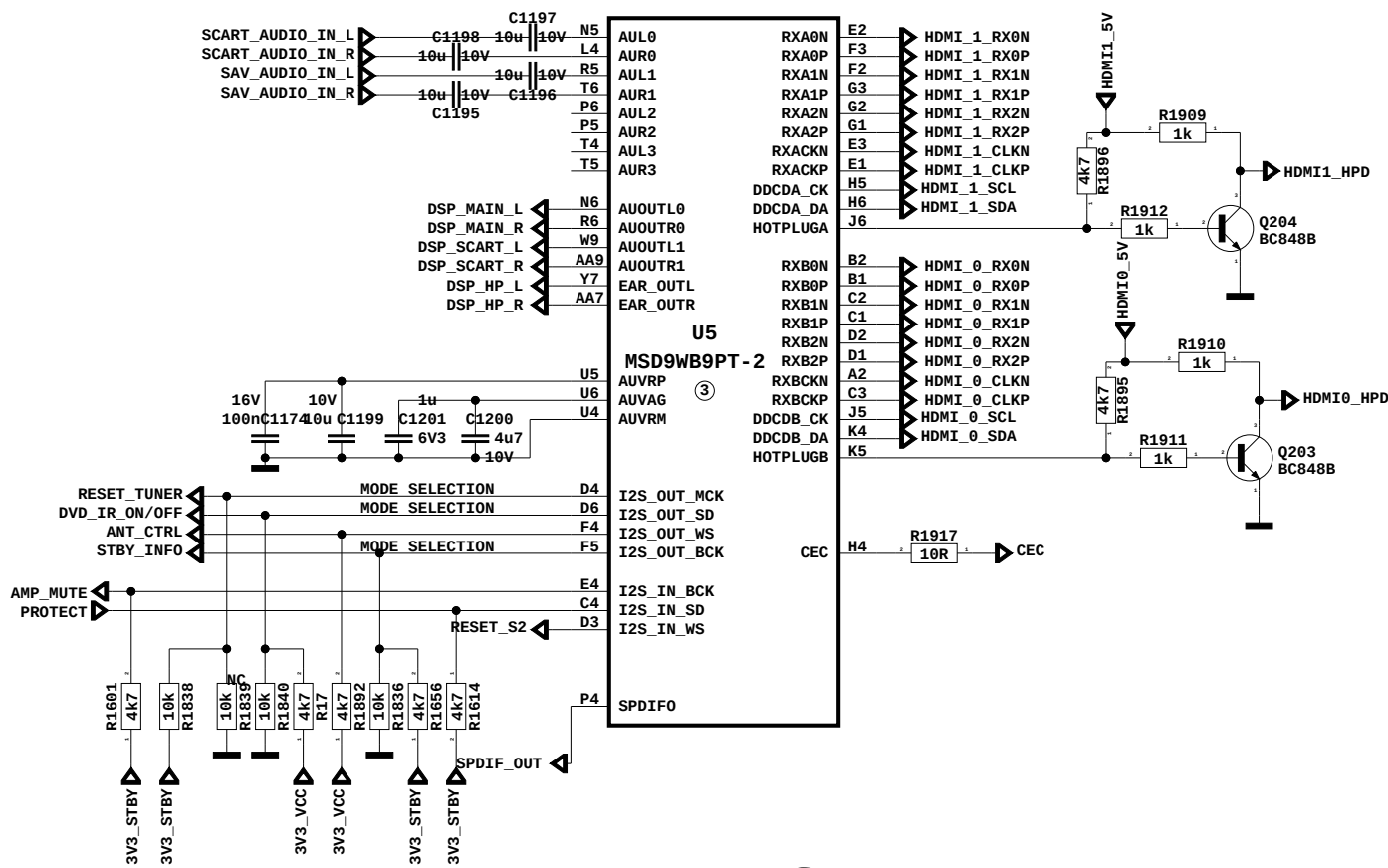
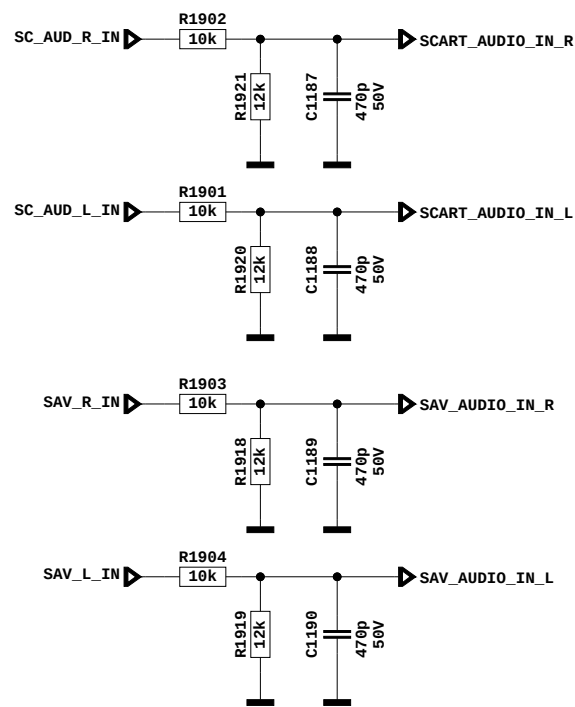




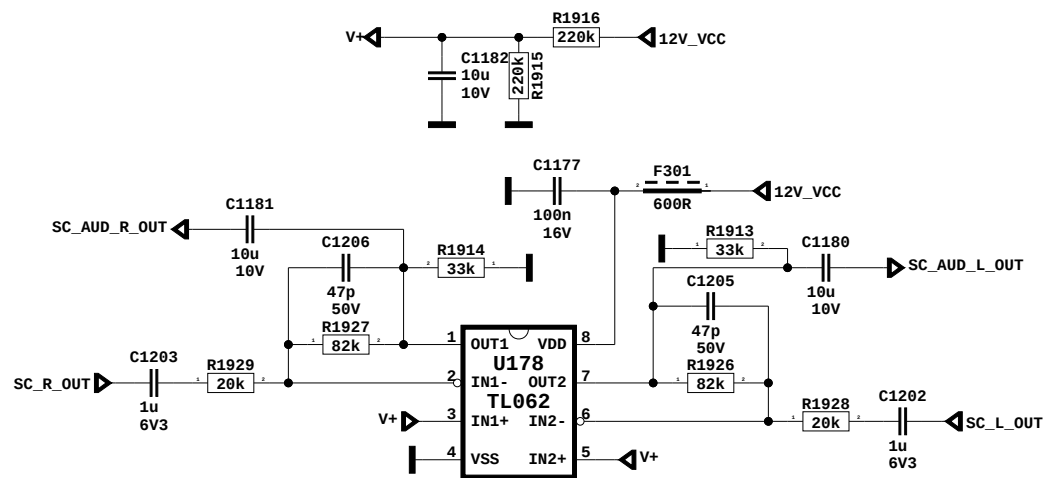
AUDIO OUTPUTS



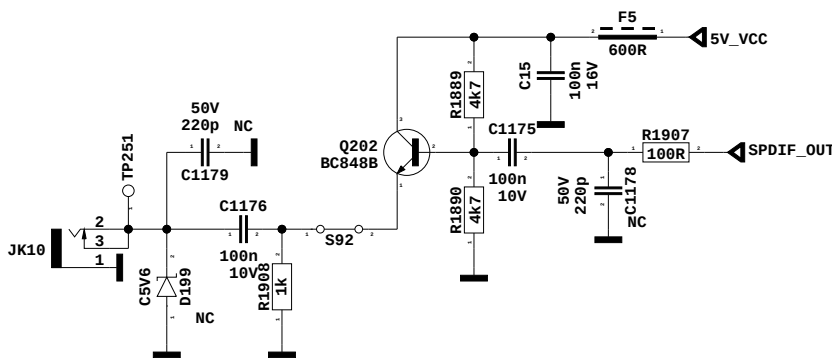
AUDIO INPUTS



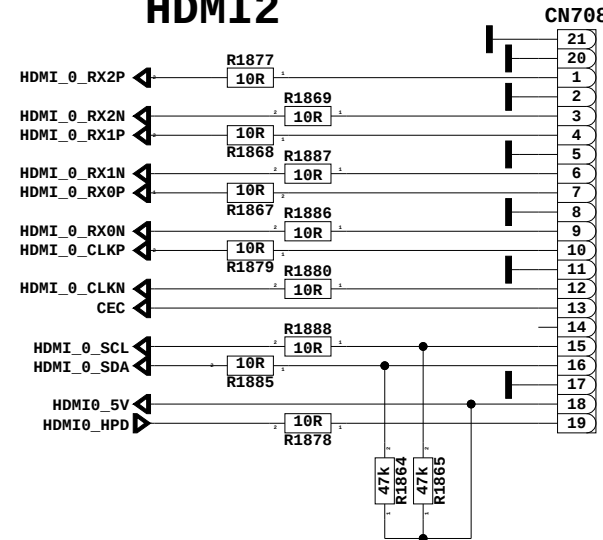
PRE-AMP for SCART AUDIO



COAX SPDIF OUT

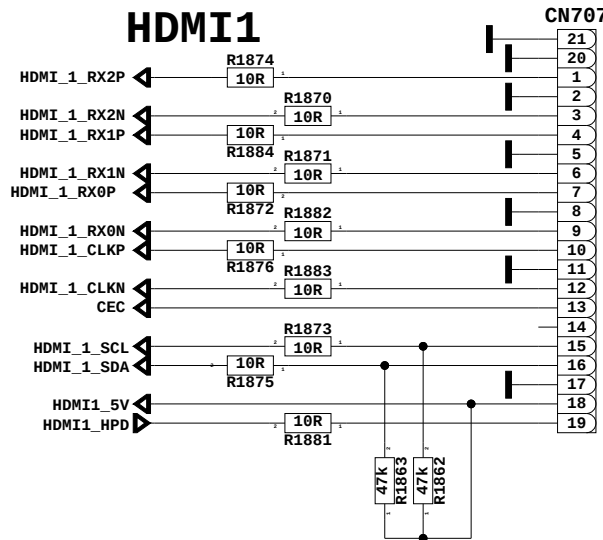


HDMI2

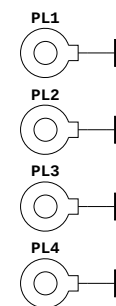


OPTIONAL

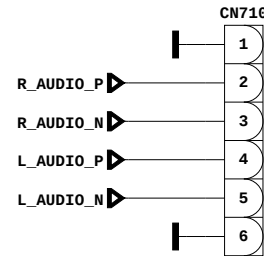
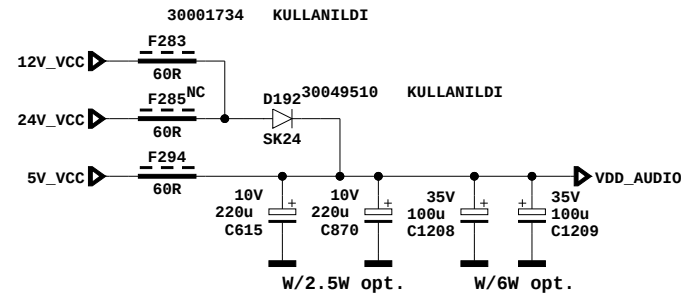
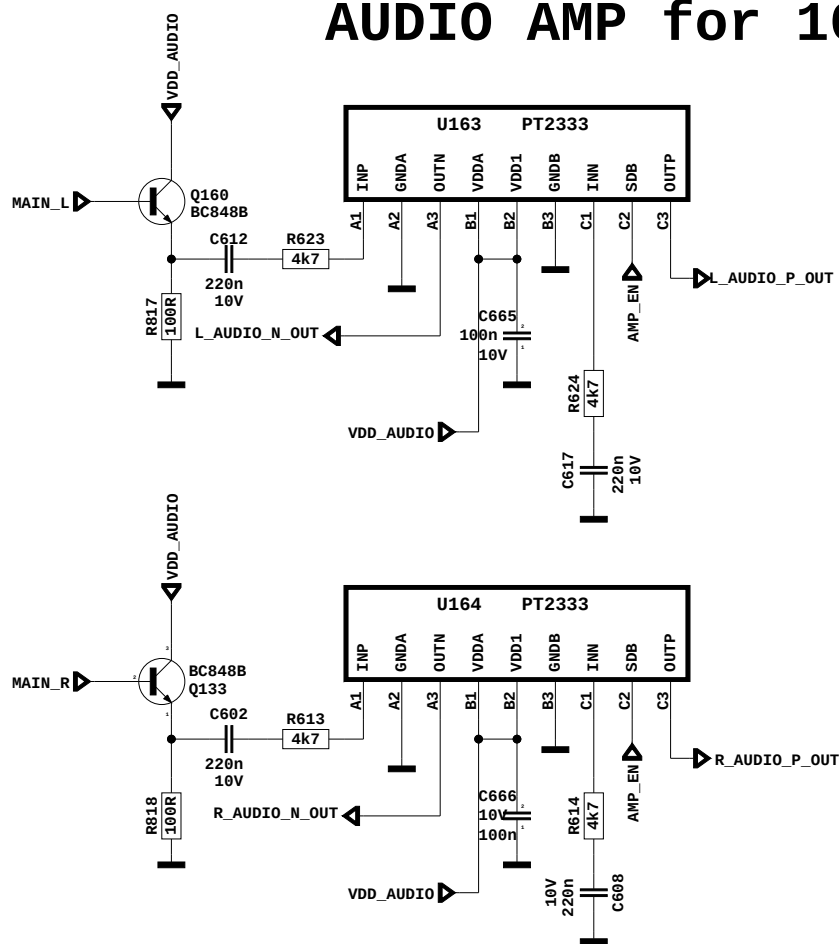
HDMI1



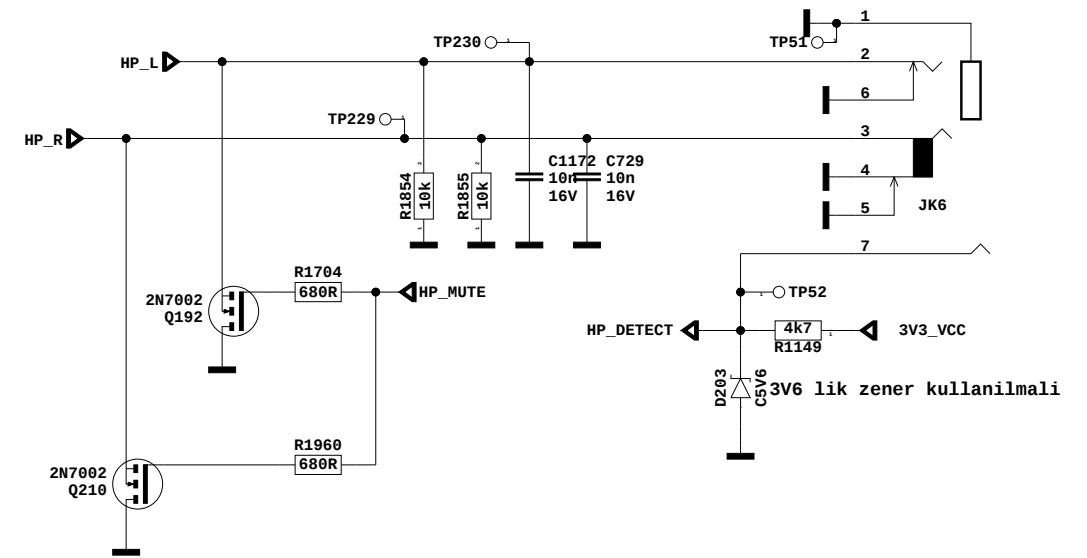
COMMON



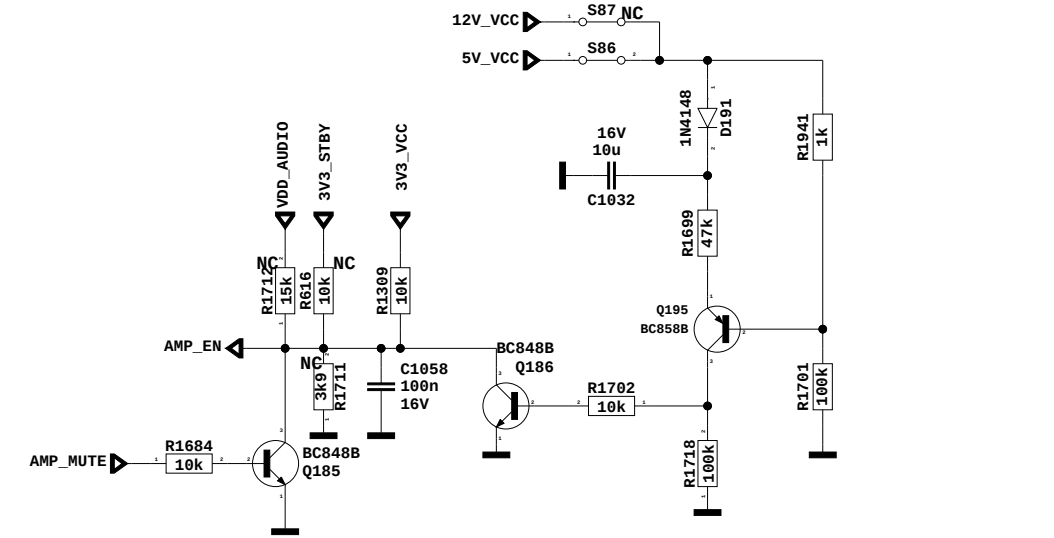
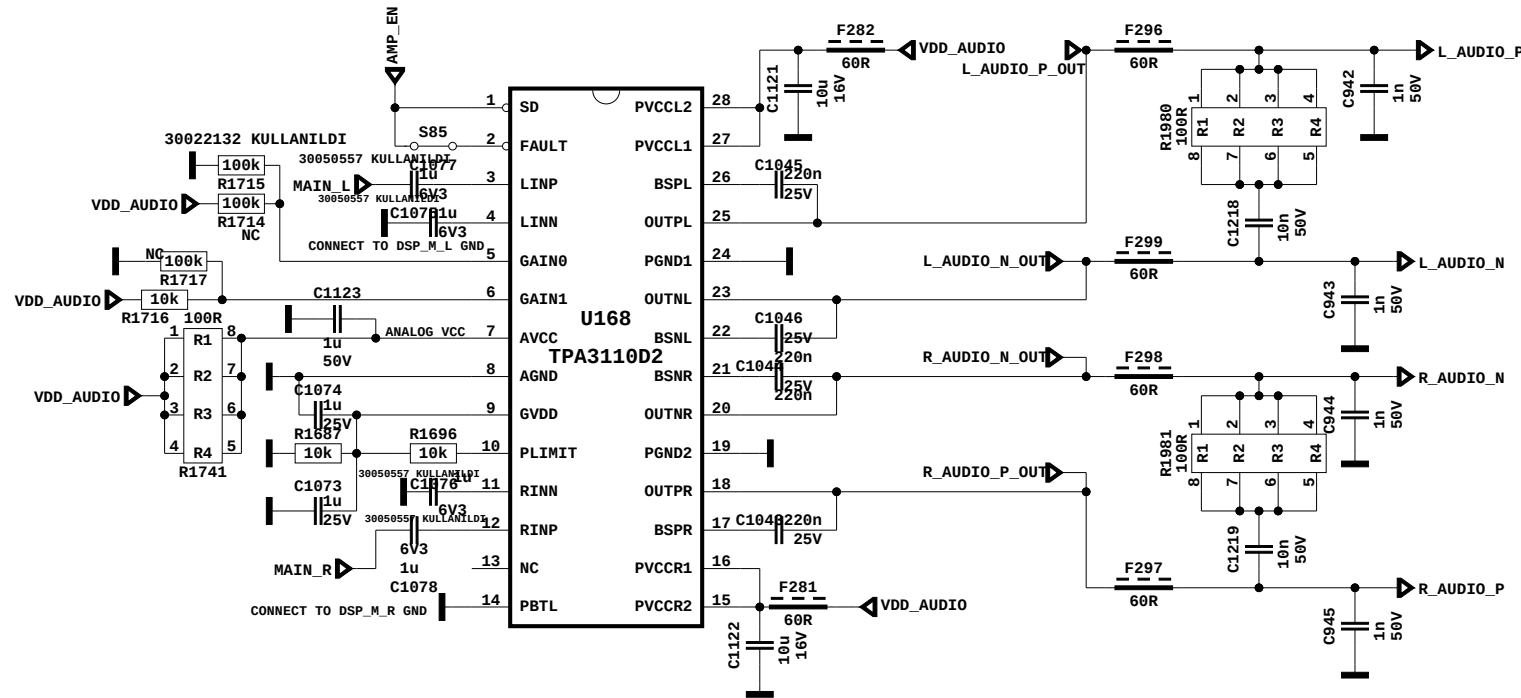
AUDIO AMP for 16" to 24"

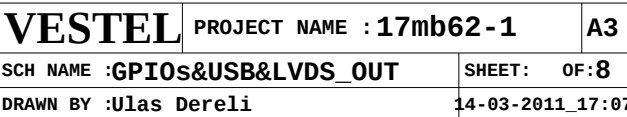


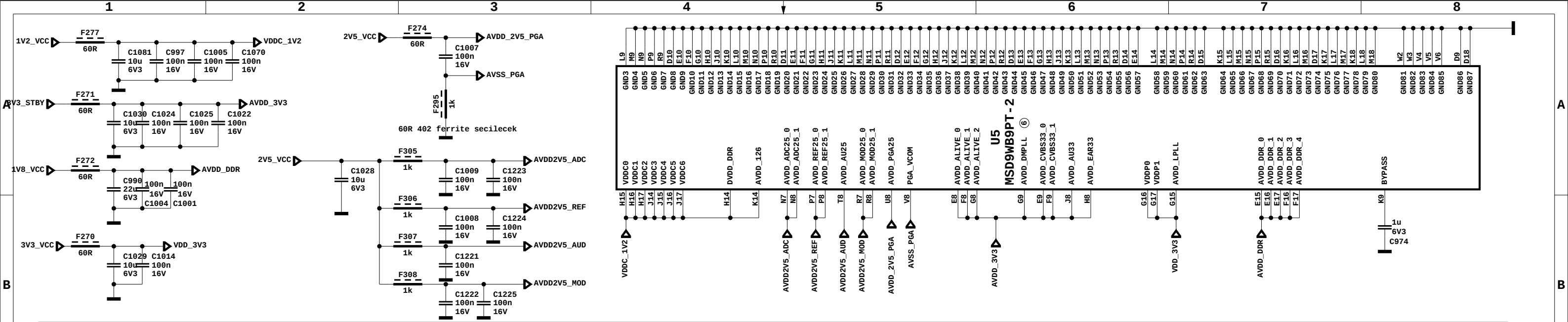
SLIM HEADPHONE OUTPUT



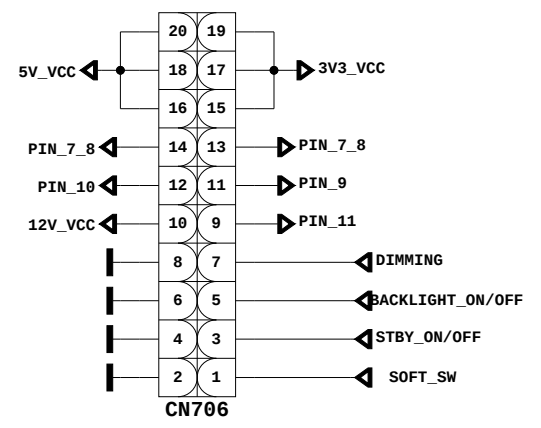
AUDIO AMP for 26" to 32"



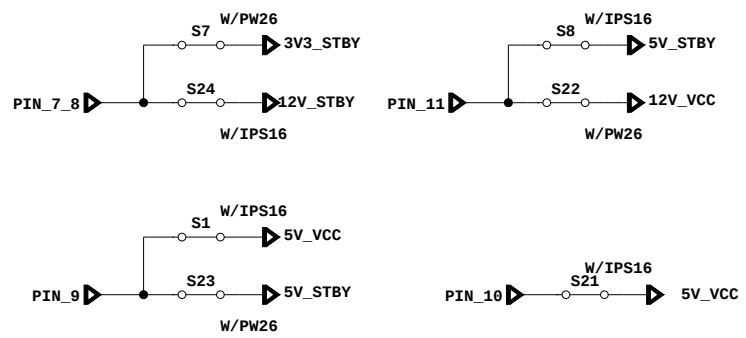
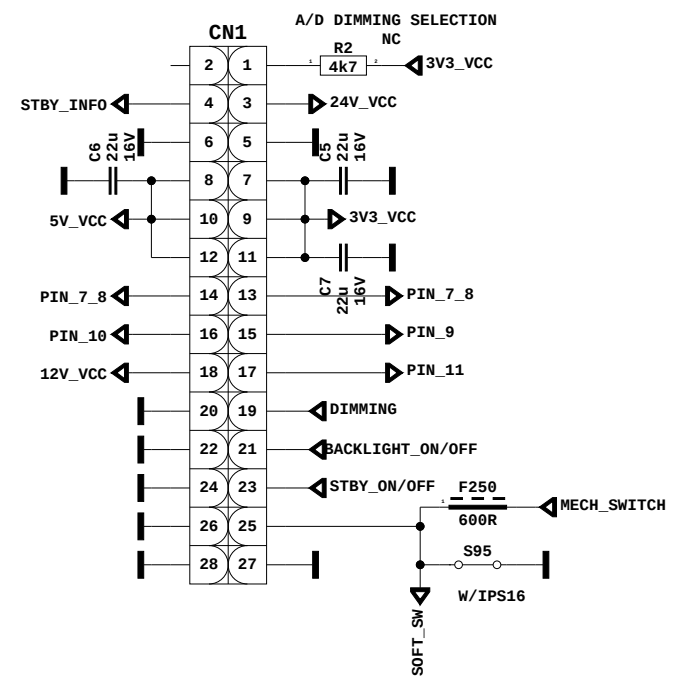




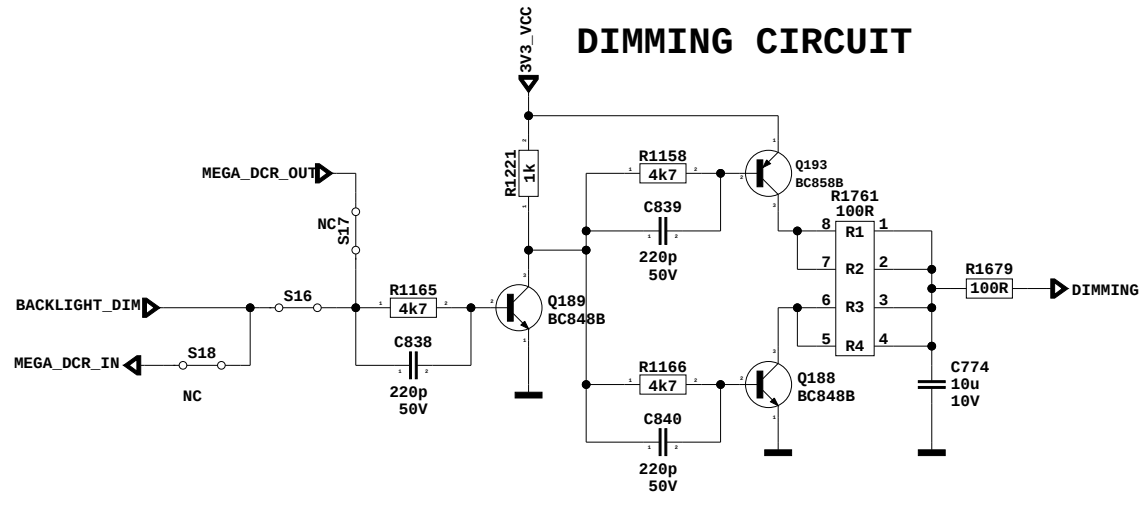
16" to 24" POWER SOCKET



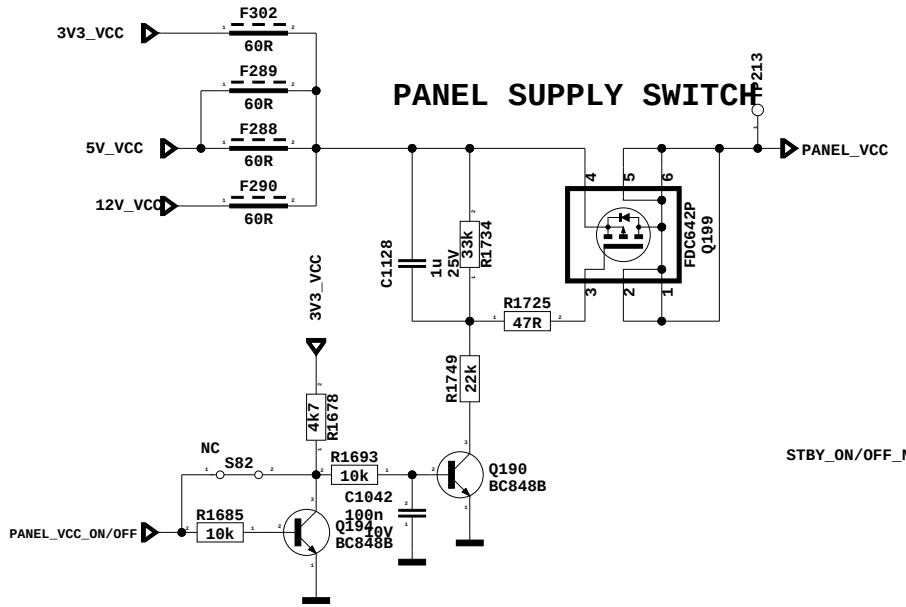
26" to 32" POWER SOCKET



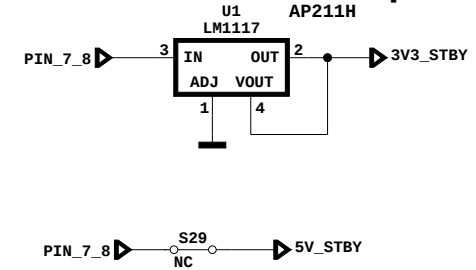
DIMMING CIRCUIT



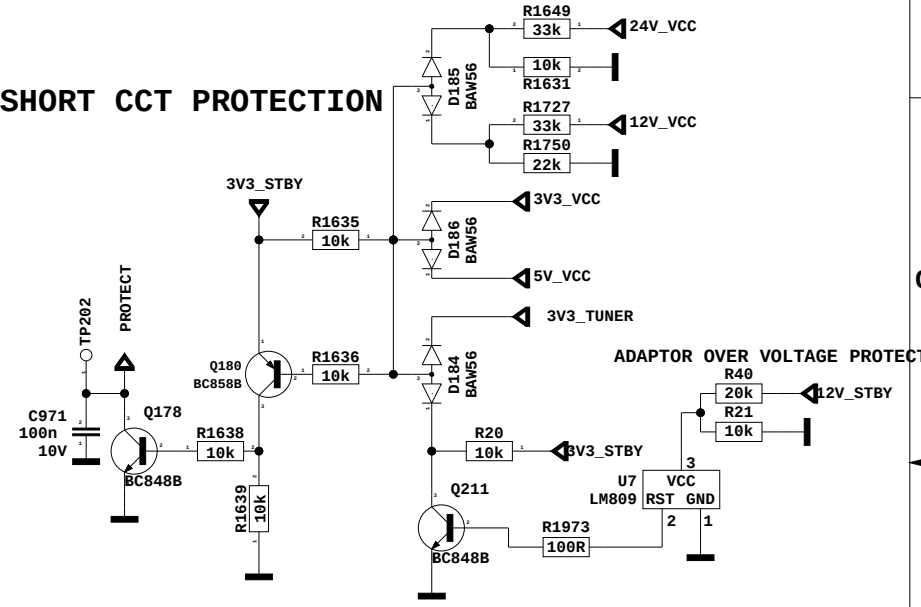
PANEL SUPPLY SWITCH



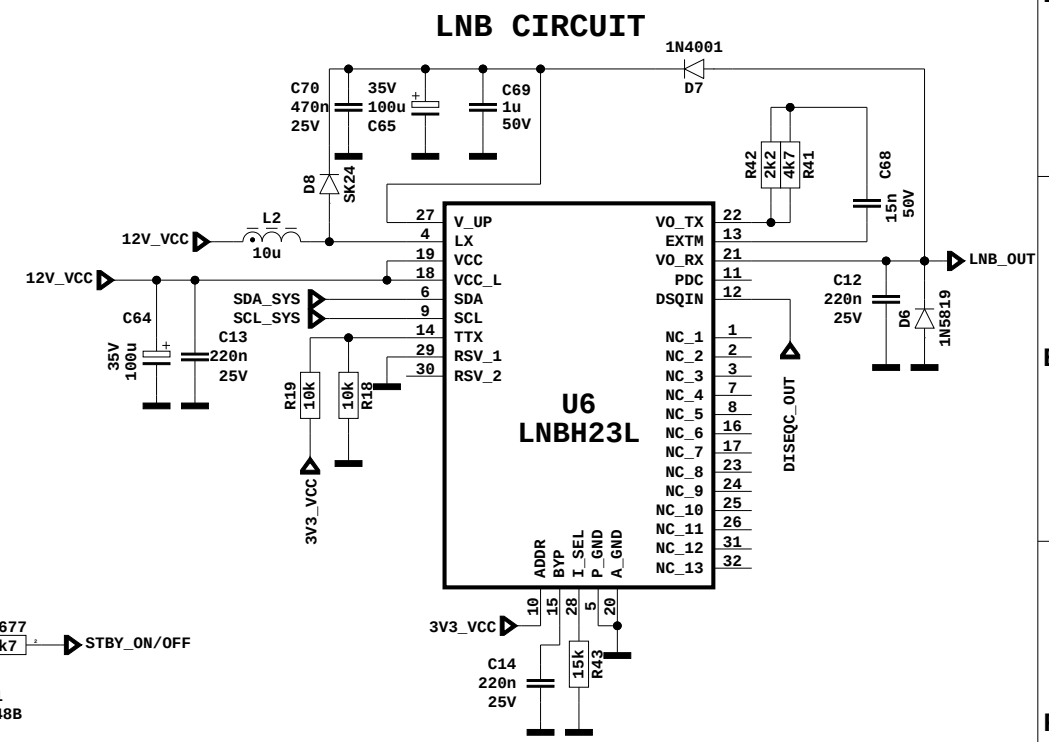
PW04 LOW POWER Option



SHORT CCT PROTECTION



LNB CIRCUIT



W_ADAPTER

5

4

3

2

1

JK9

TP239

TP36

CCFL INVERTER SOCKET

6

5

4

3

2

1

Q1

FDC684P

Q2

FDC642P

NC

12V_STBY

7A/32VDC

FS2

7A/32VDC

12V_INV

12V_INV

TP37

TP39

DIMMING

BACKLIGHT_ON/OFF

TP45

TP46

CN705

1

2

3

4

5

6

The schematic shows two power stages. The **DC/DC1** stage is a buck converter using the **MP1583** (U174) IC. It takes a **12V_STBY** input and converts it to a **5V_STBY** output. The input filter consists of a **68pF** capacitor (**F287**) and a **22uF** capacitor (**C1091**) in parallel. The feedback network includes a **10k** resistor (**R1972**) and a **10k** resistor (**R1690**) in parallel. The output filter consists of a **5nF** capacitor (**C1130**) and a **50V** capacitor (**C1092**) in parallel. The **SW2** stage is a MOSFET driver using the **BC848B** (Q184) NPN transistor. It takes a **MOSFET_CONTROL** input and drives the **5V_VCC** output. The driver circuit includes a **10k** resistor (**R1698**) and a **1k** resistor (**R1728**) in parallel. The output filter consists of a **22uF** capacitor (**C1103**) and a **16V** capacitor (**C1112**) in parallel. The output voltage is **5V_VCC**.

