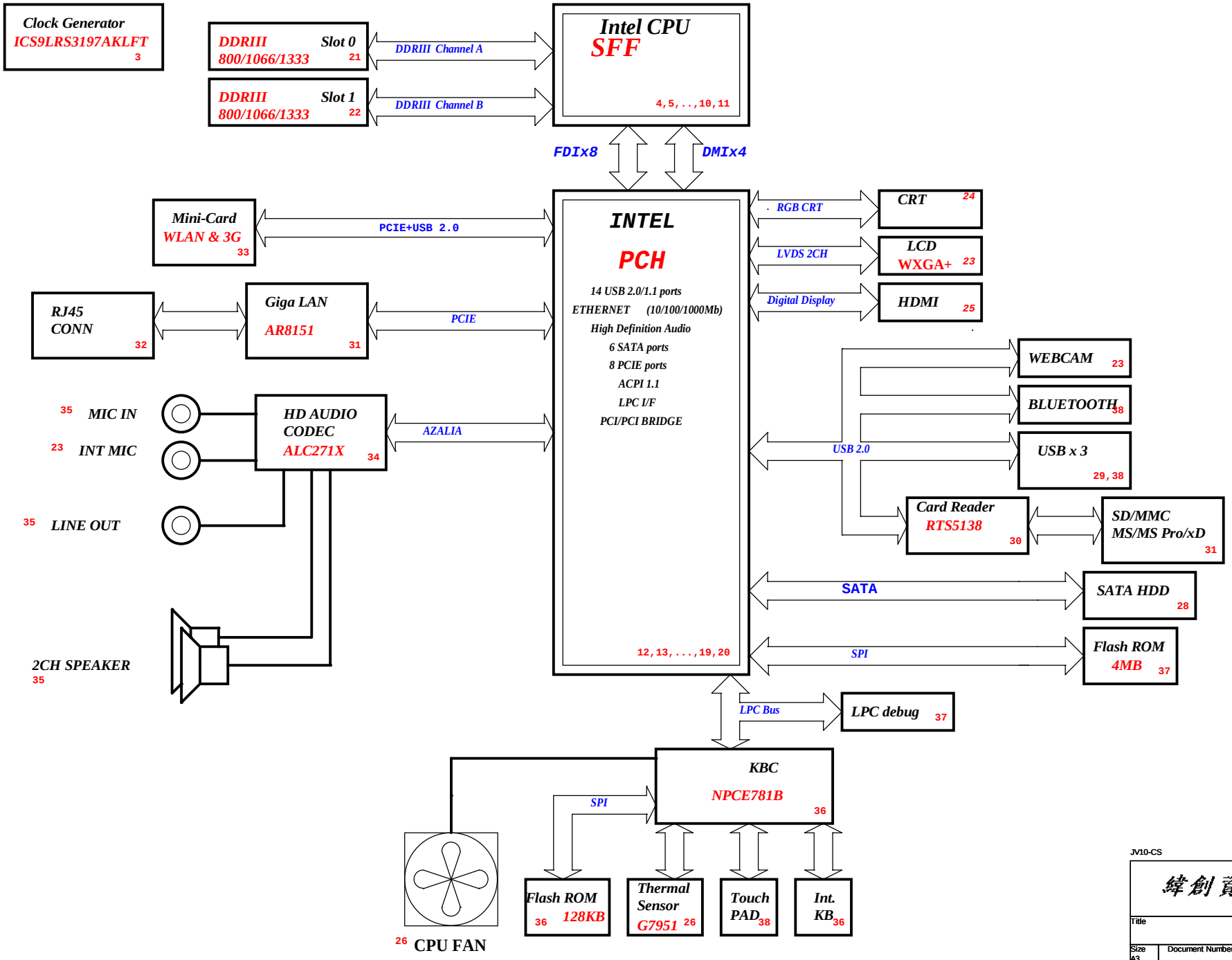
JV10-CS Block Diagram

Project code:91.4GS01.001
PCB P/N :48.4GS01.0SA
REVISION :09918-2



SYSTEM DC/DC
RT8223

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 42

SYSTEM DC/DC
RT8209E

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 43

SYSTEM DC/DC
RT8209B

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 44

SYSTEM DC/DC
RT9026

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 43

CPU DC/DC
TPS51611

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 41

INTERSIL CHARGER
ISL88731A

INPUTS	OUTPUTS
DCBATOUT	BT+ 45

PCB STACKUP

TOP
Power
S
S
GND
BOTTOM

JV10-CS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size: A3 | Document Number: JV10-CS | Rev: -1

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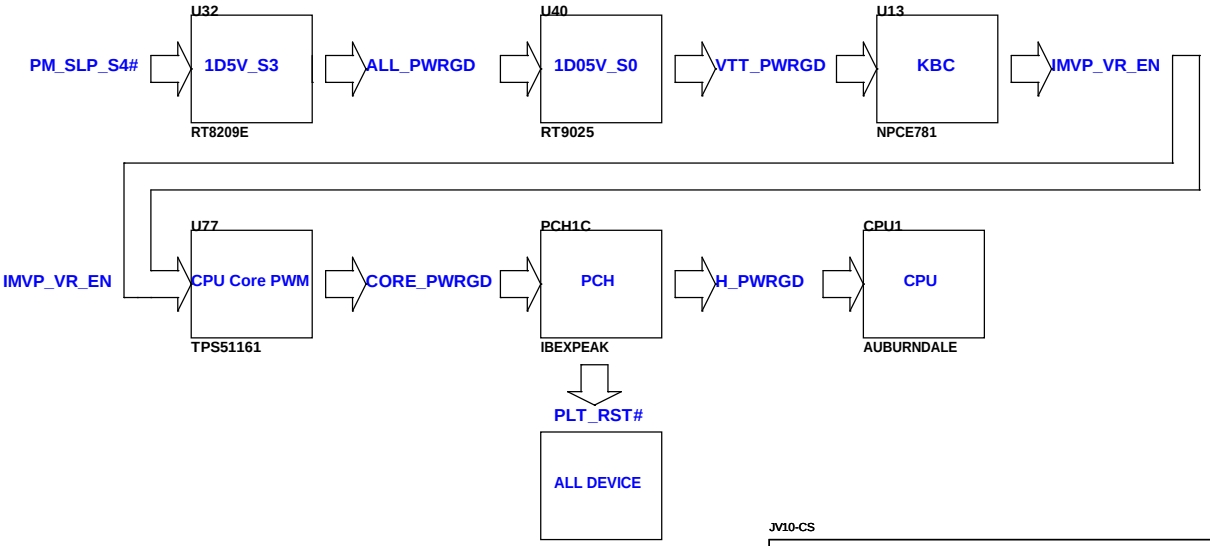
PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):**Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:**Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:**Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:**Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:**Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :**Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

Power Sequence



PCIE Routing

LANE1	LAN
LANE2	MiniCard1

USB Table

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1
4	WECAM
5	NC
6	NC
7	NC
8	NC
9	USB1(HS)
10	NC
11	Blue Tooth
12	MINIC2
13	Cardreader

JV10-CS

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Title: **Table of Content**

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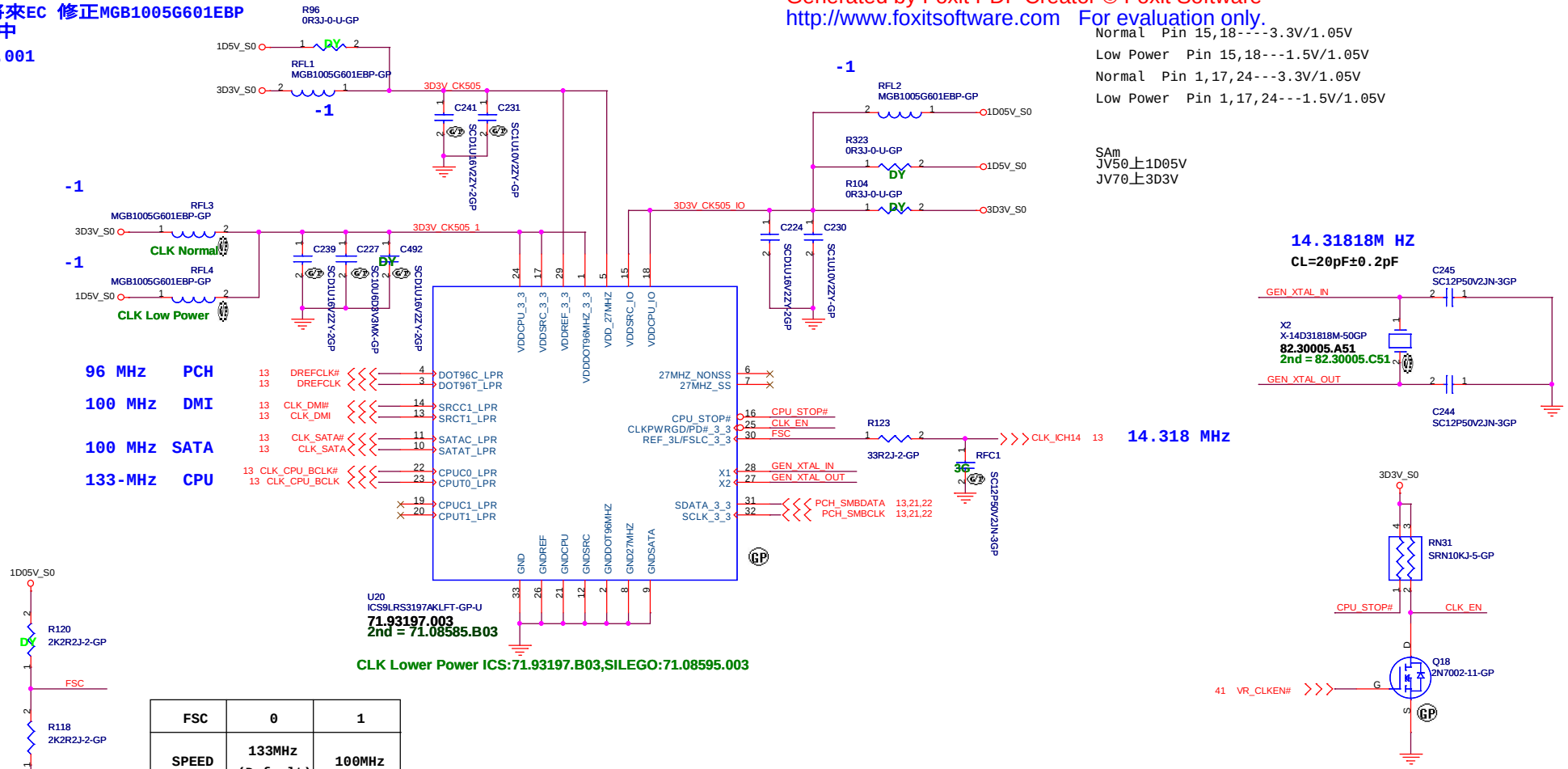
RFL1~4 將來EC 修正MGB1005G601EBP
料號申請中
68.00373.001

Normal Pin 15,18----3.3V/1.05V
Low Power Pin 15,18---1.5V/1.05V
Normal Pin 1,17,24---3.3V/1.05V
Low Power Pin 1,17,24---1.5V/1.05V

SAm
JV50上1D05V
JV70上3D3V



FSC	0	1
SPEED	133MHz (Default)	100MHz

JV10-CS

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Title: Clock Generator
Size: Custom | Document Number: JV10-CS | Rev: -1
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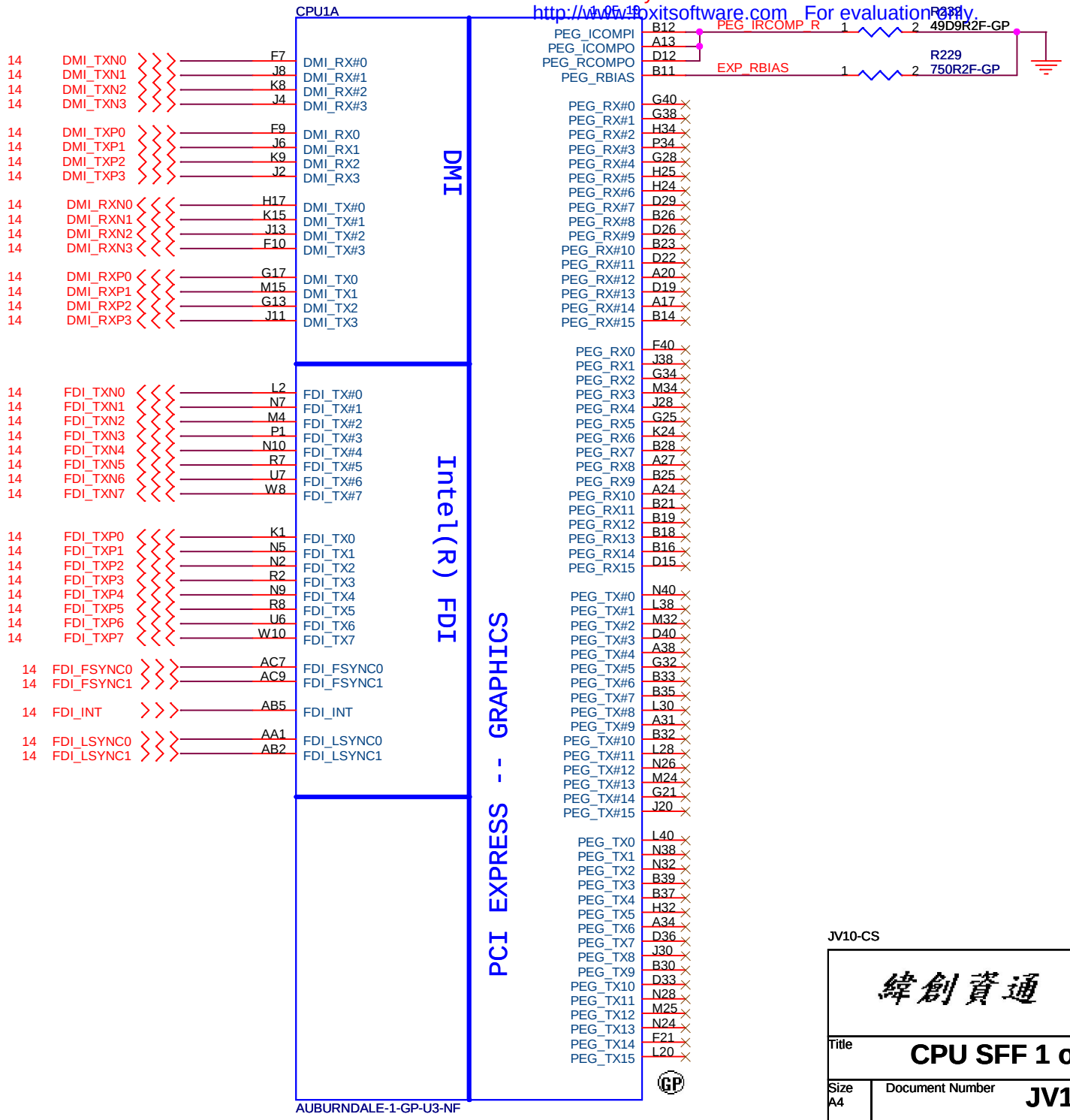

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Title: CPU SFF 1 of 8(DMI/FDI/PEG)

Size	Document Number	Rev
A4	JV10-CS	-1

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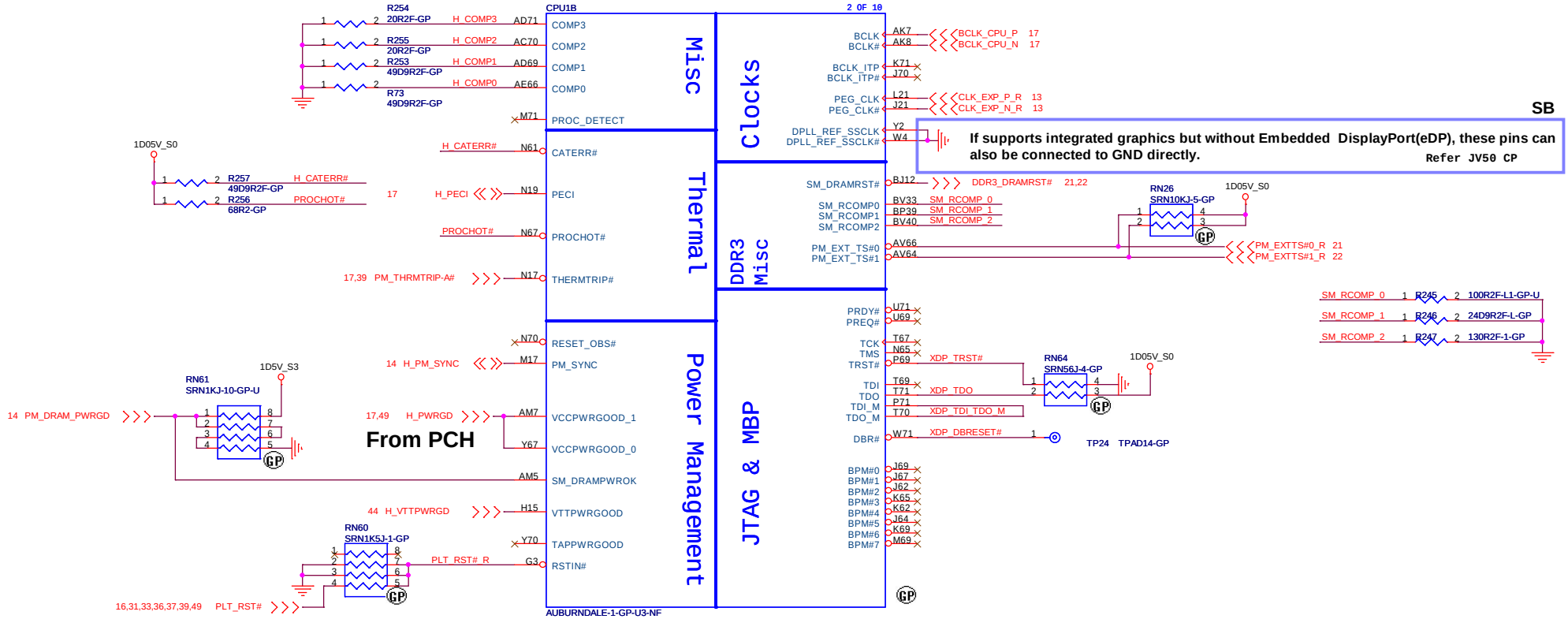

JV10-CS

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Title: **CPU SFF 2 of 8(CLK/Thermal)**

Size	Document Number	Rev
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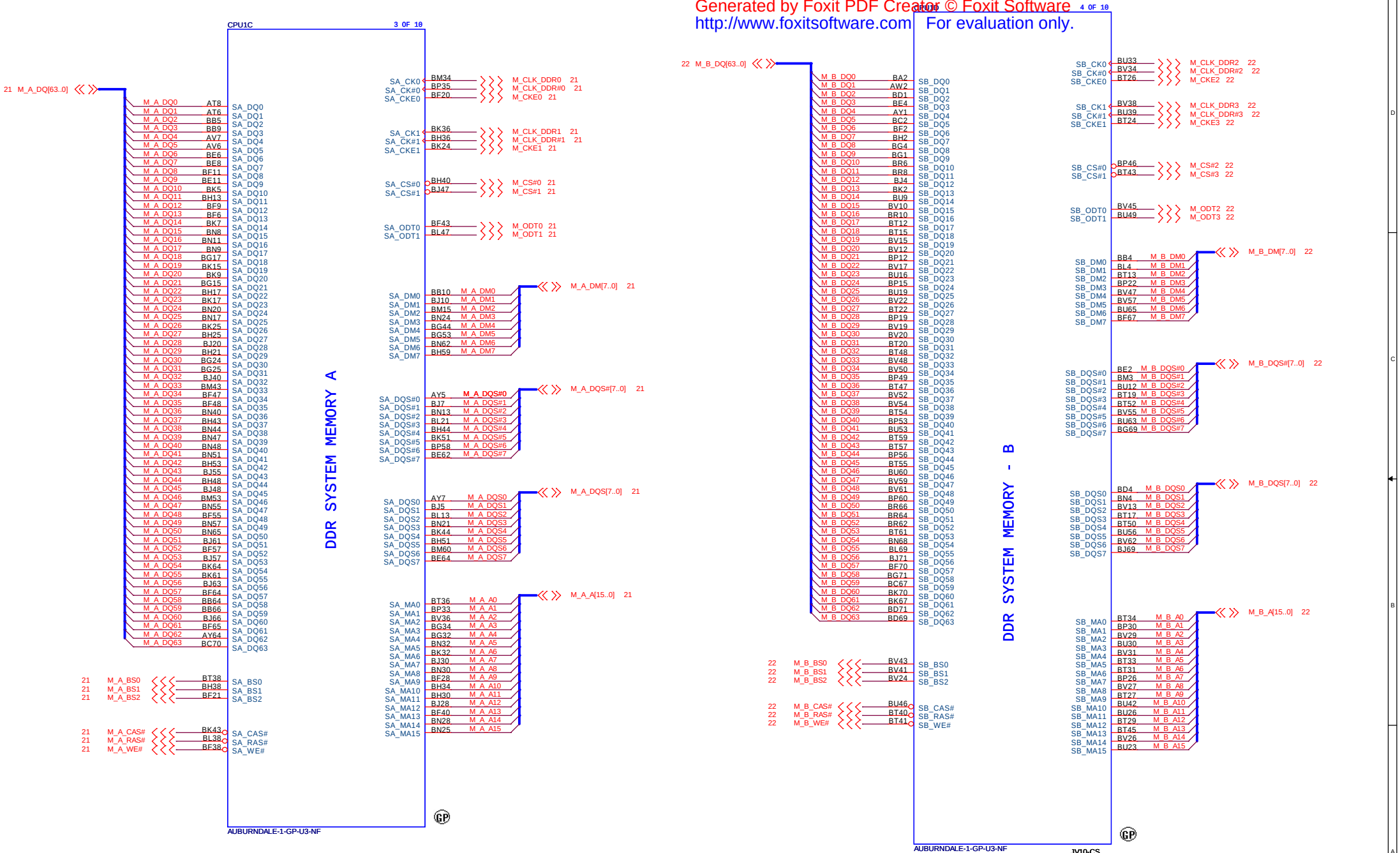

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Title	**CPU SFF 3 of 8(DDR)**	
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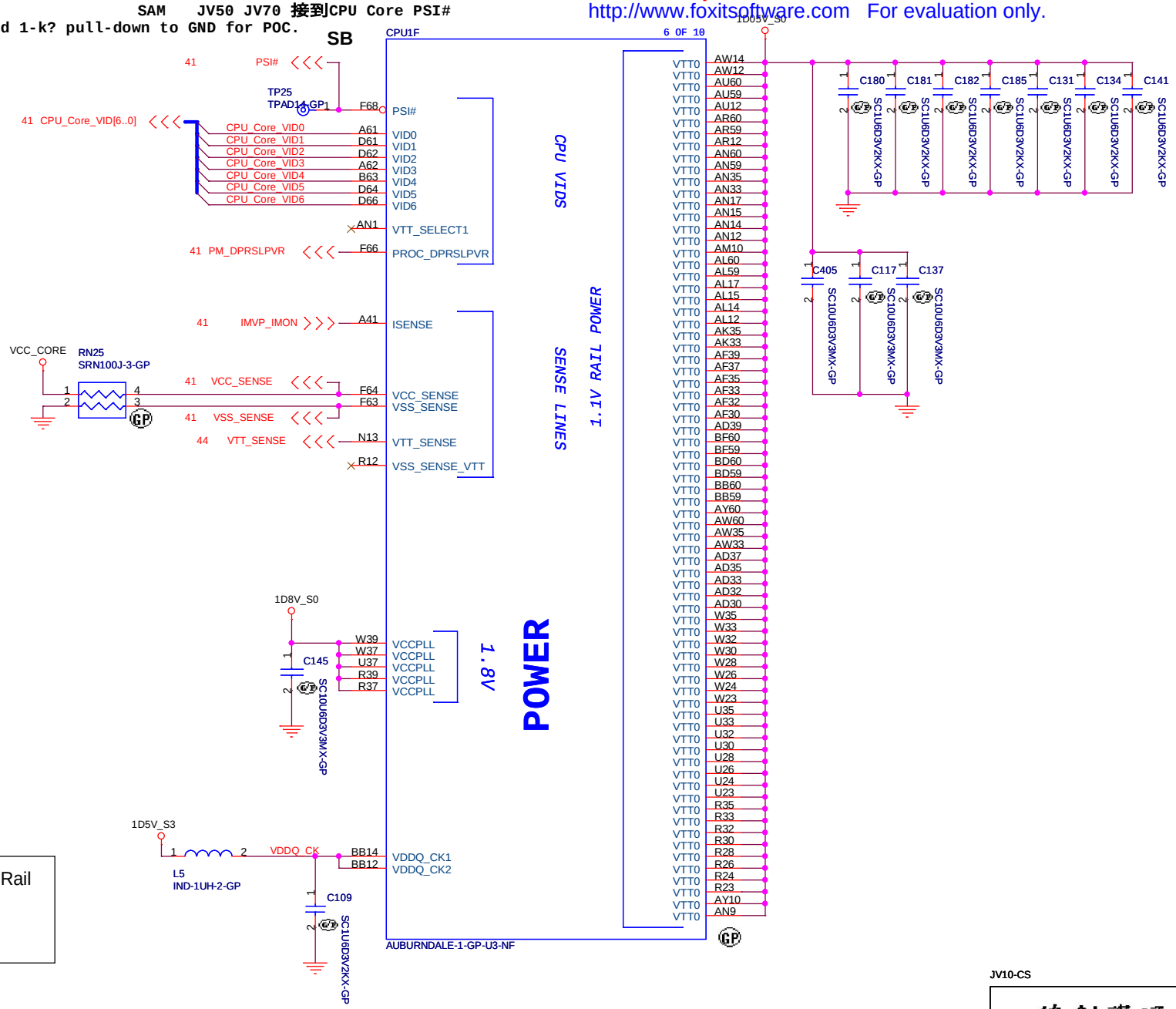
check list SAM JV50 JV70 接到CPU Core PSI#
1-k? pull-up to VTT and 1-k? pull-down to GND for POC.
1D05V_VTT



Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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Title	CPU SFF 4 of 8(POWER/VTT)		
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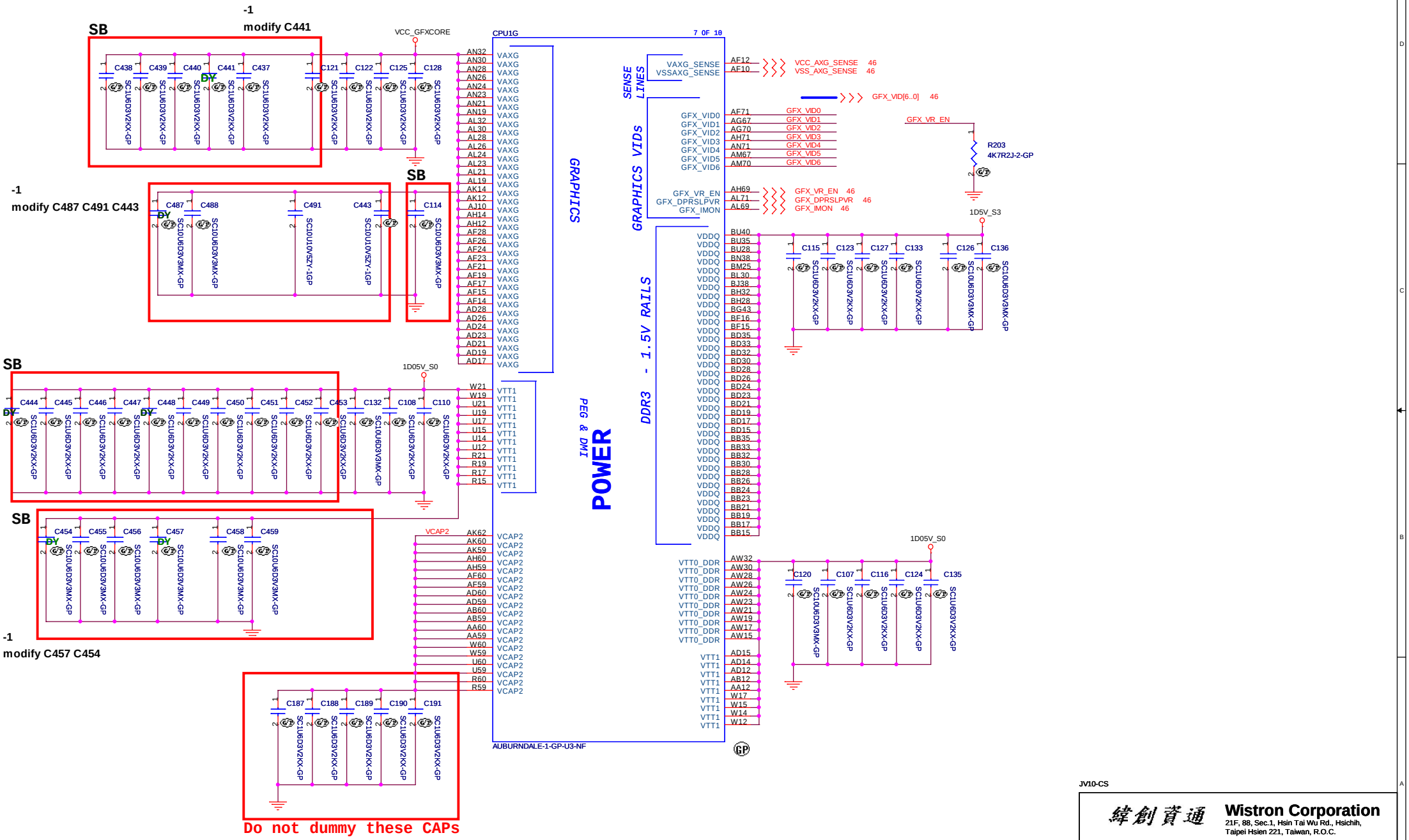

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Title	CPU SFF 5 of 8(PWR/DDR/GFX/)	
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POWER

CPU CORE SUPPLY

Sam

Processor package decoupling -
DO NOT connect to any power rail

CPU1H — 8 OF 10 — AUBURNDALE-1-GP-U3-NF

VCAP0 pins: BD55, BD51, BD48, BB55, BB51, BB48, AY57, AY53, AY50, AW57, AW53, AW50, AU55, AU51, AU48, AR55, AR51, AR48, AN57, AN53, AN50, AL57, AL53, AL50, AK57, AK53, AK50

VCAP1 pins: BD44, BD41, BD37, BB44, BB41, BB37, AY46, AY42, AY39, AW46, AW42, AW39, AU44, AU41, AU37, AR44, AR41, AR37, AN46, AN42, AN39, AL46, AL42, AL39, AK46, AK42, AK39

VCC_CORE pins: AF55, AF53, AF51, AF50, AF48, AF46, AF44, AF42, AF41, AD55, AD51, AD48, AD44, AD41, AB55, AB51, AB48, AB44, AB41, AA55, AA51, AA48, AA44, AA41, W55, W51, W48, W44, W41, U55, U51, U48, U44, U41, R55, R51, R48, R44, R41, P60, N55, N51, N48, N44, N42, M60, M51, M44, L55, K60, K51, K44, J55, H60, H51, H44, G60, G55, G51, G44, F55, E60, E57, E53, E50, E46, E42, D59, D57, D55, D54, D52, D50, D48, D47, D45, D43, B60, B56, B53, B49, B46, B42, A57, A54, A50, A47, A43

-1
modify C160 C161

-1
modify C167 C168

SB

SB

SB

-1
modify C477 C479 C476 C473

JV10-CS

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Title: CPU SFF 6 of 8(CPUCORE)

Size: Custom | Document Number: JV10-CS | Rev: -1

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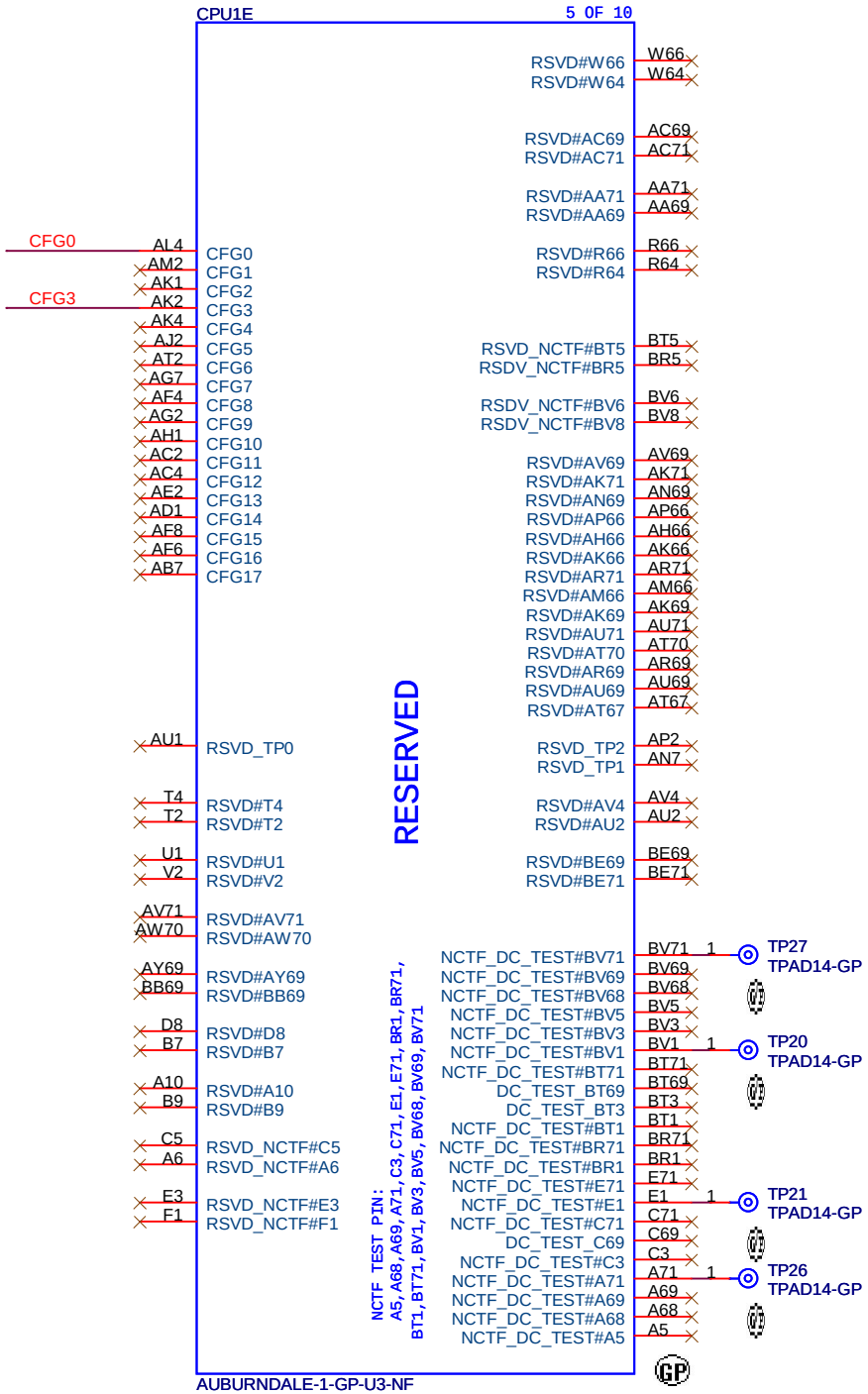

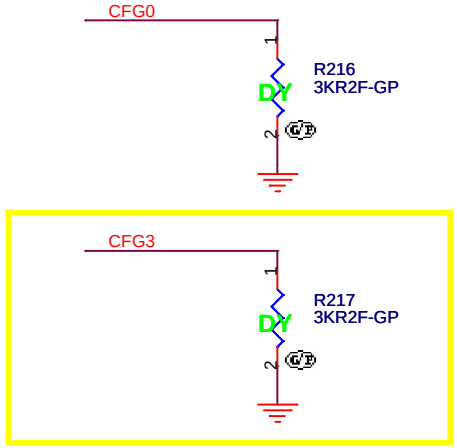

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

JV10-CS

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Title: **CPU SFF 7 of 8(RESERVED)**

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VSS

BU62 BU58 BU55 BU51 BU48 BU44 BU37 BU32 BU25 BU21 BU18 BU14 BU11 BU7 BP42 BN64 BN6 BM70 BM51 BM44 BM32 BM24 BM17 BL57 BL55 BL48 BL40 BL28 BL20 BK63 BK60 BK53 BK34 BK10 BJ64 BJ21 BJ9 BJ1 BH70 BH57 BH55 BH47 BH24 BH20 BH15 BG51 BG36 BF62 BF30 BF13 BF8 BE70 BE65 BE9 BE1 BD57 BD53 BD50 BD46 BD42 BD39 BD14 BB71 BB62 BB57 BB53 BB50 BB46 BB42 BB39 BB7 BB1 BA70 AY71 AY66 AY62 AY59 AY55 AY51 AY48 AR42 AR39 AR35 AR33 AR32 AR30 AR28 AR26 AR24 AR23 AR21 AR19 AR17 AR15 AR14 AR4 AR1 AP70 AP64 AN62 AN55 AY44 AY41 AY37 AY35 AY33 AY32 AY30 AY28 AY26

AY24 AY23 AY21 AY19 AY17 AY15 AY14 AY12 AY8 AY4 AW67 AW62 AW59 AW55 AW51 AW48 AW44 AW41 AW37 AV9 AV1 AU70 AU62 AU57 AU53 AU50 AU46 AU42 AU39 AU35 AU33 AU32 AU30 AU28 AU26 AU24 AU23 AU21 AU19 AU17 AU15 AU14 AU4 AT64 AT10 AR62 AR57 AR53 AR50 AR46 AN51 AN48 AN44 AN41 AN37 AN5 AN4 AM64 AM8 AL62 AL55 AL51 AL48 AL44 AL41 AL37 AL35 AL33 AL1 AK70 AK64 AK55 AK51 AK48 AK44 AK41 AK37 AK32 AK30 AK28 AK26 AK24 AK23 AK21 AK19 AK17 AK15 AJ70 AH62 AH57 AH55 BV66 BV64 BT68 BR69 BR68 BR3 BN71 BN1 BL71 BL1 R14 H71 F71 E69 E68 A66 A64 E5 C68

AUBURNDALE-1-GP-U3-NF

CPU1J — 10 OF 10

VSS

AH58 AH55 AH50 AH48 AH46 AH44 AH42 AH41 AH39 AH37 AH35 AH33 AH32 AH30 AH28 AH26 AH24 AH23 AH21 AH19 AH17 AH15 AH4 AG64 AG9 AG6 AF69 AF62 AF1 AE70 AE64 AD62 AD57 AD53 AD50 AD46 AD42 AD4 AC67 AC64 AC10 AC5 AC1 AB70 AB62 AB57 AB53 AB50 AB46 AB42 AB39 AB37 AB35 AB33 AB32 AB30 AB28 AB26 AB24 AB23 AB21 AB19 AB17 AB15 AB14 AB9 AA66 AA64 AA62 AA57 AA53 AA50 AA46 AA42 AA39 AA37 AA35 AA33 AA32 AA30 AA28 AA26 AA24 AA23 AA21 AA19 F20 F4 E37 E33 E30 E16 E12 D41 D38 D34 D31 D27 D24 D20 D17 D13 D10 D6 B65 B40

A48 A45 A33 A29 A26 A22 A19 A15 A12 A8 B62 B58 B55 B51 B48 B44 A59 A55 A52 A48 A45 AA17 AA15 AA14 AA4 W69 W62 W57 W53 W50 W46 W42 W6 W1 V70 U64 U62 U57 U53 U50 U46 U42 U39 U9 U4 T1 R70 R62 R57 R53 R50 R46 R42 R5 P4 N63 N57 N53 N50 N46 N30 N21 N15 M53 M42 M36 M1 L70 L57 L48 L47 L13 K64 K53 K43 K36 K34 K32 K25 K17 K11 K6 K4 J65 J57 J48 J47 J40 J9 H53 H43 H36 H1 G70 G57 G53 G48 G47 G43 G30 G24 G20 G15 F61 F48 F47 F28

AUBURNDALE-1-GP-U3-NF

JV10-CS

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integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

SB

X3
X-32D768KHZ-34GPU
82.30001.661
2ND = 82.30001.B21

C304 SC5P50V2CN-2GP
C307 SC5P50V2CN-2GP

R168 10MR2J-L-GP

RTC_X1
RTC_X2

RTC_AUX_S5
R163 330KR2F-L-GP
INTVRMEN
SM_INTRUDER#
R164 1MR2J-1-GP

RN40 SRN20KJ-GP-U
RTC_AUX_S5
ICH_RTCRST#
SRTCRST#
SM_INTRUDER#
INTVRMEN

C296 SC1U10V3KX-3GP
G80 GAP-OPEN
C297 SC1U10V3KX-3GP

RN45 SRN33J-7-GP
34 ACZ_RST#_AUDIO
34 ACZ_BITCLK_AUDIO
34 ACZ_SYNC_AUDIO
34 ACZ_SDATAOUT_AUDIO
ACZ_RST#
ACZ_BIT_CLK
ACZ_SYNC
ACZ_SDATAOUT

ACZ_BIT_CLK
EC11 DY SC22P50V2JN-4GP
PCH_SPI_CLK
EC14 DY SC22P50V2JN-4GP

PCH1A

RTC_X1	B13	RTCX1	RTC		
RTC_X2	D13	RTCX2			
ICH_RTCRST#	C14	RTCRST#			
SRTCRST#	D17	SRTCRST#			
SM_INTRUDER#	A16	INTRUDER#			
INTVRMEN	A14	INTVRMEN			
ACZ_BIT_CLK	A30	HDA_BCLK	IHDA		
ACZ_SYNC	D29	HDA_SYNC			
34 ACZ_SPKR	P1	SPKR			
ACZ_RST#	C30	HDA_RST#			
34 ACZ_SDATAIN0	G30	HDA_SDIN0			
	F30	HDA_SDIN1			
	E32	HDA_SDIN2			
	F32	HDA_SDIN3			
ACZ_SDATAOUT	B29	HDA_SDO			
36 ME_UNLOCK#	H32	HDA_DOCK_EN#/GPIO33	SATA		
	J30	HDA_DOCK_RST#/GPIO13			
TPAD14-GP TP14	M3	JTAG_TCK	JTAG		
	K3	JTAG_TMS			
	K1	JTAG_TDI			
	J2	JTAG_TDO			
	J4	TRST#			
37 PCH_SPI_CLK	BA2	SPI_CLK	SPI		
37 PCH_SPI_CS#0	AV3	SPI_CS0#			
	AY3	SPI_CS1#			
37 PCH_SPI_MOSI	AY1	SPI_MOSI			
SPI_MOSO_R	AV1	SPI_MISO			

1 OF 10

FWH0/LAD0	D33	LPC_LAD0	36,37
FWH1/LAD1	B33	LPC_LAD1	36,37
FWH2/LAD2	C32	LPC_LAD2	36,37
FWH3/LAD3	A32	LPC_LAD3	36,37
FWH4/LFRAME#	C34	LPC_LFRAME#	36,37
LDRQ0#	A34		
LDRQ1#/GPIO23	F34		
SERIRQ	AB9	INT_SERIRQ	36

SATA0RXN	AK7	SATA_RXN0_C	
SATA0RXP	AK6	SATA_RXP0_C	
SATA0TXN	AK11	SATA_TXN0_C	
SATA0TXP	AK9	SATA_TXP0_C	
SATA1RXN	AH6		
SATA1RXP	AH5		
SATA1TXN	AH9		
SATA1TXP	AH8		
SATA2RXN	AF11		
SATA2RXP	AF9		
SATA2TXN	AF7		
SATA2TXP	AF6		
SATA3RXN	AH3		
SATA3RXP	AH1		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	AD9		
SATA4RXP	AD8		
SATA4TXN	AD6		
SATA4TXP	AD5		
SATA5RXN	AD3		
SATA5RXP	AD1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	AF16	SATAICOMP	
SATAICOMPI	AF15		
SATALED#	T3	SATA_LED#	14,27
SATA0GP/GPIO21	Y9	SATA_DET#0_R	
SATA1GP/GPIO19	V1	SATA_DET#1_R	17

IBEXPEAK-M-GP-NF

HDD

SATA_RXN0_C	C273	SCD01U50V2KX-1GP	SATA_RXN0 28
SATA_RXP0_C	C272	SCD01U50V2KX-1GP	SATA_RXP0 28
SATA_TXN0_C	C87	SCD01U50V2KX-1GP	SATA_TXN0 28
SATA_TXP0_C	C83	SCD01U50V2KX-1GP	SATA_TXP0 28

When unused all JTAG pins may be NC

TPAD14-GP TP14
PCH_JTAG_TCK
SB
R292 51R2F-2-GP

-1

R40 37D4R2F-GP
1D05V_S0

R305 0R2J-2-GP SPI_CLK_R
R306 0R2J-2-GP SPI_CS#0_R
R307 0R2J-2-GP SPI_MOSI_R

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

1D8V_S0 1D5V_S0
-1
R151 10KR2J-3-GP DY
R152 10KR2J-3-GP DY
ACZ_SYNC
R150 10KR2J-3-GP DY

RN17 SRN10KJ-7GP 3D3V_S0
17 PCH_GPIO17
17 PCH_GPIO37
SATA_DET#0_R
INT_SERIRQ

If reserve 1.5/1.8V option for VCCVRM.Not Power plan change only.
Please refer figure2.HDA_SYNC will be strap to define VCCVRM is 1.5 or 1.8V source.
Means need have Pull high/low resistor to option,
P/H voltage base on HAD Link is 1.5V or 3.3V(Figure 3).

3D3V_AUX_S5
RTC_AUX_S5
C381 SC1U16V2ZY-GP
D26 BAS40CW-GP
83.00040.E81
2nd = 83.00040.M81
RTC_BAT_1
R233 1KR2J-1-GP
RTC_BAT
RTC2 ACES-CON2-11-GP
20.F0772.002
2nd = 20.F1035.002

-1 SWPA Pin define

RTC CONN

23.25218.001
Pin define 要換,確認connector part number

JV10-CS

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Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH 1 of 9(SATA/RTC/HDA)	
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LAN
MINICARD1
MINICARD2

PCIE_RXN1 PCIE_RXP1 PCIE_TXN1 PCIE_TXP1
PCIE_RXN2 PCIE_RXP2 PCIE_TXN2 PCIE_TXP2
PCIE_RXN3 PCIE_RXP3 PCIE_TXN3 PCIE_TXP3

SCD1U10V2KX-5GP C359 TXN1 C358 TXP1
SCD1U10V2KX-5GP C361 TXN2 C360 TXP2
SCD1U10V2KX-5GP C374 TXN3 C372 TXP3

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

PCI-E*

SMBus
SMBALERT#/GPIO11 PCH_GPIO11
SMBCLK SMB_CLK
SMBDATA SMB_DATA
SML0ALERT#/GPIO60 PCH_GPIO60 17
SML0CLK SML0_CLK
SML0DATA SML0_DATA
SML1ALERT#/GPIO74 PCH_GPIO74 17
SML1CLK/GPIO58 KBC_SCL1 36
SML1DATA/GPIO75 KBC_SDA1 36

Controller Link
CL_CLK1
CL_DATA1
CL_RST1#

PEG
PEG_A_CLKRQ#/GPIO47 PEG_A_CLKRQ#
CLKOUT_PEG_A_N CLKOUT_PEG_A_P
CLKOUT_DMI_N CLKOUT_DMI_P

From CLK BUFFER
CLKOUT_DP_N/CLKOUT_BCLK1_N CLKOUT_DP_P/CLKOUT_BCLK1_P
CLKIN_DMI_N CLKIN_DMI_P
CLKIN_BCLK_N CLKIN_BCLK_P
CLKIN_DOT_96N CLKIN_DOT_96P
CLKIN_SATA_N/CKSSCD_N CLKIN_SATA_P/CKSSCD_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN XTAL25_OUT
XCLK_RCOMP

Clock Flex
CLKOUTFLEX0/GPIO64 33MHZ
CLKOUTFLEX1/GPIO65 33MHZ
CLKOUTFLEX2/GPIO66 33MHZ
CLKOUTFLEX3/GPIO67 CLK48

IBEXPEAK-M-GP-NF

SB

RN12 SRN2K2J-2-GP
SML0_CLK KBC_SCL1
SML0_DATA KBC_SDA1

Change 4.7K
KBC_SCL1
KBC_SDA1

RN47 SRN2K2J-2-GP
3D3V_S5 3D3V_S0
SMB_CLK SMB_DATA
3,21,22 PCH_SMBDATA
PCH_SMBCLK 3,21,22
Q23 2N7002KDW-GP
84.2N702.A3F

check list
100-MHz differential clock from PCH to processor.
Connect to PEG_CLK#/PEG_CLK pins of the processor
沒電阻

SB
CLK_EXP_N R308 0R0201-PAD-GP CLK_EXP_N_R 5
CLK_EXP_P R309 0R0201-PAD-GP CLK_EXP_P_R 5
CLKOUT_DP_N TP45 AFTE14P-GP
CLKOUT_DP_P TP46 AFTE14P-GP

SB
MINICARD1 100 MHz
MINICARD2
LAN
R299 R300 R35 R301 R302 R130 R303 R304 R158 0R0201-PAD-GP
CLK_PCIE_MINI1# CLK_PCIE_MINI1 MINI1_CLKREQ#
CLK_PCIE_MINI2# CLK_PCIE_MINI2 MIN2_CLKREQ#
CLK_PCIE_LAN# CLK_PCIE_LAN LAN_CLKREQ#
CLK_PCH_SRC1_N CLK_PCH_SRC1_P PCIE_CLK_RQ1#
CLK_PCH_SRC2_N CLK_PCH_SRC2_P PCIE_CLK_RQ2#
CLK_PCH_SRC3_N CLK_PCH_SRC3_P PCIE_CLK_RQ3#
PCIE_CLK_RQ0# PCIE_CLK_RQ1# PCIE_CLK_RQ4#
PCIE_CLK_RQ5# PEG_B_CLKRQ#

CLKOUT_PCIE0N CLKOUT_PCIE0P PCIECLKRQ0#/GPIO73
CLKOUT_PCIE1N CLKOUT_PCIE1P PCIECLKRQ1#/GPIO18
CLKOUT_PCIE2N CLKOUT_PCIE2P PCIECLKRQ2#/GPIO20
CLKOUT_PCIE3N CLKOUT_PCIE3P PCIECLKRQ3#/GPIO25
CLKOUT_PCIE4N CLKOUT_PCIE4P PCIECLKRQ4#/GPIO26
CLKOUT_PCIE5N CLKOUT_PCIE5P PCIECLKRQ5#/GPIO44
CLKOUT_PEG_B_N CLKOUT_PEG_B_P PEG_B_CLKRQ#/GPIO56

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

RN9 SRN10KJ-7GP 3D3V_S5
17 PCH_GPIO28 PCIE_CLK_RQ4#
PEG_B_CLKRQ#
14 PM_RSMRST#

SB
RN44 SRN10KJ-7GP 3D3V_S5
PCH_GPIO11 PCIE_CLK_RQ3# PCIE_CLK_RQ5#
14 PCH_GPIO72

XCLK_RCOMP R37 90D9R2F-1-GP 1D05V_S0
CLK48 R185 33R2J-2-GP 48MHZ EC38 SC222P50V2JN-4GP CLK48_Cardreader 30

XTAL25_IN R215 1MR2J-1-GP C349 SC12P50V2JN-3GP
XTAL25_OUT X4 XTAL-25MHZ-102-GP C350 SC12P50V2JN-3GP
82.30020.851
2nd = 82.30020.971

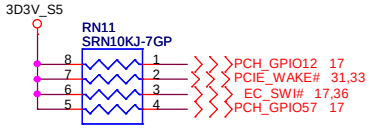
RN13 SRN10KJ-7GP
3D3V_S0 3D3V_S5
PCIE_CLK_RQ2# PEG_A_CLKRQ#
PCH_GPIO39 17
SUS_PWR_DN_ACK 14,36

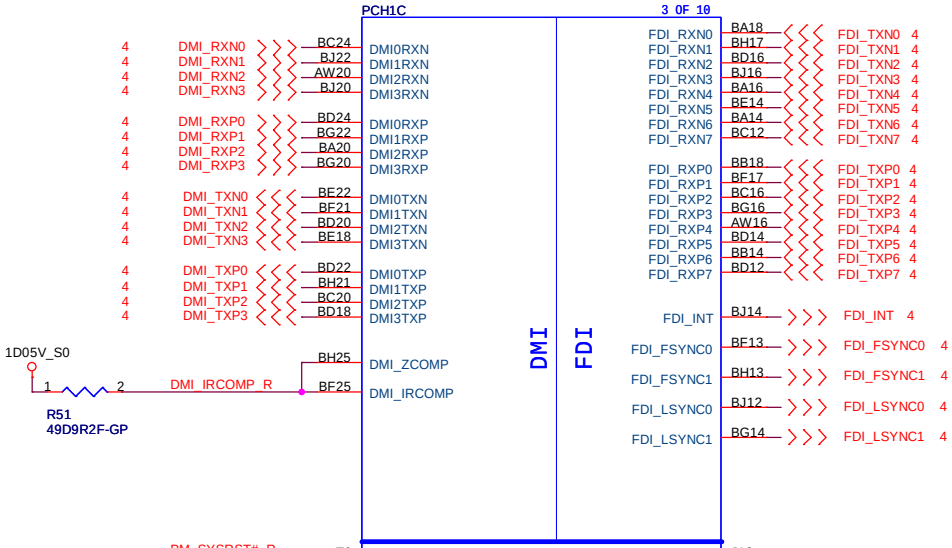
CLK_PCIE_LAN EC7 SC222P50V2JN-4GP
CLK_PCIE_LAN# EC5 SC222P50V2JN-4GP
CLK_PCI_FB EC12 SC222P50V2JN-4GP

SB Hosonic 改12P
ITTI C349 12P,C350 15P

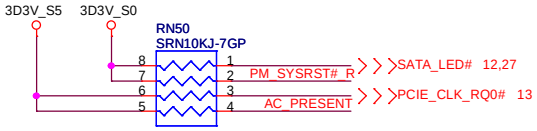
JV10-CS

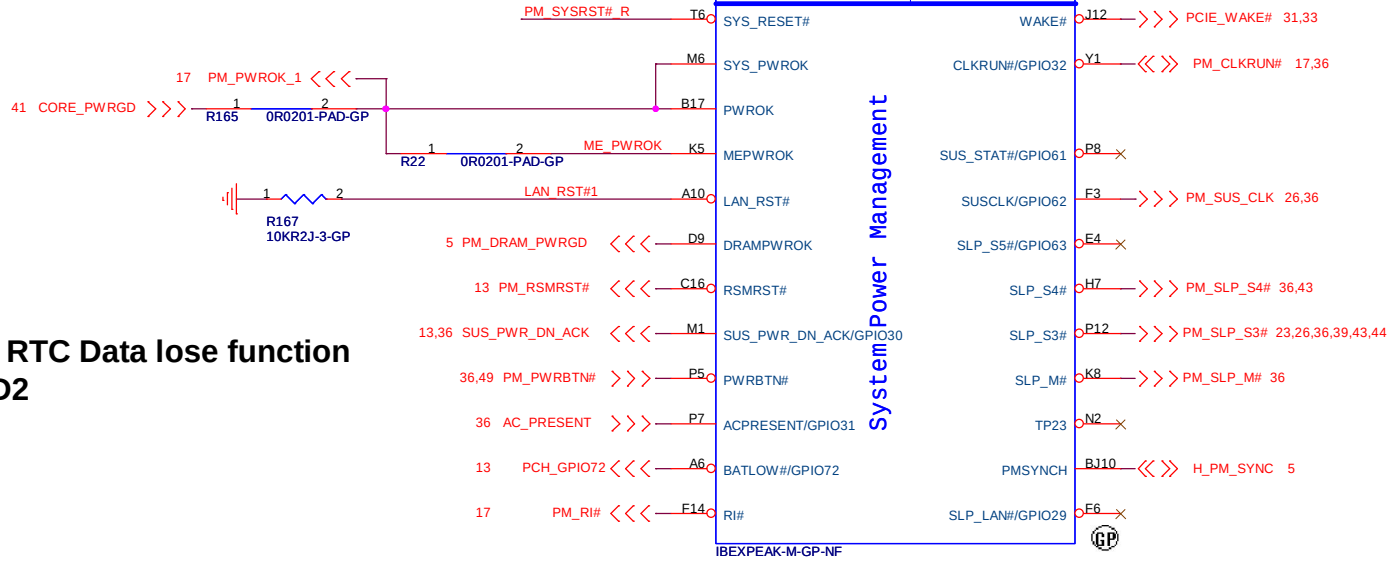
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH 2 of 9(PCIE/CLK/SMB)	
Size A3	Document Number JV10-CS	Rev -1
Date: Wednesday, February 10, 2010	Sheet 13 of 50	

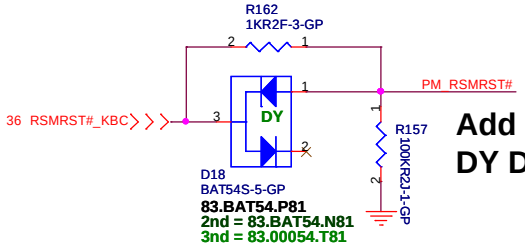




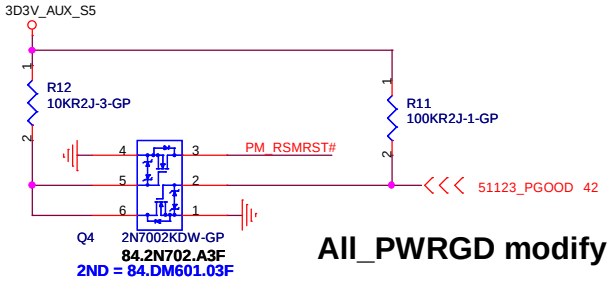
Delete PM_PWRBTN# pull high







Add RTC Data lose function
DY D2



All_PWRGD modify 51123_PGOOD from 3V/5V power

JV10-CS

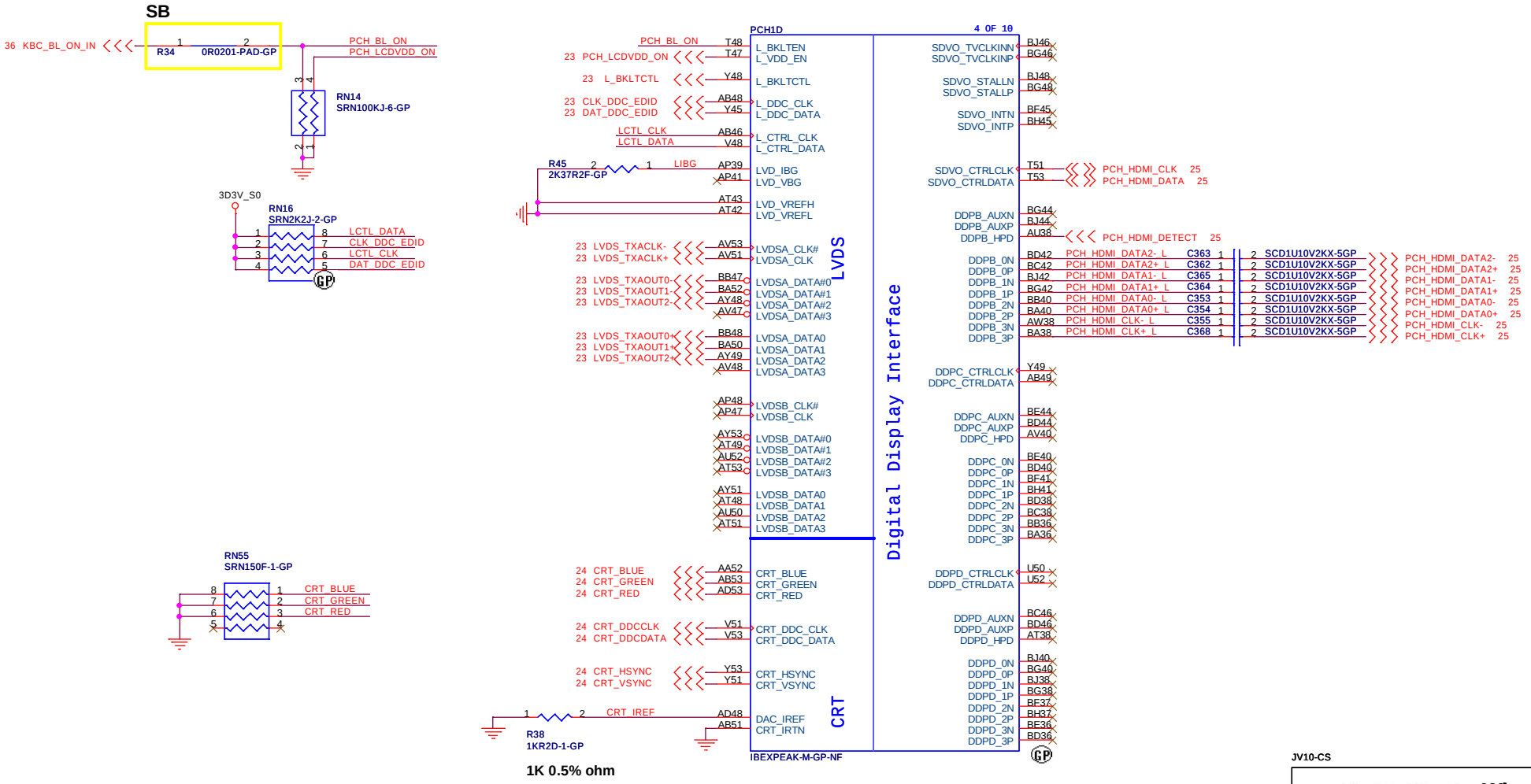
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 3 of 9(DMI/FDI)

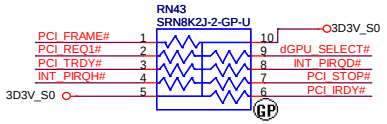
Size	Document Number	Rev
Custom	JV10-CS	-1

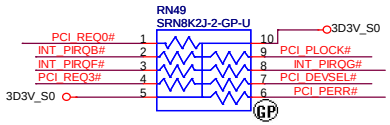
Date: Wednesday, February 10, 2010 Sheet 14 of 50

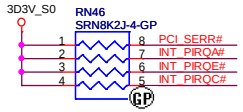
Panel backlight enable control for LVDS -
used to gate power into the backlight circuit

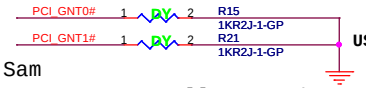


JV10-CS	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PCH 4 of 9(LVDS/CRT/DP)
Size: Custom	Document Number: JV10-CS
Rev	-1
Date: Wednesday, February 10, 2010	Sheet 15 of 50







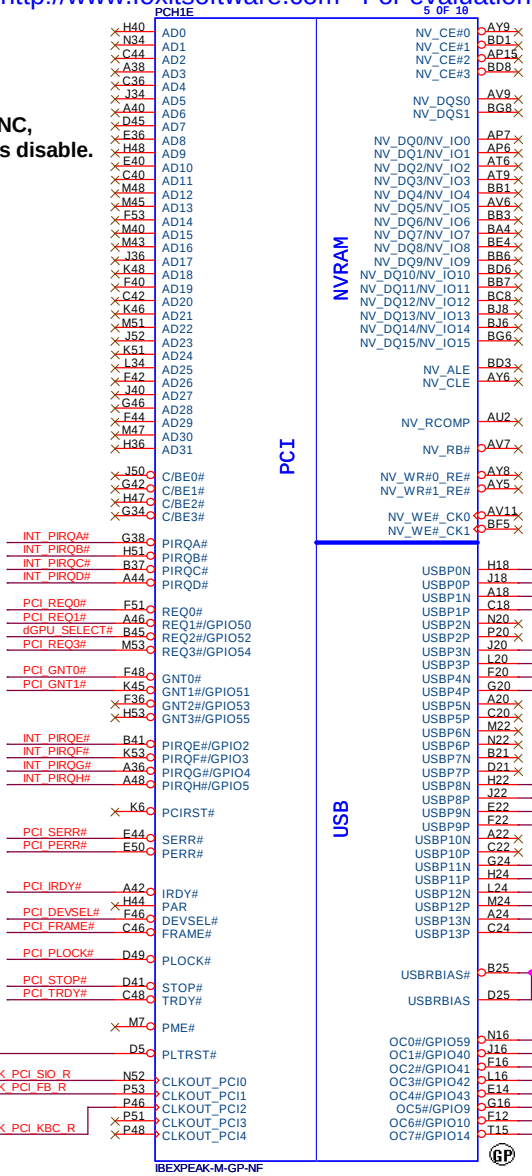


Sam

3D3V_S0 Pull up 8.2k?

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

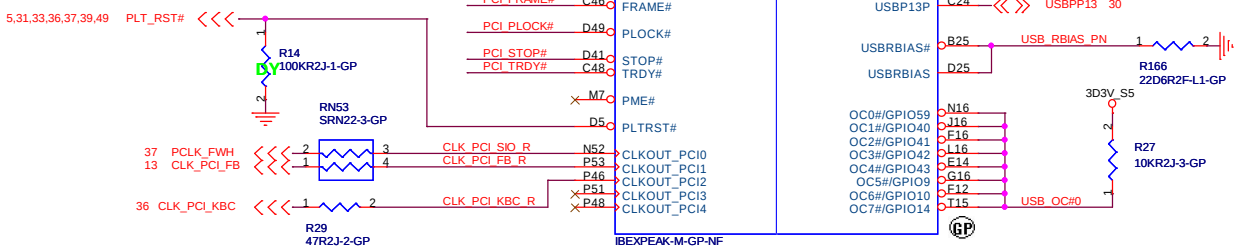
These pins are left as NC, because the function is disable.

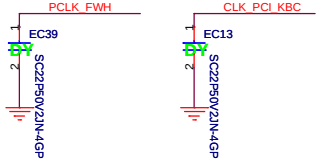


These pins are left as NC, because the function is disable.

USB Table

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1
4	WECAM
5	NC
6	NC
7	NC
8	3G
9	USB1(HS)
10	NC
11	Blue Tooth
12	MINIC2(3G)
13	Cardreader





JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH 5 of 9(PCI/USB)**

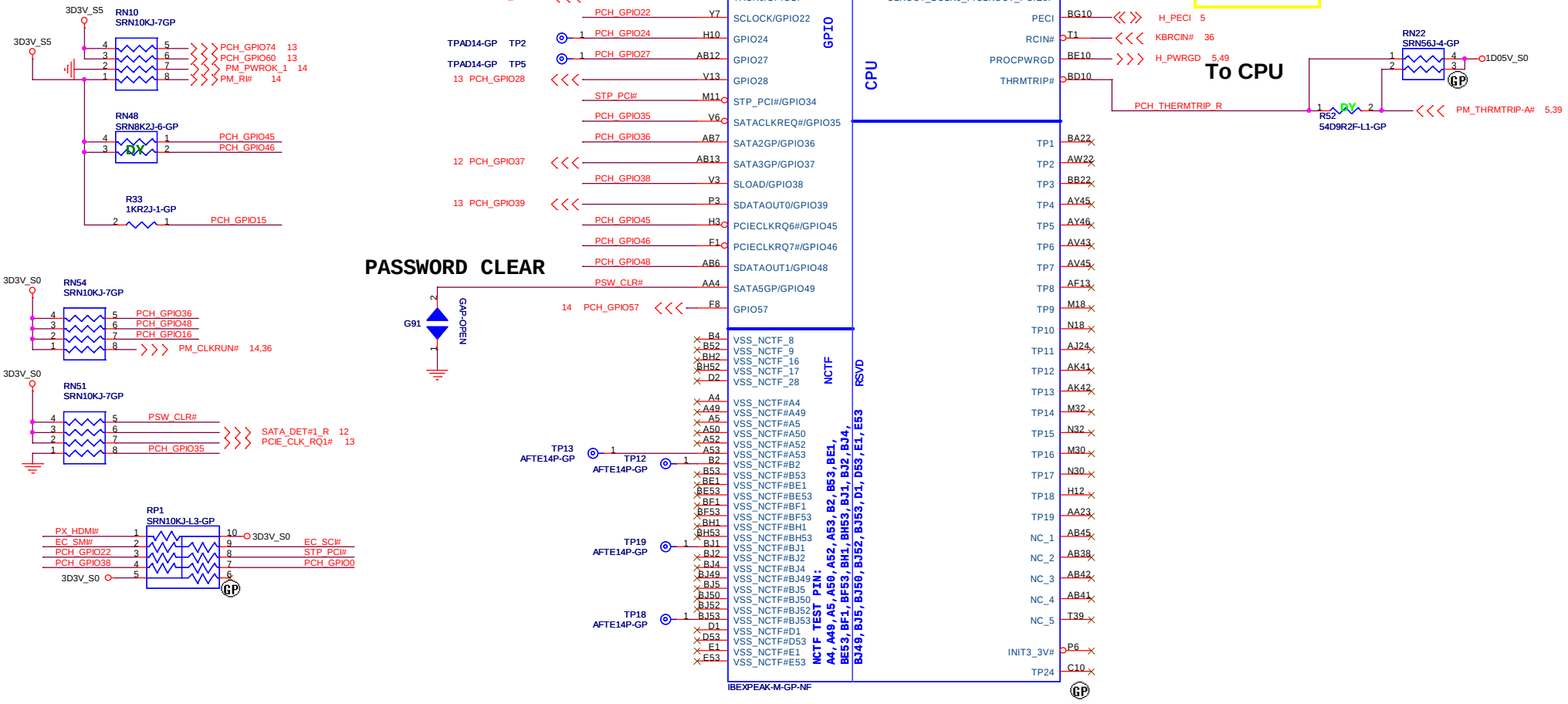
Size	Document Number	Rev
A3	JV10-CS	-1

Date: Wednesday, February 10, 2010 Sheet 16 of 50

GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



JV10-CS

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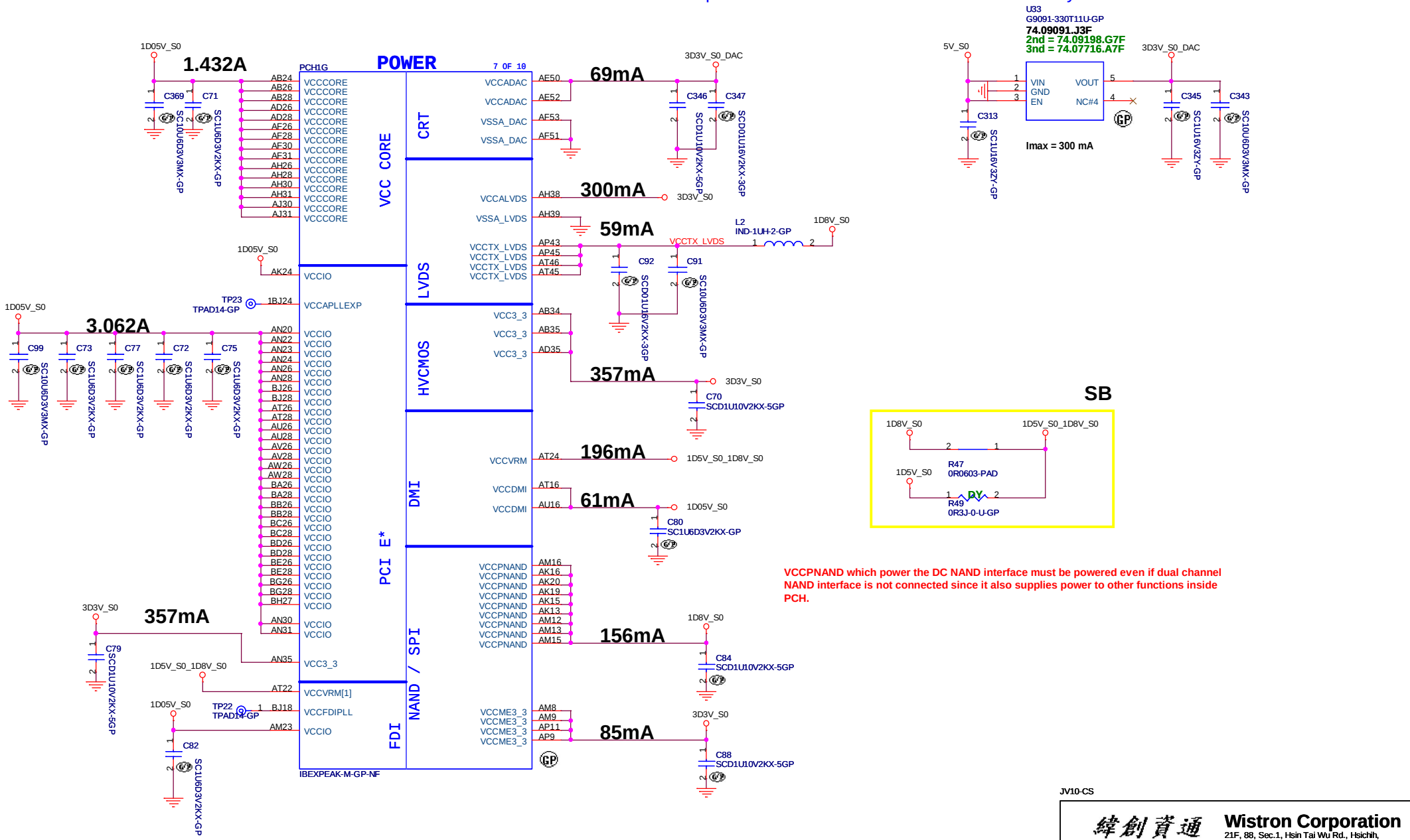
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 6 of 9(GPIO/RSVD)

Size: A3 | Document Number: JV10-CS | Rev: -1

Date: Wednesday, February 10, 2010 | Sheet 17 of 50



JV10-CS

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PCH 7 of 9(PWR/VCORE/LVDS)
Size: Custom	Document Number: JV10-CS
Rev: -1	
Date: Wednesday, February 10, 2010	Sheet 18 of 50

POWER

PCH1J

10 OF 10

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | PCI/GPIO/LPC | CPU | RTC | HDA

1.849A

68mA

69mA

-1

163mA

1mA

1mA

-1

1D05V_VCCA_A_DPL

1D05V_VCCA_B_DPL

+VCCSST

RTC_AUX_S5

5VALW_PCH_VCCSREFSUS

5VS_PCH_VCCSREF

IBEXPEAK-M-GP-NF

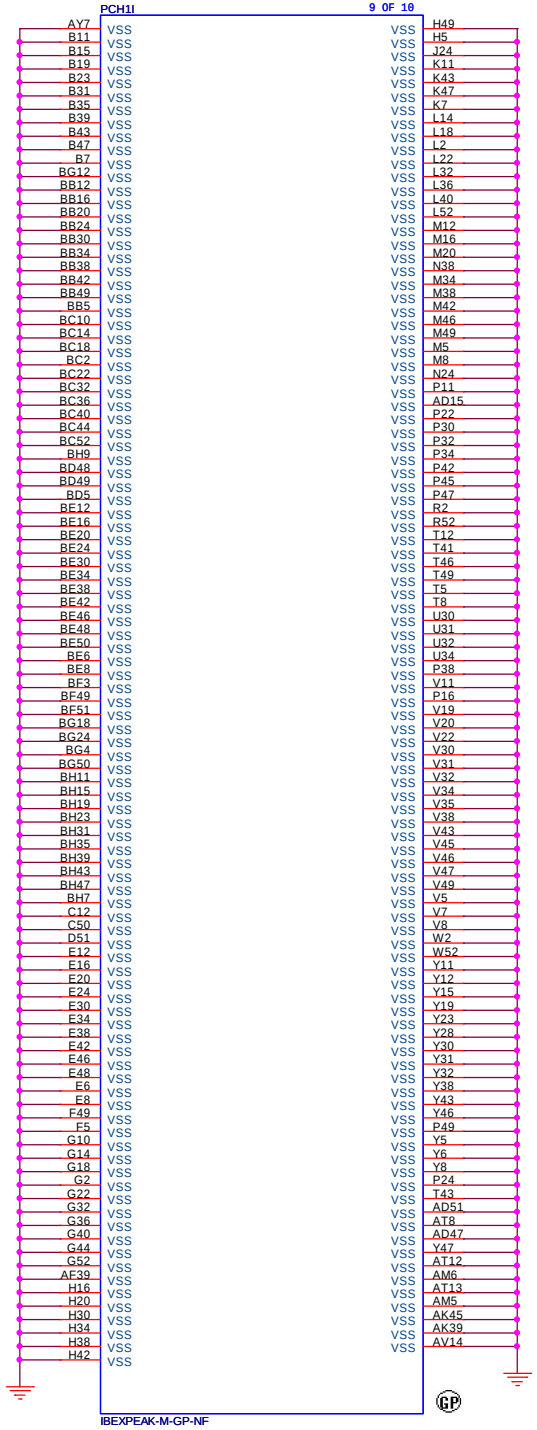
JV10-CS

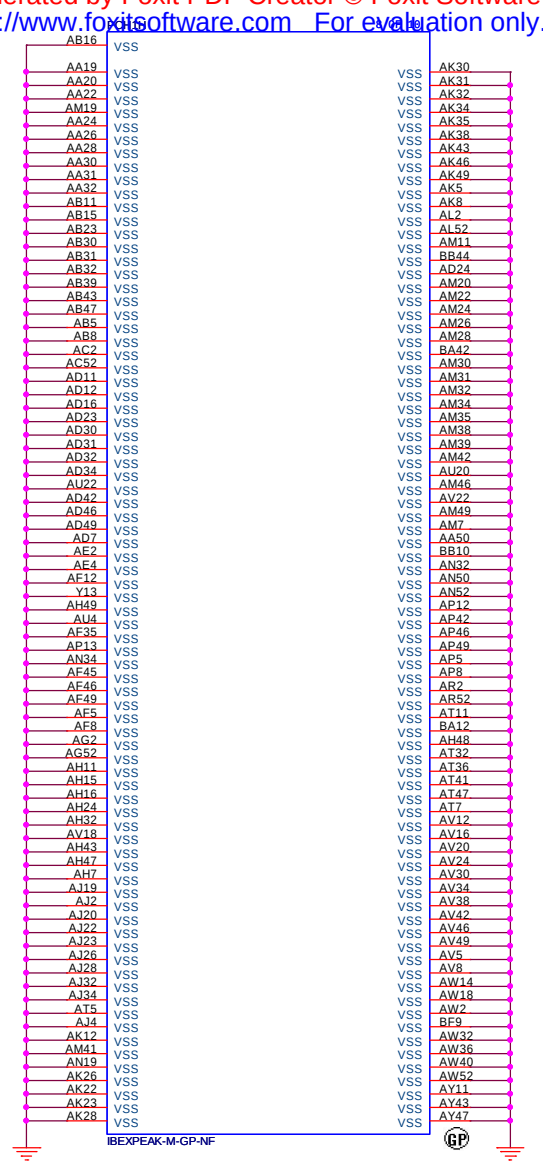
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 8 of 9(PWR\SATA\USB)

Size: Custom | Document Number: JV10-CS | Rev: -1

Date: Wednesday, February 10, 2010 | Sheet 19 of 50





JV10-CS

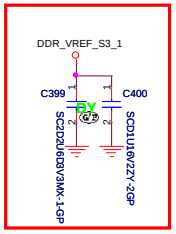
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH 9 of 9(VSS)	
Size A3	Document Number JV10-CS	Rev -1
Date: Wednesday, February 10, 2010	Sheet 20 of 50	

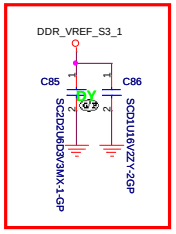
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

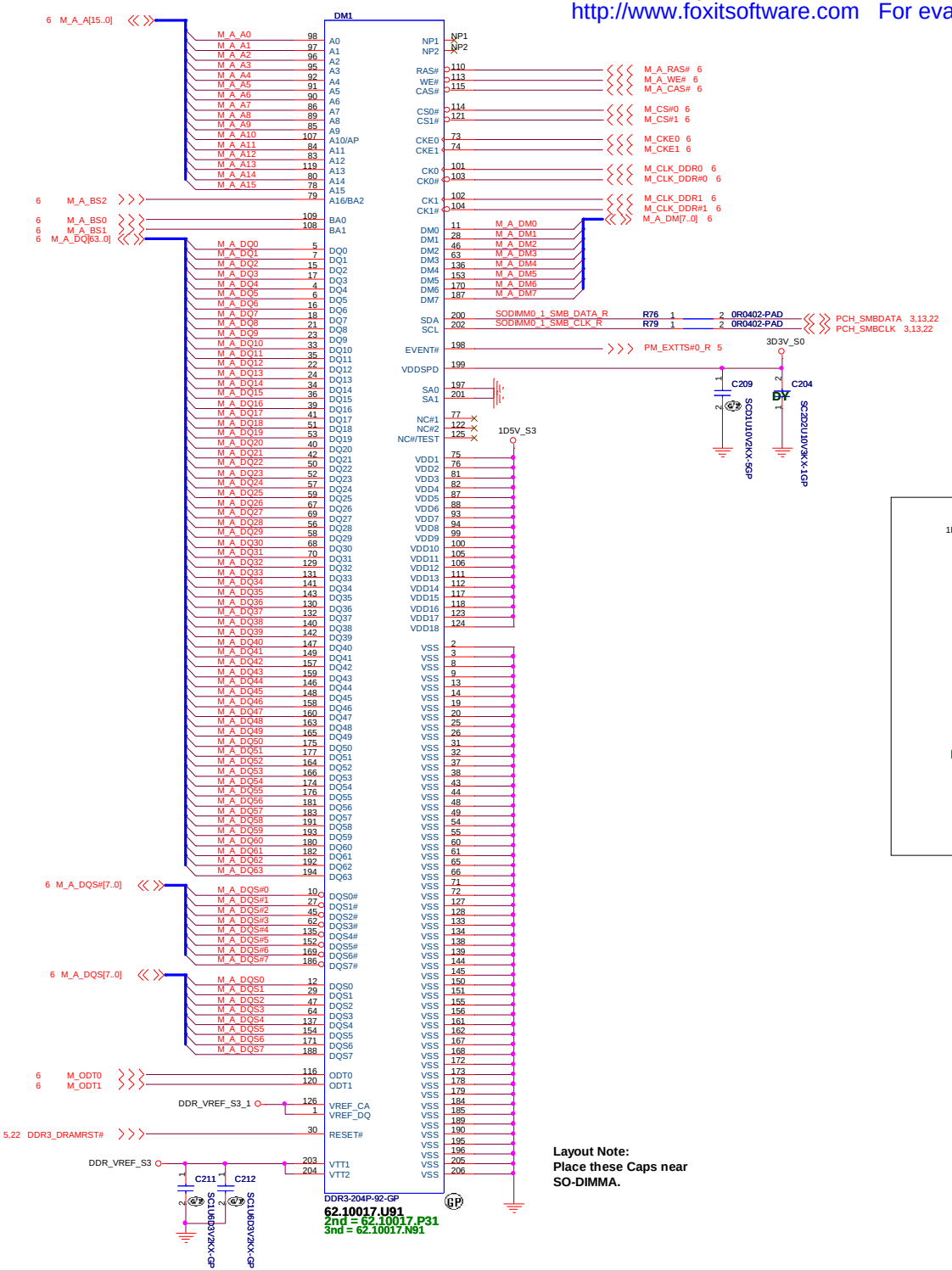
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Layout Note：Near Pin 126

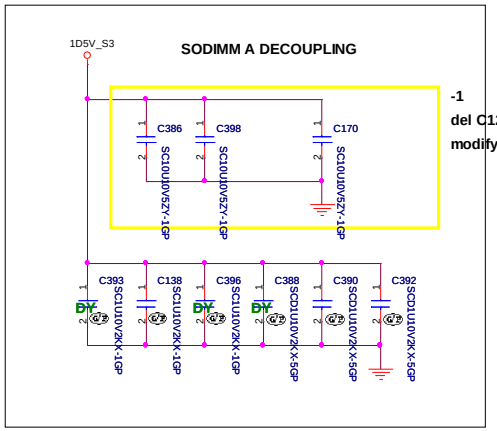


Layout Note：Near Pin 1





Layout Note:
Place these Caps near SO-DIMMA.



-1
del C129 C183
modify C386,C398,C170

JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR3 SODIMM1	
Size: Custom	Document Number: JV10-CS	Rev: -1
Date: Wednesday, February 10, 2010	Sheet 21 of 50	

DM2

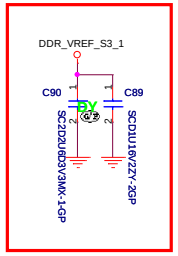
REVERSE TYPE

DDR3-204P-41-GP-U

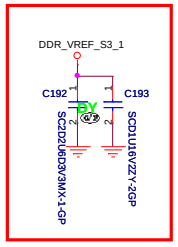
62.10017.N41
2nd = 62.10017.P41
3nd = 62.10017.V01

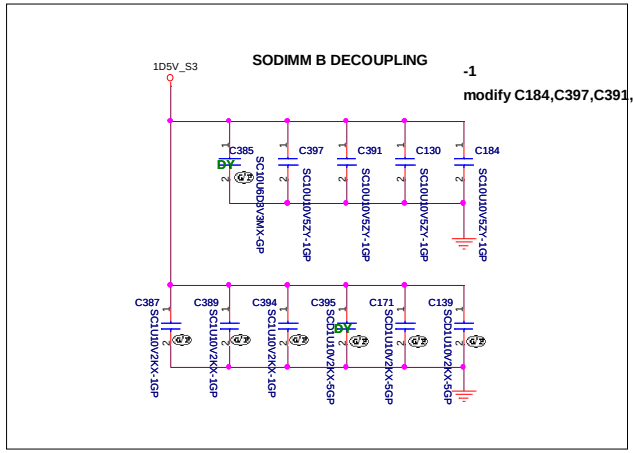
H = 5.2mm

Layout Note：Near Pin 1



Layout Note：Near Pin 126

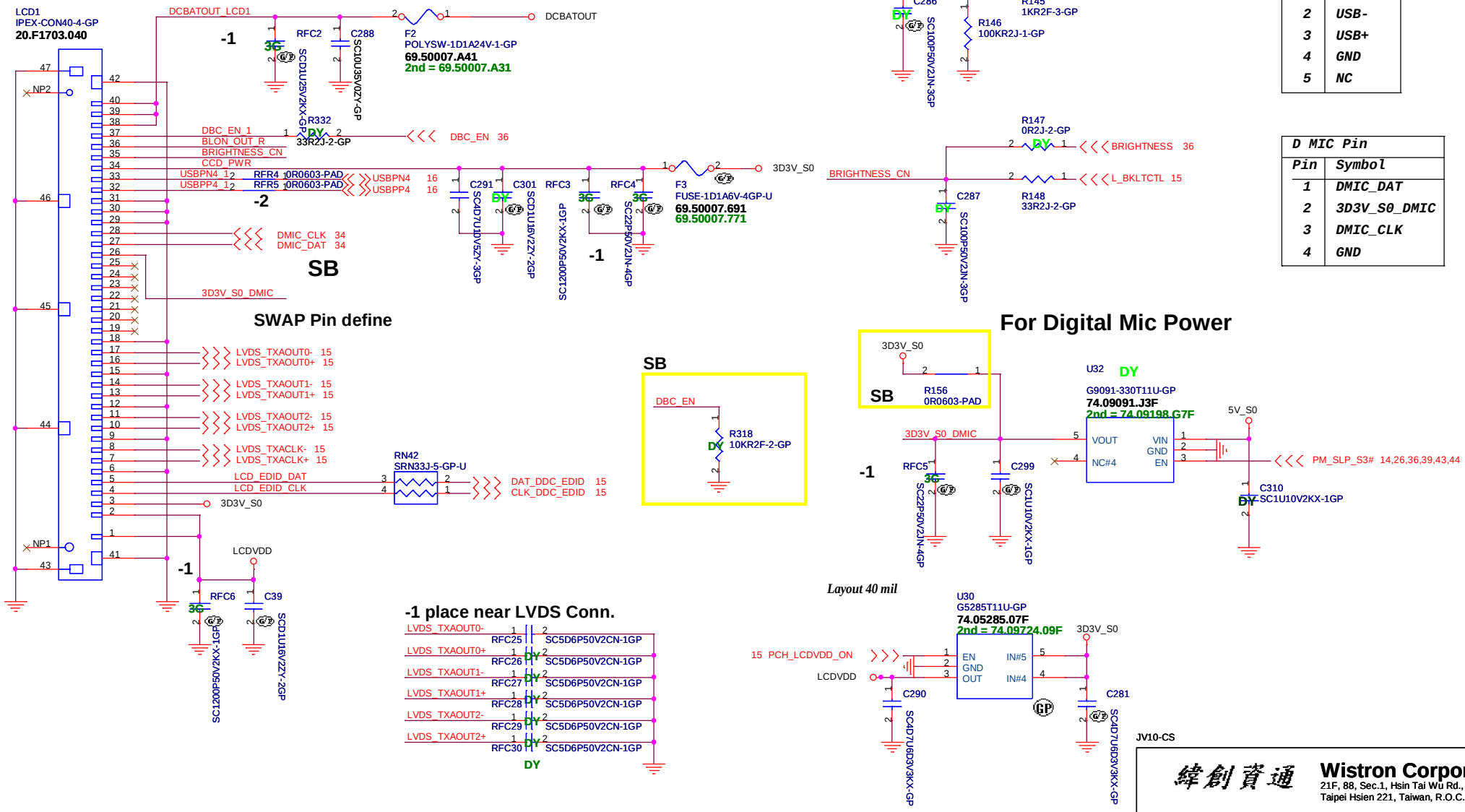




JV10-CS		
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR3 SODIMM2		
Size: Custom	Document Number: JV10-CS	Rev: -1
Date: Wednesday, February 10, 2010	Sheet 22 of 50	

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	NC

D MIC Pin	
Pin	Symbol
1	DMIC_DAT
2	3D3V_S0_DMIC
3	DMIC_CLK
4	GND



JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

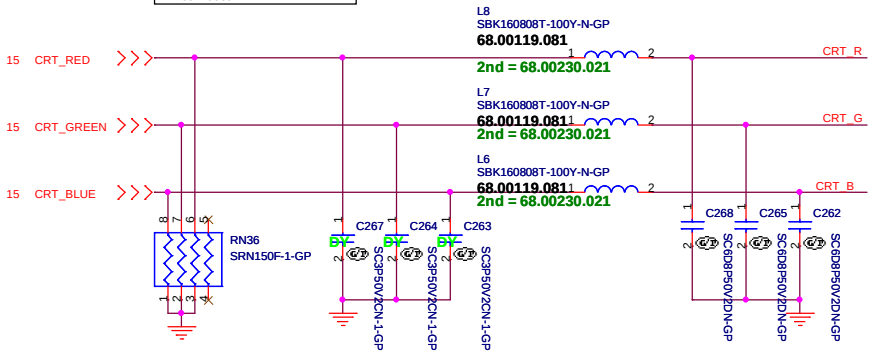
Title: LCD CCD CONN

Size	Document Number	Rev
Custom	JV10-CS	-1

Date: Wednesday, February 10, 2010 Sheet 23 of 50

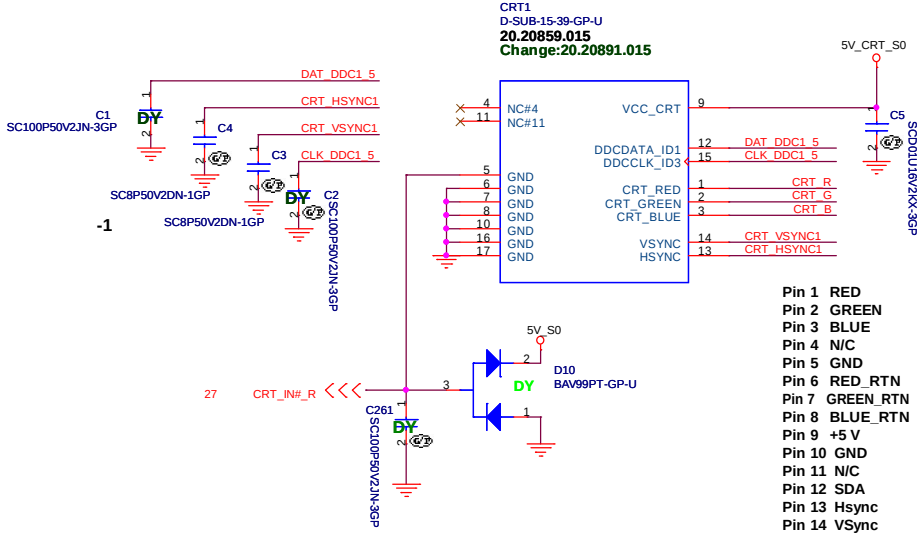
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz



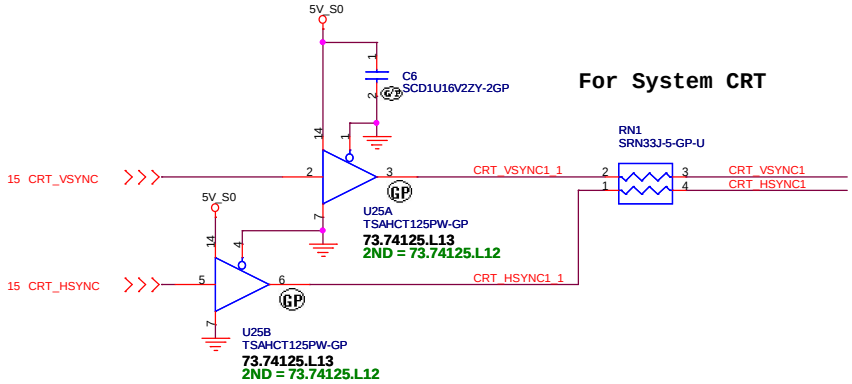
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

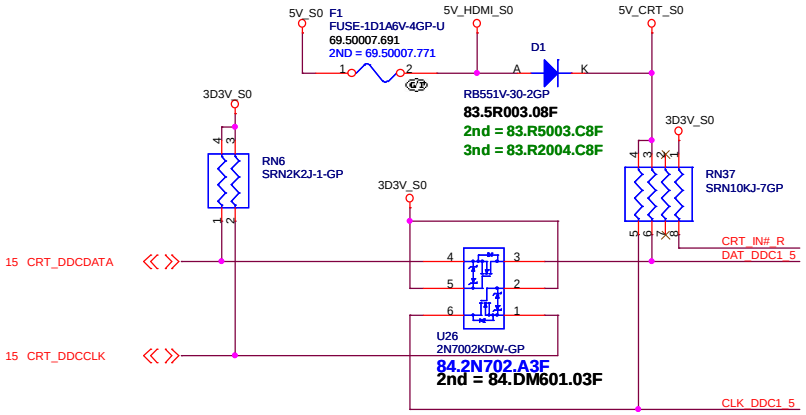


Pin 1 RED
Pin 2 GREEN
Pin 3 BLUE
Pin 4 N/C
Pin 5 GND
Pin 6 RED_RTN
Pin 7 GREEN_RTN
Pin 8 BLUE_RTN
Pin 9 +5 V
Pin 10 GND
Pin 11 N/C
Pin 12 SDA
Pin 13 Hsync
Pin 14 VSync
Pin 15 SCL

Hsync & Vsync level shift



DDC_CLK & DATA level shift

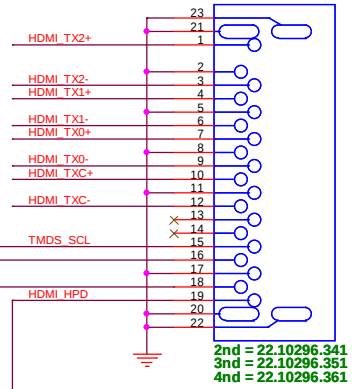


JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CRT conn**	
Size A3	Document Number **JV10-CS**	Rev **-1**
Date: Thursday, February 11, 2010	Sheet 24 of 50	

HDMI CONNECTOR

HDMI1
SKT-HDMI19P-20-GP-U
22.10296.051



2nd = 22.10296.341
3nd = 22.10296.351
4nd = 22.10296.361

Pin 1 TMDS Data2+
Pin 2 TMDS Data2 Shield
Pin 3 TMDS Data2–
Pin 4 TMDS Data1+
Pin 5 TMDS Data1 Shield
Pin 6 TMDS Data1–
Pin 7 TMDS Data0+
Pin 8 TMDS Data0 Shield
Pin 9 TMDS Data0–
Pin 10 TMDS Clock+
Pin 11 TMDS Clock Shield
Pin 12 TMDS Clock–
Pin 13 CEC
Pin 14 Reserved (N.C. on device)
Pin 15 SCL
Pin 16 SDA
Pin 17 DDC/CEC Ground
Pin 18 +5 V Power (max 50 mA)
Pin 19 Hot Plug Detect

EC40 SC220P50V2JN-3GP
EC41 SC220P50V2JN-3GP

C309 C46 C56 C53 C42 SCD01U50V2KX-1GP / SCD01U16V2ZY-2GP

RN52 SRN2K2J-2-GP

D5 BAV99PT-GP-U

R48 20KR2J-L2-GP

Q5 2N7002-11-GP
84.27002.W31

HDMI in : Hi
HDMI out : Low

U34
PS8101-GP
71.P8101.003
2ND = 71.03411.B03

Recommended Equalization: [PC1,PC0]=01, 4dB

R32 4K7R2J-2-GP
R28 5K1R2F-2-GP
R196 499R2F-2-GP
R30 100KR2J-1-GP

RN15 SRN4K7J-10-GP

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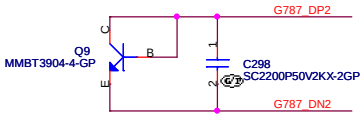
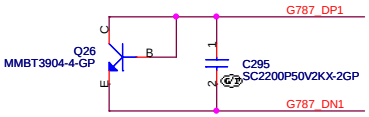
Title: HDMI conn	
Size: Custom	Document Number: JV10-CS	Rev: -1
Date: Wednesday, February 10, 2010	Sheet 25 of 50	

JV10-CS

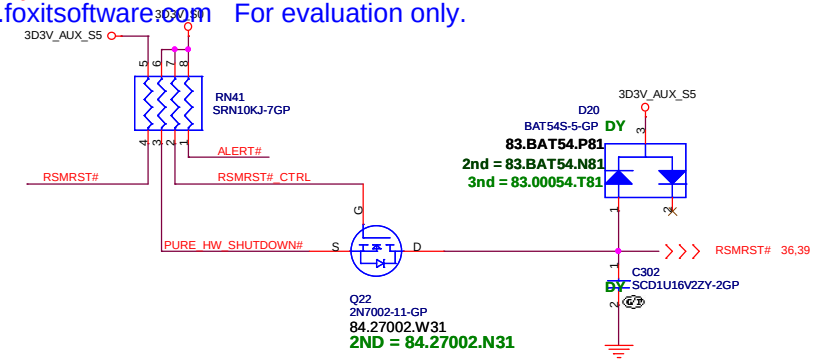
For T8 thermal diode



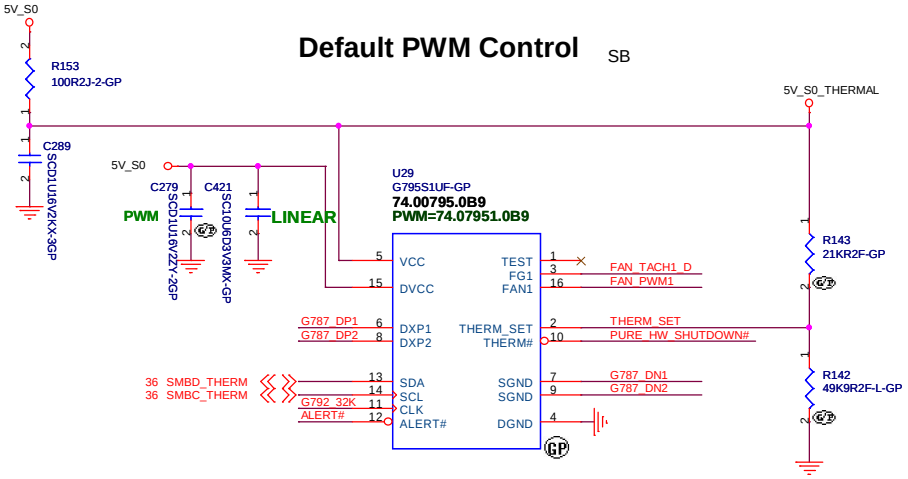
For System thermal diode



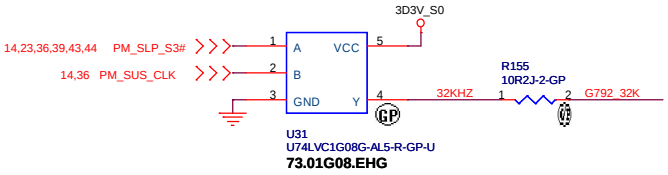
C298& C295 CLOSE to G795



Default PWM Control SB



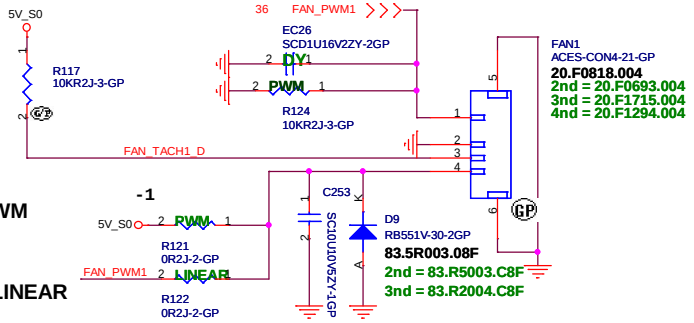
T8=90C
THERM_SET = [(Tset-72) x 0.02+0.34] x VCC



CPU FAN Connector

PWM FAN		LINEAR FAN	
PIN1	PWM	PIN1	NC
PIN2	GND	PIN2	GND
PIN3	FG	PIN3	FG
PIN4	VCC	PIN4	VCC

PWM FOR EC



JV10-CS

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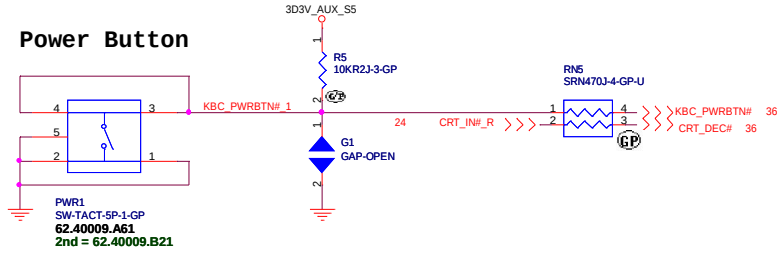
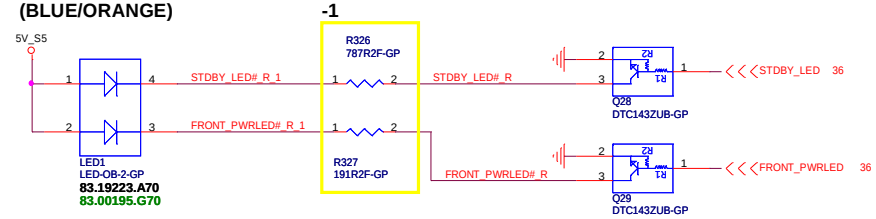
Taipei Hsien 221, Taiwan, R.O.C.

Title	Thermal/Fan Conn	
Size A3	Document Number JV10-CS	Rev -1
Date: Wednesday, February 10, 2010	Sheet 26 of 50	

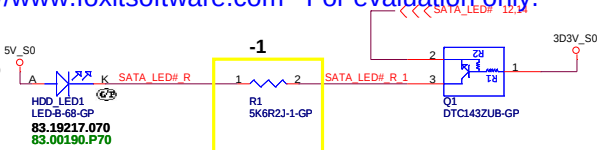
Power Button



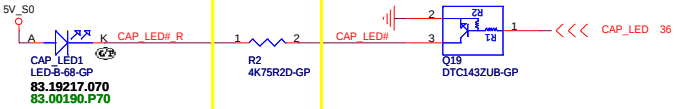
Power Button LED
(BLUE/ORANGE)



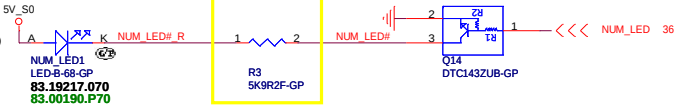
HDD LED
(BLUE)



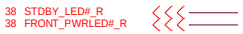
CAP LED
(BLUE)



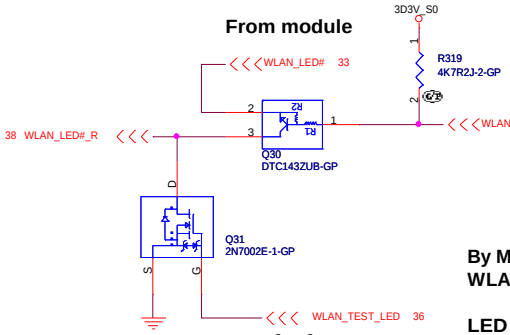
NUM LED
(BLUE)



To USBCN1 Connector



From module



for factory test

From KBC

Delete ALL LED OFF

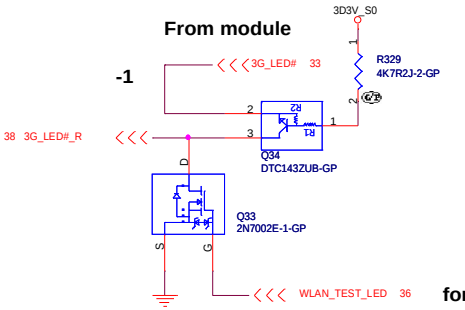
ALL LED OFF GPIO14 change WLAN_LED
WLAN_LED GPIO81 change WLAN_TEST_LED

By Module (LED Flash)
WLAN_LED_OFF# High

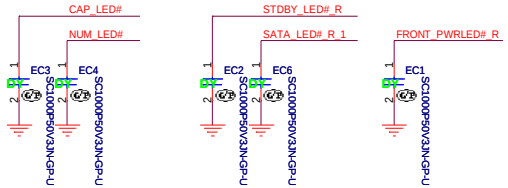
LED Always On
WLAN_LED_OFF# Low
WLAN_TEST_LED High

Factory test use
WLAN_TEST_LED High

From module



for factory test



JV10-CS

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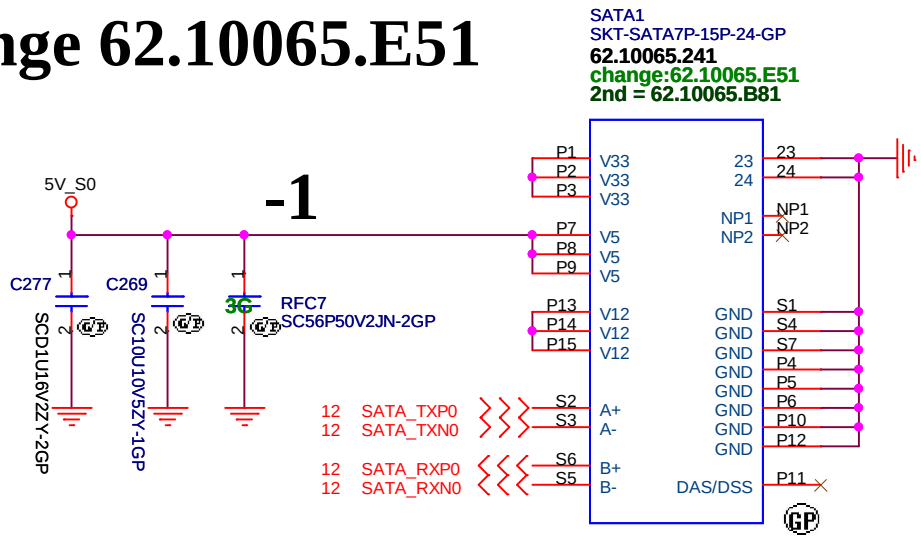
Title: **LED**

Size	Document Number	Rev
Custom	**JV10-CS**	-1

Date: Thursday, February 11, 2010 Sheet 27 of 50

SATA Connector

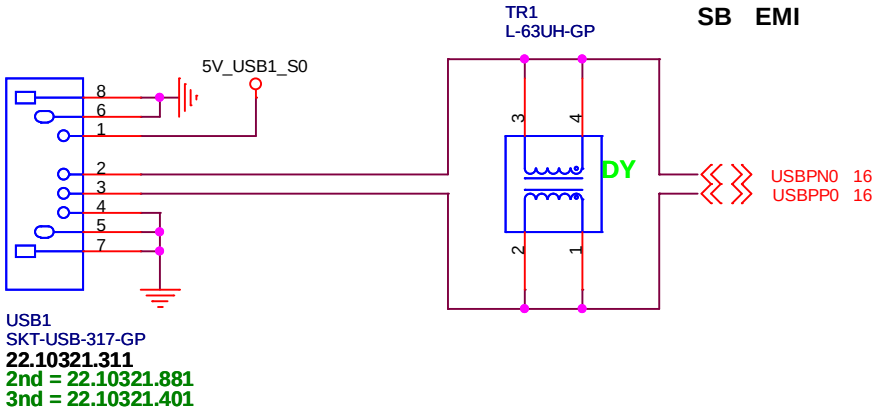
change 62.10065.E51

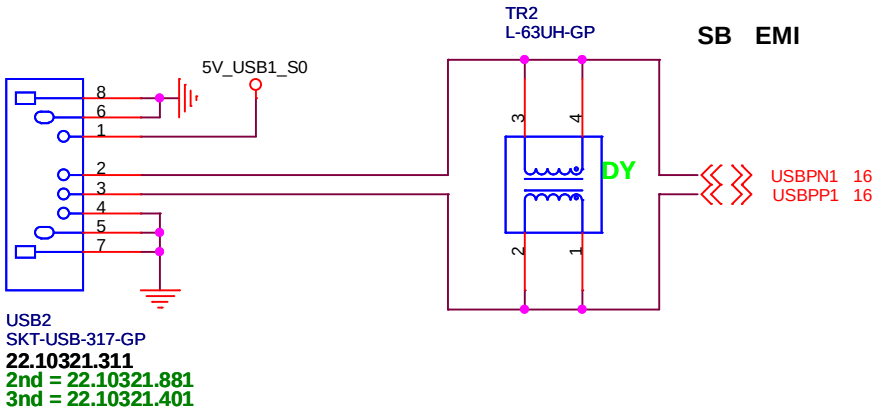


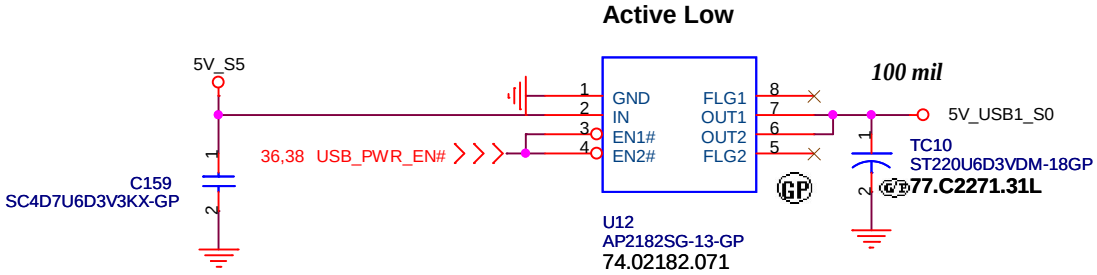
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD***	
Size A4	Document Number JV10-CS	Rev *-1*
Date: Wednesday, February 10, 2010	Sheet 28 of 50	

USB MODULE







USB Port_LED Function

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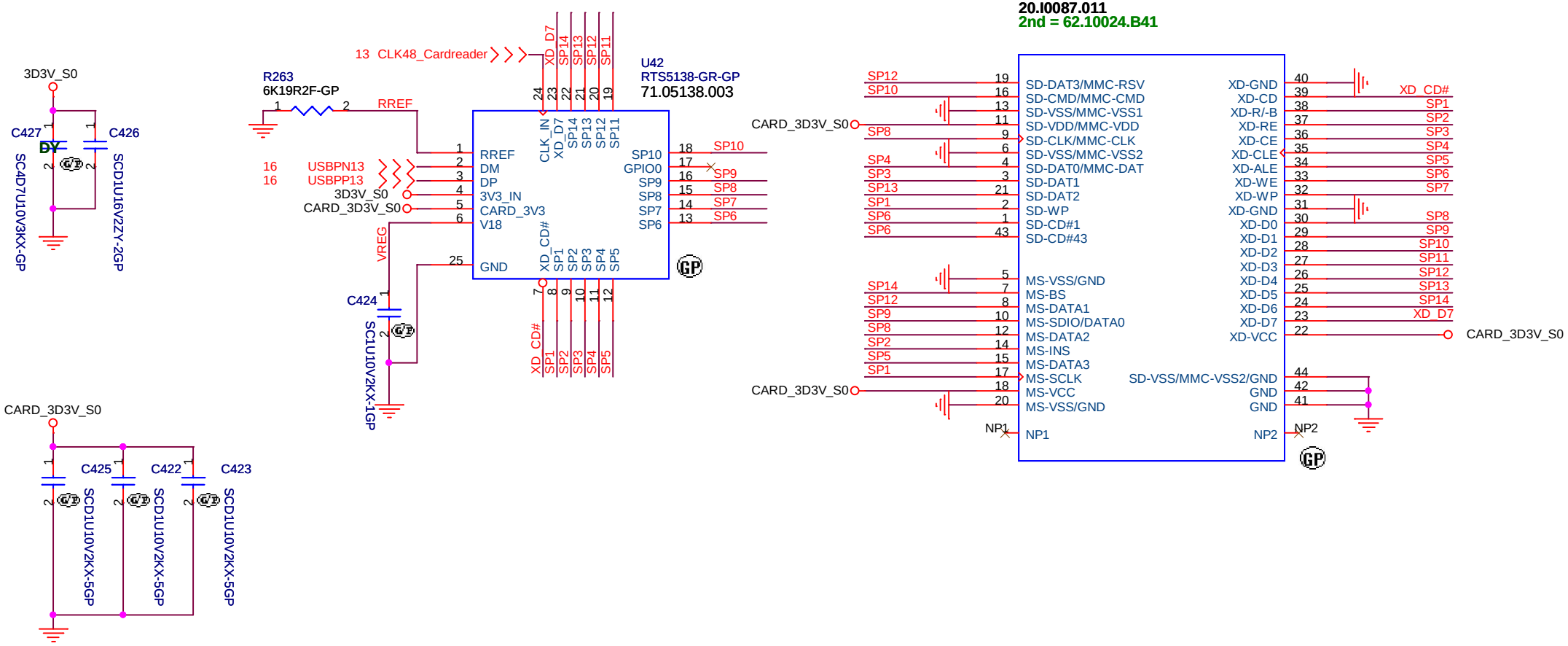
Title: *USB Port*		
Size: A4	Document Number: JV10-CS	Rev: -1
Date: Wednesday, February 10, 2010	Sheet 29 of 50	

5 IN1 CARD-READER

SB
與 ALPS Co-Layout



Near CARD1 Pin11, Pin18, Pin22

Audio Jack_CardReader

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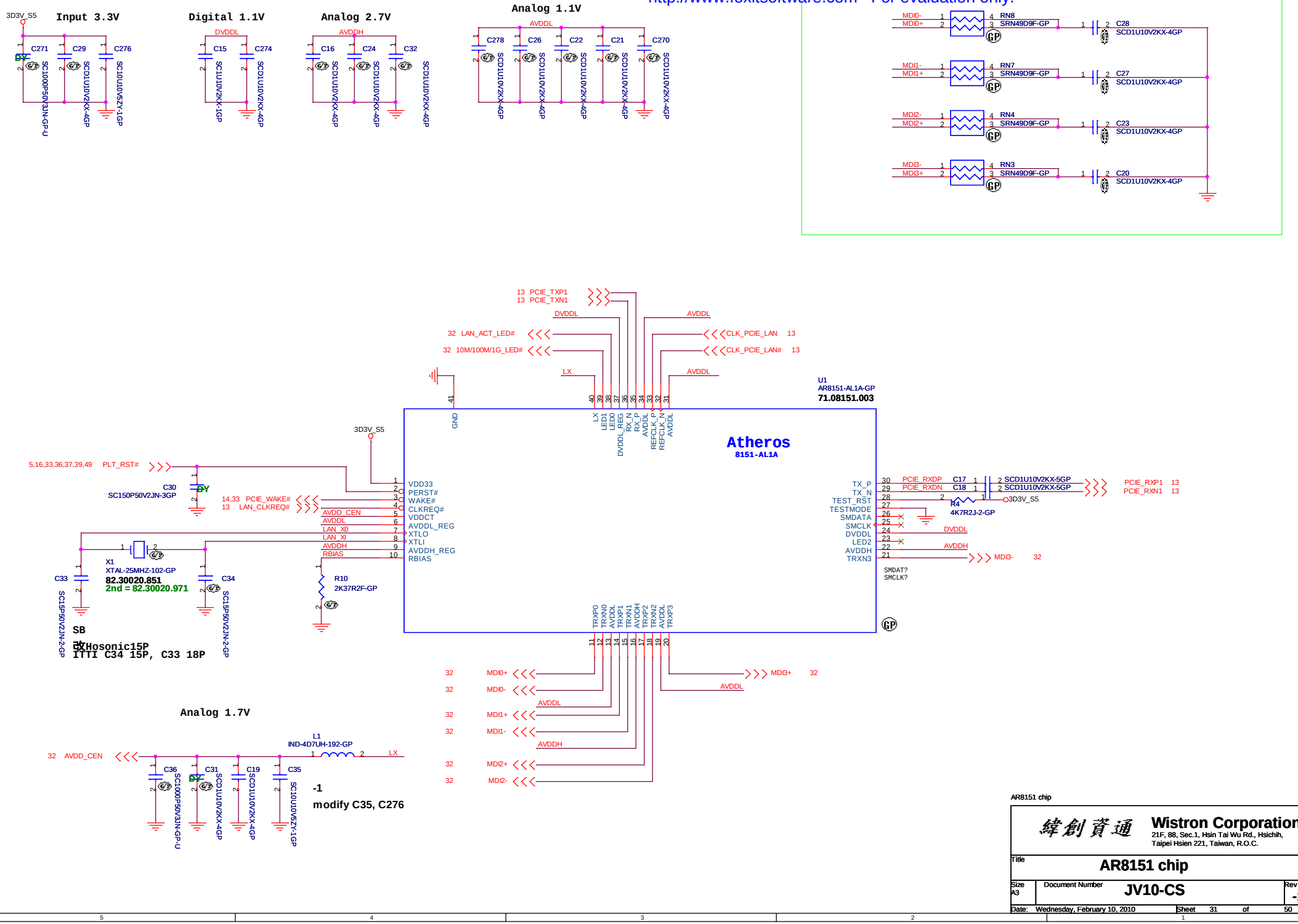
Title	***CARDREADER***	
Size A4	Document Number JV10-CS	Rev -1
Date: Thursday, February 11, 2010	Sheet 30 of 50	



AR8151 chip

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Taipei Hsien 221, Taiwan, R.O.C.

Title	AR8151 chip	
Size A3	Document Number JV10-CS	Rev -1
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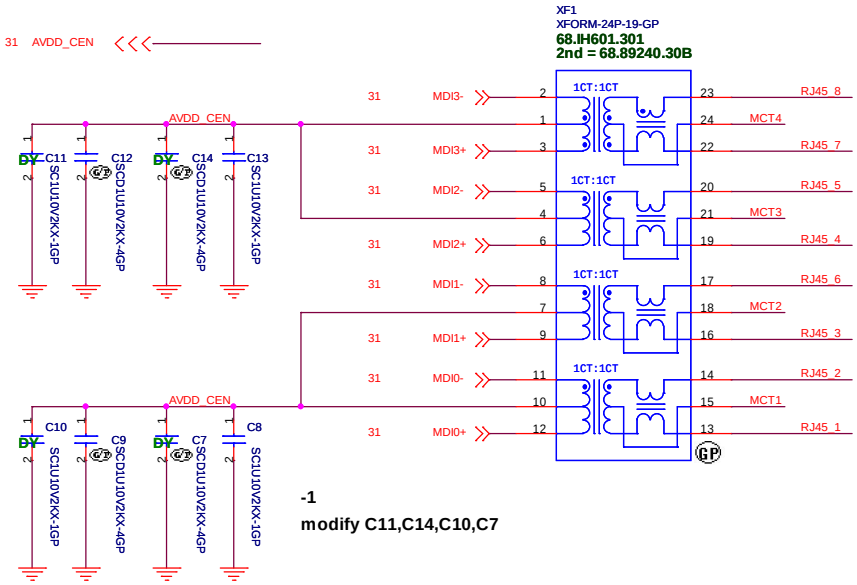
LAN Connector

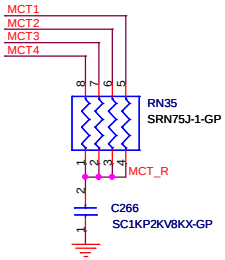
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

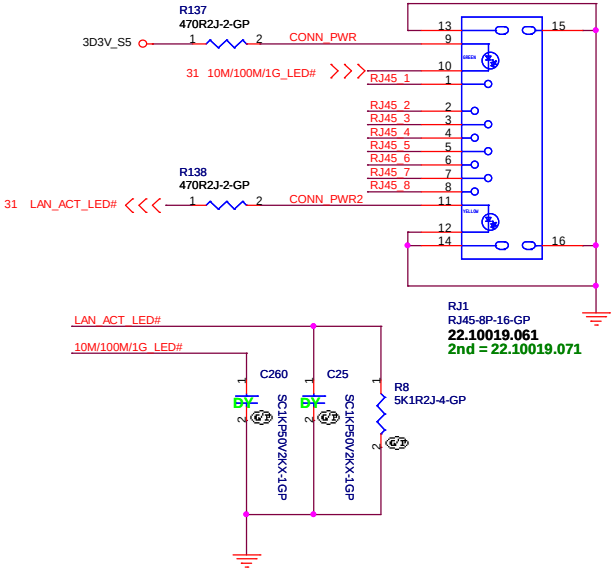
GIGA Lan Transformer



-1

modify C11,C14,C10,C7





LED COLOR

B1(+) B2(-)::GREEN

A1(+) A2(-):YELLOW

Green(A3), behavior is the same for 10/100/1000 bits

Yellow(B2), when LAN is transfering data.

LAN Connector

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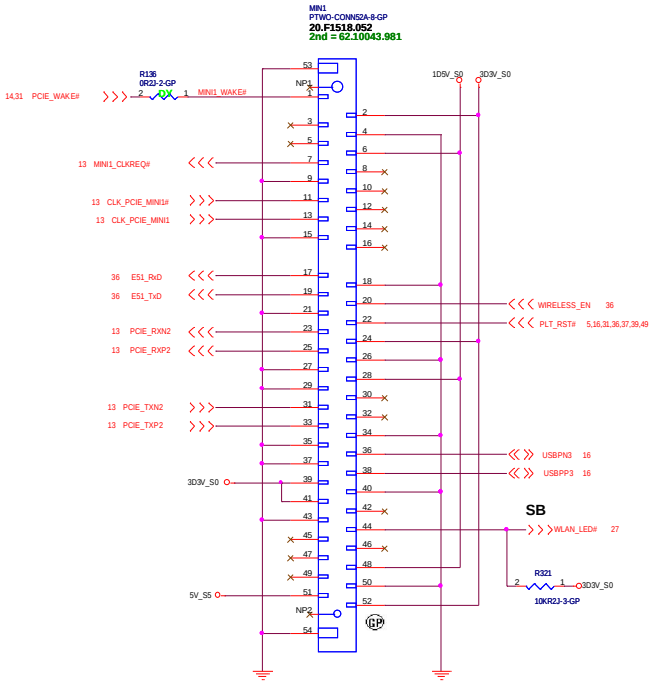
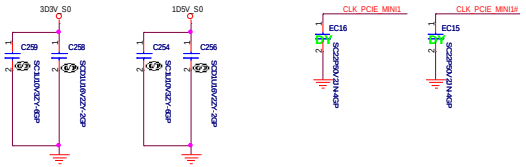
Title: LAN Connector		
Size: A3	Document Number: JV10-CS	Rev: -1
Date: Thursday, February 11, 2010	Sheet 32 of 50	

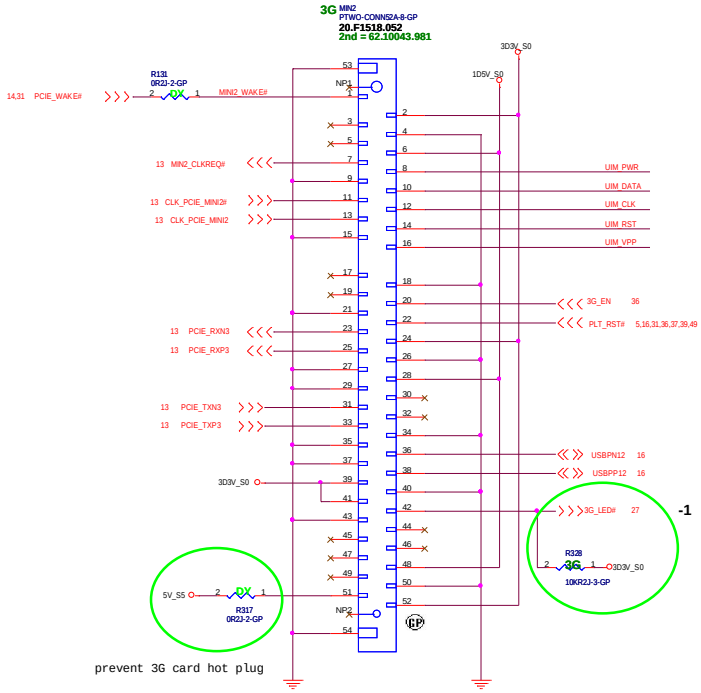
Mini Card Connector(WLAN)
Support debug-card



Place near MINI1

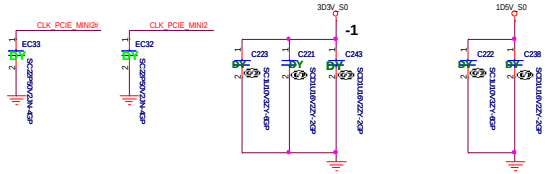


Mini Card Connector(3G)

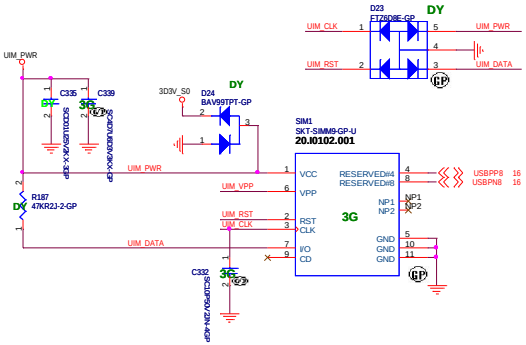


prevent 3G card hot plug

Place near MINIC2

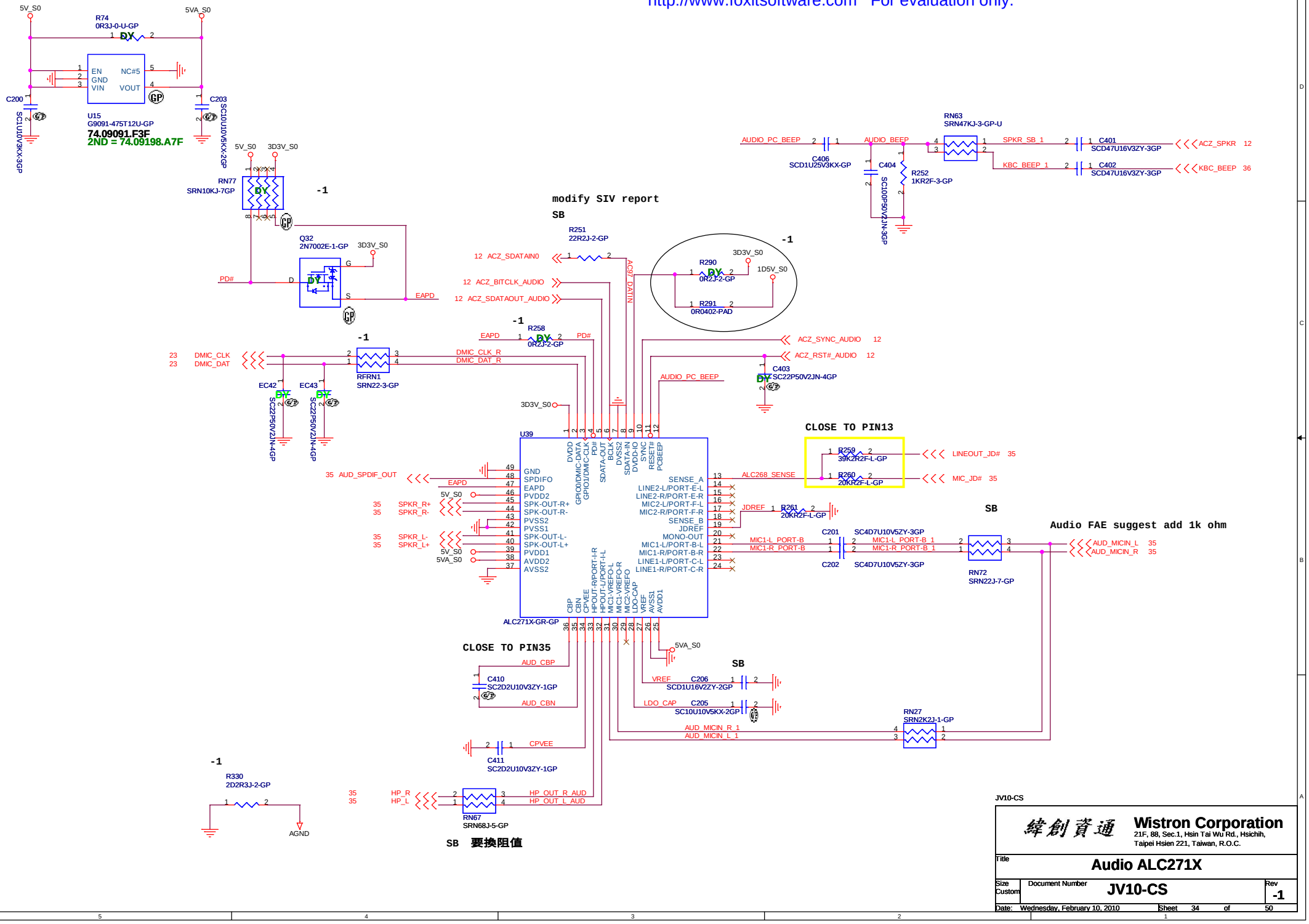


SIM Card



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI Conn	
Size: Custom	Document Number: JV10-CS	Rev: -1
Date: Wednesday, February 10, 2010	Sheet 33 of 50	



JV10-CS

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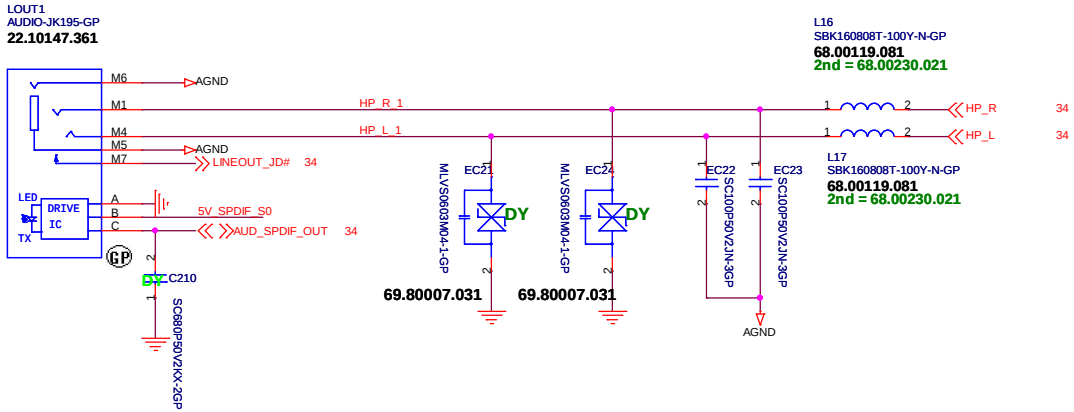
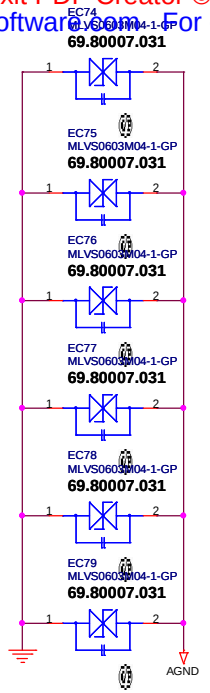
Title: Audio ALC271X		
Size: Custom	Document Number: JV10-CS	Rev: -1
Date: Wednesday, February 10, 2010	Sheet 34 of 50	

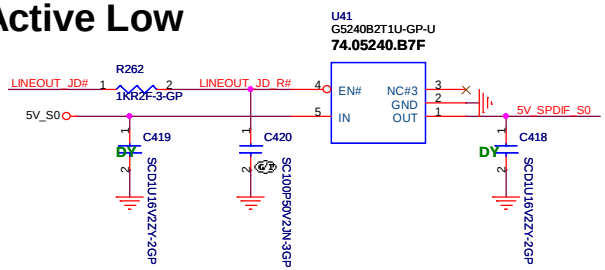
LINE OUT

SB

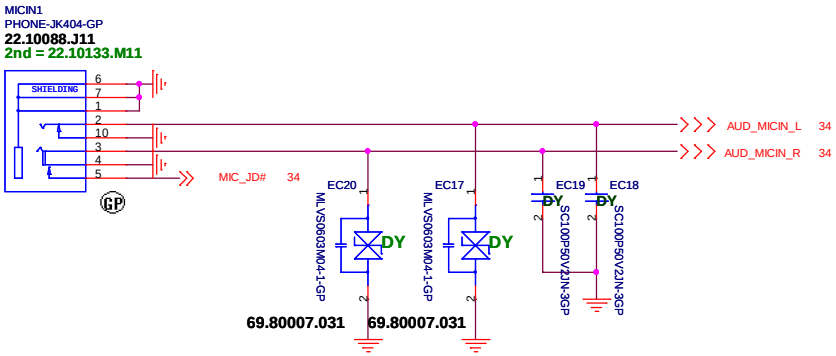




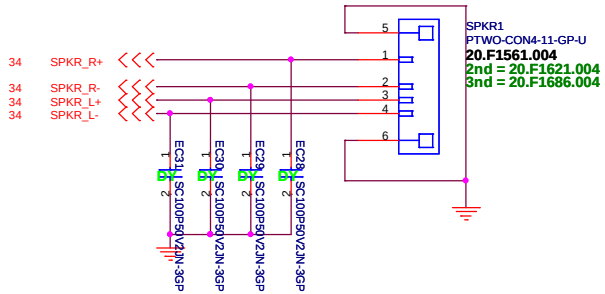
Active Low



MIC IN



Internal Speaker



Audio Jack_CardReader

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Audio Jack/Mic In/ SPKR*	
Size A3	Document Number JV10-CS	Rev -1
Date: Thursday, February 11, 2010	Sheet 35 of 50	

PCB Version		
	Pull-Low	Pull-High
SA	10K	1K
SB	10K	2K
-1	10K	3K
-2	10K	4.7K

Internal KeyBoard Connector

KB1 PTWO-CON24-1-GP
20.K0391.024
2nd = 20.K0320.024

-1
Change 掀蓋式下接觸

D7 BAT54S-5-GP
83.BAT54.P81
2nd = 83.BAT54.N81
3nd = 83.00054.T81

To Vcore

THERMAL ----->
BATTERY ----->

SB

From 1.05V_S0

From PCH

change 上件

SB
add U43 For BIOS data lose

SB

FOR KBC DEBUG

U21A NPCE781BA0DX-GP
U21B NPCE781BA0DX-GP
U43 G690L293T73UF-GP 74.00690.I7B
Q21 2N7002KDW-GP 84.2N702.A3F
Q15 MMBT3906-4-GP

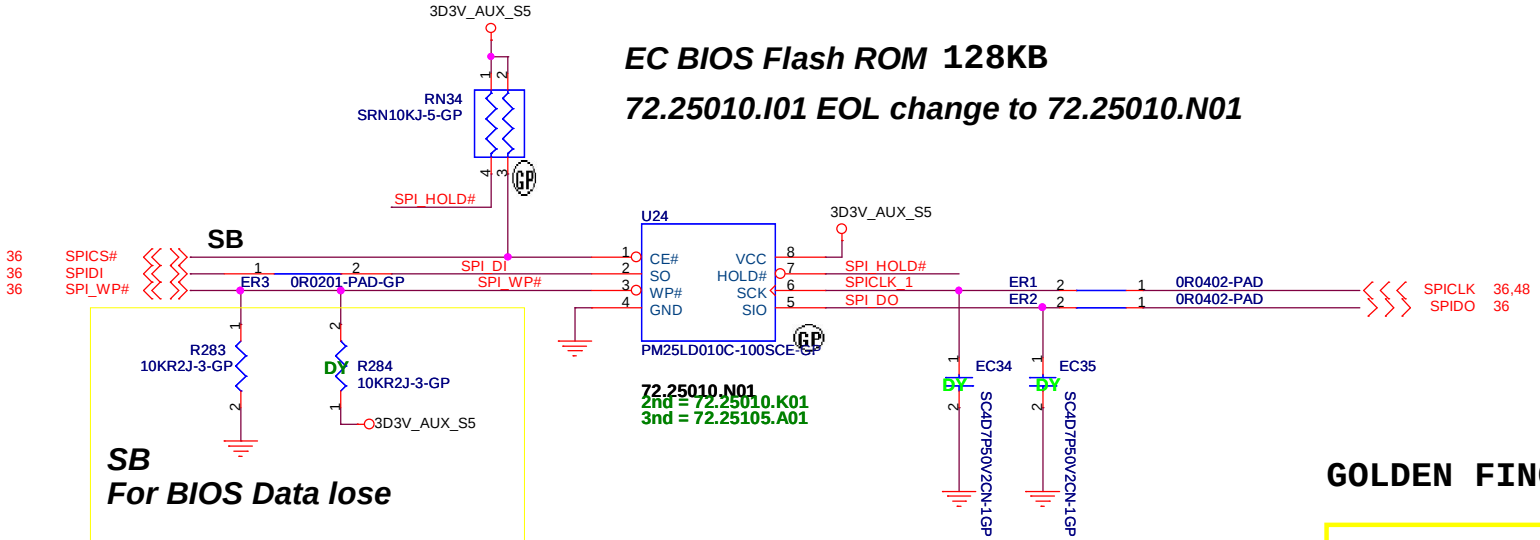
JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

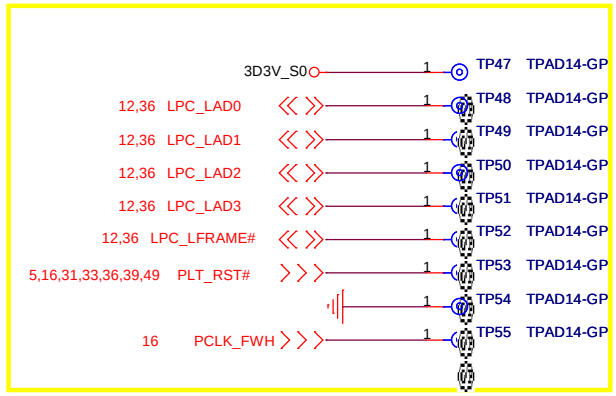
Title: KBC NPCE781B
Size: Custom | Document Number: JV10-CS | Rev: -1
Date: Wednesday, February 10, 2010 | Sheet 36 of 50

EC BIOS Flash ROM 128KB

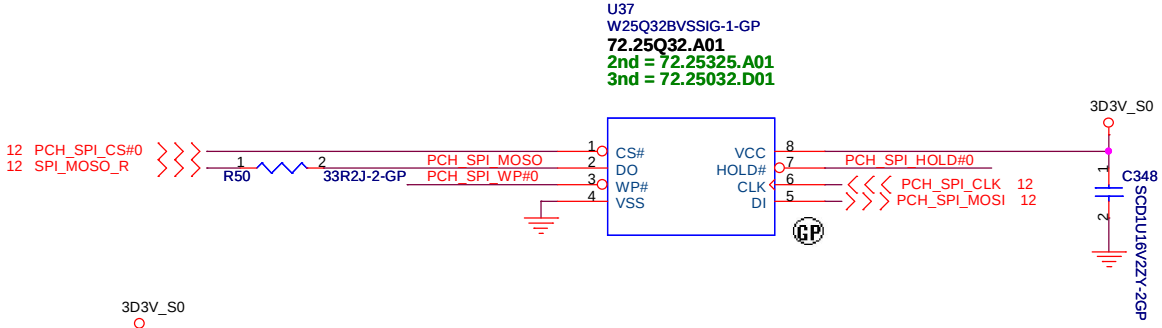
72.25010.I01 EOL change to 72.25010.N01

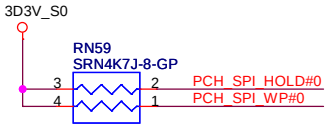


GOLDEN FINGER FOR DEBUG BOARD



System BIOS Flash ROM 4MB



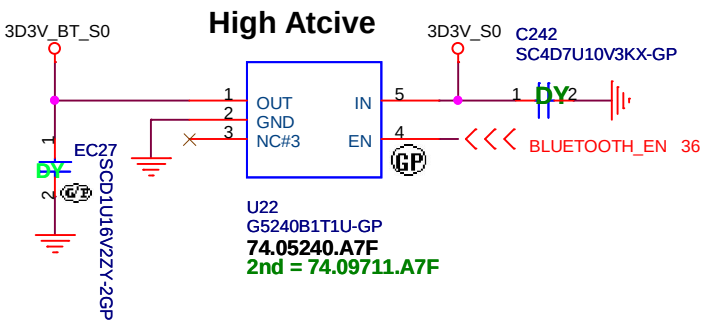


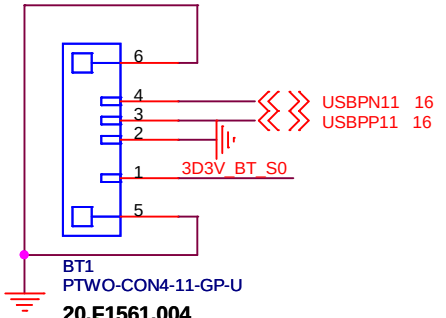
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BIOS	
Size: Custom	Document Number: JV10-CS	Rev: -1
Date: Wednesday, February 10, 2010	Sheet 37 of 50	

BLUETOOTH Connector

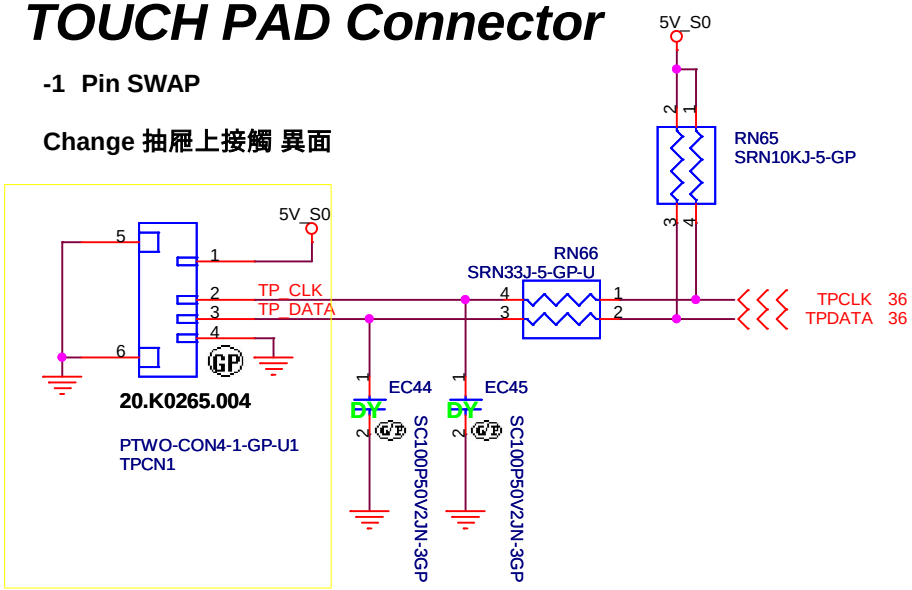




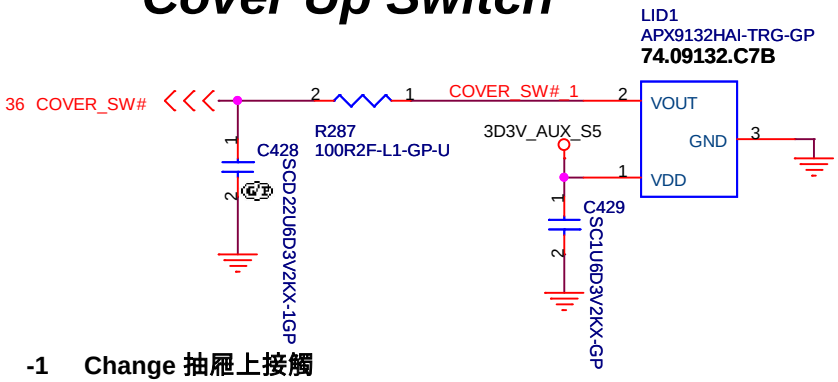
TOUCH PAD Connector

-1 Pin SWAP

Change 抽屜上接觸 異面

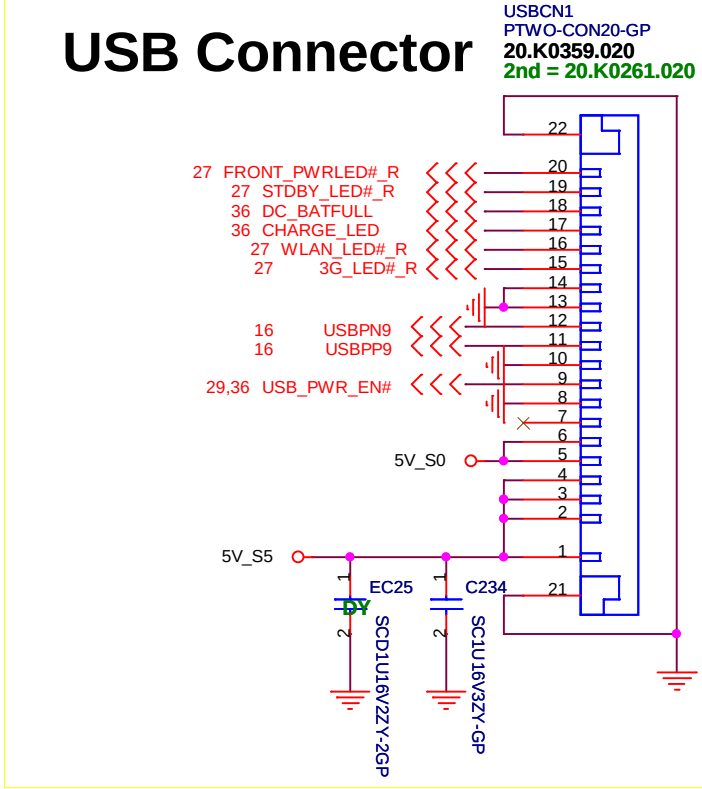


Cover Up Switch



-1 Change 抽屜上接觸

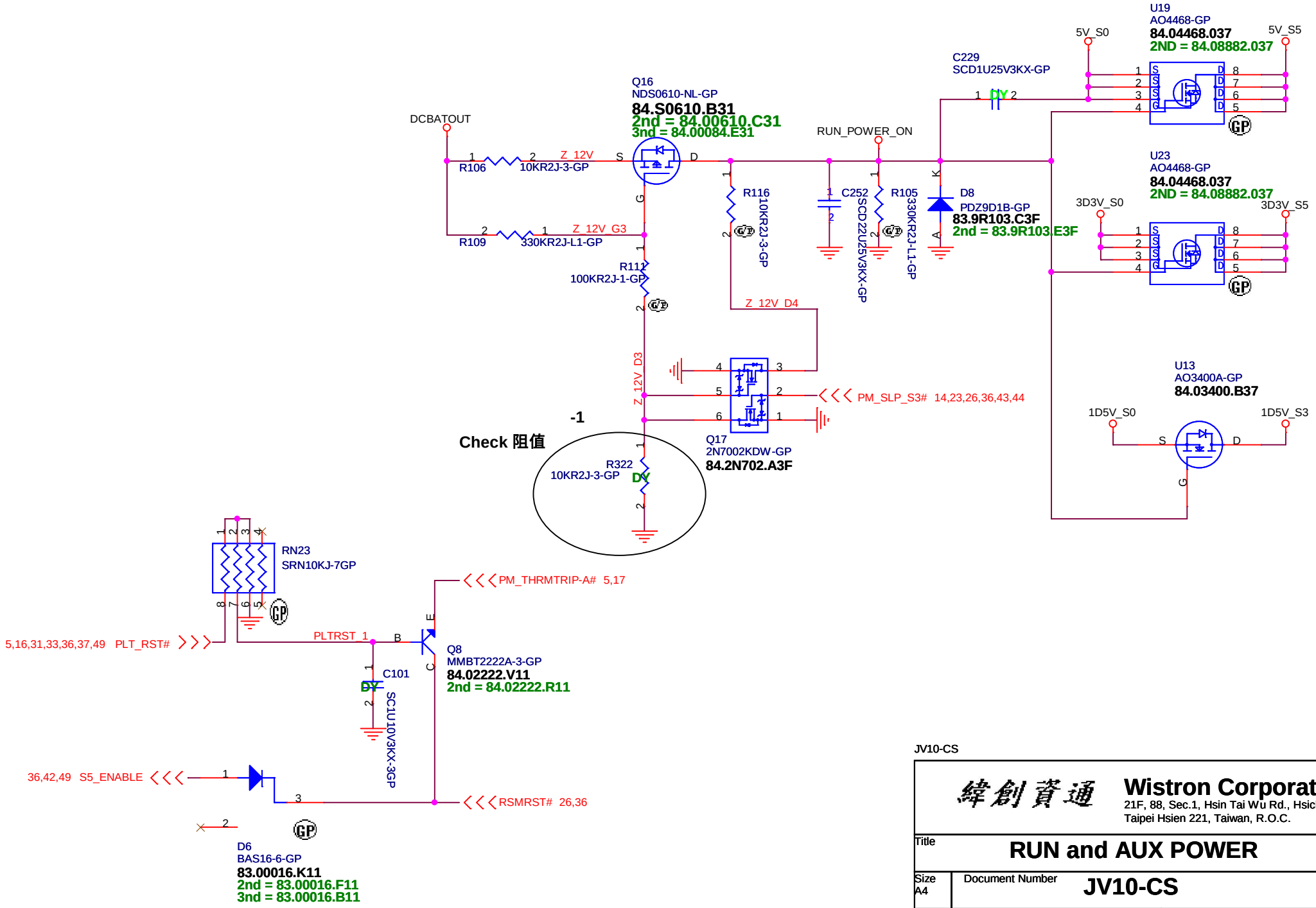
USB Connector



JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CONNECTOR**	
Size A4	Document Number **JV10-CS**	Rev **-1**
Date: Wednesday, February 10, 2010	Sheet 38 of 50	

Run Power



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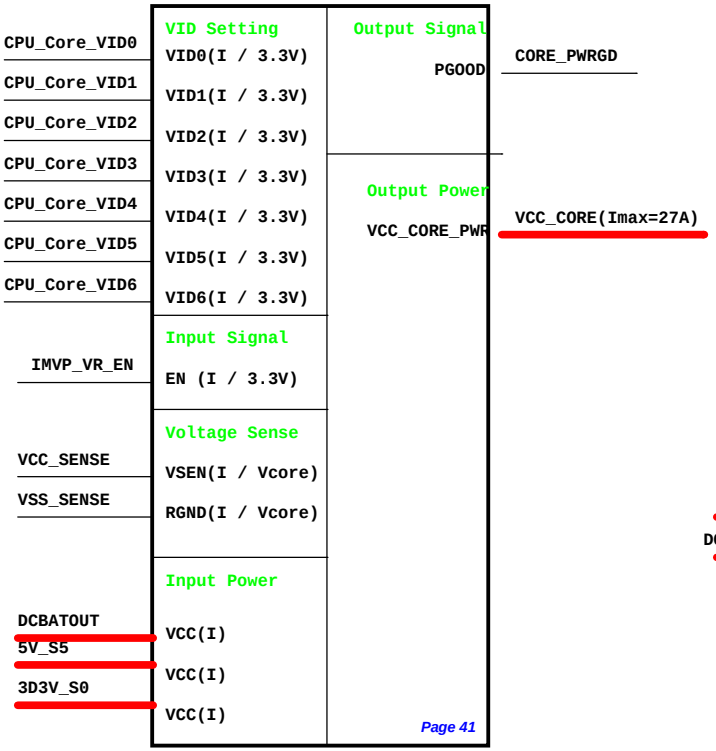
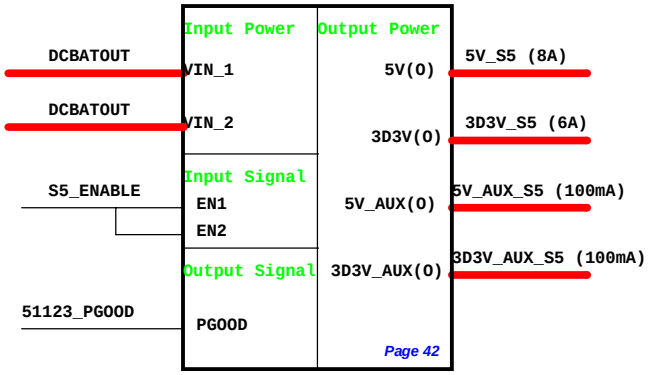
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**RUN and AUX POWER**	
Size A4	Document Number **JV10-CS**	Rev **-1**
Date: Wednesday, February 10, 2010	Sheet 39 of 50	

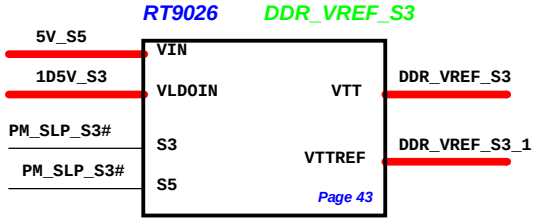
TPS51611 VCC_CORE



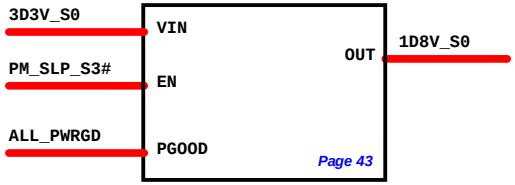
RT8223 5V/3D3V_S5



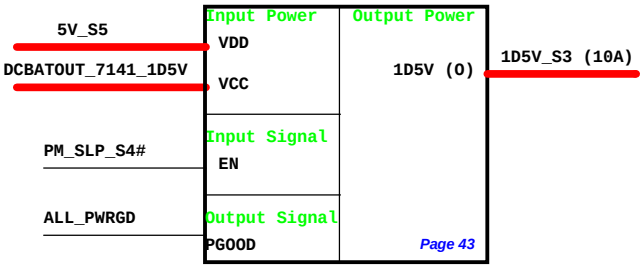
RT9026 DDR_VREF_S3



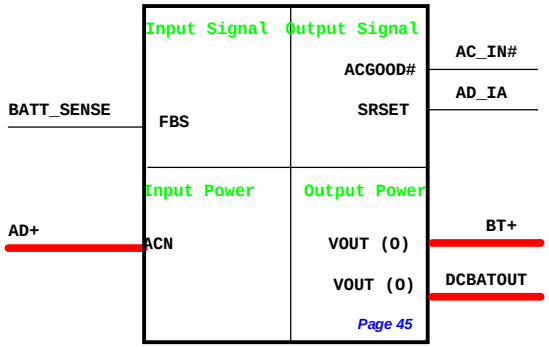
RT9025 1D8V_S0



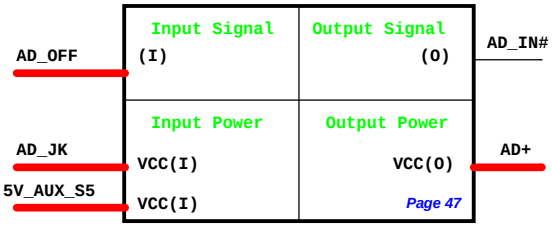
RT8209E 1D5V_S3



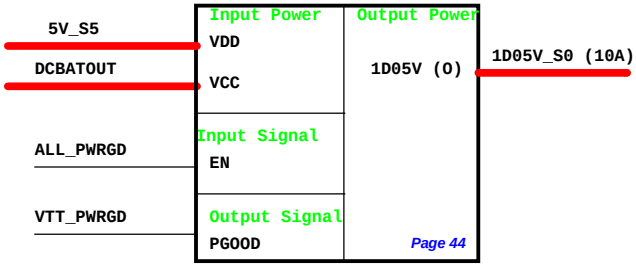
Charger ISL88731A



Adapter



RT8209B 1D05V



JV10-CS

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
	JV10-CS	-1

Date: Wednesday, February 10, 2010 Sheet 40 of 50

CPU VCC_CORE

From KBC 36 IMVP_VR_EN
43,44 ALL_PWRGD
To PCH
VR_CLKEN# 3
CORE_PWRGD 14

TPS51611RHBR-GP
U11
74.51611.073

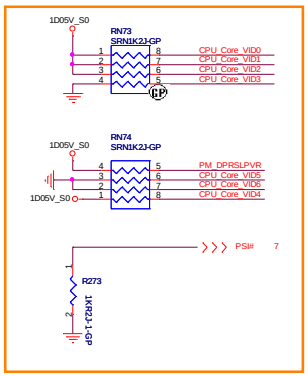
-2 chage 2K2
20100113
20091014
20091011
20090911
SB

Iomax=27A
OCP>45A

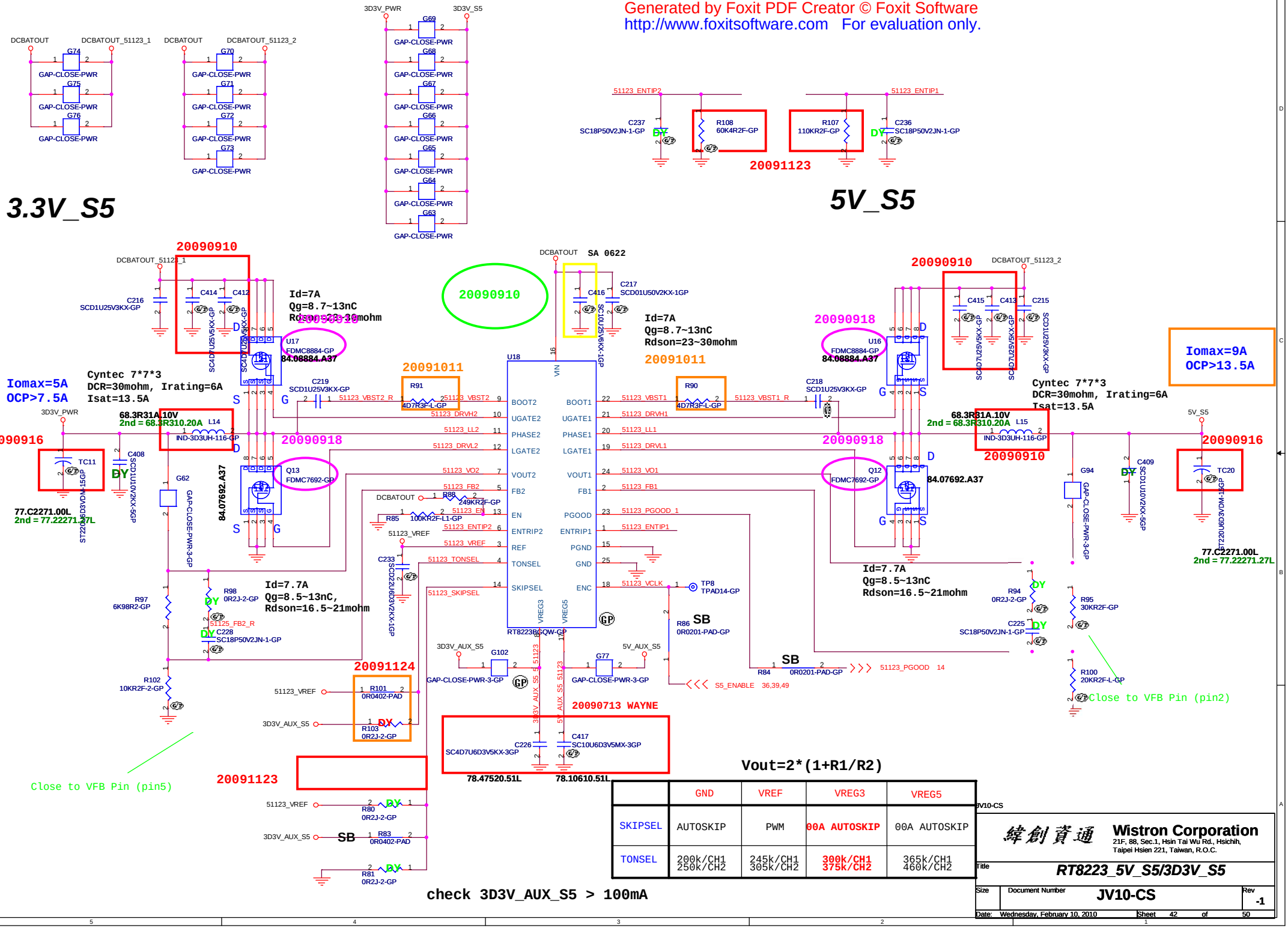
-2 change 23k2R
R527 close to L32
-2 change 56K2R

-2
Intel support POC (power on current).

-2
VID 5~3 change 010



JV10-CS			
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: TPS51611_CPU CORE			
Size	Document Number: JV10-CS		Rev: -1
Date: Wednesday, February 10, 2010	Sheet 41 of 50		



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

JV10-CS

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223_5V_S5/3D3V_S5

Size	Document Number	Rev
	JV10-CS	-1

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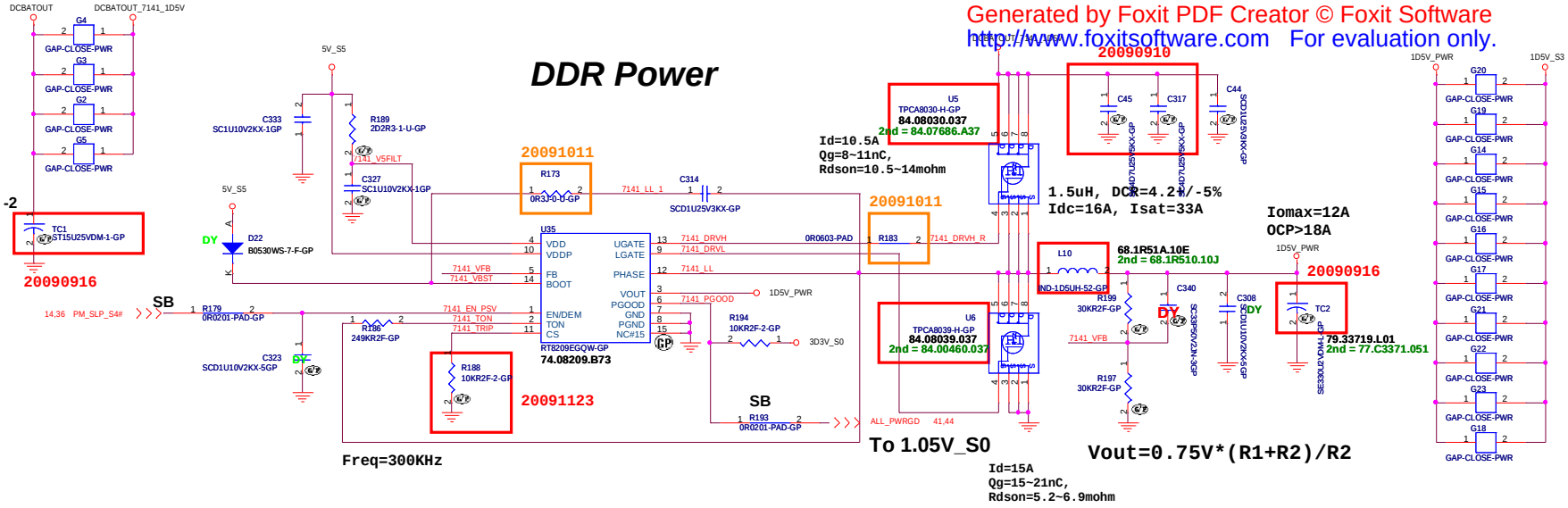
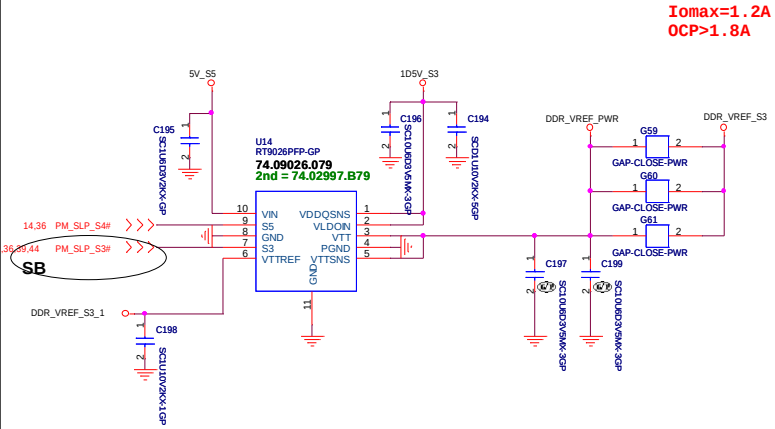
DDR Power

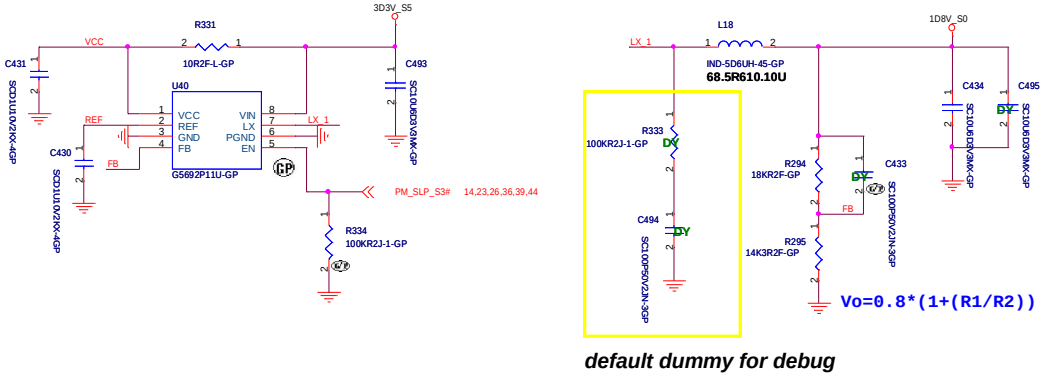


DDR_VREF_S3

RT9026 for DDR_VREF_S3_1



-2 RT8015A for 1D8V_S0



default dummy for debug

JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT8209E_1D5V_S3	
Size	Document Number JV10-CS	Rev -1
Date: Wednesday, February 10, 2010	Sheet 43 of 50	

CPU, PCH 1.05V_S0

DCBATOUT
DCBATOUT_RT8209B_VCCP
G47 GAP-CLOSE-PWR
G45 GAP-CLOSE-PWR
G46 GAP-CLOSE-PWR
G48 GAP-CLOSE-PWR
G49 GAP-CLOSE-PWR
G50 GAP-CLOSE-PWR
20090916
TC15 ST15U25VDM-1-GP

5V_S5
20091011
RFC9 SC1200P50V2KX-1GP
C366 SC1U10V2KX-1GP
R231 2D2R3-1-U-GP
C373 SC1U10V2KX-1GP
RFC10 SC1200P50V2KX-1GP
RT8209B_VCCP_V5FILT
RT8209B_VCCP_VBST
20091011
R219 0R3J-0-U-GP
RT8209B_VCCP_LL_1
C356 SCD1U25V3KX-GP

From 1.5V_S3
41,43 ALL_PWRGD
14,23,26,36,39,43 PM_SLP_S3#
SB
DY
R65 0R0201-PAD-GP
R66 0R2J-2-GP
VCCP_RUN ON
R67 200KR2F-L-GP
RT8209B_VCCP_TON
RT8209B_VCCP_TRIP
R218 10KR2F-2-GP
20091123

U10 RT8209EGQW-GP
VDD VDDP FB BOOT EN/DEM TON CS
UGATE LGATE PHASE VOUT PGOOD GND PGND NC#15
RT8209B_VCCP_VFB
RT8209B_VCCP_DRVH
RT8209B_VCCP_DRVL
RT8209B_VCCP_LL
+VCCP_PWR
VTT_PWRGD 36
To KBC

Freq=360KHz

20090623 Wayne
20091011
R54 0R0603-PAD
20090910
U8 TPCA8028-H-GP
84.08028.037
2nd = 84.00164.037
U38 TPCA8028-H-GP
DY
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm

DCBATOUT_RT8209B_VCCP
20090910
20090910
U9 TPCA8030-H-GP
84.08030.037
2nd = 84.07686.A37
C105 SC4D7U25V5KX-GP
C102 SC4D7U25V5KX-GP
C106 SC4D7U25V5KX-GP
RFC8 SC1200P50V2KX-1GP
-1

20090820
L11 IND-D45UH-14-GP
68.R4510.10K
2nd = 68.R4510.10C
Vout=1.1054(Cal)
Iomax=19A
OCP>28.5A
C112 SCD1U50V2JN-1-GP
R68 10KR2F-2-GP
R69 24KR2F-GP
RT8209B_VCCP_VFB
Vout=0.75*(1+R1/R2)
+VCCP_PWR
20090916
TC4 TC3 ST330U2V5VBM-1-GP

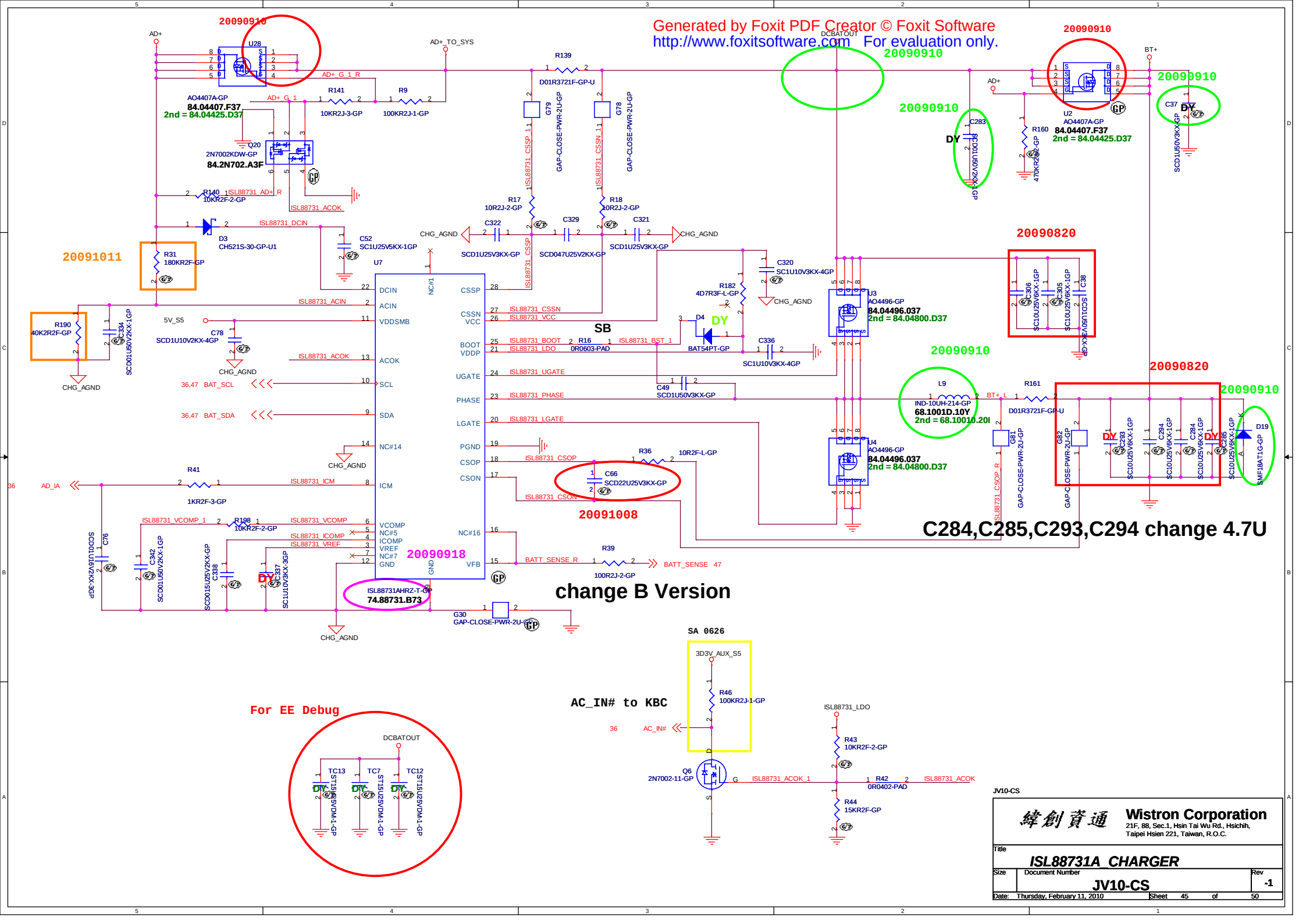
+VCCP_PWR
1D05V_S0
G83 G24 G27 G28 G29 G32 G33 GAP-CLOSE-PWR
G84 G85 G86 G87 G12 G13 GAP-CLOSE-PWR

RT8209B_VCCP_VFB
R61 0R2J-2-GP
DY
VTT_SENSE 7

3D3V_S0
R56 10KR2J-3-GP
Q7 2N7002KDW-GP
84.2N702.A3F
3D3V_S5
R53 100KR2J-1-GP
VTT_PWRGD
H_VTTPWRGD_R
C100 SCD1U10V2KX-5GP
1D05V_S0
R55 1KR2J-1-GP
H_VTTPWRGD 5

JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8209B_1D05V_S0		
Size	Document Number: JV10-CS	Rev: -1
Date: Wednesday, February 10, 2010	Sheet 44 of 50	



JV10-CS
Wistron Corporation
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Title: ISL88731A CHARGER

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VCC_GFXCORE

TPS51611RHBR-GP

Iomax=15A
OCP>24A

R527 close to L32

JV10-CS	
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Title	TPS51611_GFX_CORE
Size	A2
Document Number	JV10-CS
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Date:	Wednesday, February 10, 2010
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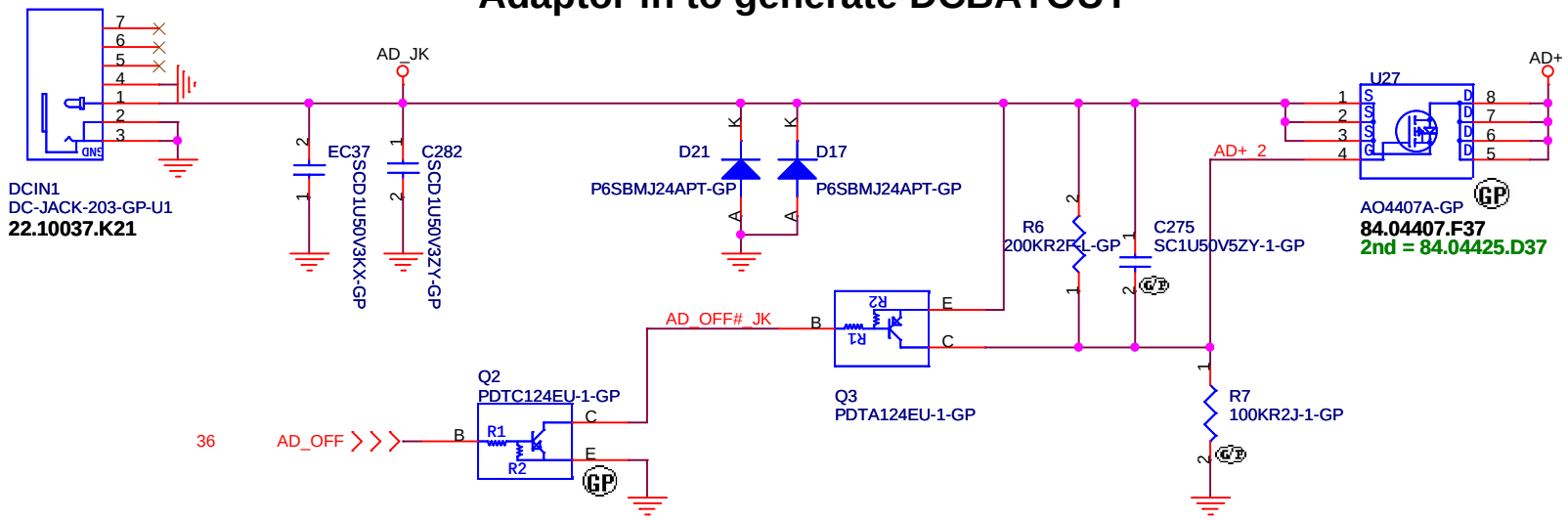
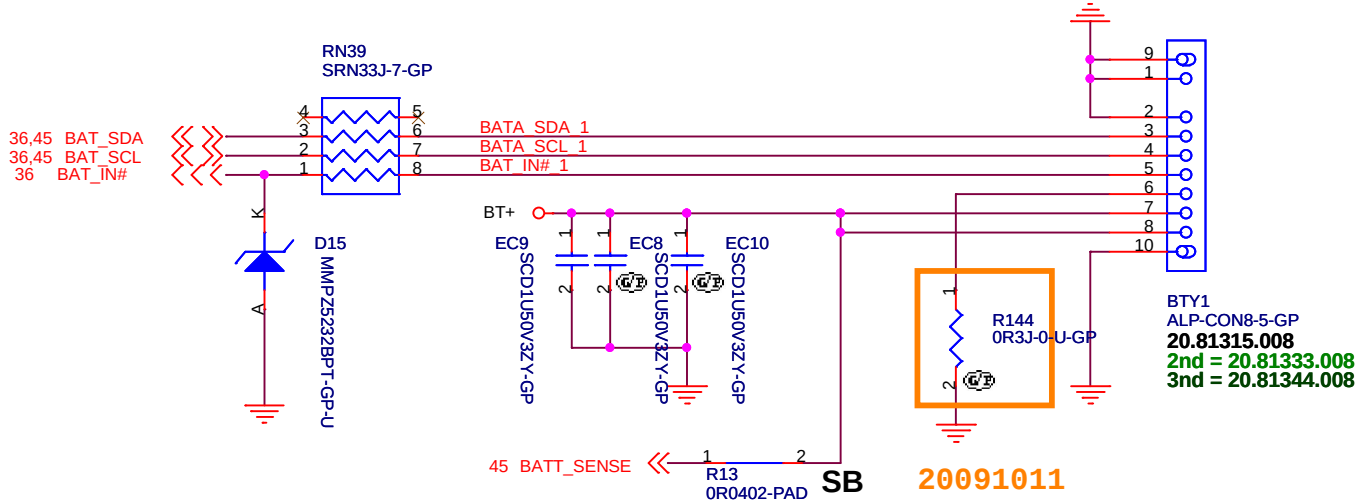
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title	AD/BATT CONN	
Size	Document Number: JV10-CS	Rev: -1
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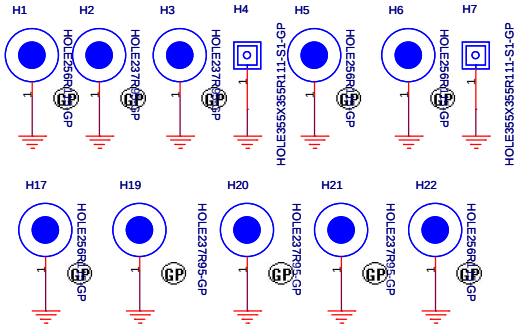
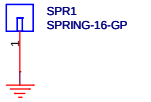
MB HOLE



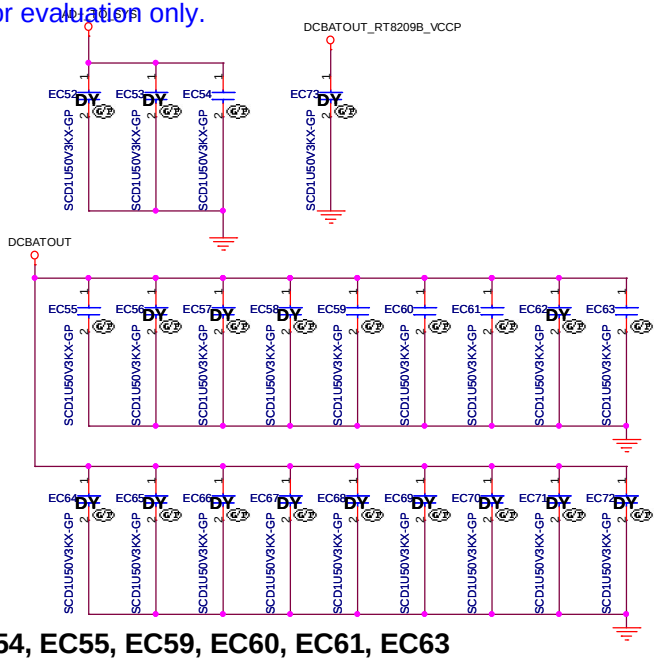
SPRING



-1

SB

EMI

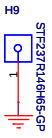


EC54, EC55, EC59, EC60, EC61, EC63

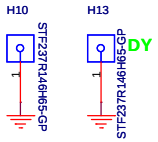
MINI CARD BOSS

(BTN Side)

HALF MINI CARD

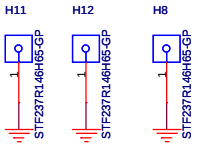


FULL MINI CARD

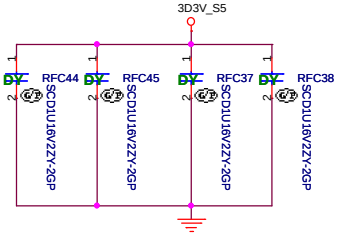


CPU PCH BOSS

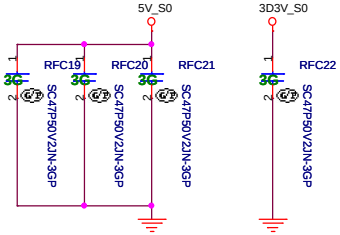
(BTN Side)



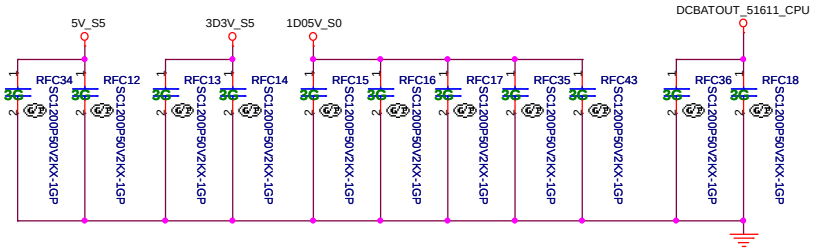
For RF power point Page 26



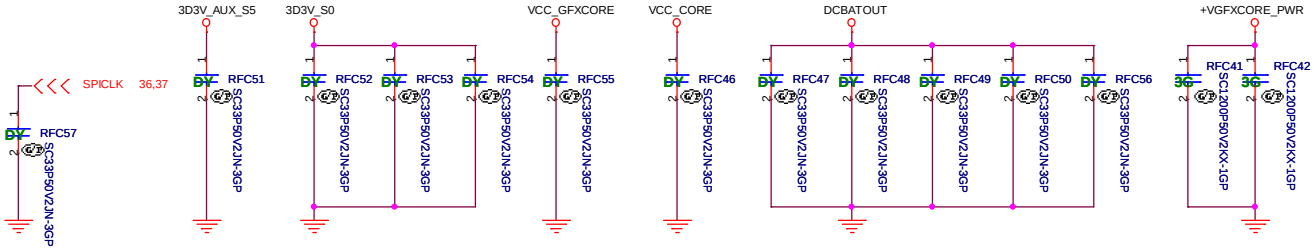
For RF power point Page 12



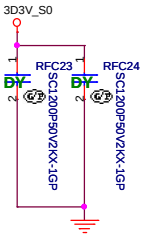
For RF power point Page 4

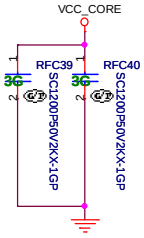


For RF power point Page 17



For RF power point Page 13

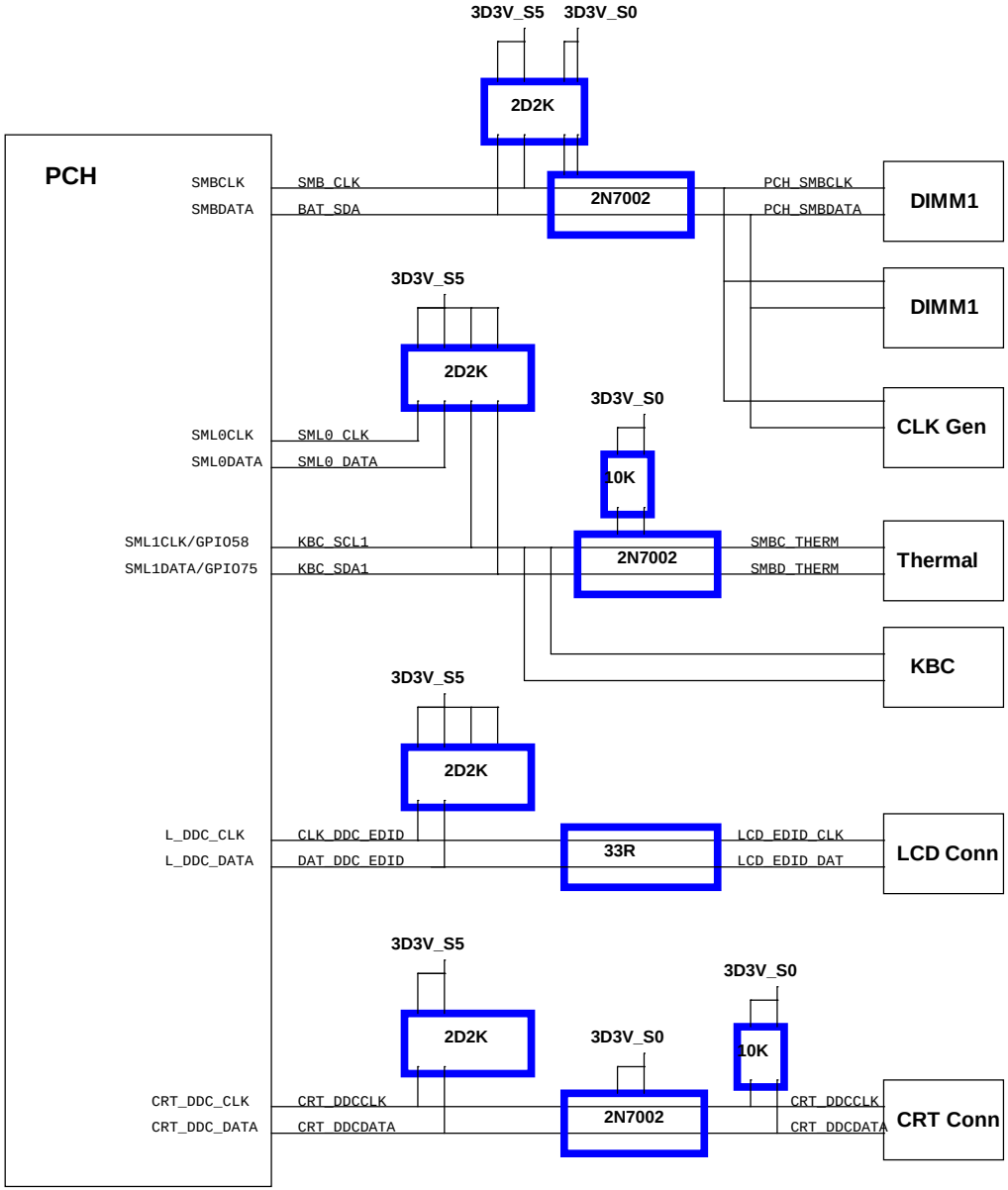




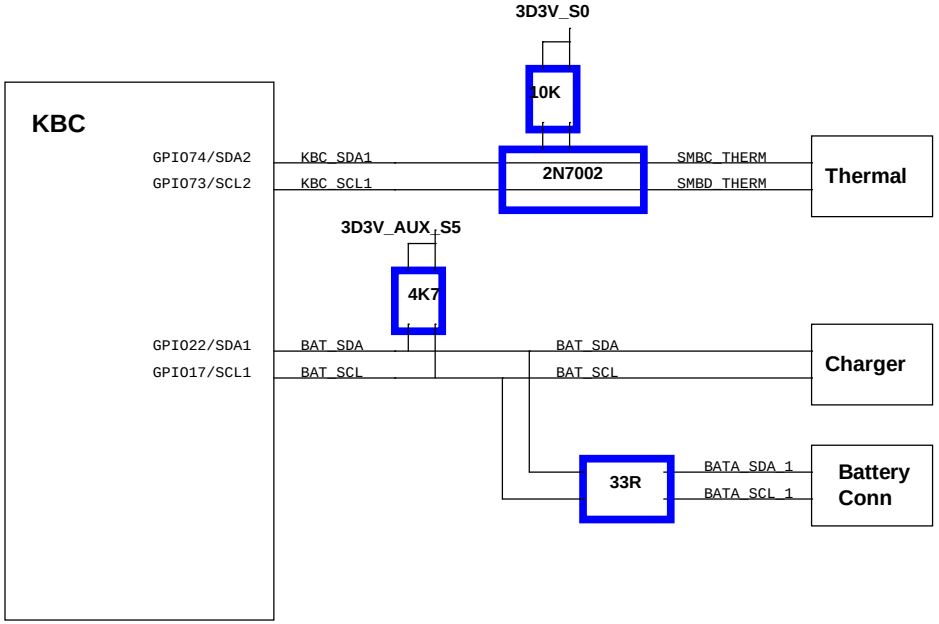
JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***EMI/Spring/Boss***	
Size	Document Number **JV10-CS**	Rev -1
Date: Wednesday, February 10, 2010	Sheet 48 of 50	

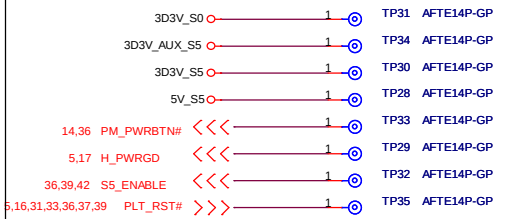
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Check test point



Test Point放在Dimm Door打開可量測處

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AFTE_TP/SMB Diagram	
Size	Document Number: JV10-CS	Rev: -1
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SJM80 Schematic EC Tracking Record LAB 0325 , 2009
EC #/ Page / Description / Part Affected

EC SB11/04 add Intel support POC Function(power on current).
EC SB11/04 SWAP Touch Pad Pin define
EC SB11/04 R230 add 1K
EC SB11/04 change LOUT1 part number
EC SB11/11 SWAP Digital Mic DATA/CLK Pin define
EC SB11/11 Delete 3G_BTN#,Wireless_BTN#, function
EC SB11/11 add Cover switch to MB
EC SB11/11 add RN72 22ohm for Mic in
EC SB11/16 change U40 1D8V_S0 power solution
EC SB11/19 modify all LED off Function
EC SB11/19 change HDD Connector Type
EC SB11/19 Close Powert team Gap
EC PD 01/11 modify keyborad connector KB1
EC PD 01/11 modify USB Touch pad connector TPCN1 USBCN1
EC PD 01/11 add 3G module LED Function
EC PD 01/11 EMI add EC54, EC55, EC59, EC60, EC61, EC63, C37
EC PD 01/11 TPCN1 SWAP Pin define
EC PD 01/14 delete RN2 add R326 R327
EC PD 01/15 change C239 C277 and add C492 to Net 3D3V_CK505_1
SWAP RN74 Pin define
EC PD 01/20 add Q33, deleteRN62, add R329 for LED function
EC PD 01/27 Modify HDD connector part number
EC PD 01/27 Modify H19 Hole footprint

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Modify History**		
Size: A3	Document Number: **JV10-CS**	Rev: **-1**
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