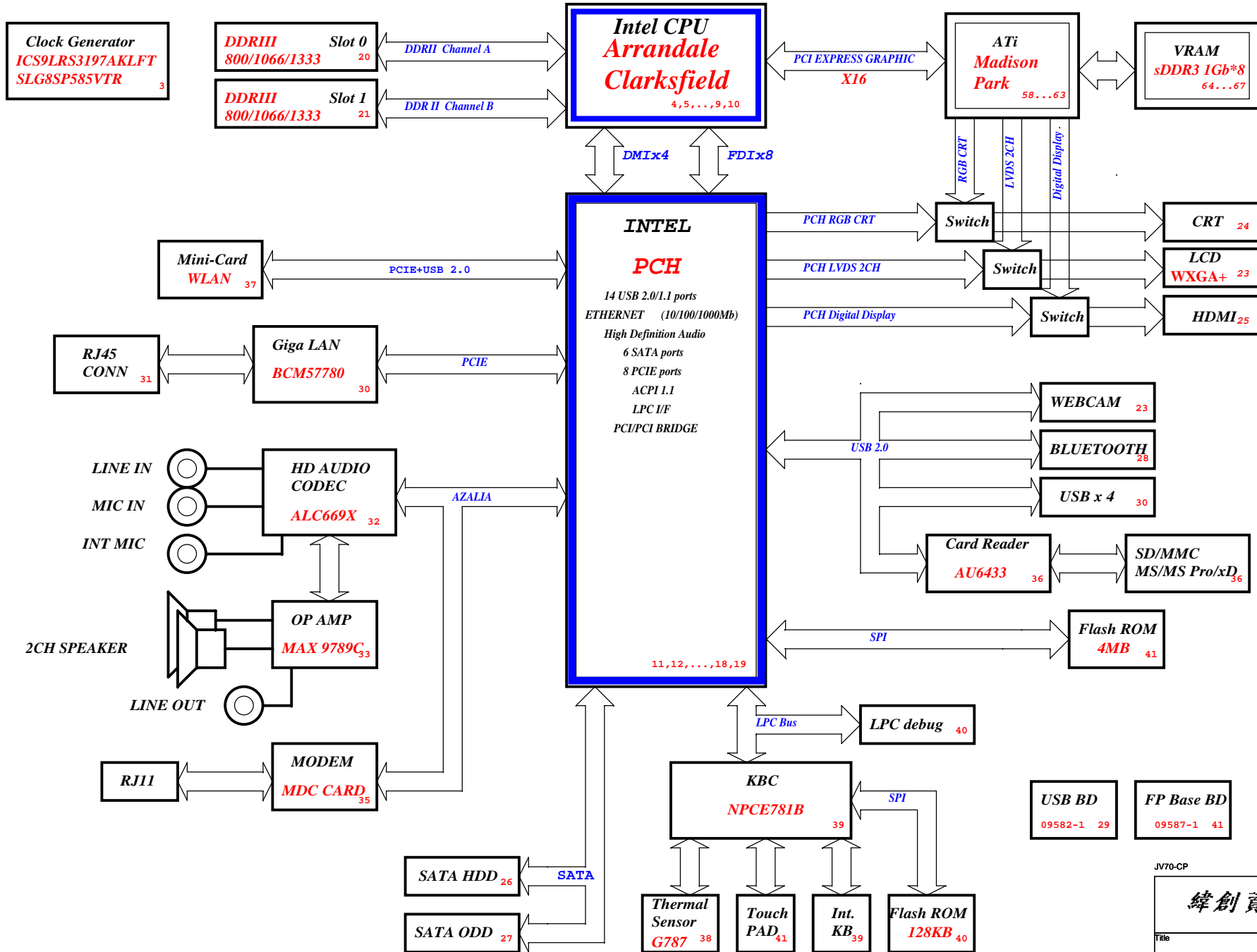
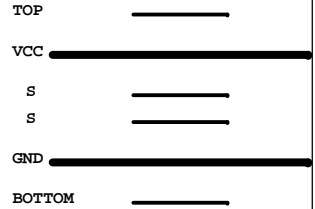


JV70-CP Block Diagram

Project code: 91.4GC01.001
 PCB P/N : 48.4GC01.011
 REVISION : 09293--1

PCB STACKUP



SYSTEM DC/DC TPS51123	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 47
SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 48
SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 48
SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 49
CPU DC/DC ISL62883	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 45,46
MAXIM CHARGER ISL88731A	
INPUTS	OUTPUTS
DCBATOUT	BT+ 51

JV70-CP

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size A3 Document Number **JV70-CP** Rev **-1**

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PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (xPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCIE Routing

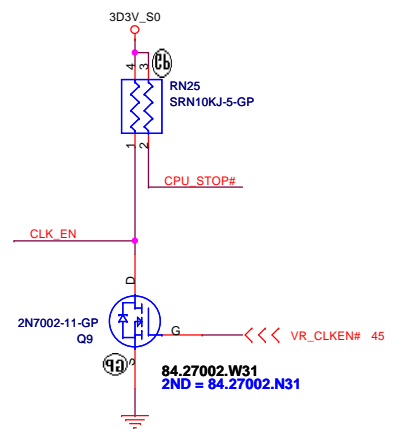
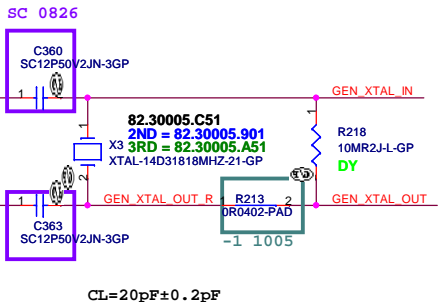
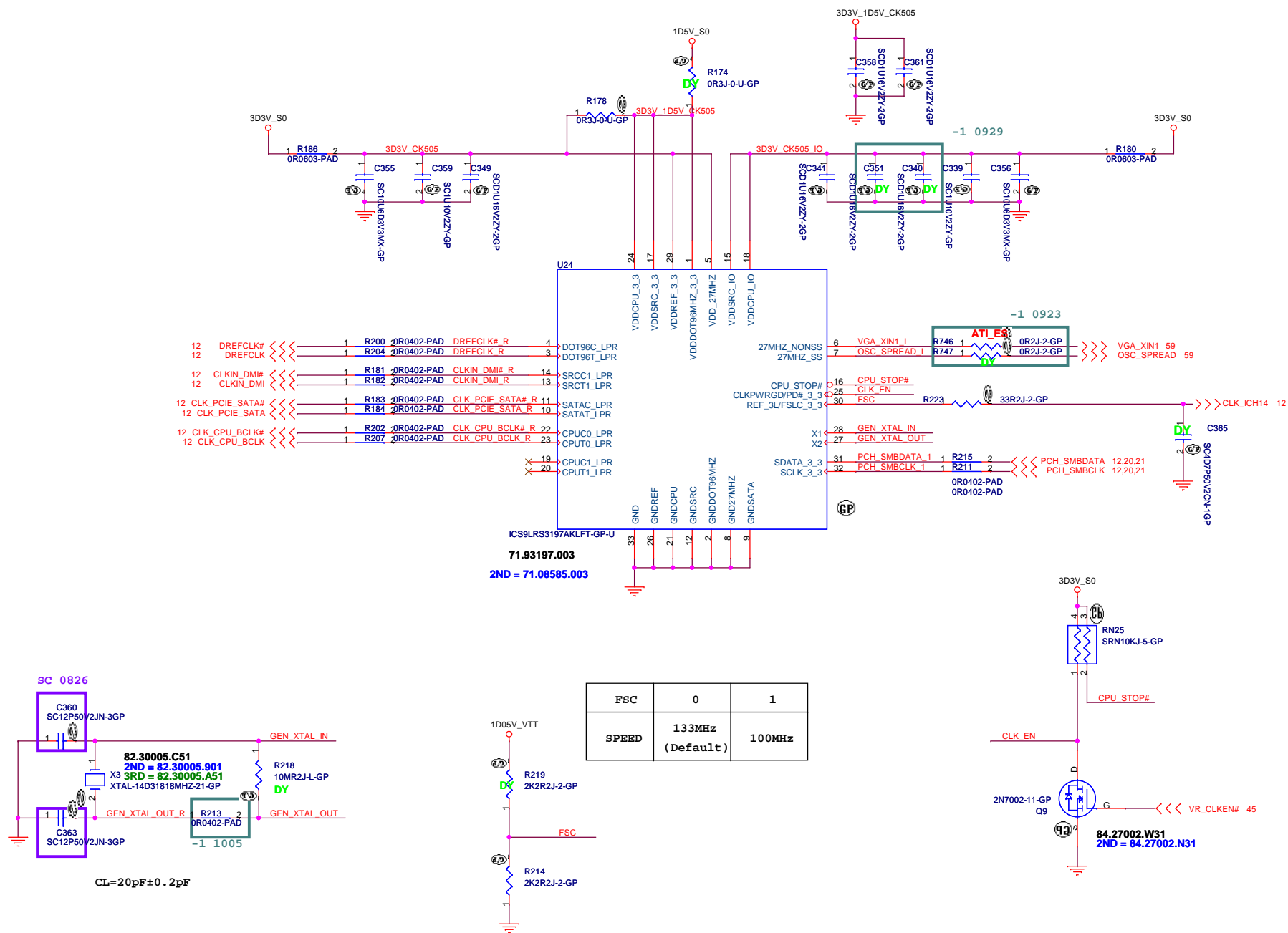
LANE1	LAN
LANE2	MiniCard WLAN

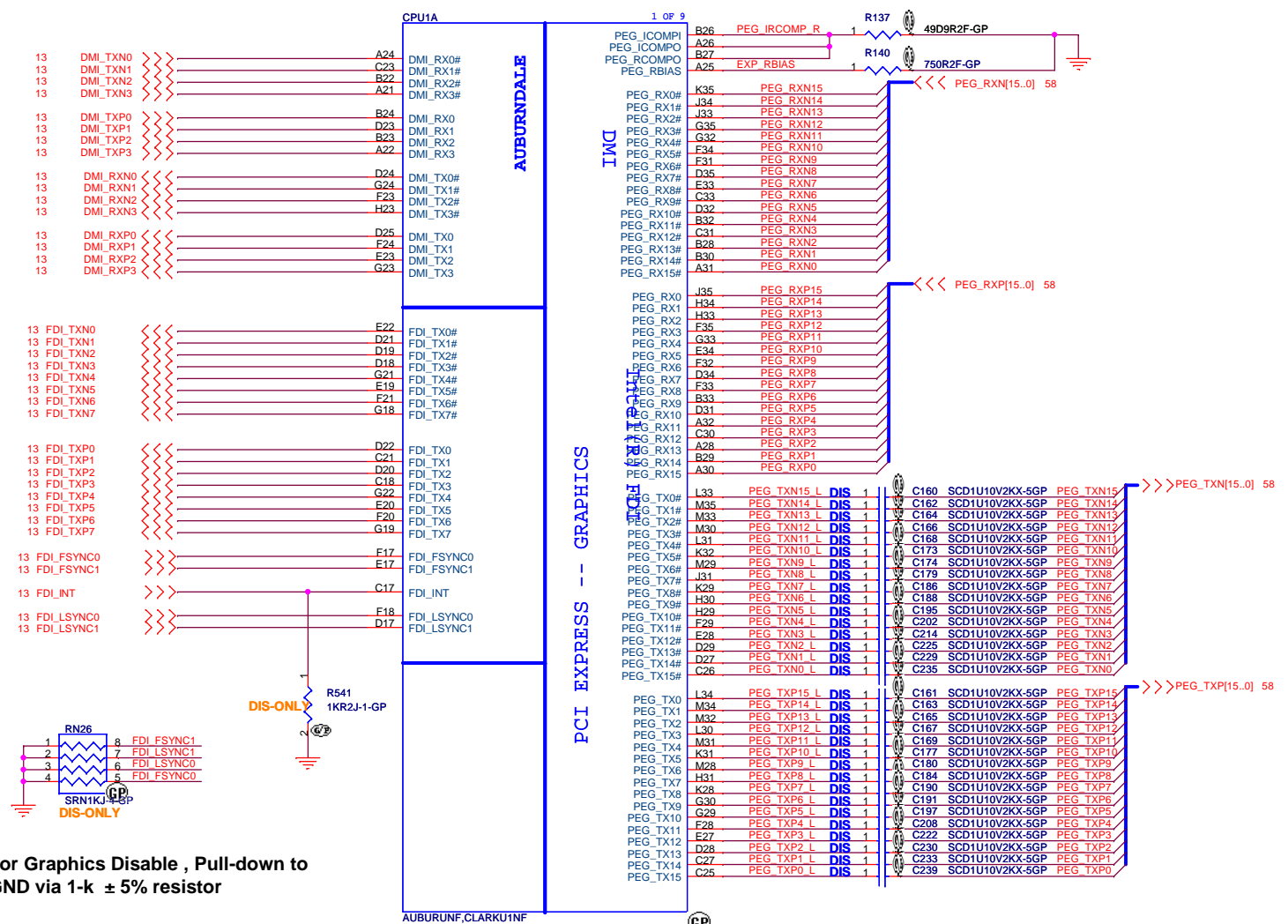
USB

Pair	Device
0	USB1
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	NC
6	NC
7	NC
8	NC
9	USB3(HS)
10	Finger Print
11	Blue Tooth
12	NC
13	Cardreader

JV70-CP

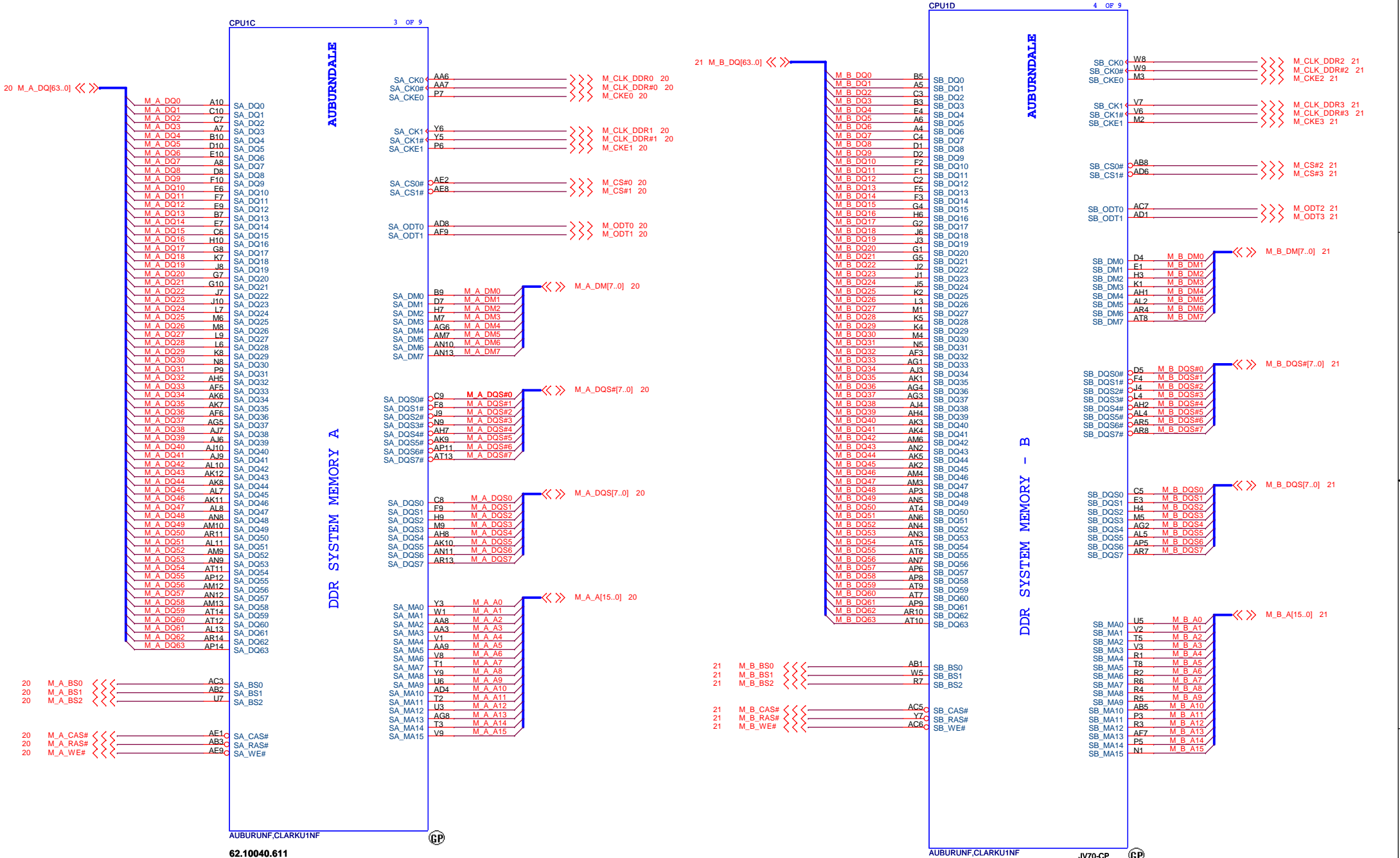
緯創資通		Wistron Corporation	
		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
Table of Content			
Size	Document Number	Rev	
A3	JV70-CP	-1	
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For Graphics Disable, Pull-down to GND via 1-k ± 5% resistor

62.10040.611
2ND = 62.10055.321

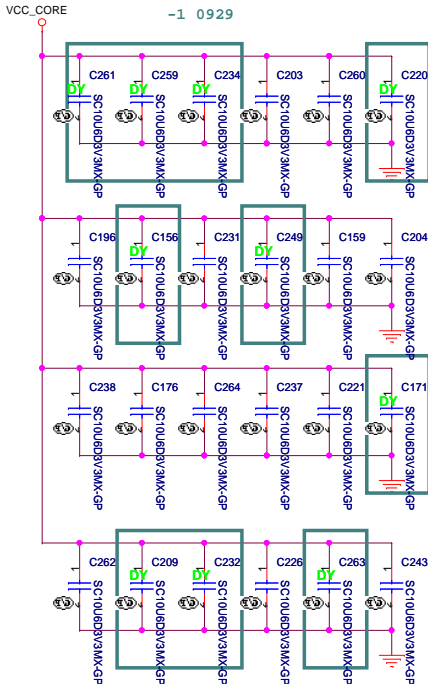


AUBURUNDF, CLARKU1NF
 62.10040.611
 2ND = 62.10055.321

AUBURUNDF, CLARKU1NF
 62.10040.611
 2ND = 62.10055.321

JV70-CP

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CPU (3/7)	
Title	Rev
Size	-1
JV70-CP	
Date: Thursday, October 08, 2009	Sheet 6 of 68



VCC_CORE
65A

PROCESSOR CORE POWER

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- V35 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- P35 VCC
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- P27 VCC
- P26 VCC

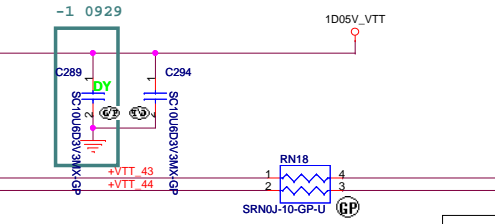
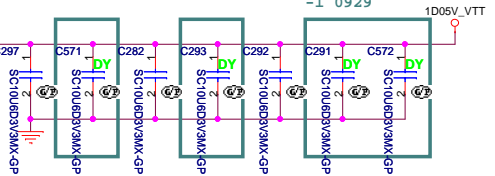
- AH14 VTT0
- AH12 VCC
- AH11 VCC
- AH10 VCC
- J14 VCC
- J13 VCC
- H14 VTT0
- H12 VCC
- H11 VCC
- G14 VTT0
- G13 VCC
- G12 VCC
- F14 VTT0
- F13 VCC
- F12 VCC
- F11 VCC
- E14 VTT0
- E12 VCC
- E11 VCC
- D14 VTT0
- D13 VCC
- D12 VCC
- D11 VCC
- C14 VTT0
- C13 VCC
- C12 VCC
- C11 VCC
- B14 VTT0
- B12 VCC
- A14 VTT0
- A13 VCC
- A12 VCC
- A11 VCC

- AF10 VTT0
- AE10 VTT0
- AC10 VTT0
- AB10 VTT0
- Y10 VTT0
- W10 VTT0
- U10 VTT0
- T10 VTT0
- J12 VTT0
- J11 VTT0
- J16 VTT0
- J15 VTT0

- PSI# AN33 >>> PSI# 45
- AK35 H_VID0 >>> H_VID[6..0] 45
- AK33 H_VID1 >>> H_VID[6..0] 45
- AK34 H_VID2 >>> H_VID[6..0] 45
- AL35 H_VID3 >>> H_VID[6..0] 45
- AL33 H_VID4 >>> H_VID[6..0] 45
- AM33 H_VID5 >>> H_VID[6..0] 45
- AM35 H_VID6 >>> H_VID[6..0] 45
- AM34 >>> PM_DPRSLPVR 45

G15 H_VTTVID1 >>> H_VTTVID1 49
 Clarksfield H_VTTVID1 = Low, VTT = 1.1V
 Arrandale H_VTTVID1 = High, VTT = 1.05V

- ISENSE AN35 <<< IMVP_MON 45
- VCC_SENSE AJ34 >>> VCC_SENSE 45
- VSS_SENSE AJ35 >>> VSS_SENSE 45
- VTT_SENSE B15 >>> VTT_SENSE 49
- VSS_SENSE_VTT A15 >>> TP VSS SENSE VTT 1



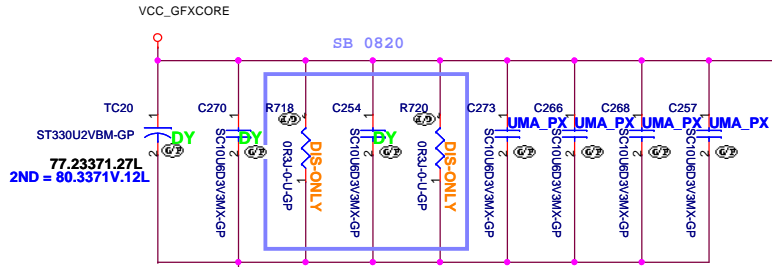
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

AUBURUNF.CLARKU1NF
62.10040.611
2ND = 62.10055.321

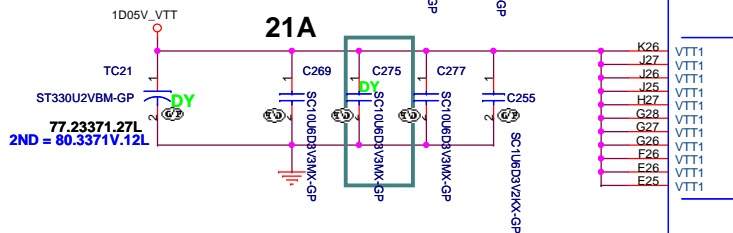
JV70-CP

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CPU (4/7)	
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Size	Document Number
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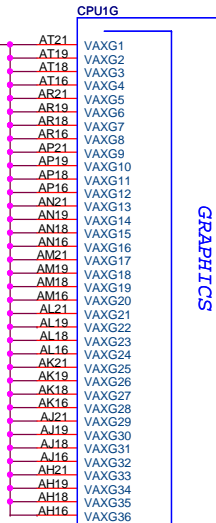
For Graphics Disable, Can be connected to GND directly

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



21A

77.23371.27L
2ND = 80.3371V.12L



AUBURDALE

GRAPHICS

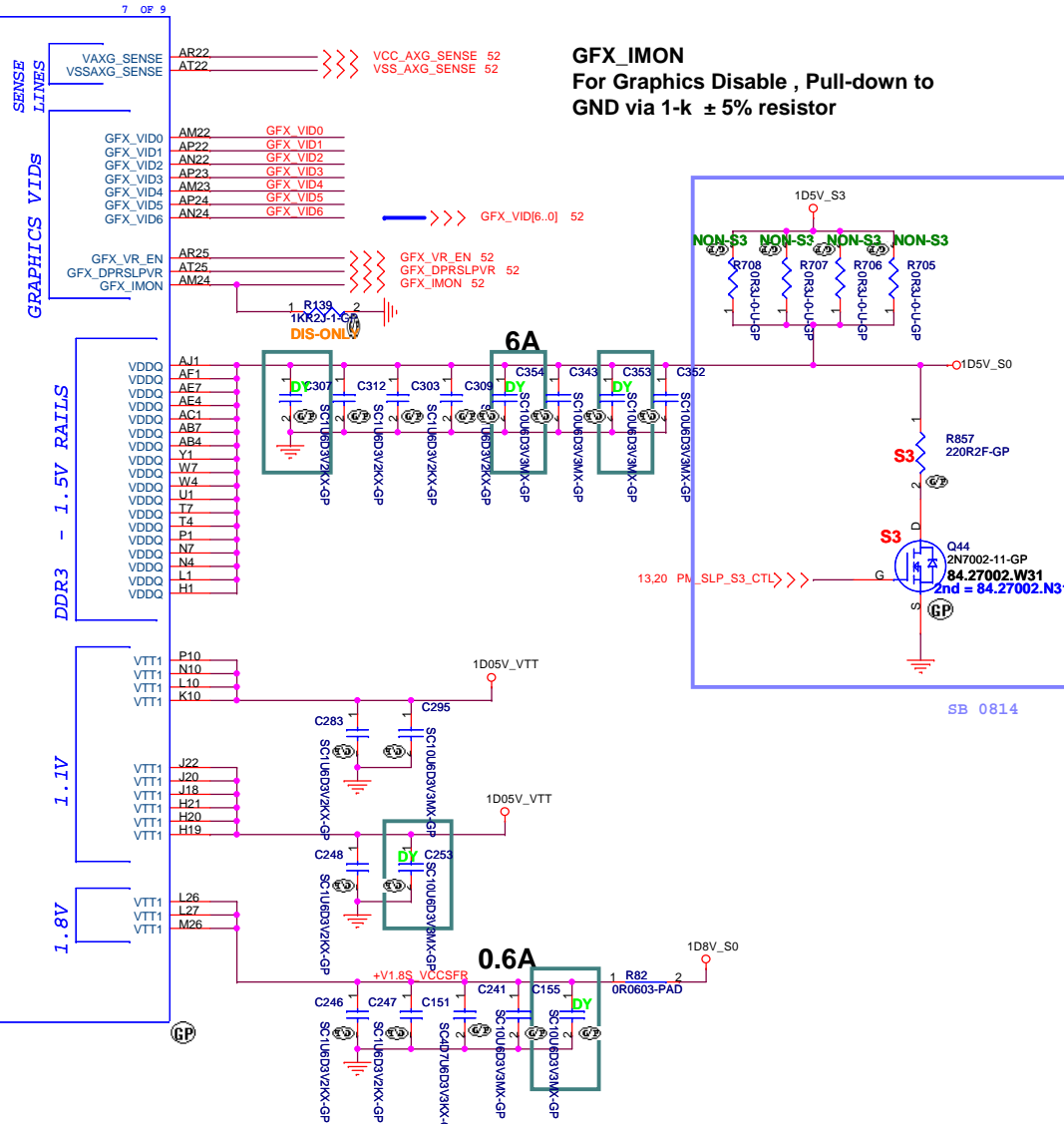
POWER

PEG & DMI

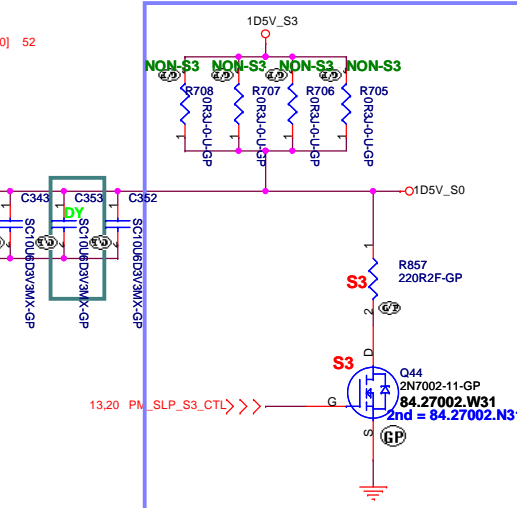
AUBURUNF,CLARKU1NF

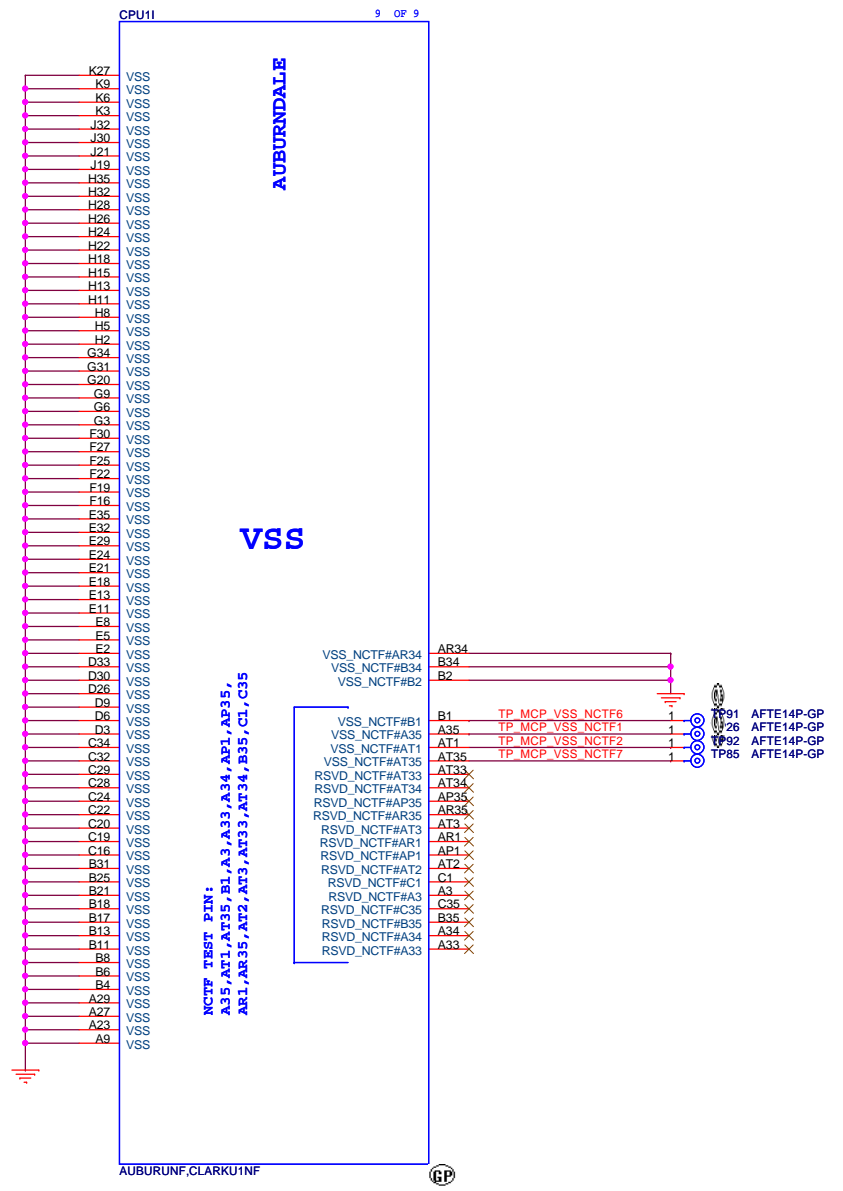
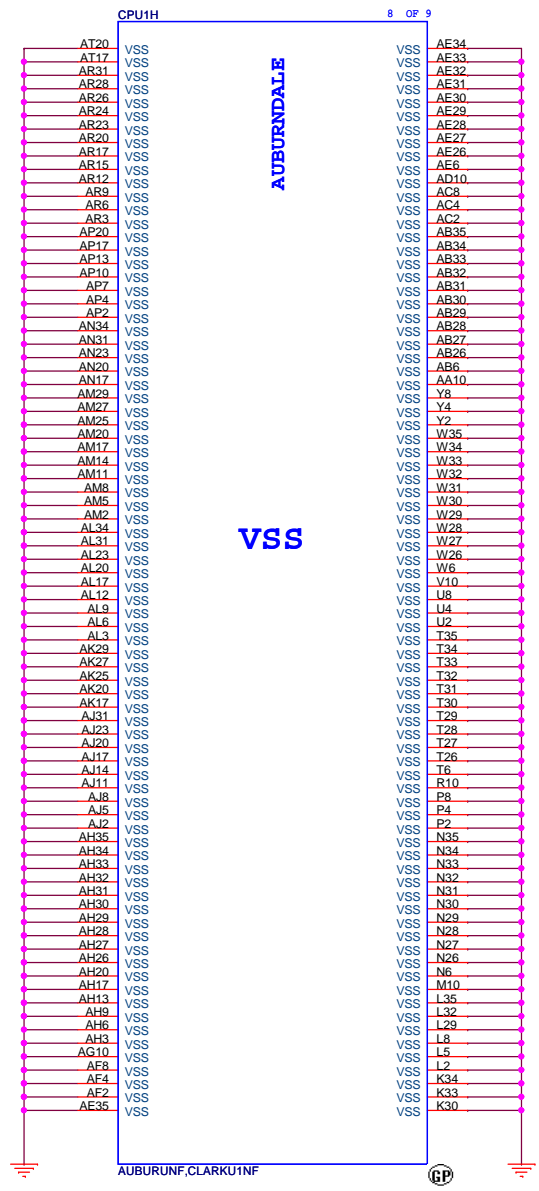
62.10040.611

2ND = 62.10055.321



GFX_IMON
For Graphics Disable, Pull-down to GND via 1-k ± 5% resistor





JV70-CP

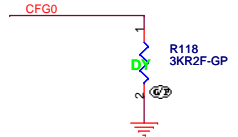
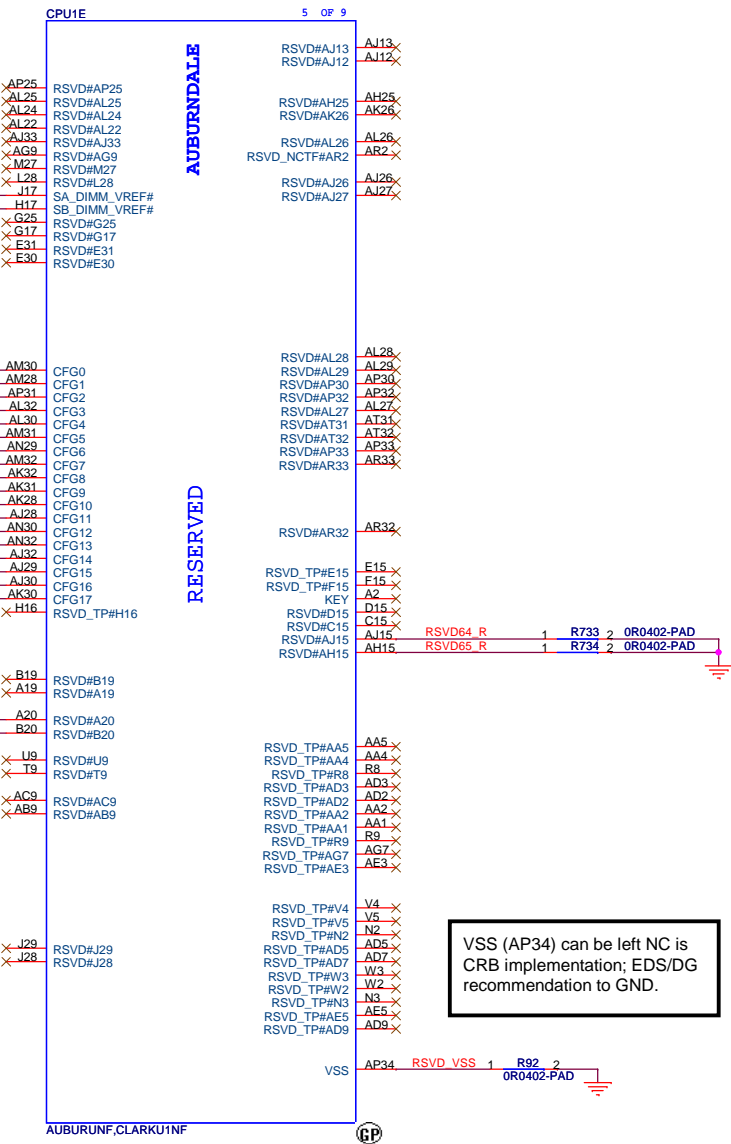
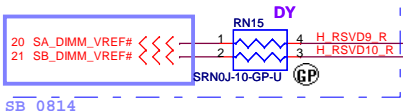
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (6/7)**

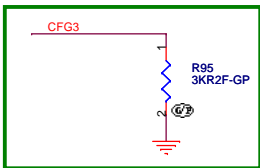
Size A3	Document Number	Rev
	JV70-CP	-1

Date: Thursday, October 08, 2009 Sheet 9 of 68

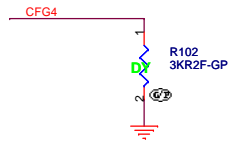
SO-DIMM VREFDQ (M3) Circuit for Clarkfield Processor



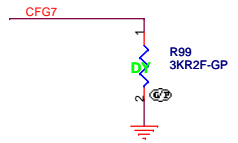
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarkfield samples.	
CFG7	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

62.10040.611 BOM change to 62.10055.321
 2ND = 62.10053.561
 3RD = 62.10055.341

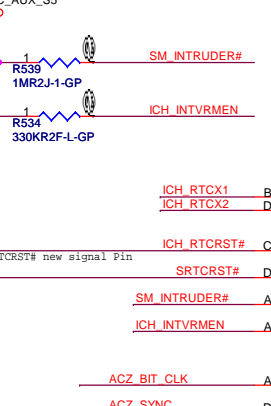
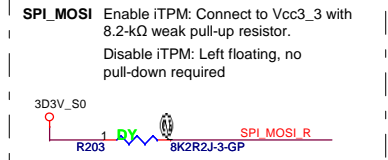
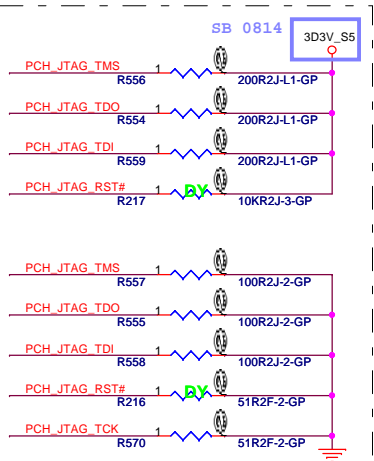
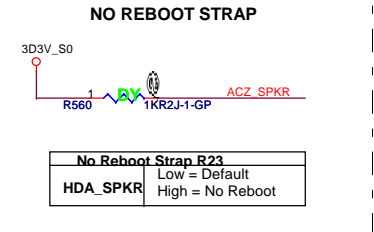
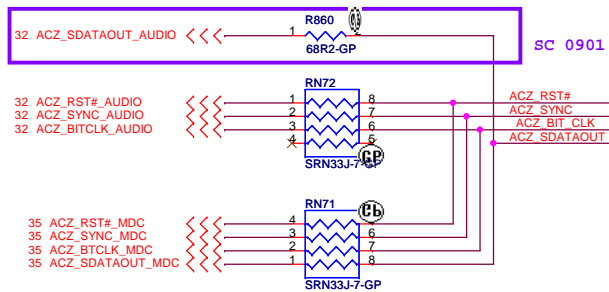
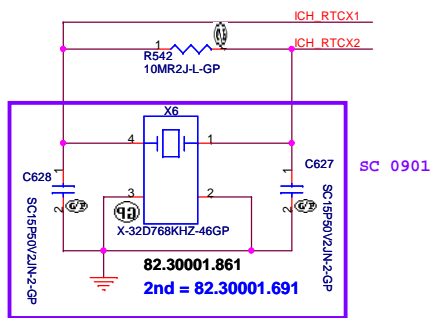
JV70-CP

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Title: **CPU (7/7)**

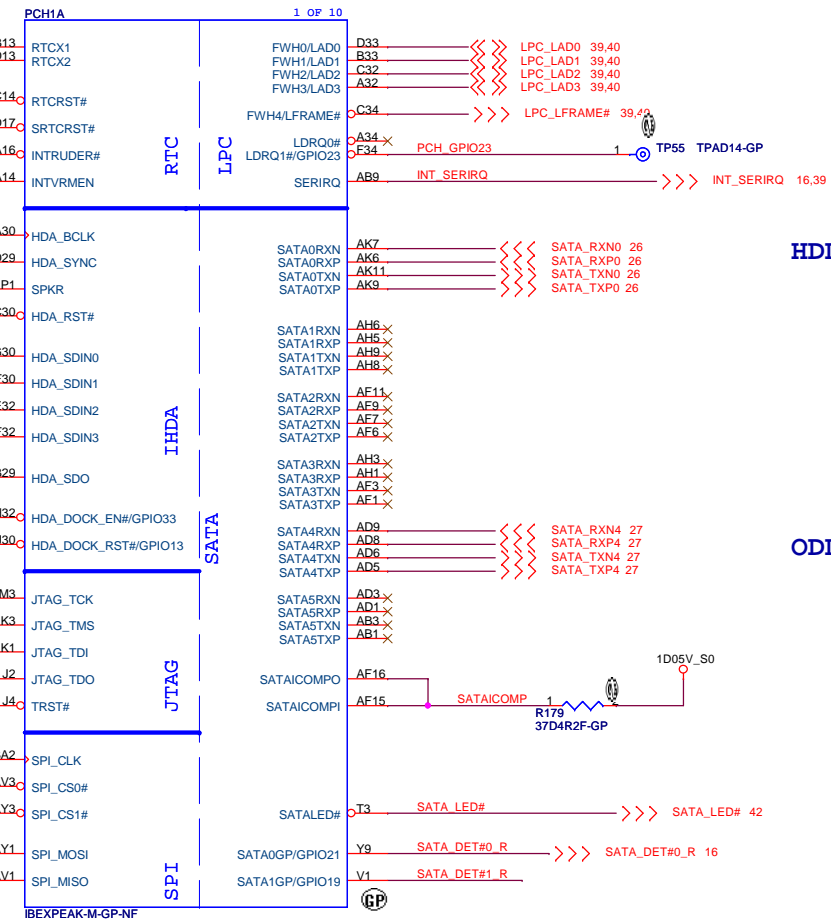
Size A3 Document Number: **JV70-CP** Rev: **-1**

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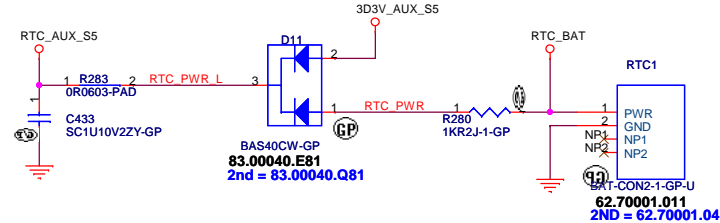
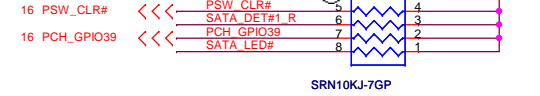
INTVRMEN- Integrated SUS
1.1V VRM Enable
High - Enable internal VRs

Integrated VccSusi_05,VccSusi_5,VccCl1_5	
INTVRMEN	High=Enable Low=Disable
Integrated VccLan1_05VccCl1_05	
LAN100_SLP	High=Enable Low=Disable



HDD

ODD



ES2 PCH verison

JV70-CP

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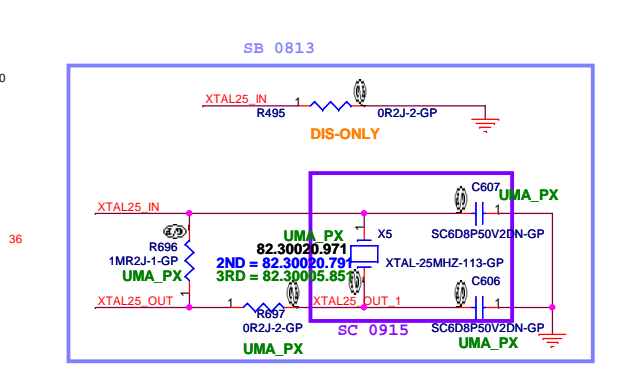
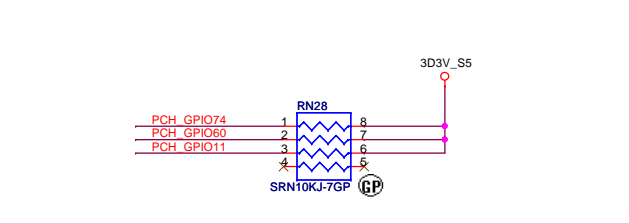
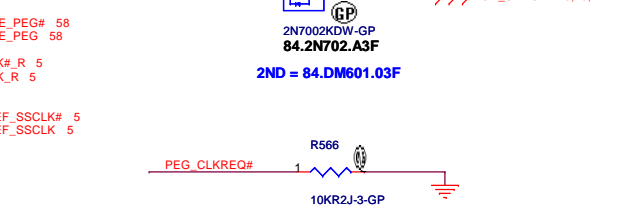
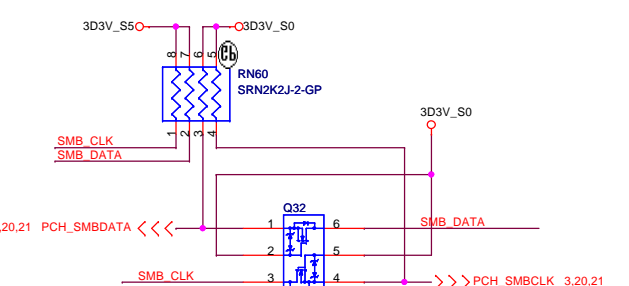
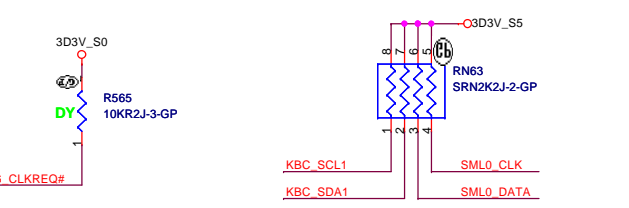
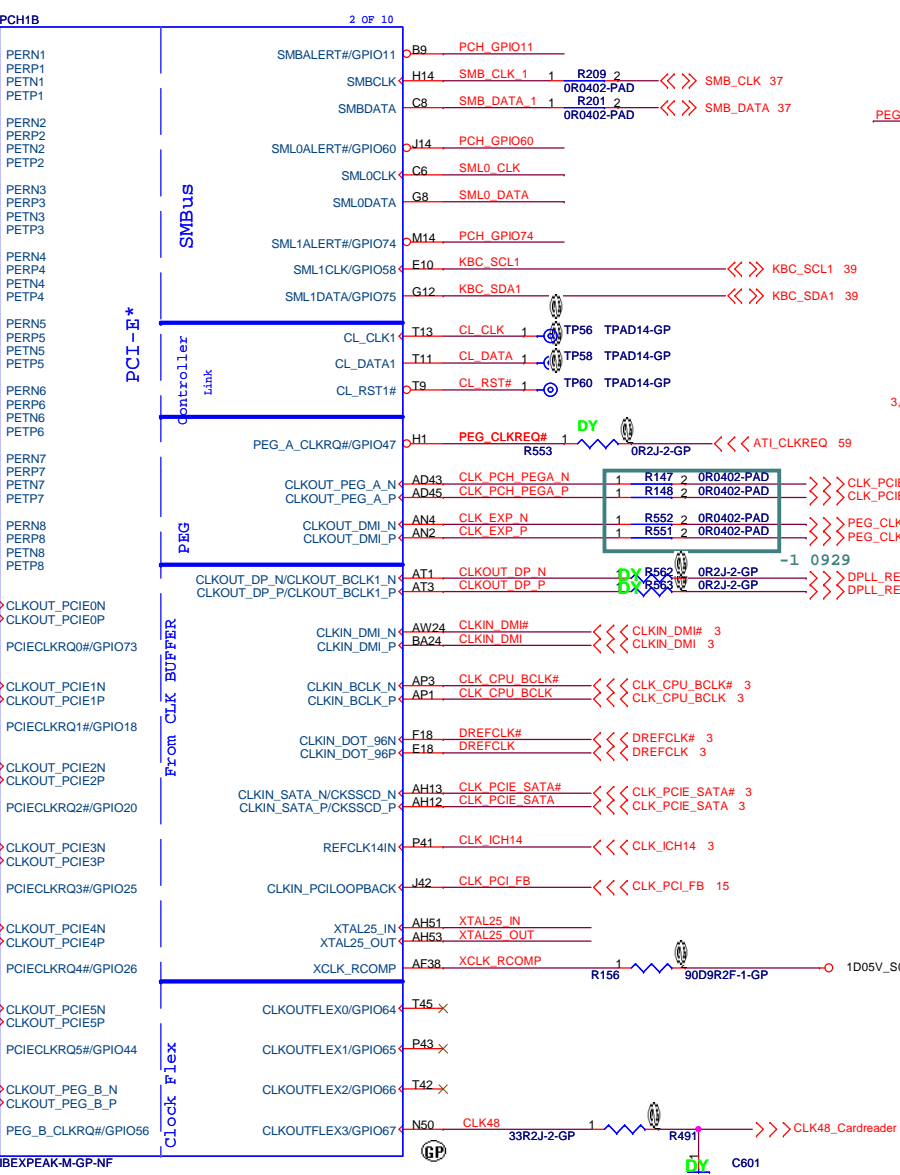
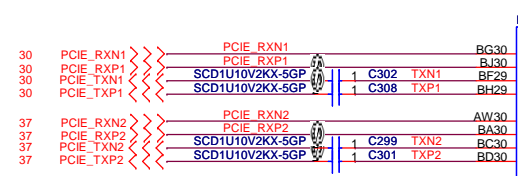
Title PCH (1/9)

Size A3 Document Number JV70-CP Rev -1

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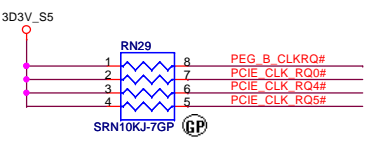
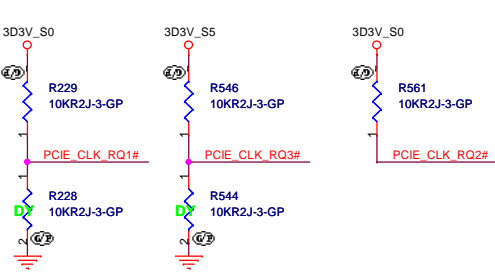
LAN

MINICARD1



PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).



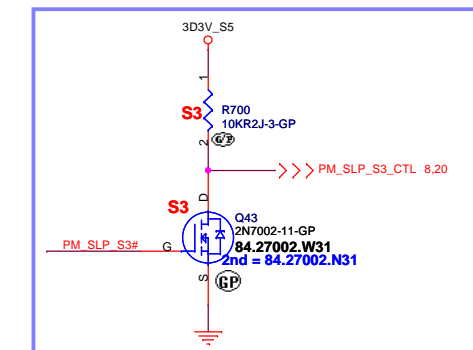
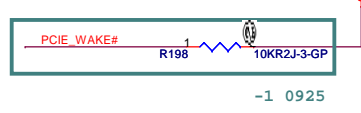
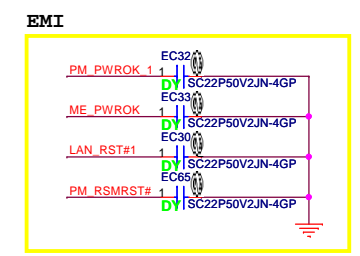
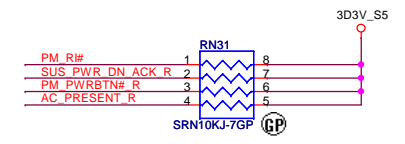
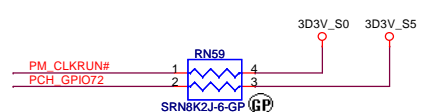
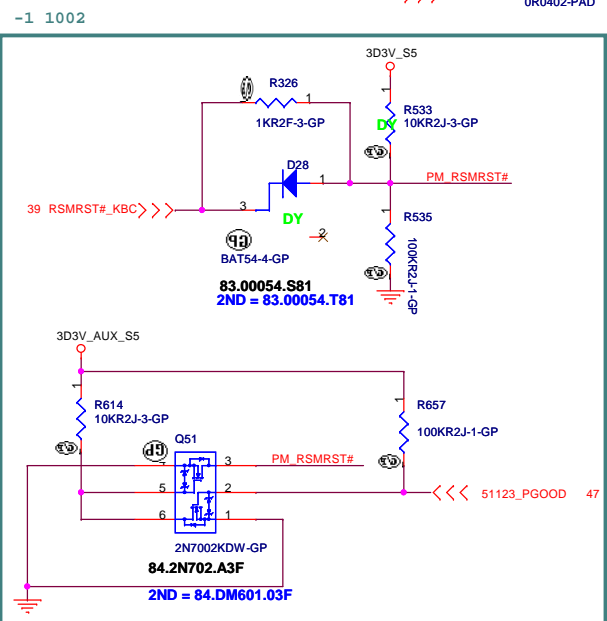
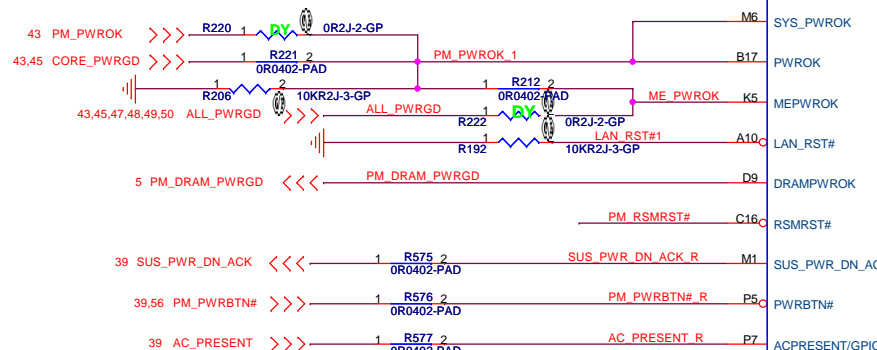
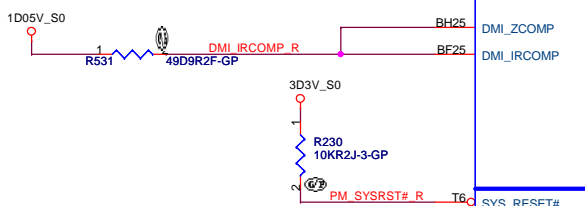
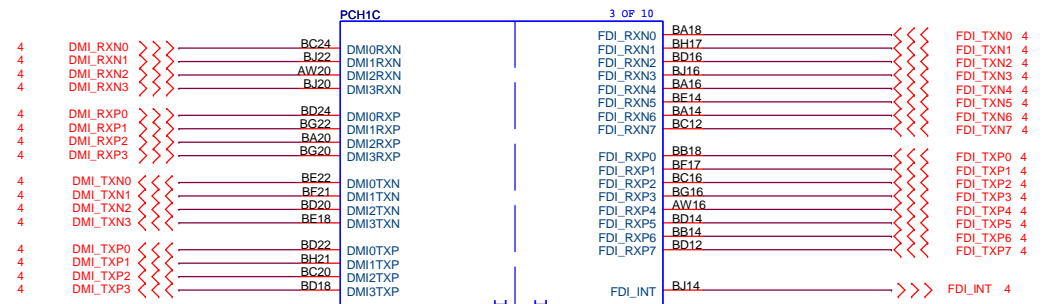
JV70-CP

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Title: **PCH (2/9)**

Size A3 Document Number: **JV70-CP** Rev: **-1**

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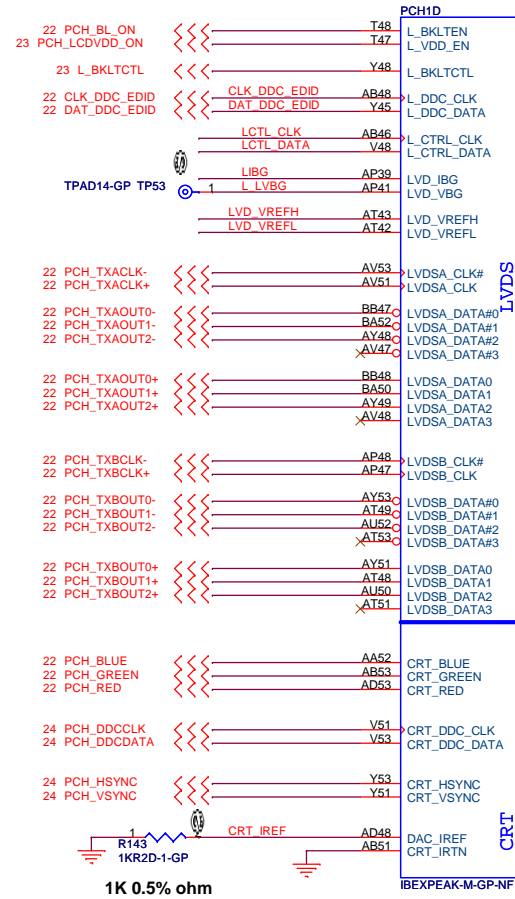
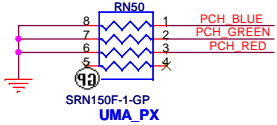
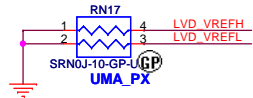
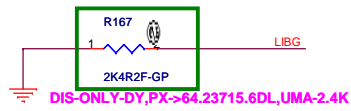
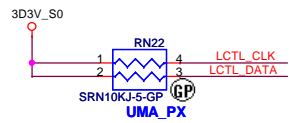
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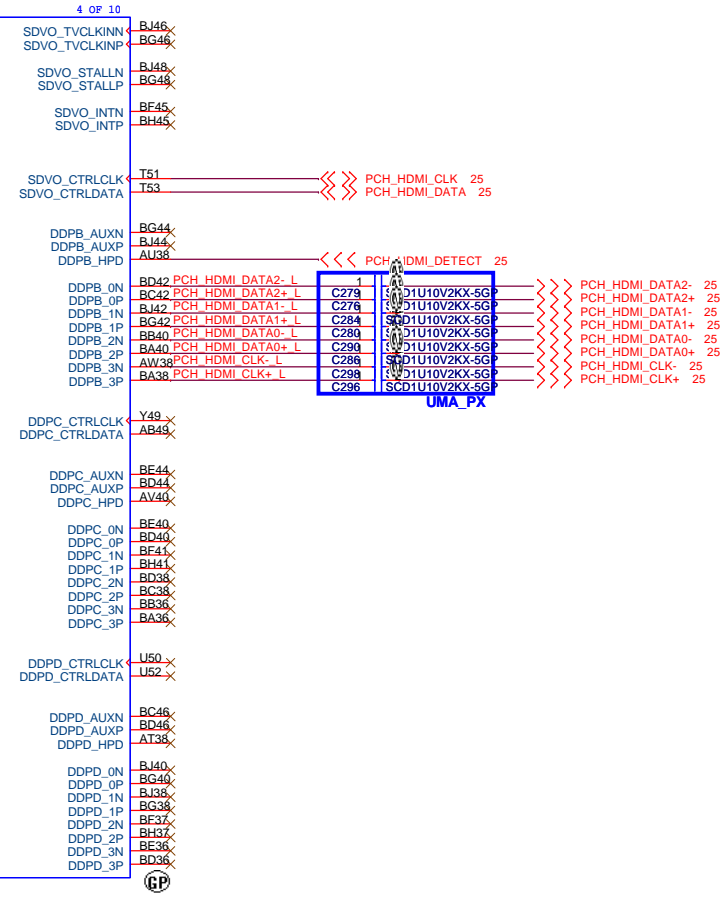
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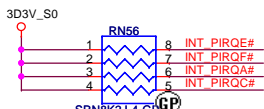
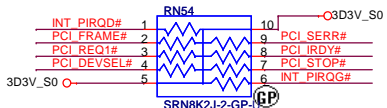
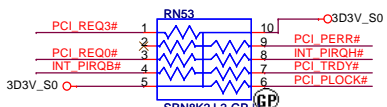
Size: A3 Document Number: **JV70-CP** Rev: **-1**

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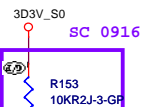
Digital Display Interface





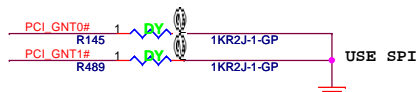
L=> DIS
H=> UMA

These pins are left as NC, because the function is disable.

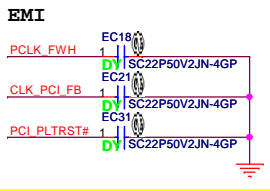


22,23,24 dGPU_SELECT# <<<

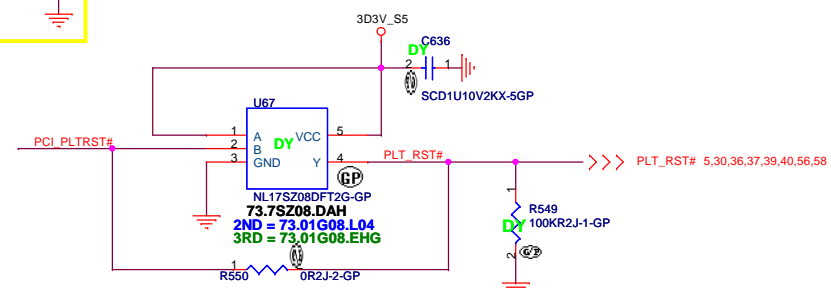
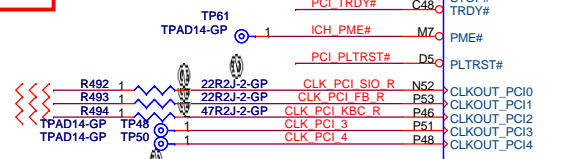
23 dGPU_PWM_SELECT# <<<



BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI



40 PCLK_FWH
12 CLK_PCI_FB
39 CLK_PCI_KBC



- H40 AD0
- N34 AD1
- C44 AD2
- A38 AD3
- C36 AD4
- J34 AD5
- A40 AD6
- D45 AD7
- E36 AD8
- H48 AD9
- E40 AD10
- C40 AD11
- M48 AD12
- M45 AD13
- F53 AD14
- M40 AD15
- M43 AD16
- J36 AD17
- K48 AD18
- F40 AD19
- C42 AD20
- K46 AD21
- M51 AD22
- J52 AD23
- K51 AD24
- L34 AD25
- F42 AD26
- J40 AD27
- G46 AD28
- F44 AD29
- M47 AD30
- H36 AD31
- J50 C/BE0#
- G42 C/BE1#
- H47 C/BE2#
- G34 C/BE3#
- G38 INT_PIRQA#
- H51 INT_PIRQB#
- B37 INT_PIRQC#
- A44 INT_PIRQD#
- F51 REQ0#
- A46 REQ1#
- E45 REQ2#
- M53 REQ3#
- F48 PCI_GNT0#
- K46 PCI_GNT1#
- F36 PCI_GNT2#
- H53 PCI_GNT3#
- B41 INT_PIROE#
- K53 INT_PIROF#
- A36 INT_PIROG#
- A48 INT_PIROH#
- K6 PCI_SERR#
- E44 PCI_SERR#
- E50 PCI_PERR#
- L34 PCI_IRDY#
- A42 PCI_IRDY#
- F46 PCI_DEVSEL#
- C46 PCI_FRAME#
- D49 PCI_PLOCK#
- D41 PCI_STOP#
- C48 PCI_TRDY#
- M7 ICH PME#
- D5 PCI_PLTRST#
- N52 CLK_PCI_SIO_R
- P53 CLK_PCI_FB_R
- P46 CLK_PCI_KBC_R
- P51 CLK_PCI_3
- P48 CLK_PCI_4

- 5 OP 10 NV_CE#0
- AY9 NV_CE#1
- BD1 NV_CE#2
- AP15 NV_CE#3
- BDE NV_DQ#0
- AV9 NV_DQ#1
- BG8 NV_DQ#2
- AP7 NV_DQ#3
- AP6 NV_DQ#4
- AT6 NV_DQ#5
- AT9 NV_DQ#6
- AV6 NV_DQ#7
- B3 NV_DQ#8
- BA4 NV_DQ#9
- BE4 NV_DQ#10
- BB6 NV_DQ#11
- BD6 NV_DQ#12
- BB7 NV_DQ#13
- BC8 NV_DQ#14
- BJ8 NV_DQ#15
- BJ6 NV_DQ#16
- BG6 NV_DQ#17
- BD3 NV_ALE
- AY6 NV_CLE
- AU2 NV_RCOMP
- AV7 NV_RB#
- AY8 NV_WR#0_RE#
- AY5 NV_WR#1_RE#
- AV11 NV_WE#_CK0
- BE5 NV_WE#_CK1
- H18 USBP0N
- J18 USBP0P
- A18 USBP1N
- C18 USBP1P
- M20 USBP2N
- F20 USBP2P
- L20 USBP3N
- J20 USBP3P
- L20 USBP4N
- F20 USBP4P
- G20 USBP5N
- A20 USBP5P
- M22 USBP6N
- N22 USBP6P
- B21 USBP7N
- D21 USBP7P
- H22 USBP8N
- J22 USBP8P
- E22 USBP9N
- F22 USBP9P
- A22 USBP10N
- C22 USBP10P
- G24 USBP11N
- H24 USBP11P
- L24 USBP12N
- M24 USBP12P
- A24 USBP13N
- C24 USBP13P
- N16 USB_OC#0
- J16 USB_OC#1
- F16 USB_OC#2
- C16 USB_OC#3
- E14 USB_OC#4
- G16 USB_OC#5
- F12 USB_OC#6
- I15 USB_OC#7
- B25 USBRBIAS#
- D25 USBRBIAS
- N16 OC0#/GPIO59
- J16 OC1#/GPIO40
- F16 OC2#/GPIO41
- C16 OC3#/GPIO42
- E14 OC4#/GPIO43
- G16 OC5#/GPIO9
- F12 OC6#/GPIO10
- I15 OC7#/GPIO14

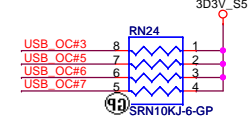
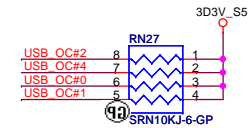
If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect.

DMI Termination Voltage		
NV_CLE	Set to Vss when low.	Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

USB

Pair	Device
0	USB1
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	NC
6	NC
7	NC
8	NC
9	USB3(HS)
10	Finger Print
11	Blue Tooth
12	NC
13	Cardreader



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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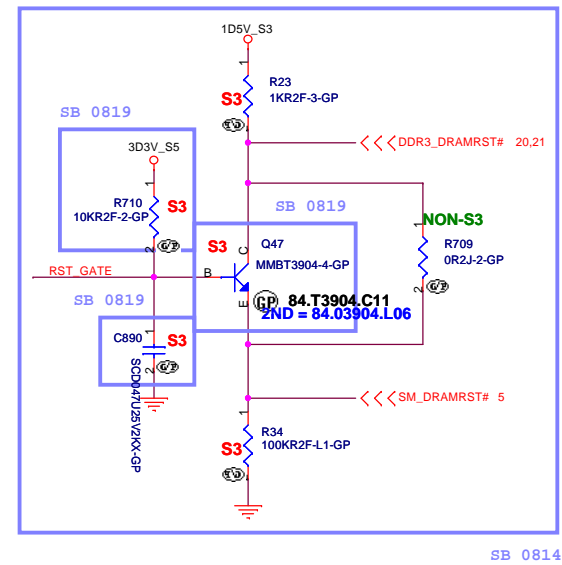
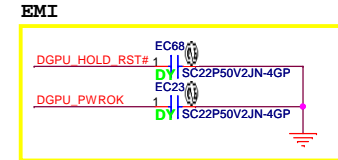
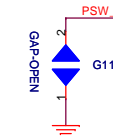
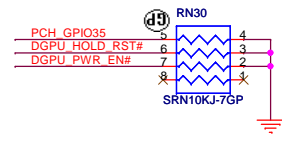
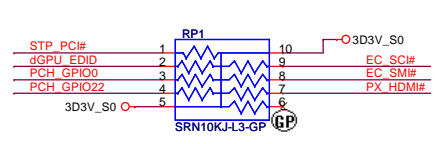
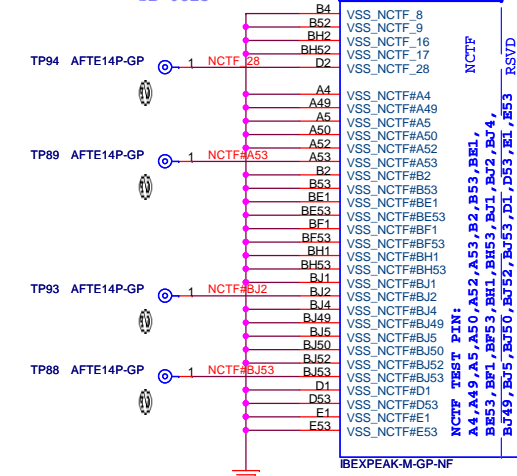
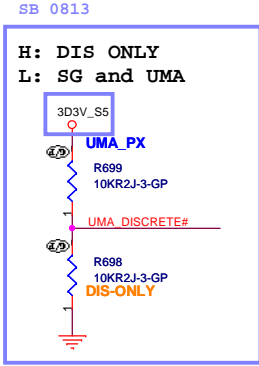
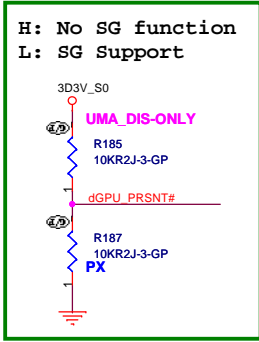
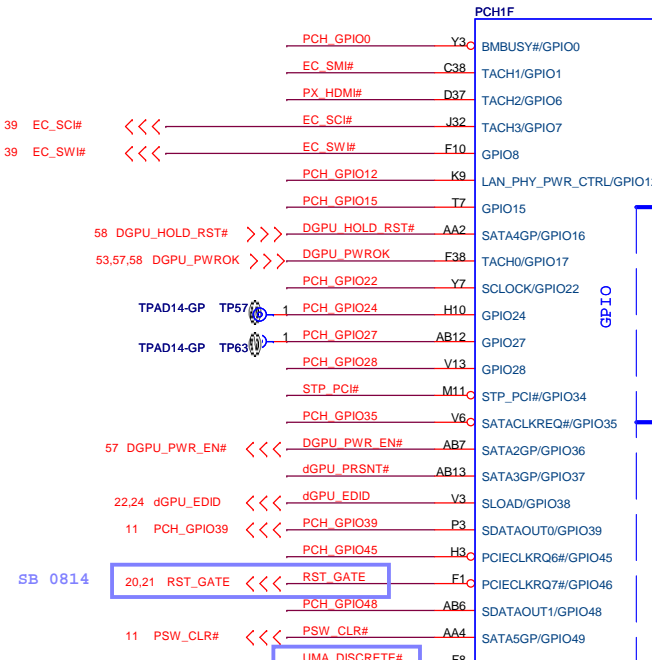
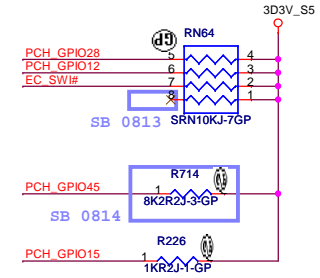
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GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



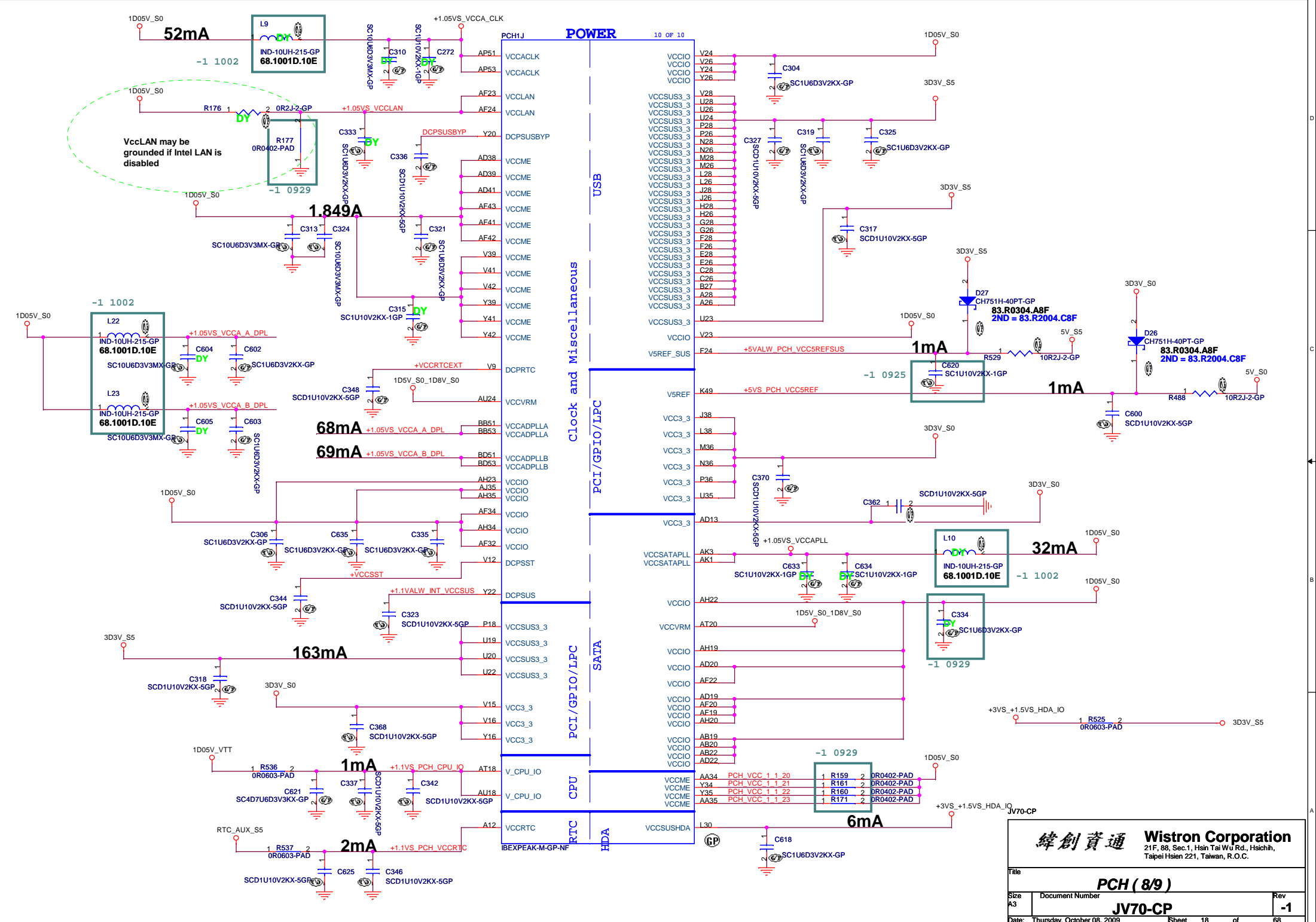
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Title: **PCH (6/9)**

Size: A3 Document Number: **JV70-CP** Rev: **-1**

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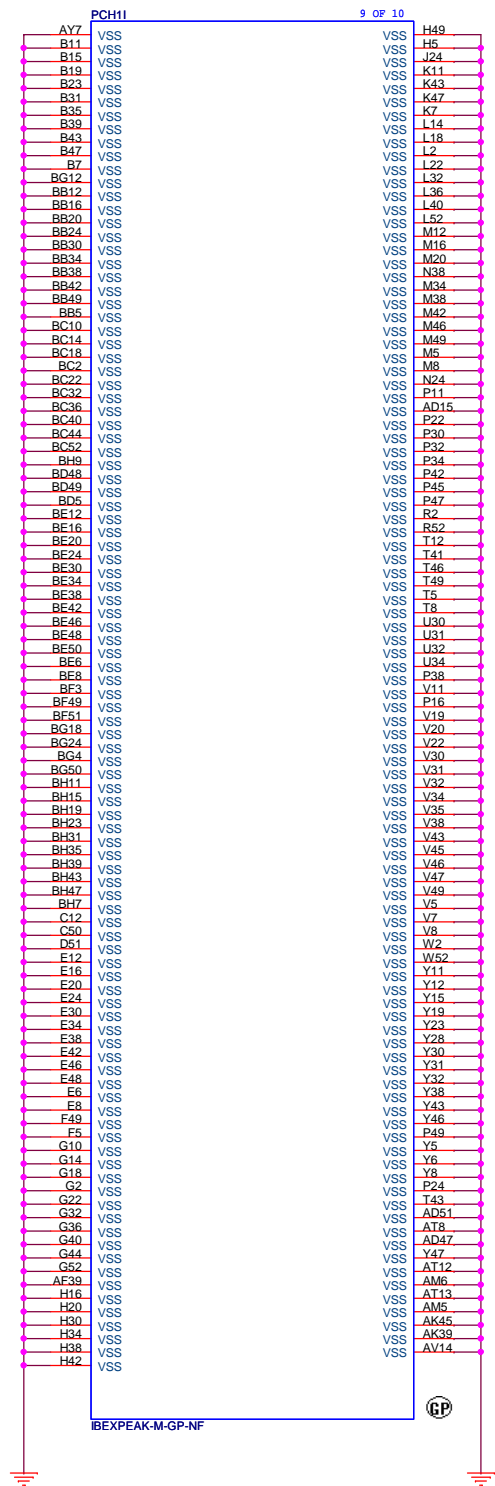
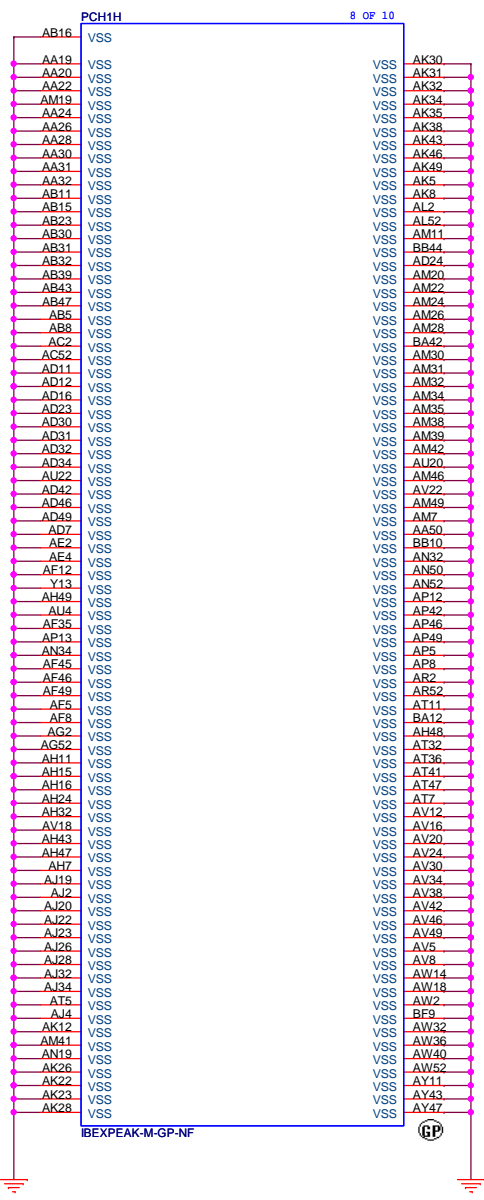


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Title: **PCH (8/9)**

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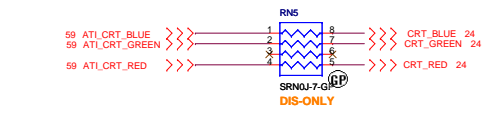
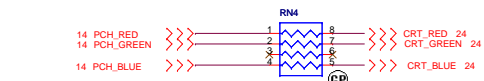
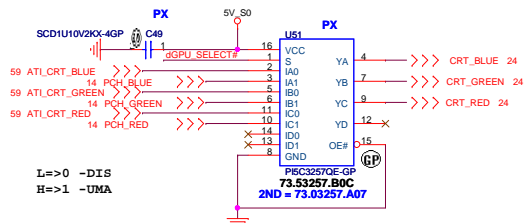
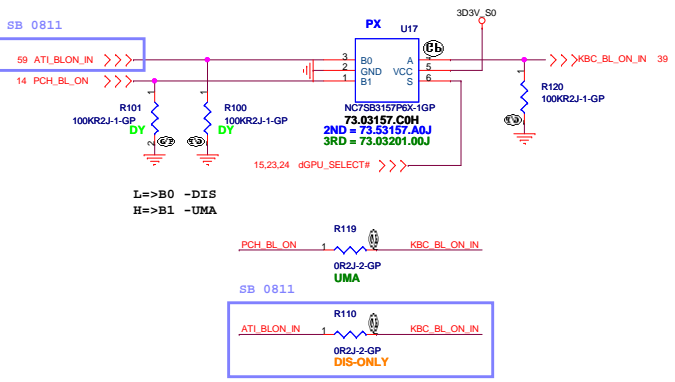
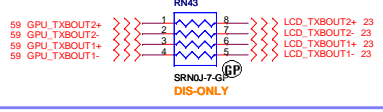
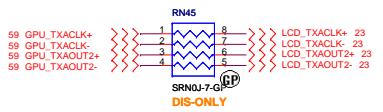
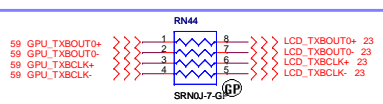
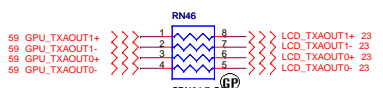
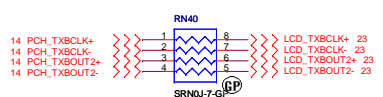
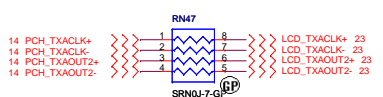
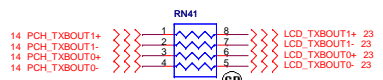
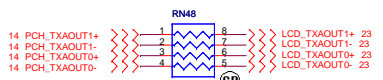
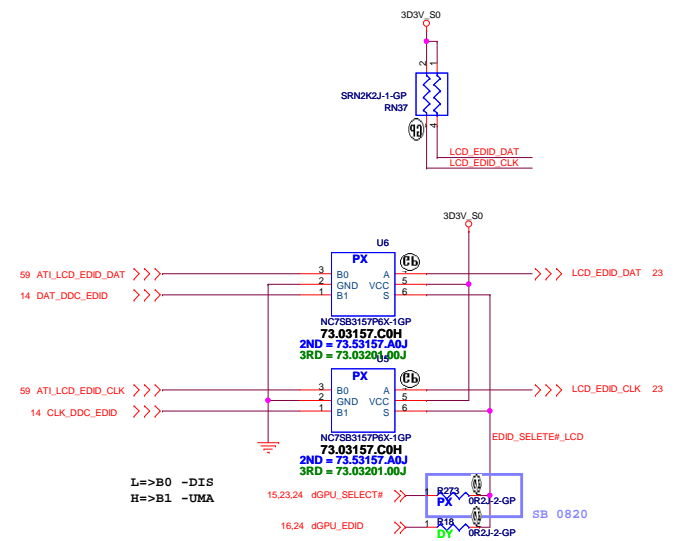
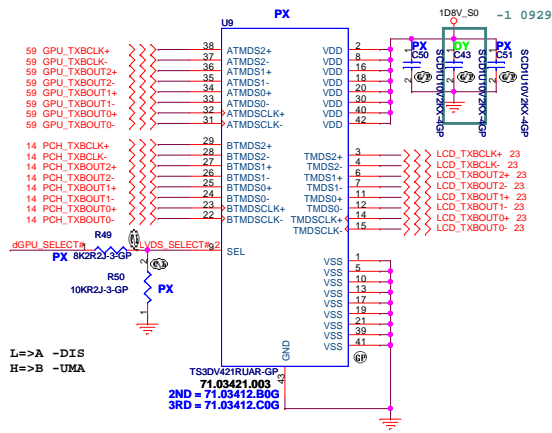
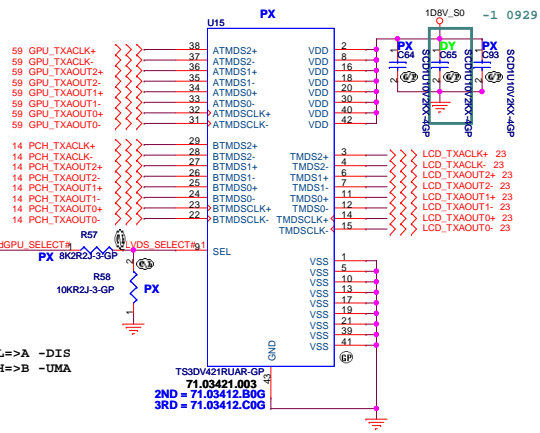
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Title: **PCH (9/9)**

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LVDS

FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLk+ = ATMDSCLk+ TMDSCLk- = ATMDSCLk- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLk+ = High Impedance BTMDSCLk- = High Impedance	TMDSn+ TMDSn- TMDSCLk+ TMDSCLk-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLk+ = BTMDSCLk+ TMDSCLk- = BTMDSCLk- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLk+ = High Impedance ATMDSCLk- = High Impedance	TMDSn+ TMDSn- TMDSCLk+ TMDSCLk-

CRT

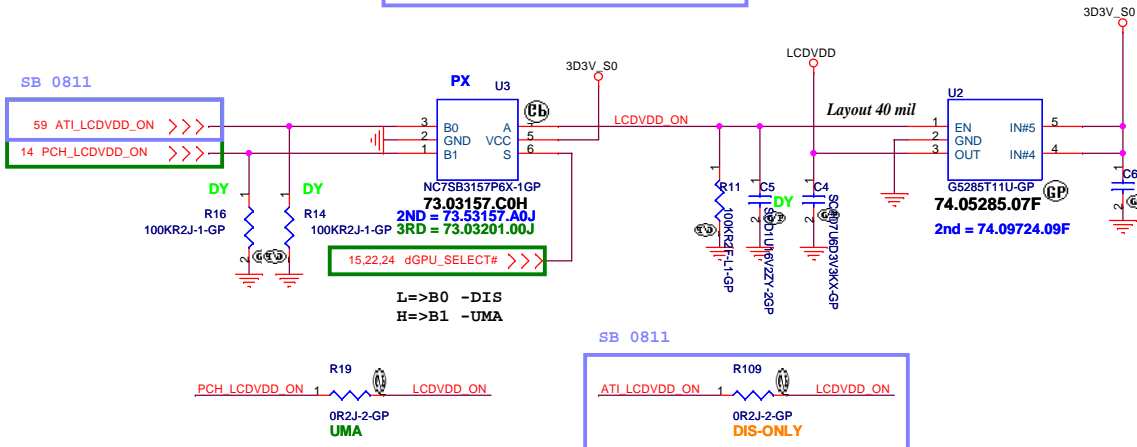
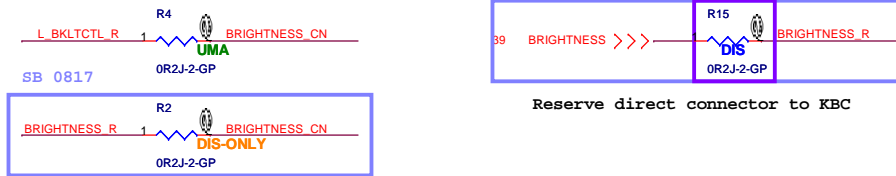
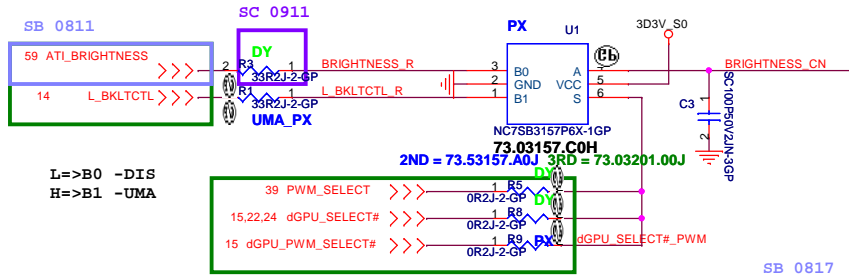
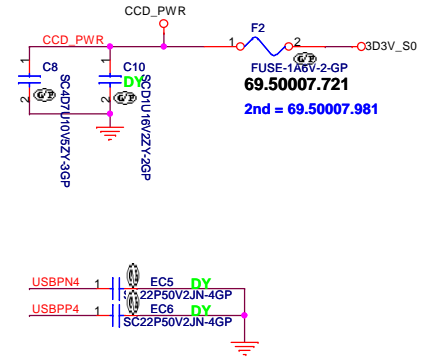
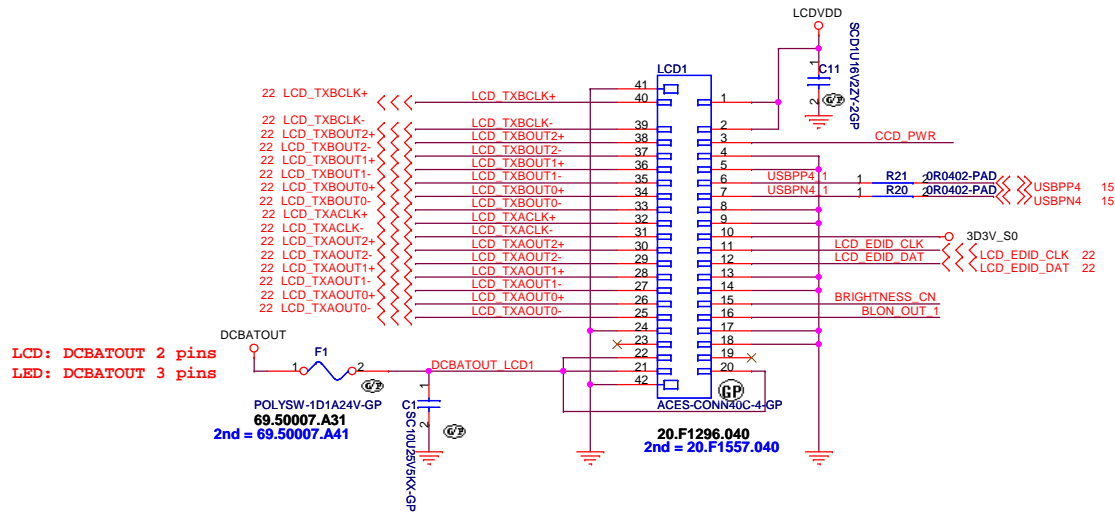
\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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File		PX SWITCH	
Size	Document Number	Rev	-1
Custom			
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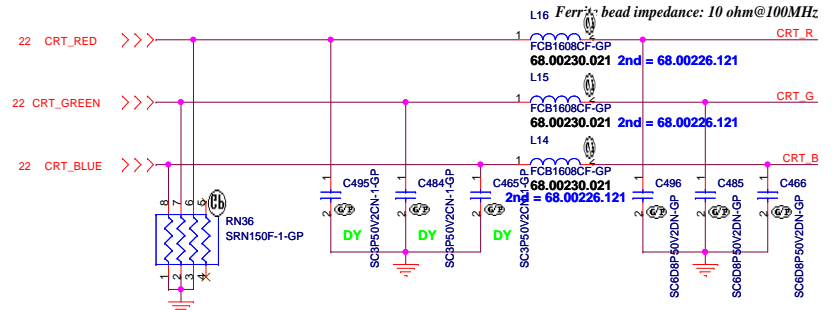
LCD/INVERTER/CCD CONN



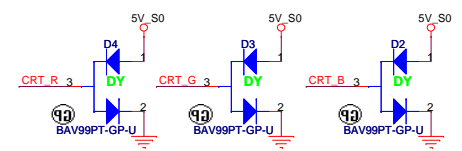
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LCD CONN			
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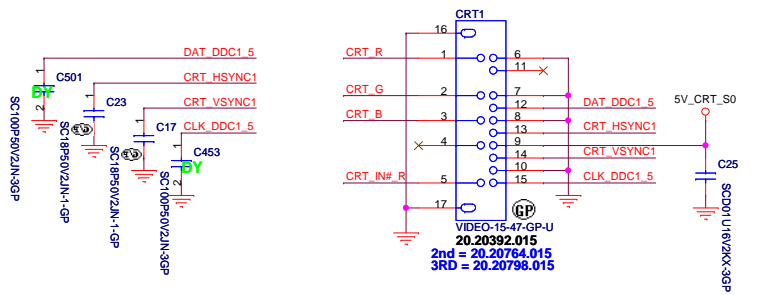
Layout Note:
Place these resistors close to the CRT-out connector



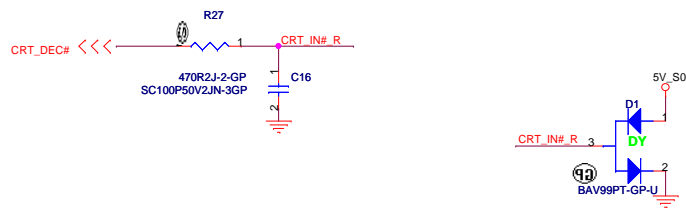
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



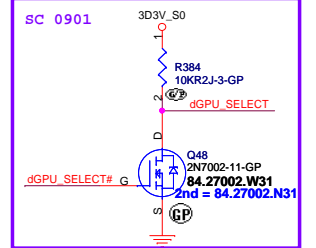
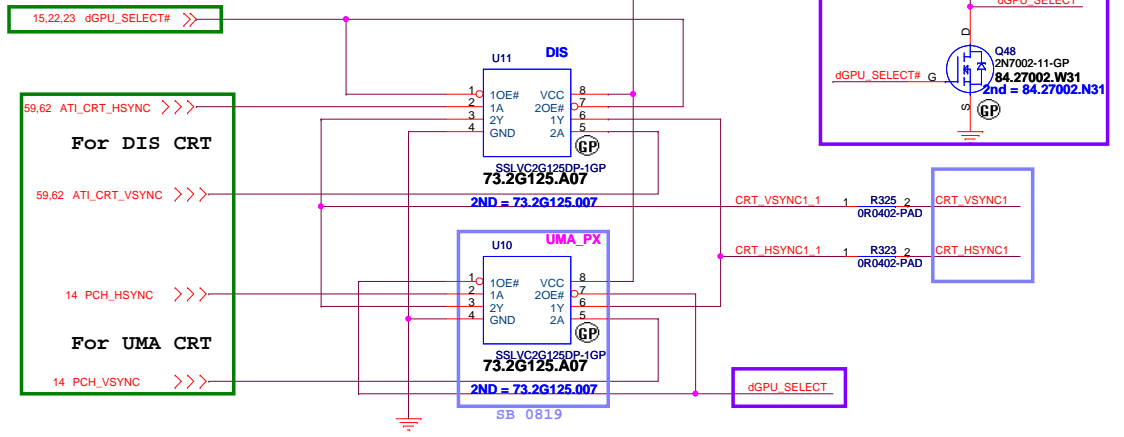
CRT I/F & CONNECTOR



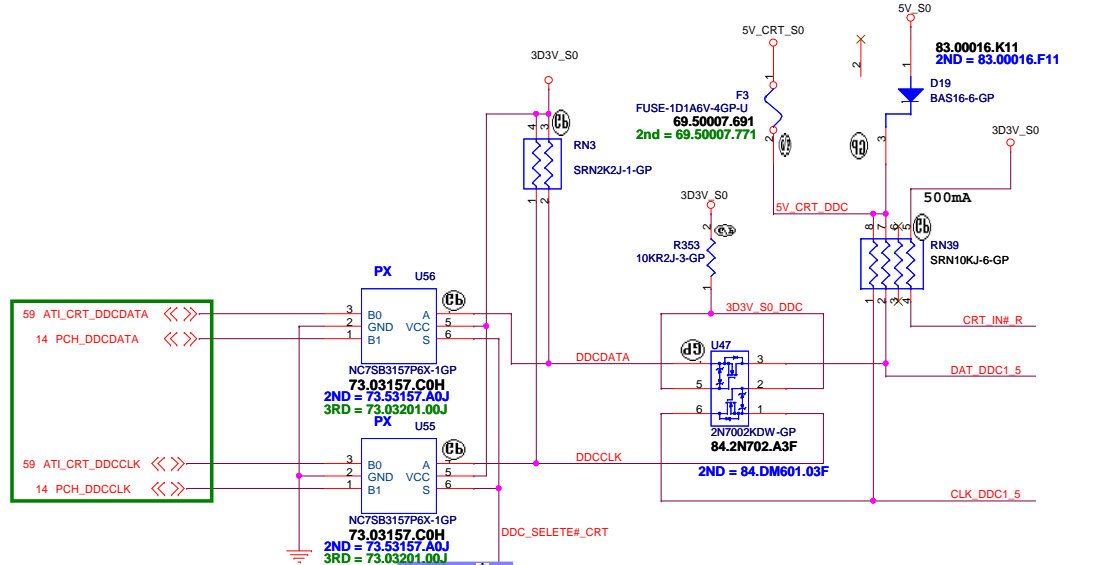
- 6
- 1
- 7
- 2
- 8
- 3
- 9
- 4
- 10
- 5



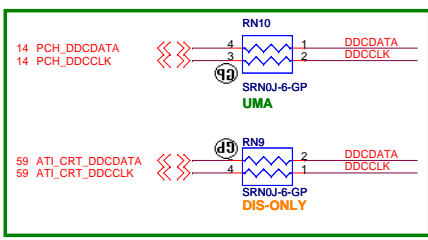
L=> DIS
H=> UMA



DDC_CLK & DATA level shift



L=>B0 -DIS
H=>B1 -UMA

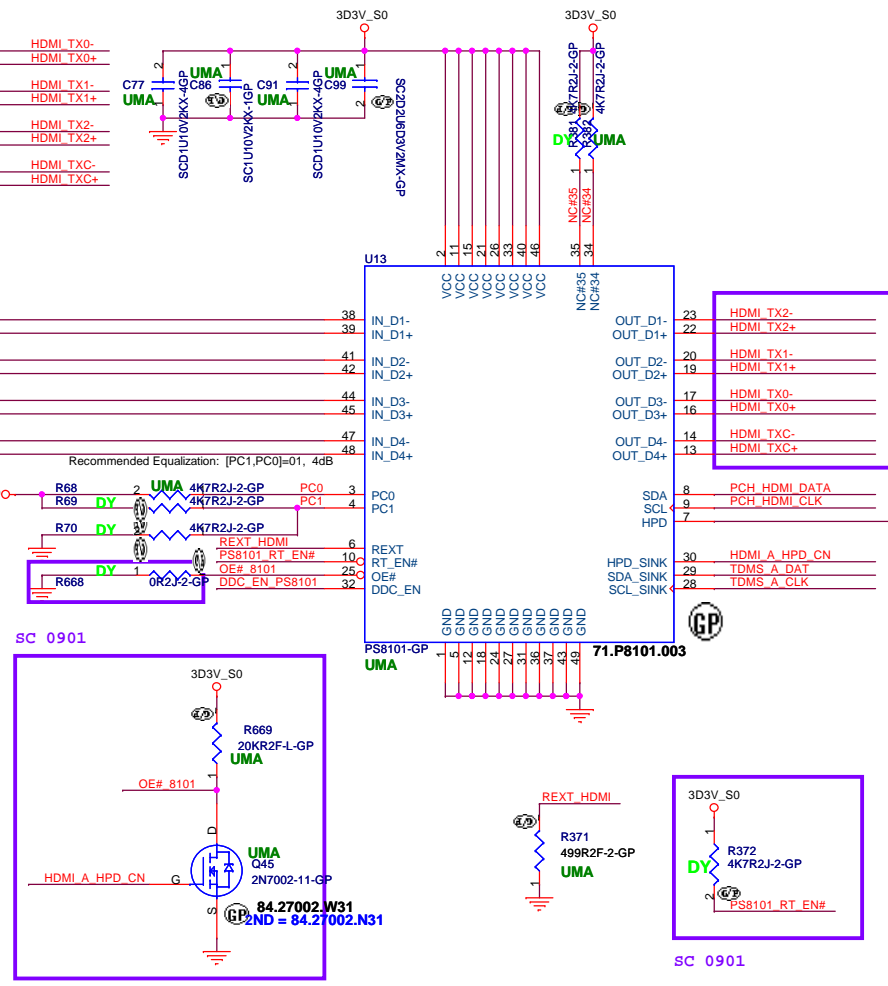
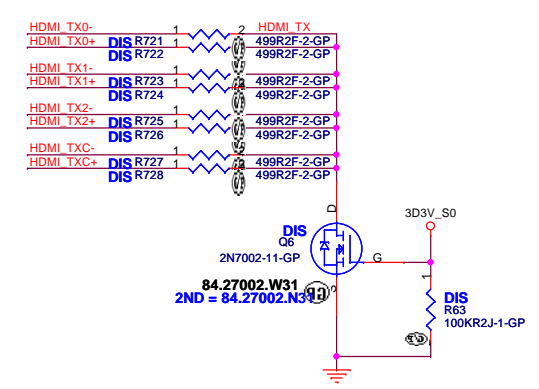
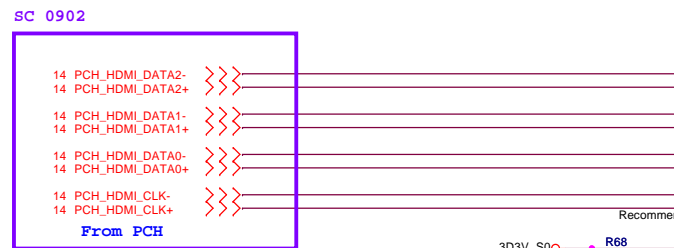
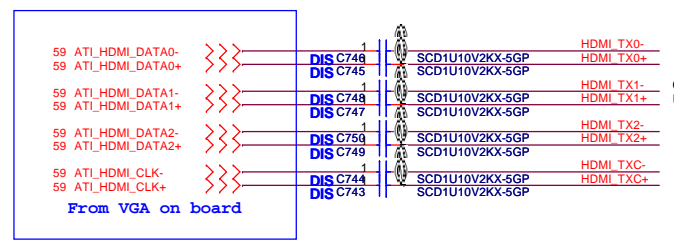
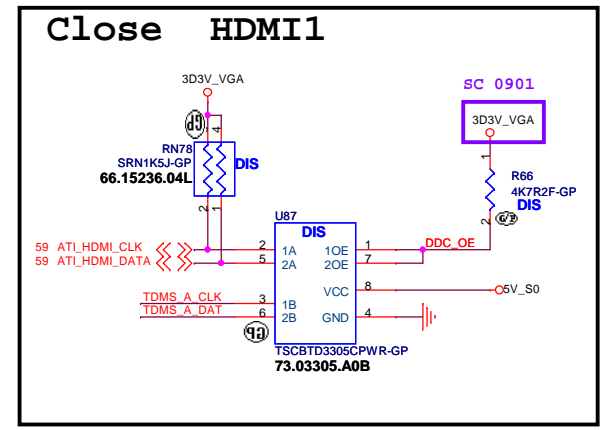
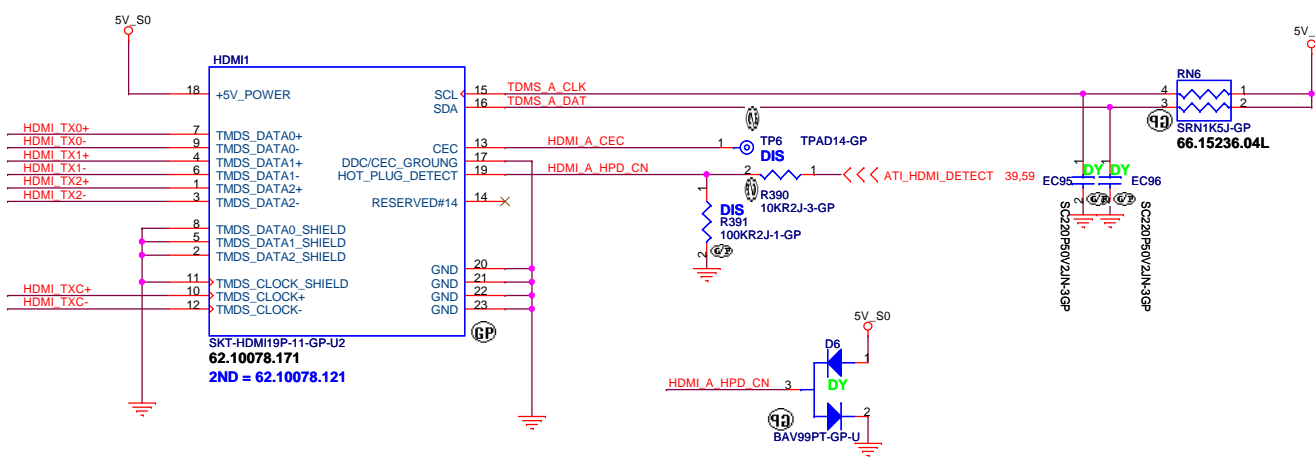


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT CONN**

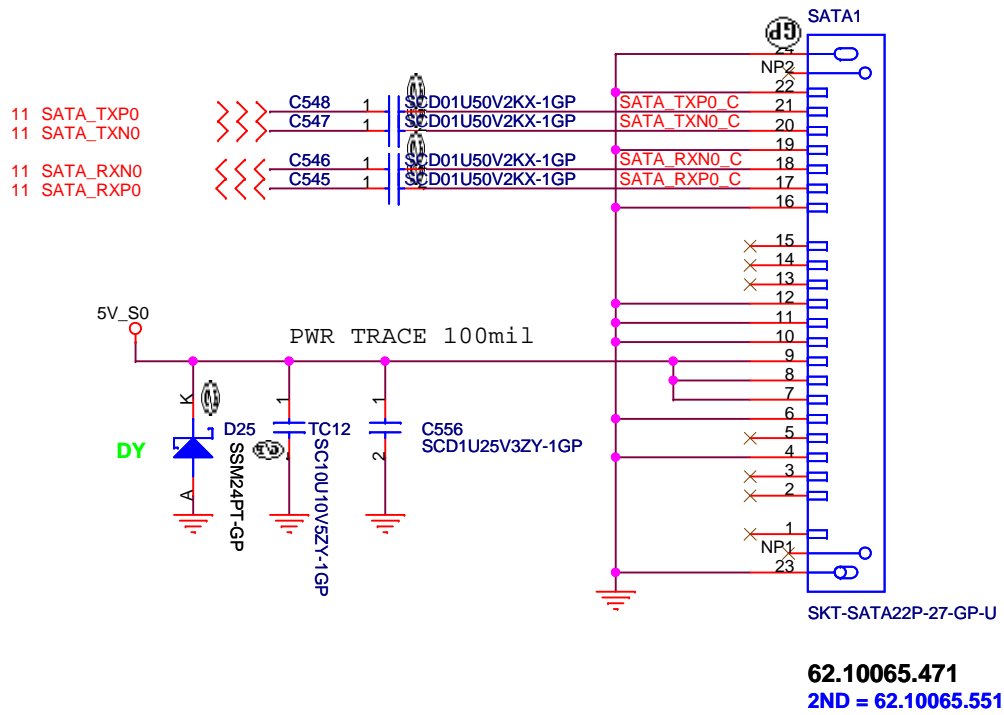
Size: Document Number: **JV70-CP**

Date: Thursday, October 08, 2009 Sheet 24 of 68



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
HDMI CONNECTOR	
Title:	Document Number:
Size:	Rev:
JV70-CP	
Date: Thursday, October 06, 2009	Sheet 25 of 57

SATA Connector

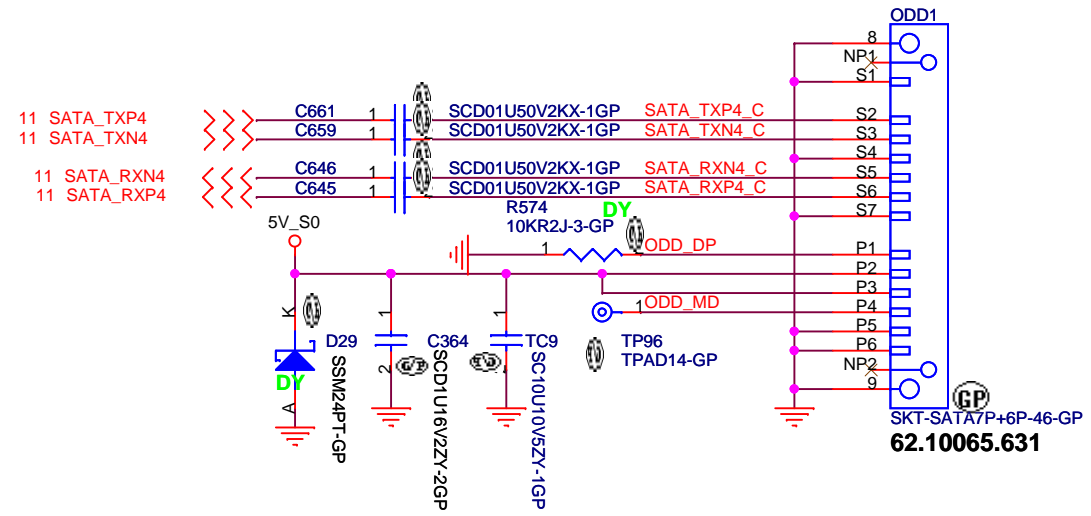


JV70-CP

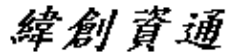
	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
---	---

Title			HDD CONN
Size	Document Number	Rev	
	JV70-CP	-1	
Date:	Thursday, October 08, 2009	Sheet	26 of 68

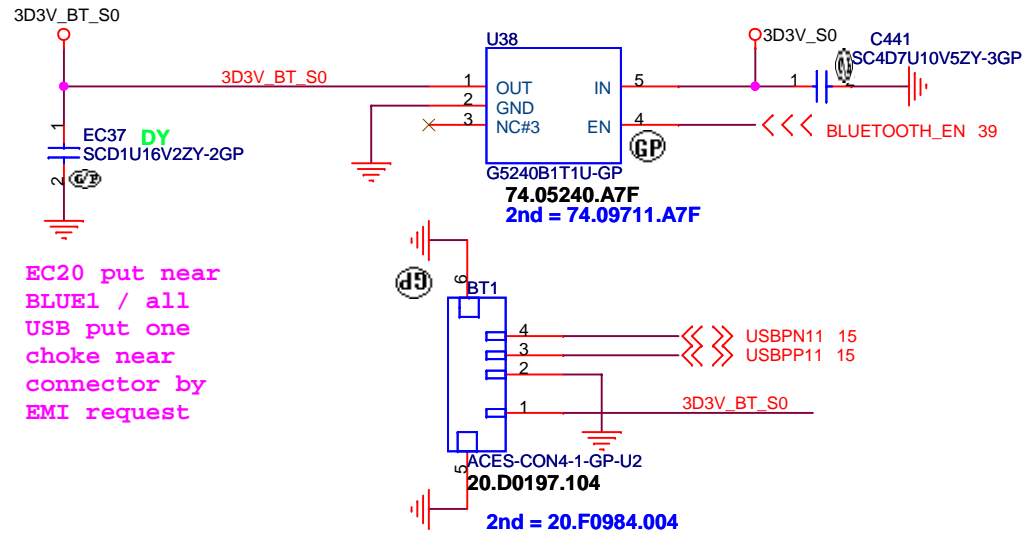
ODD Connector



JV70-CP

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
ODD	
Size	Document Number
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BLUETOOTH MODULE



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Taipei Hsien 221, Taiwan, R.O.C.

Title

BLUETOOTH

Size

Document Number

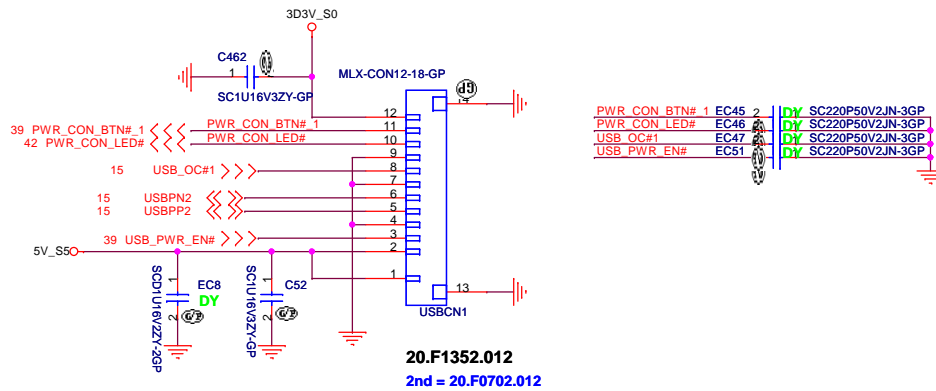
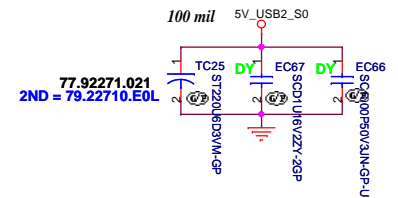
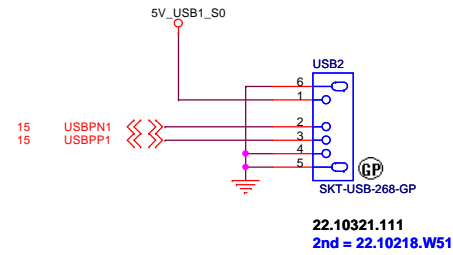
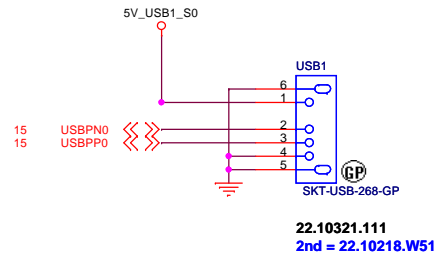
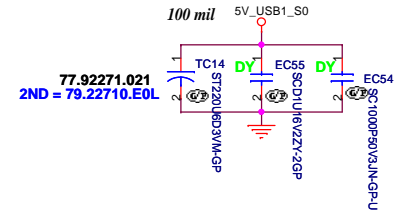
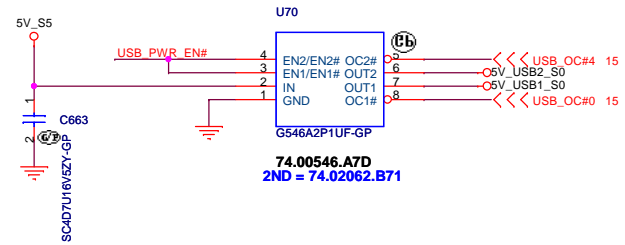
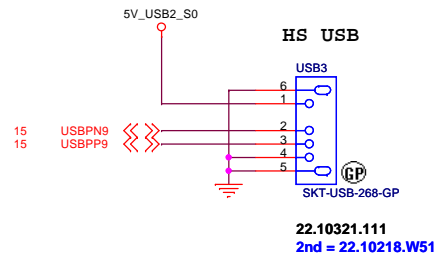
Rev

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Date: Thursday, October 08, 2009

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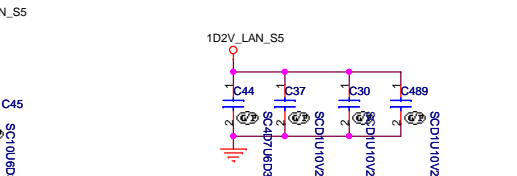
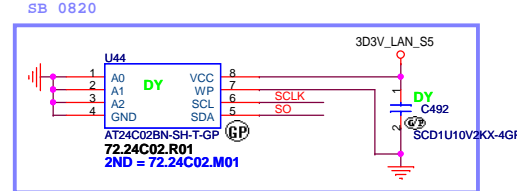
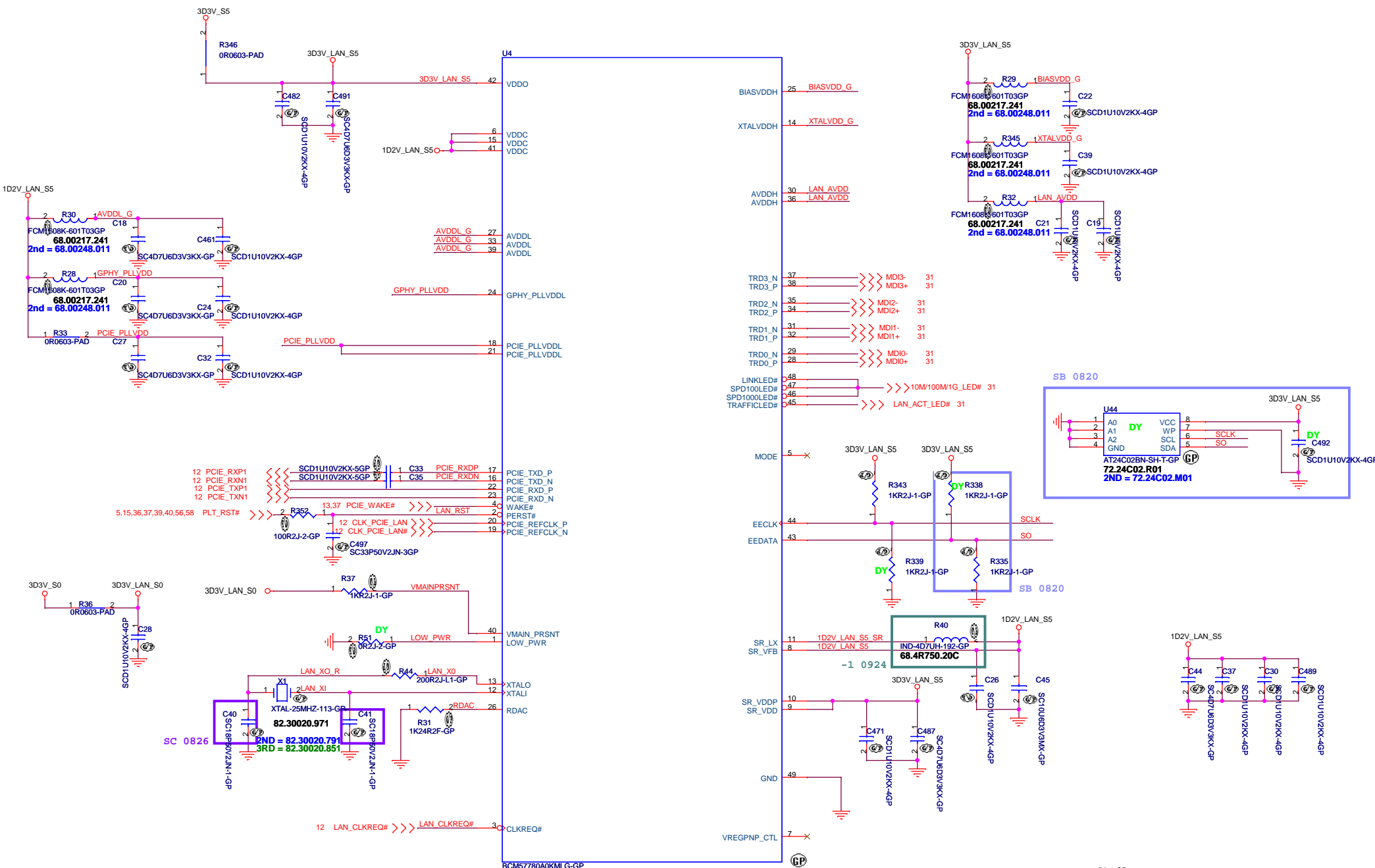
JV70-CP

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB CONN**

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71.57780.M01
BOM change to 71.57780.M04

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **BCM57780**

Size	Document Number	Rev
Custom	JV70-CP	-1

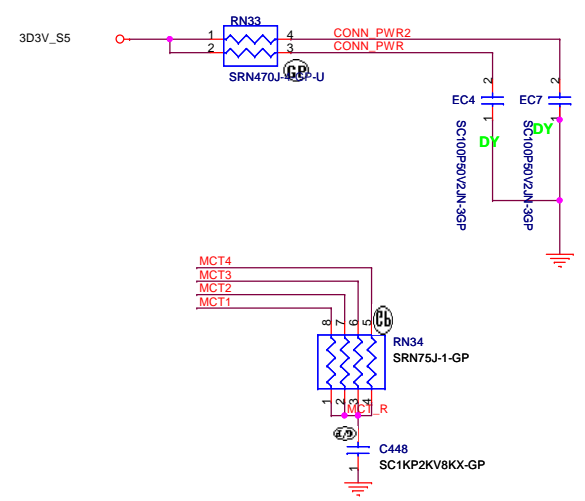
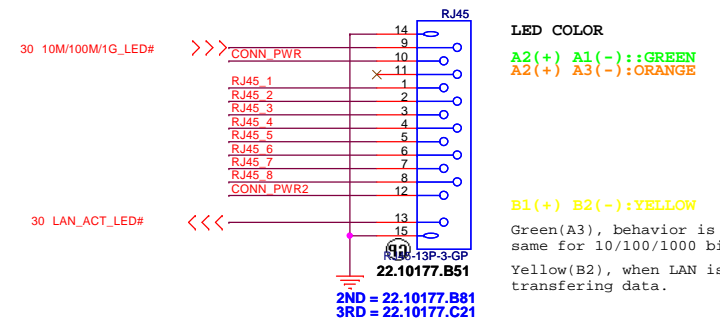
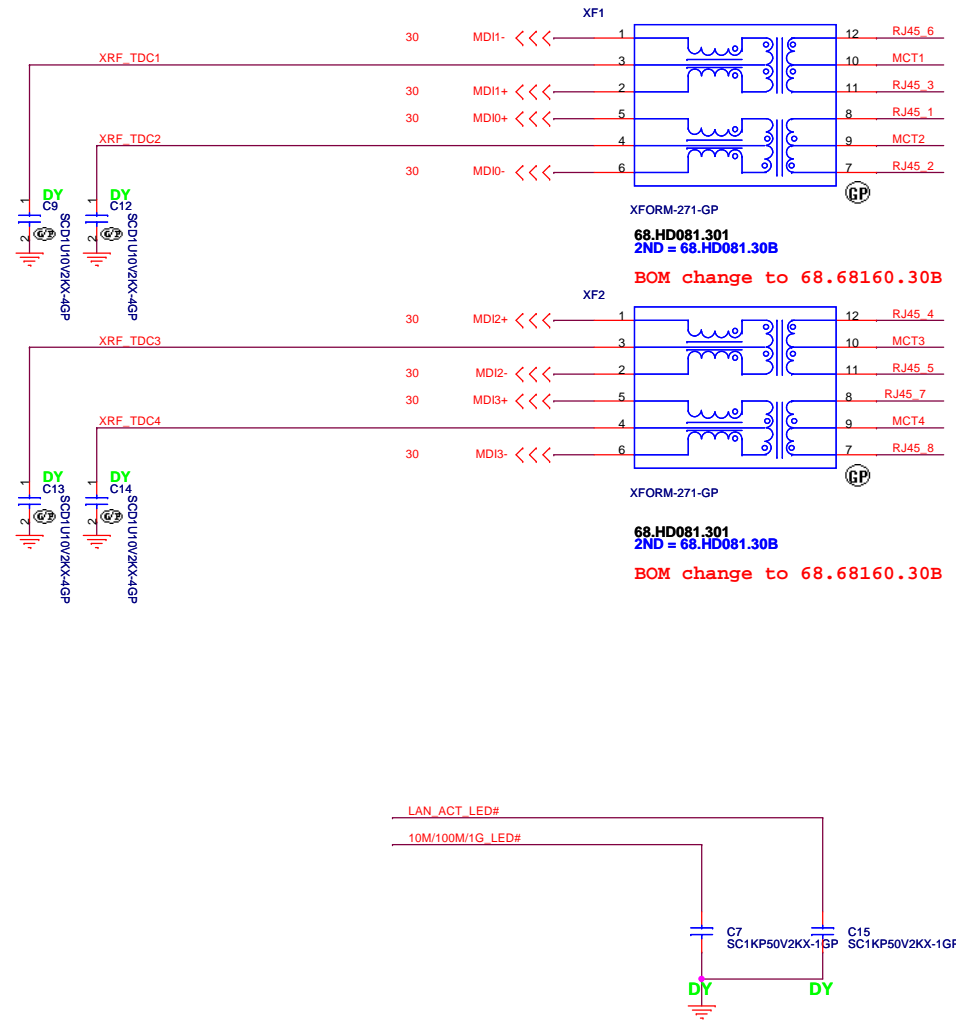
Date: Thursday, October 08, 2009 Sheet 30 of 68

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

LAN Connector

GIGA Lan Transformer

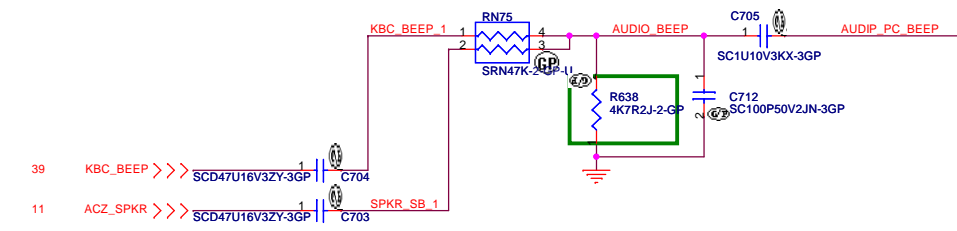
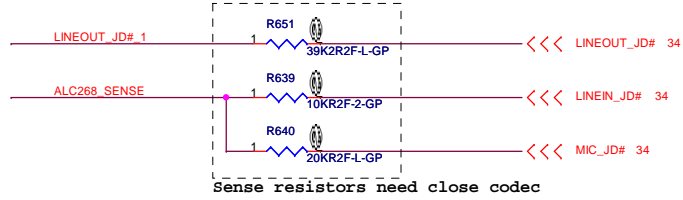
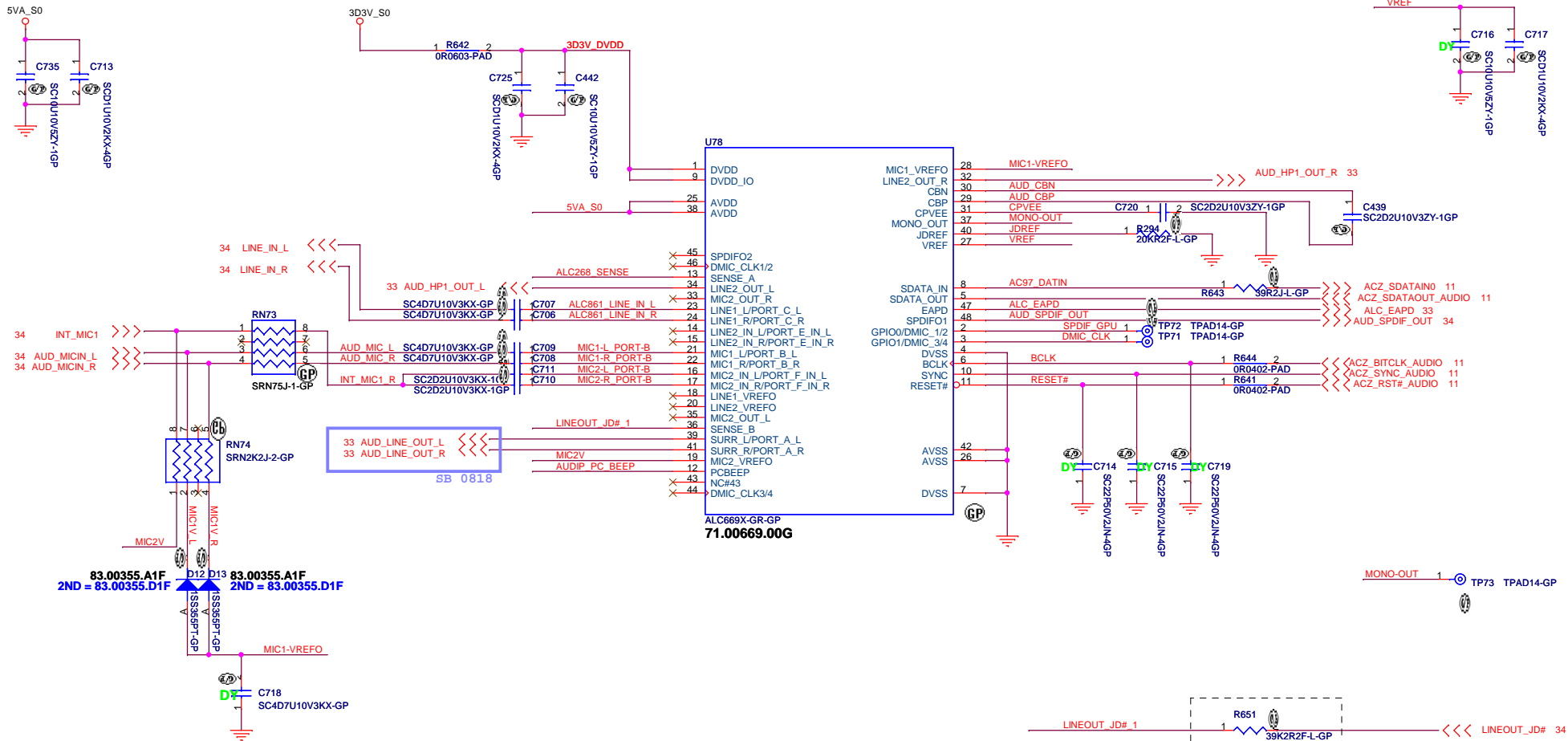


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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

Size: A3	Document Number: JV70-CP	Rev: -1
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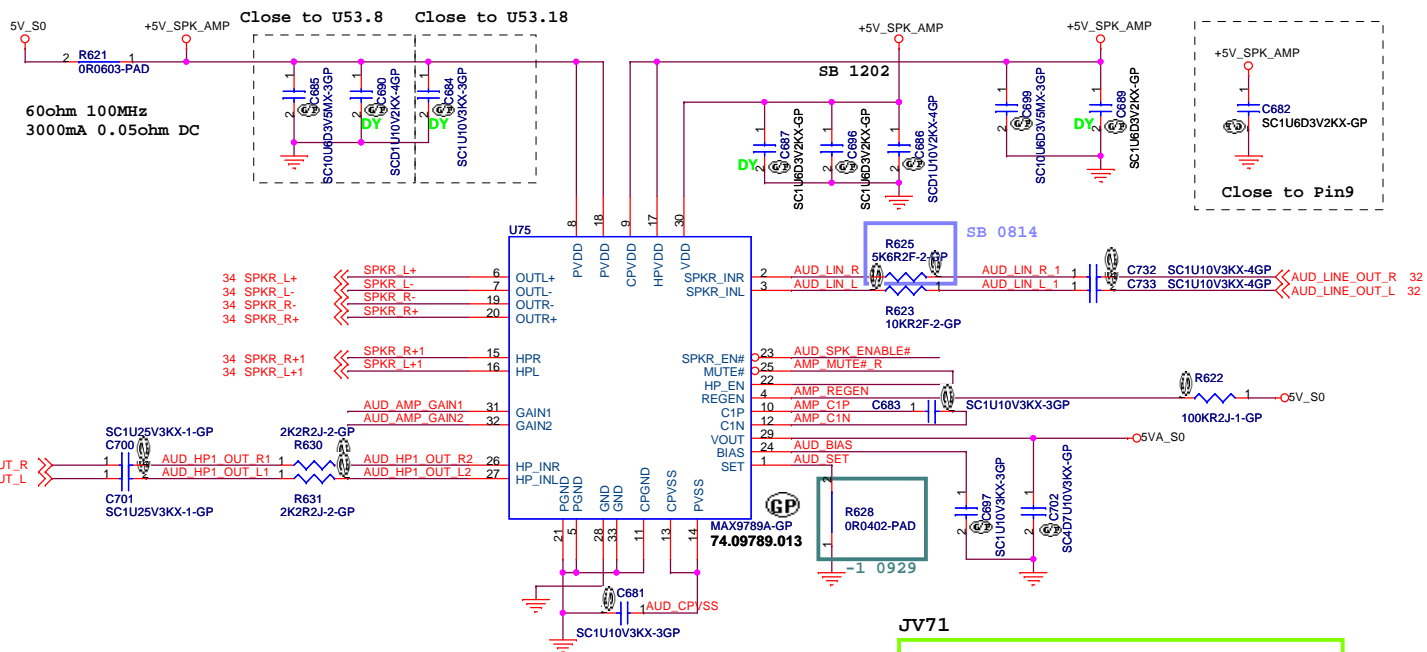
JV70-CP

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC669X**

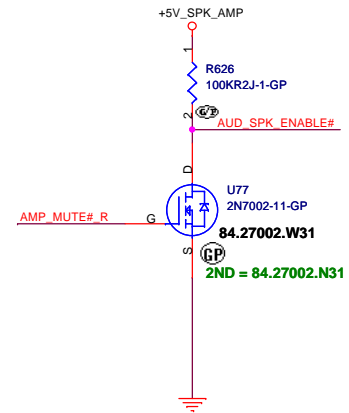
Size A3	Document Number	Rev
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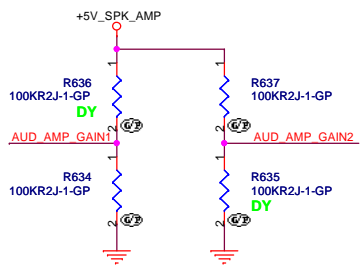


BOM change to 74.09789.B13

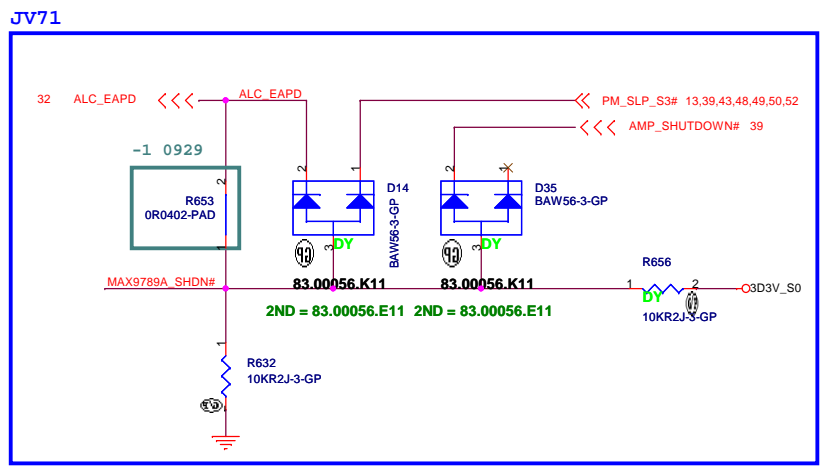
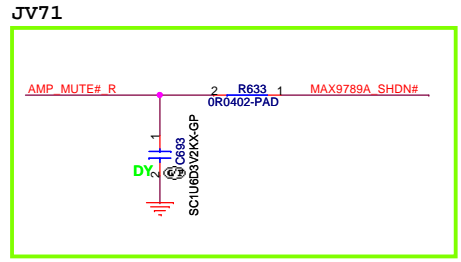
Signal inverter for speaker shutdown



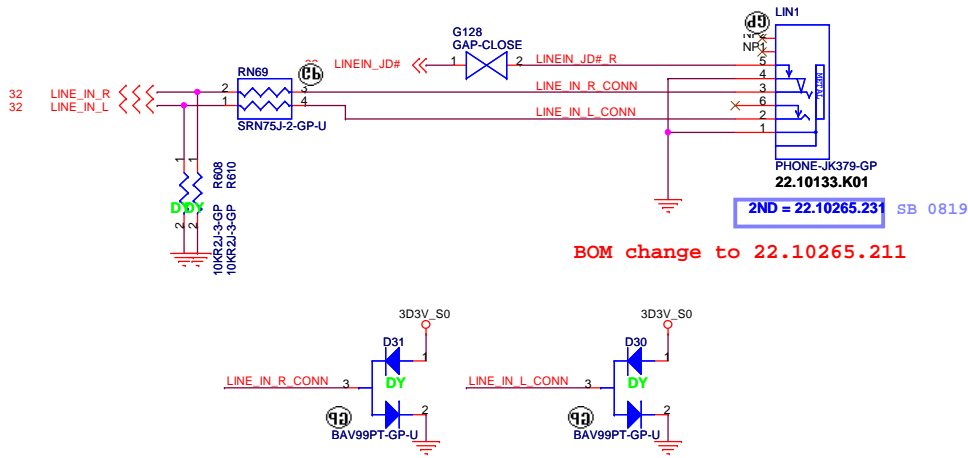
GAIN SETTING



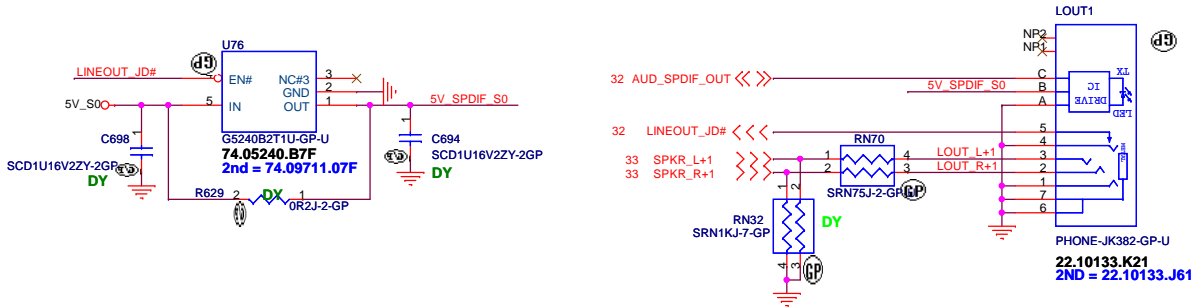
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



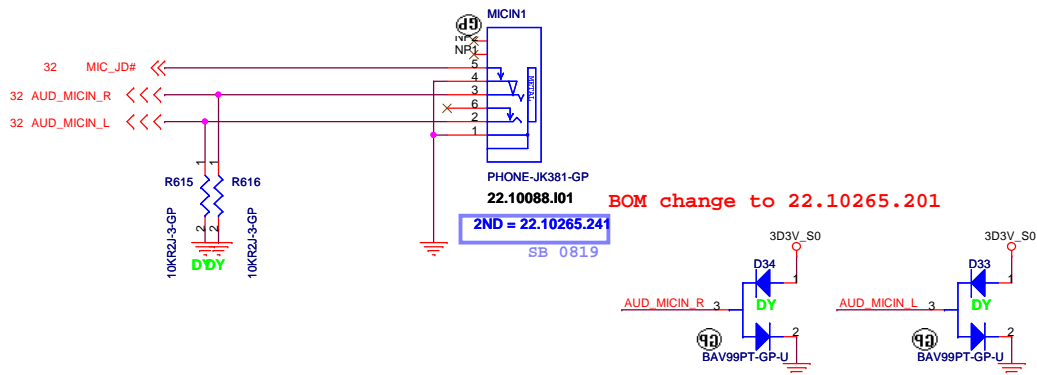
LINE IN



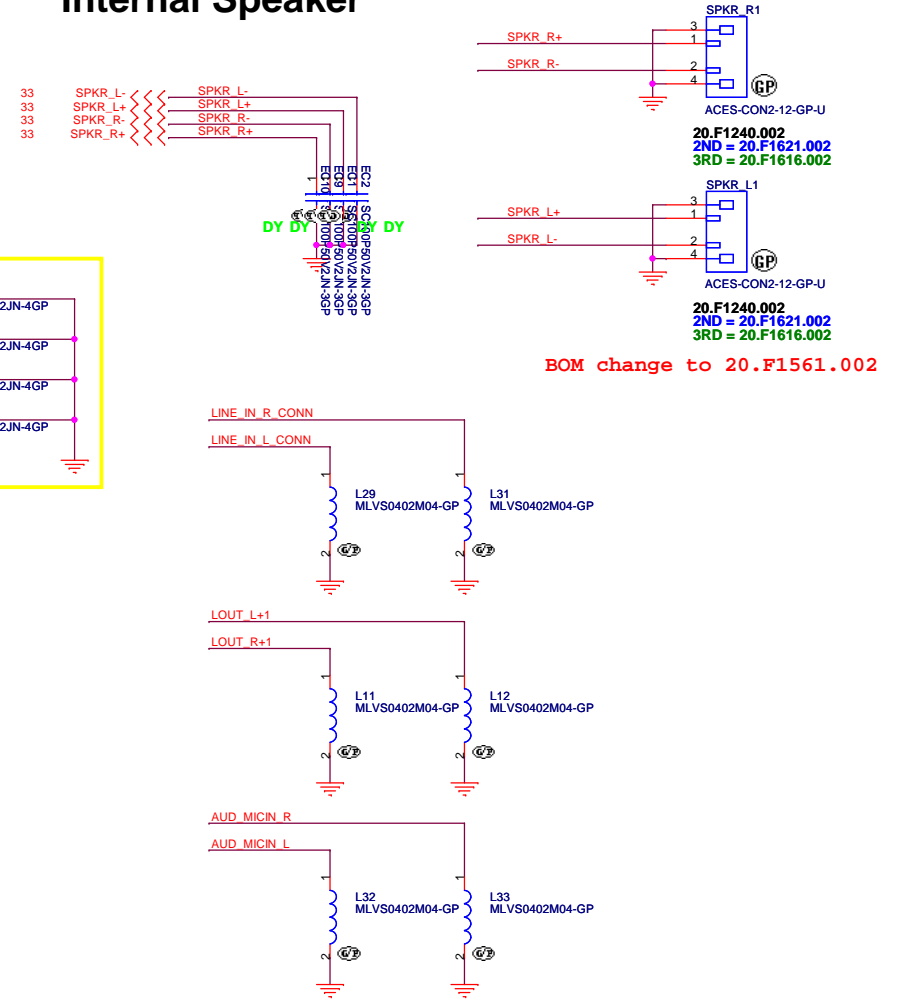
LINE OUT



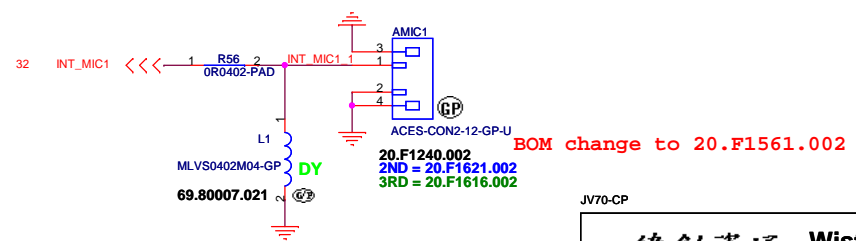
MIC IN



Internal Speaker



Internal Mic



JV70-CP

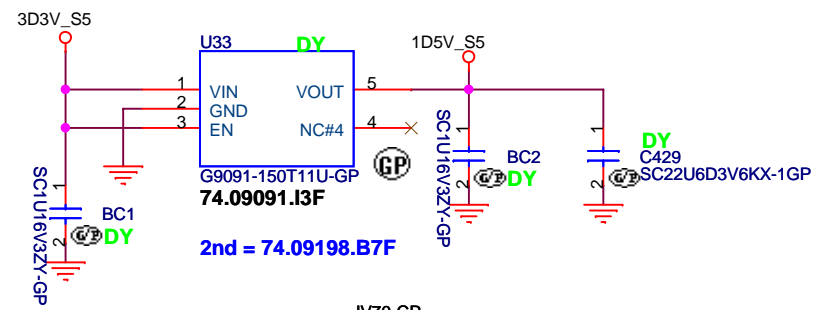
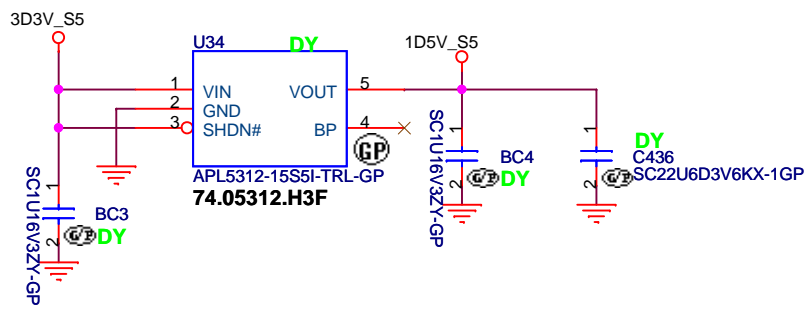
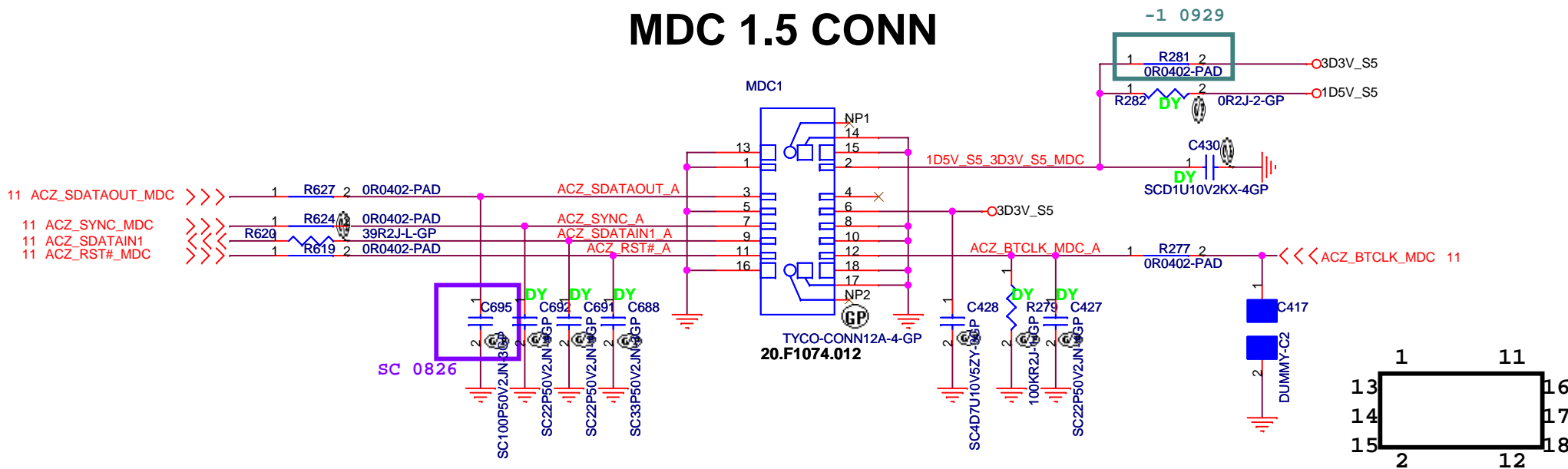
緯創資通 **Wistron Corporation**
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Title: **AUDIO Jack**

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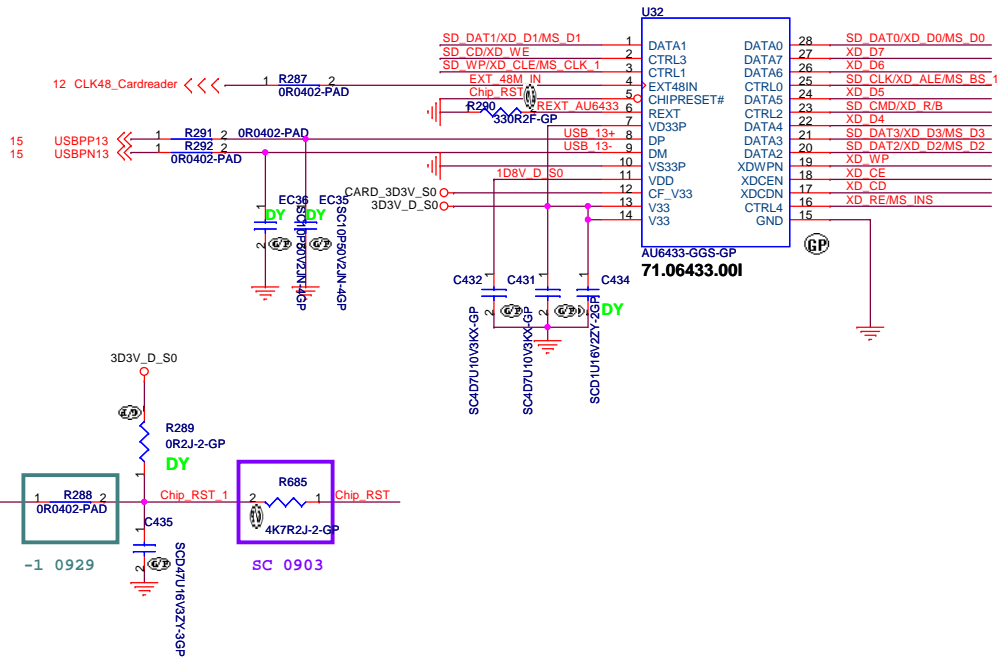
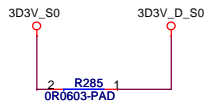
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MDC 1.5 CONN

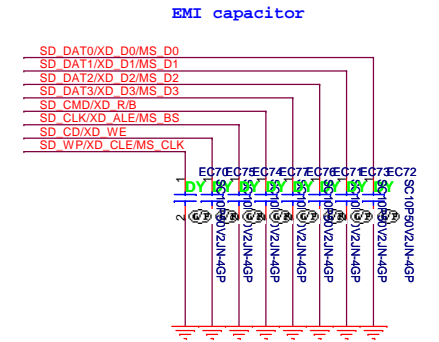
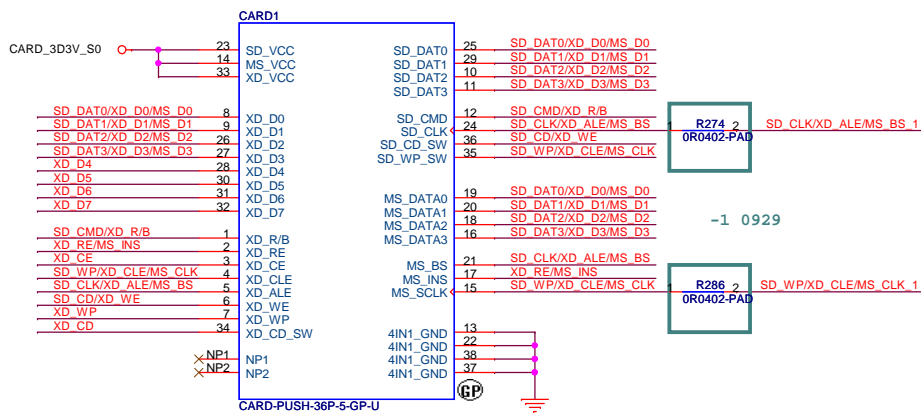
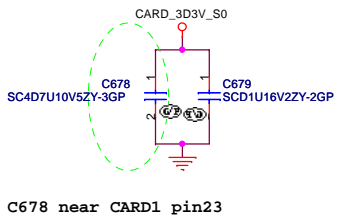


JV70-CP

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MDC			
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5 IN 1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

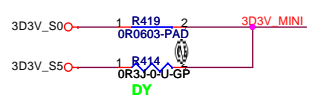
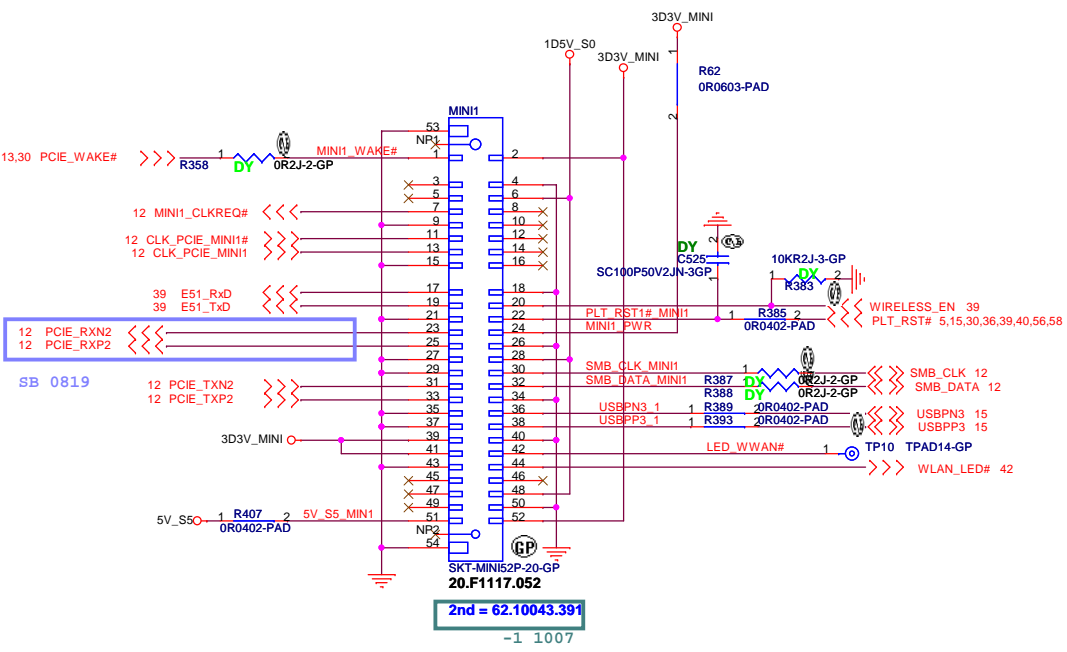
Title: Cardreader AU6433

Size: Document Number: JV70-CP, Rev: -1

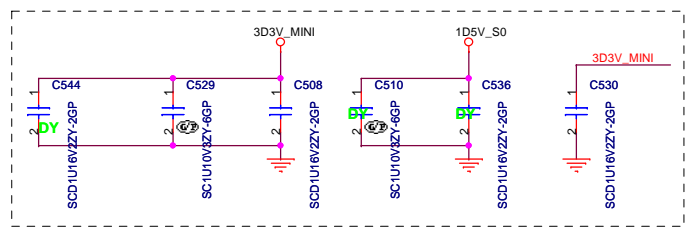
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Mini Card Connector(WLAN) Support debug-card

Mini Card Connector



Place near MINI1

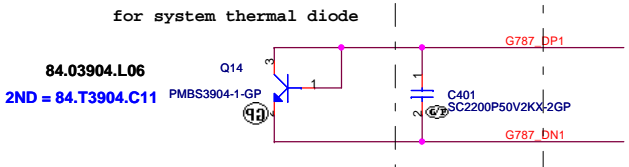
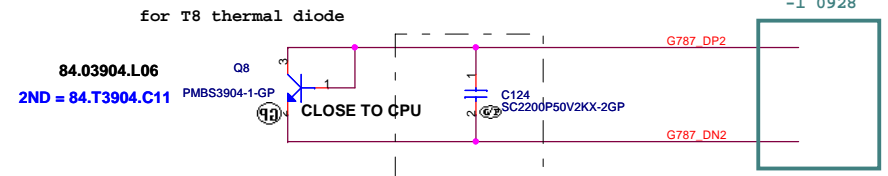


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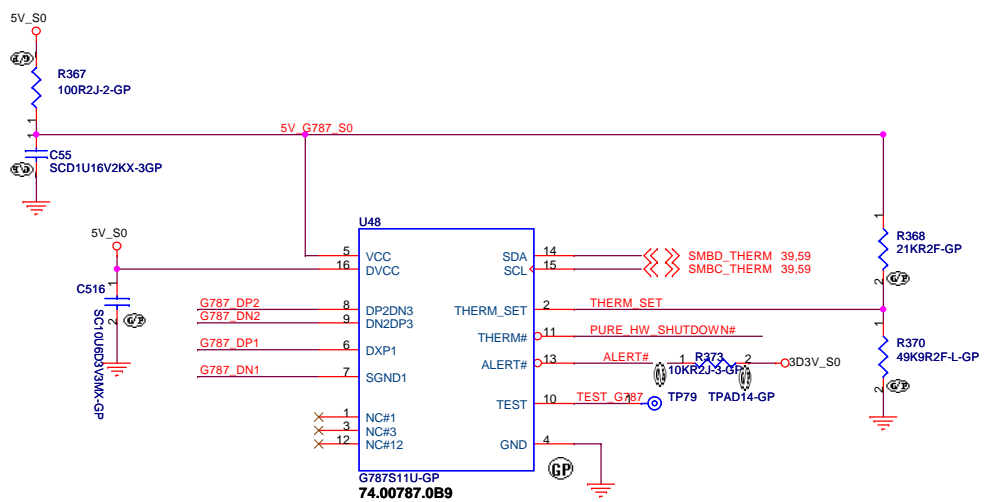
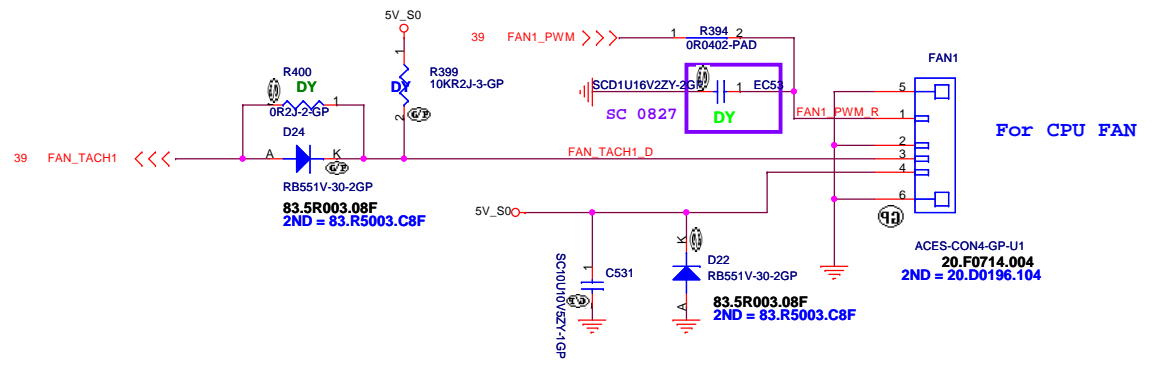
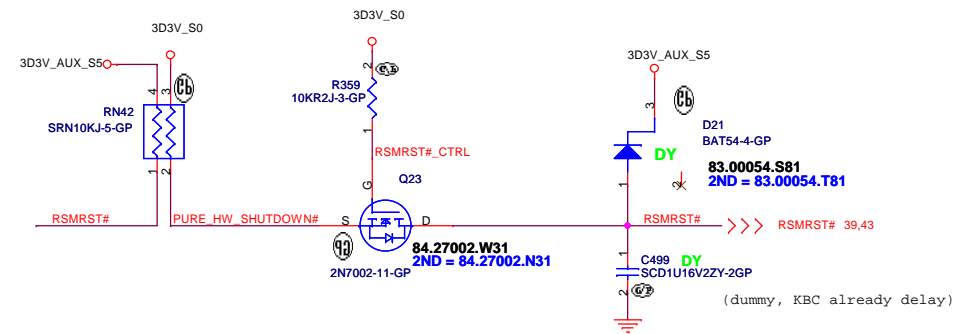
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **MINI CARD**

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C124 & C401 CLOSE TO G787



T8=90

$THERM_SET = [(Tset-72) \times 0.02 + 0.34] \times VCC$

JV70-CP

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Taipei Hsien 221, Taiwan, R.O.C.

Title

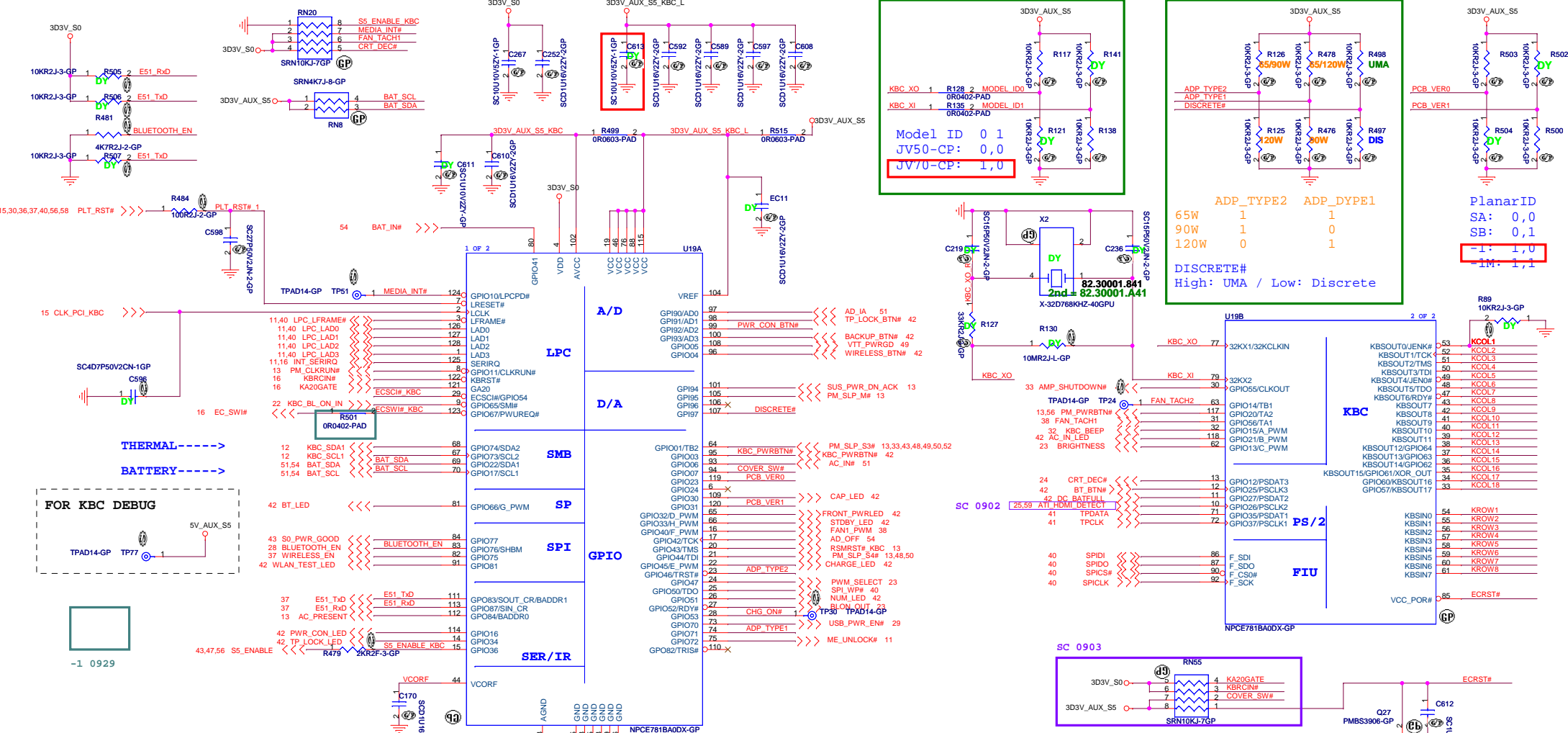
Thermal/Fan Connector

Size Document Number

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Rev -1



3D3V_AUX_S5

KBC XO 1 R128 2 MODEL_ID0
KBC XI 1 R135 2 MODEL_ID1
OR0402-PAD

Model ID 0 1
JV50-CP: 0, 0
JV70-CP: 1, 0

3D3V_AUX_S5

ADP_TYPE2 ADP_DYPE1
ADP_TYPE1
DISCRETE#

65W	1	1
90W	1	0
120W	0	1

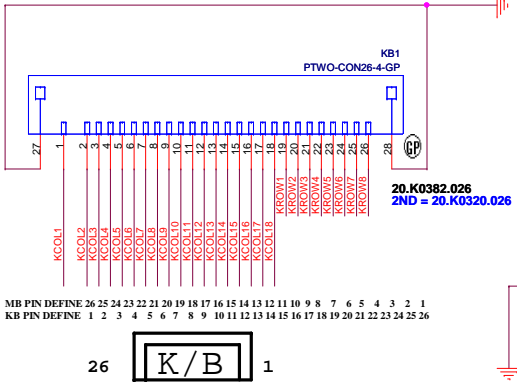
DISCRETE#
High / Low: Discrete

3D3V_AUX_S5

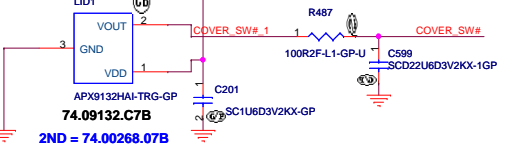
PCB_VER0
PCB_VER1

PlanarID
SA: 0, 0
SB: 0, 1
-1: 1, 0
IM: 1, 1

Internal Keyboard Connector



Cover Up Switch



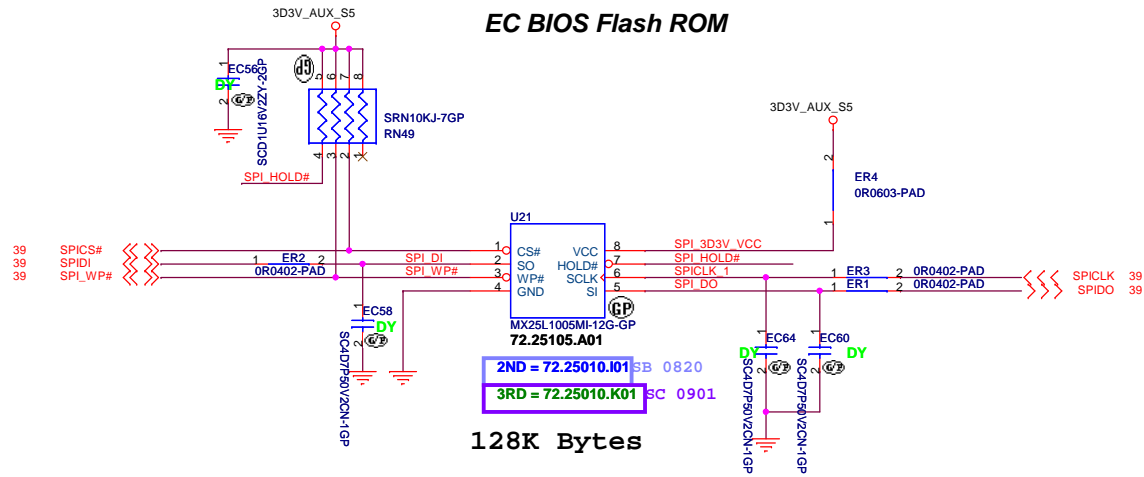
JV70-CP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

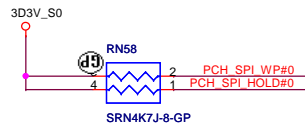
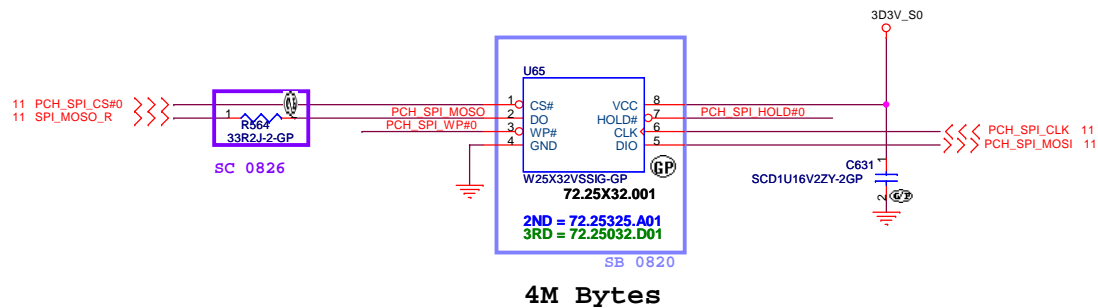
Title: **KBC NPCE781B**

Size: Document Number **JV70-CP** Rev: -1

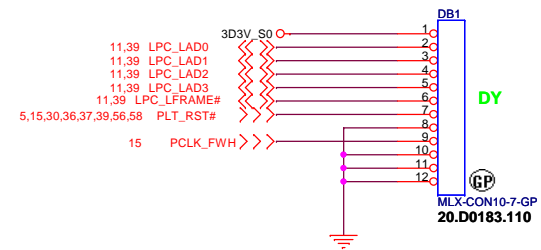
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System BIOS Flash ROM

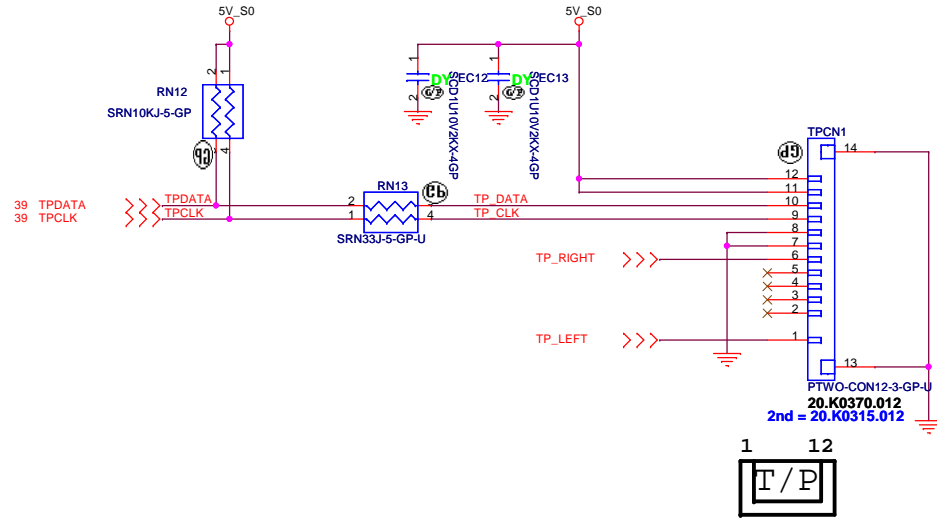


GOLDEN FINGER FOR DEBUG BOARD

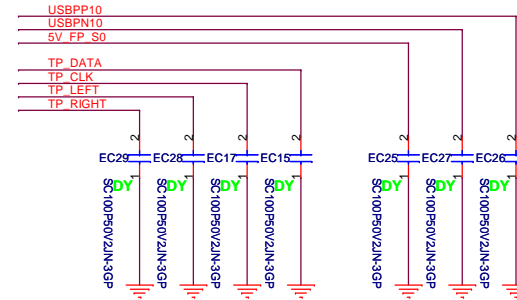
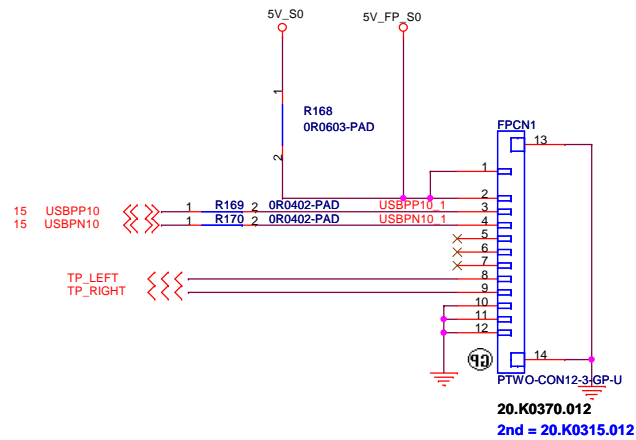


JV70-CP

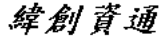
TOUCH PAD



Finger printer

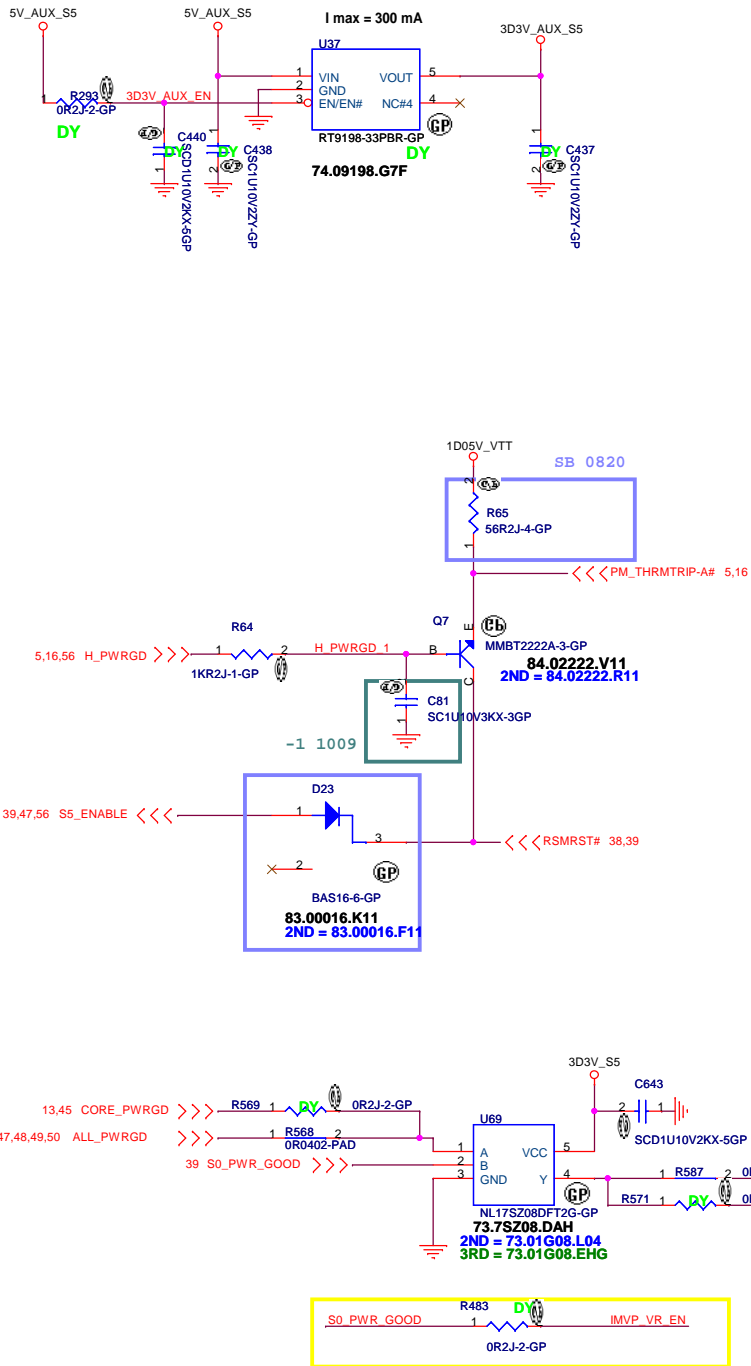


JV70-CP

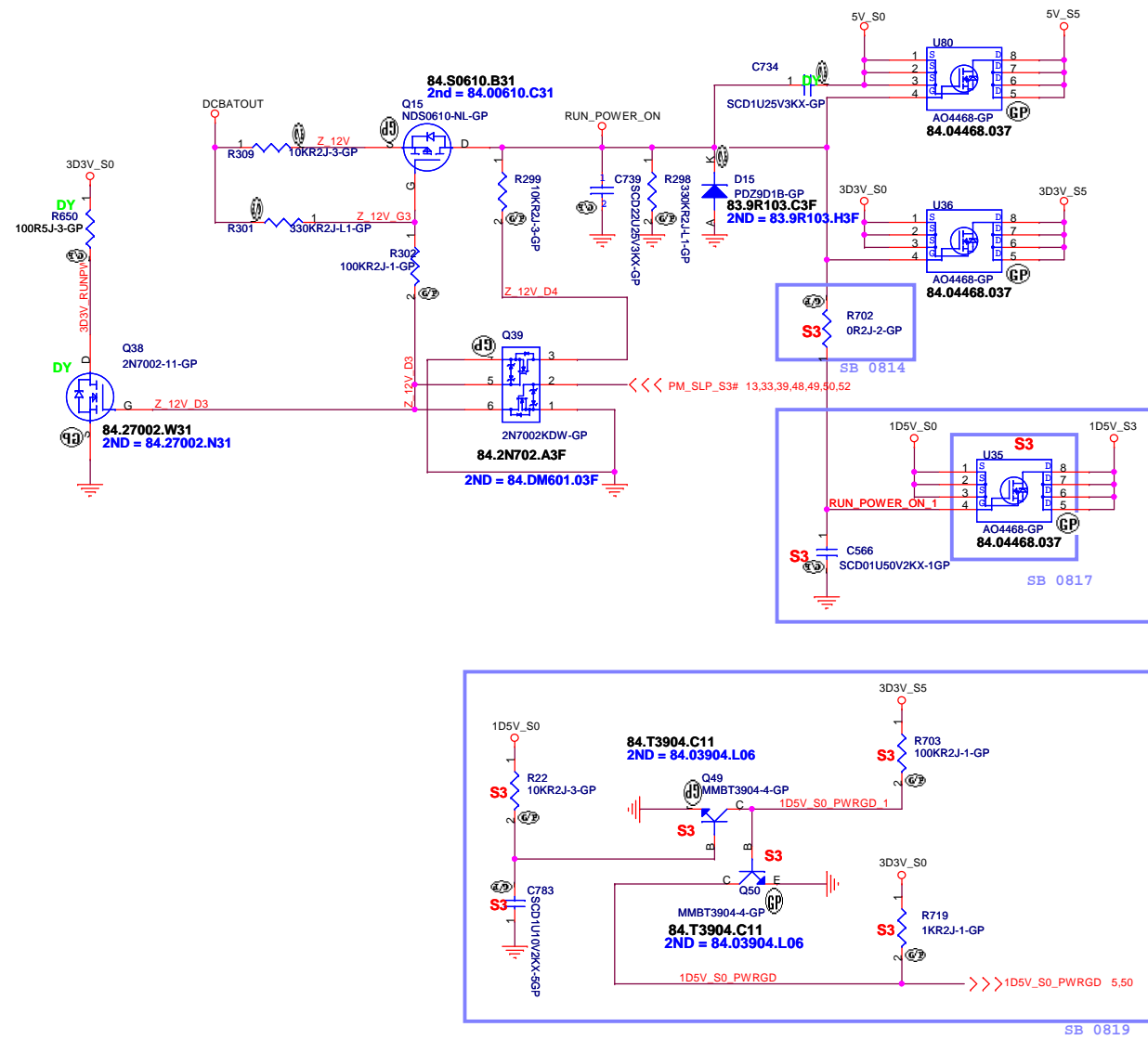
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Touch PAD and FP		
Size	Document Number	Rev
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Aux Power

3D3V_AUX_S5



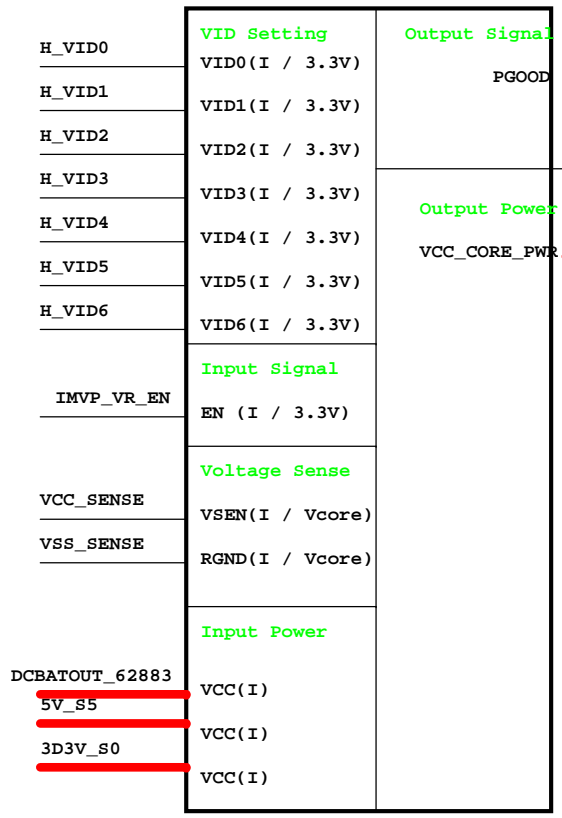
Run Power



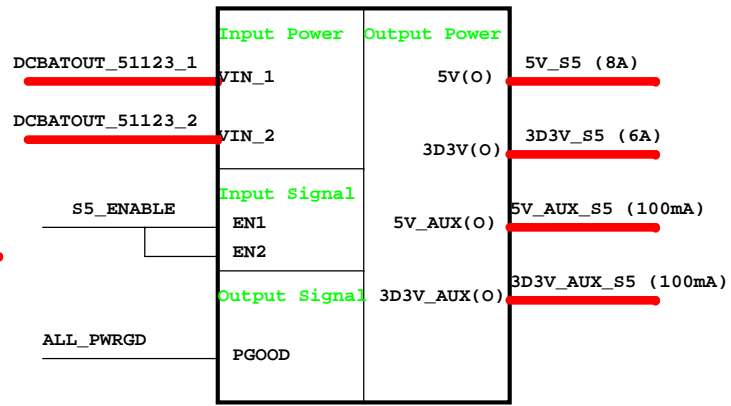
JV70-CP

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
RUN POWER and 3D3V AUX S5	
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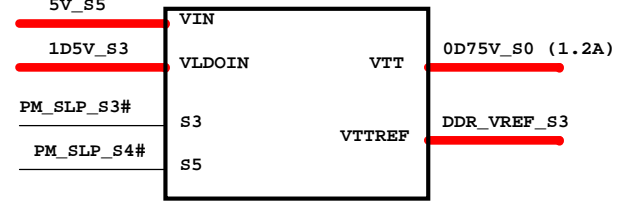
ISL62883 VCC_CORE



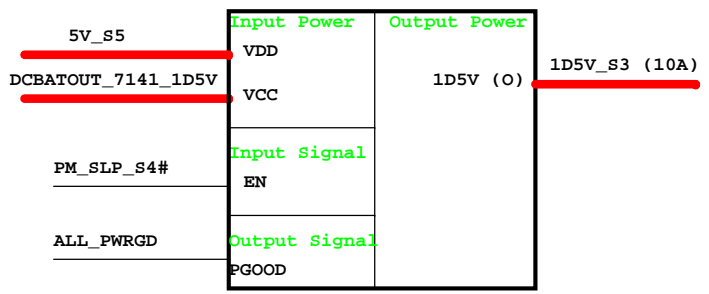
TPS51123 5V/3D3V



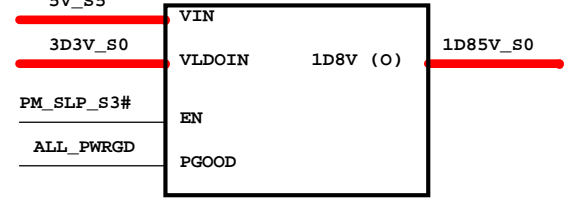
G2997 0D75V_S0



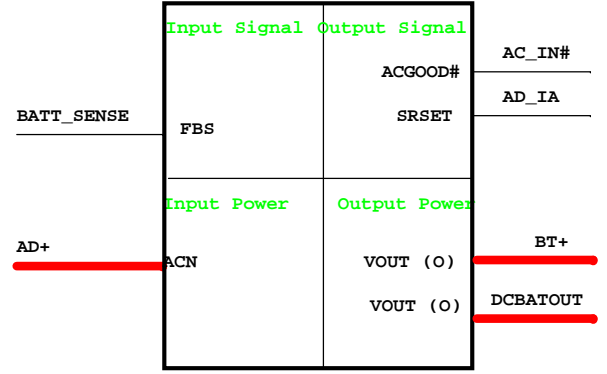
TPS51117 1D5V



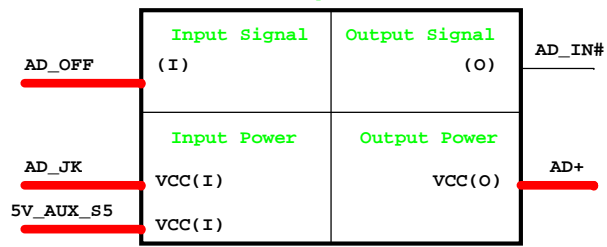
RT9025 1D8V



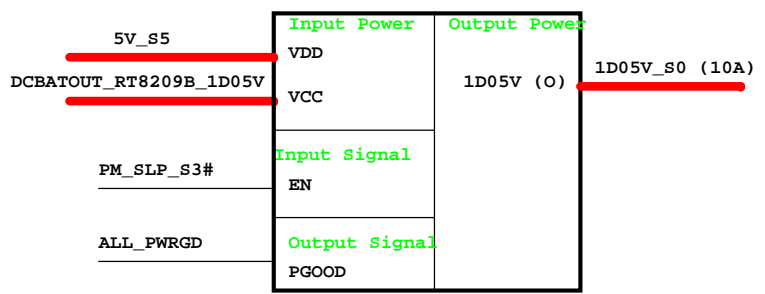
Charger BQ24745



Adapter

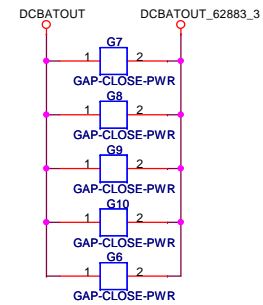
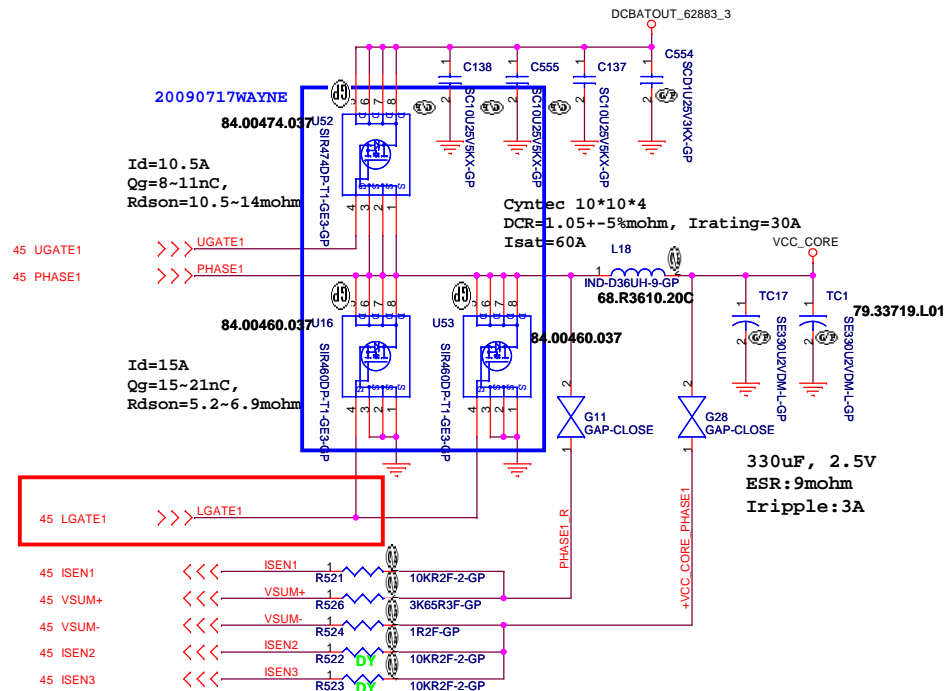
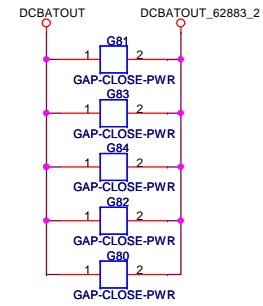
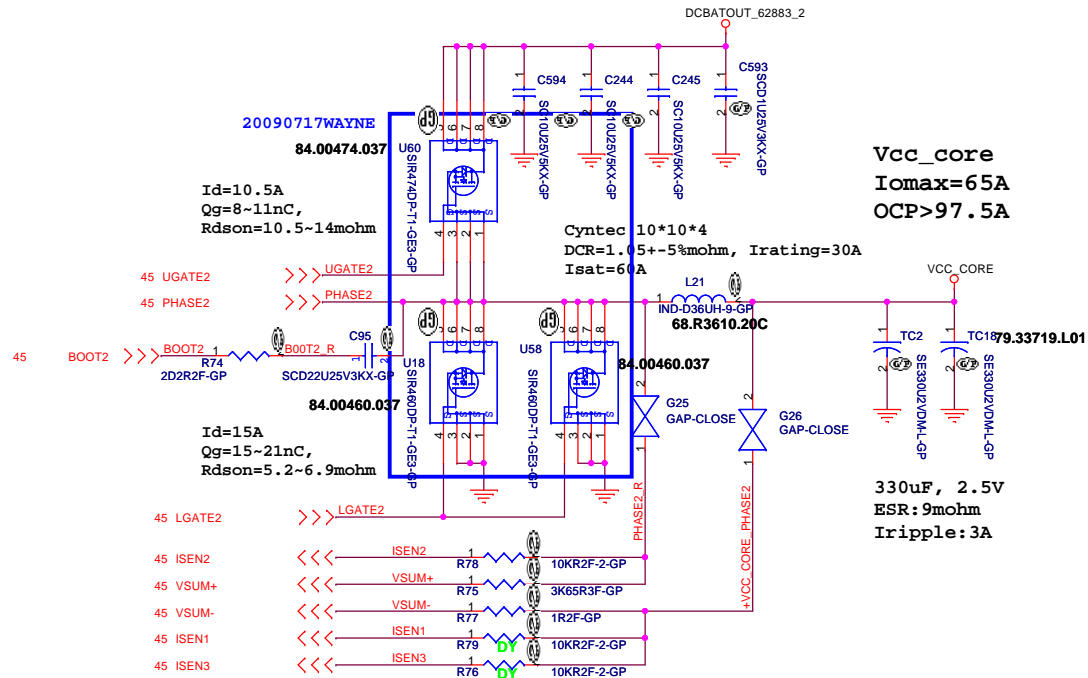


TPS51117 1D05V



JV70-CP

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wuj Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Power Block Diagram	
Title	Rev
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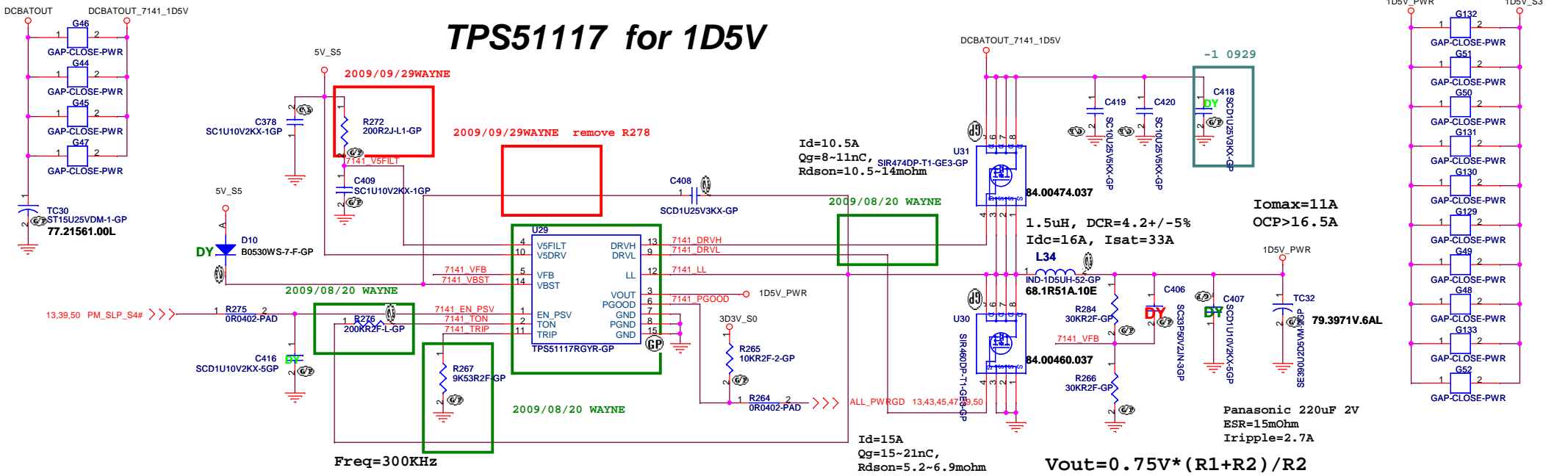


JV70-CP

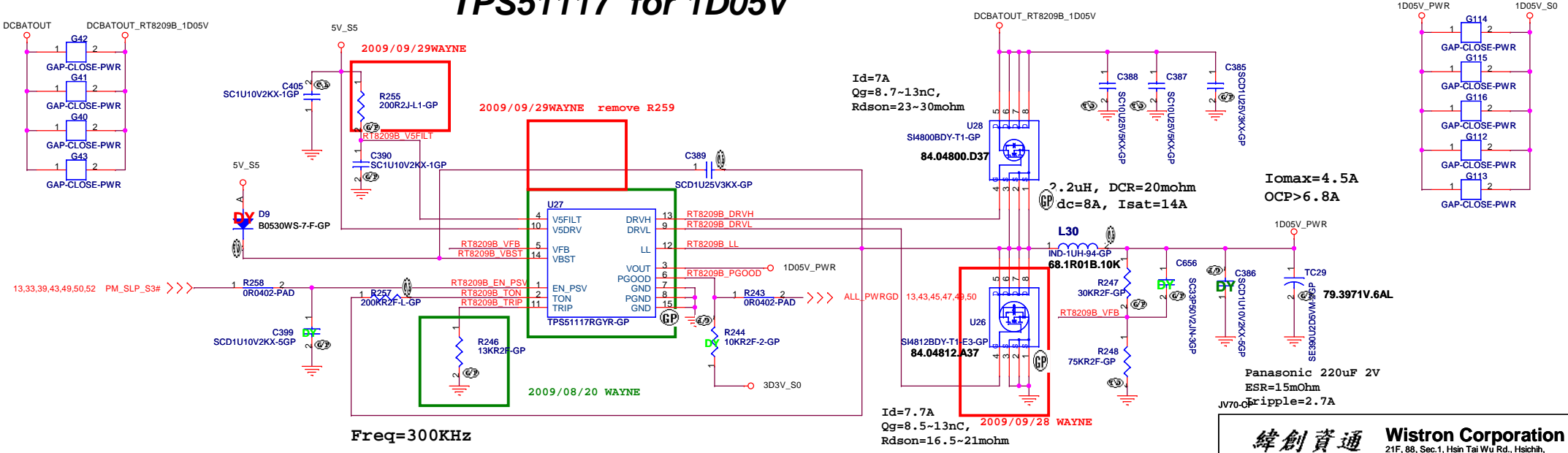
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		ISL62883 CPU CORE (1/2)	
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TPS51117 for 1D5V



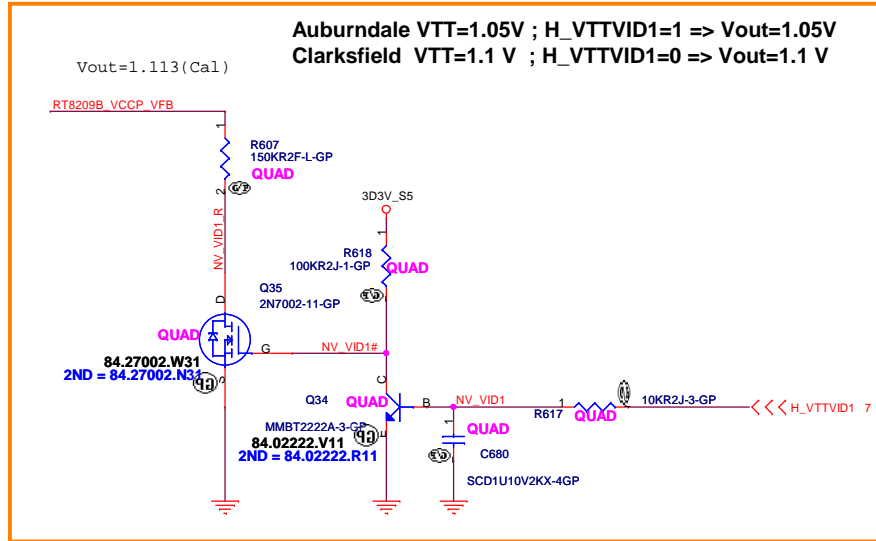
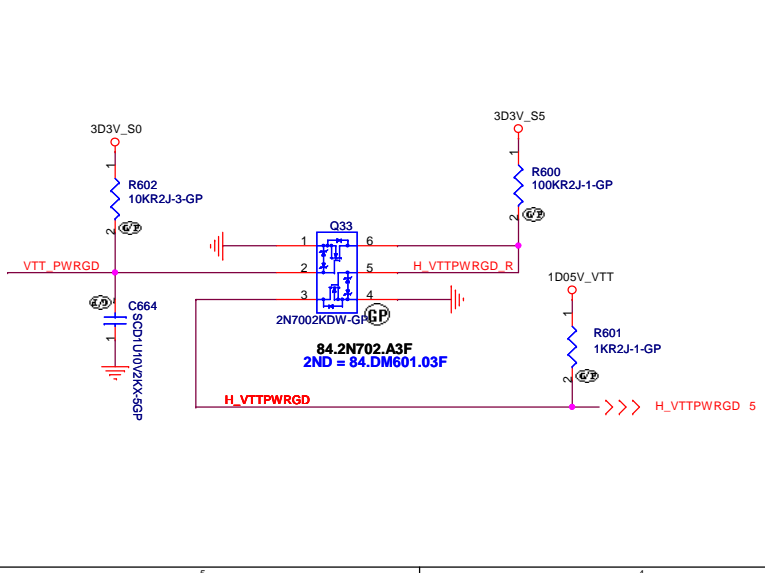
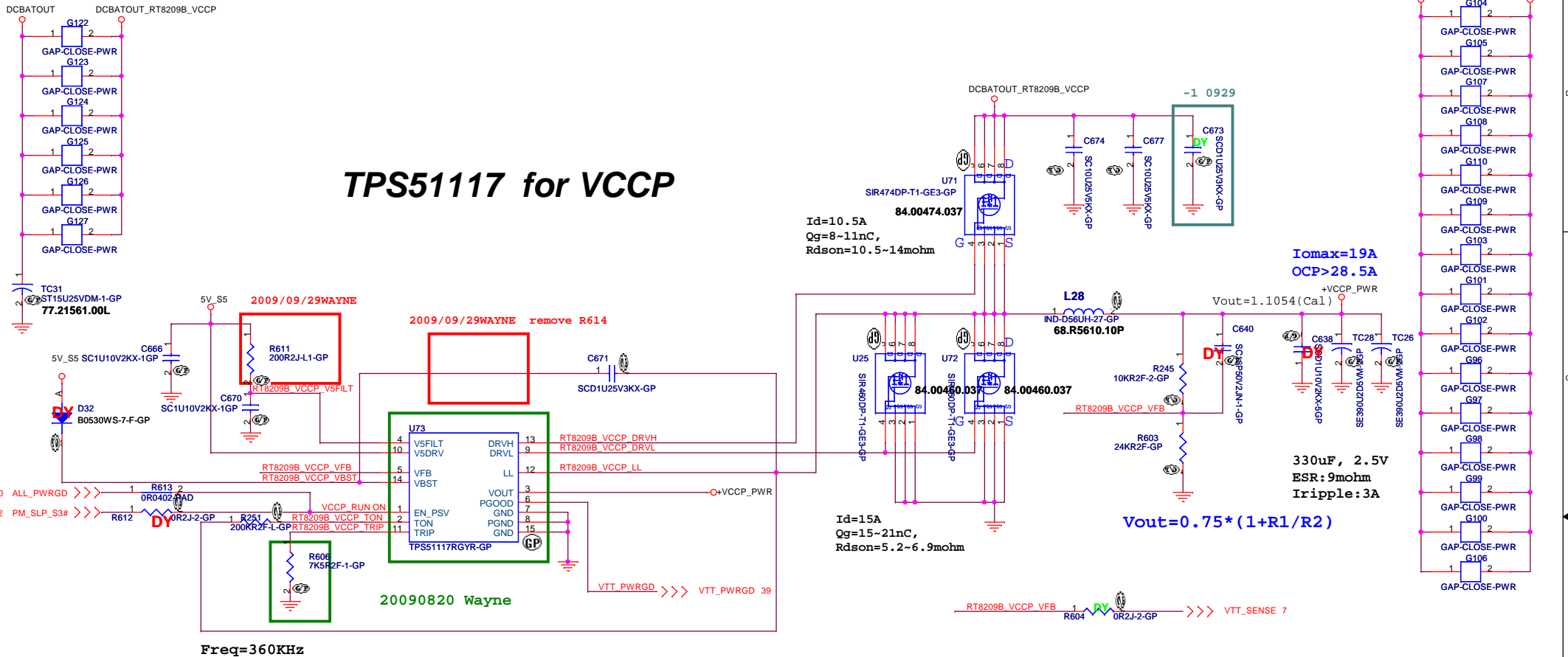
TPS51117 for 1D05V



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TPS51117 1D5V/TPS51117 1D05V		
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TPS51117 for VCCP



JV70-CP

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Taipei Hsien 221, Taiwan, R.O.C.

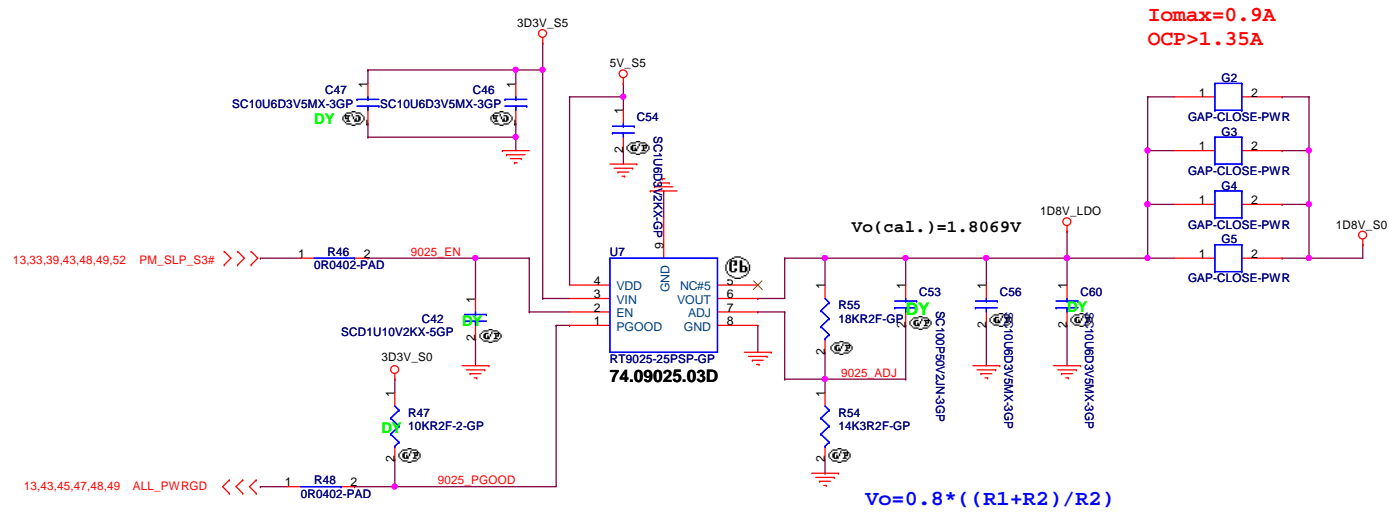
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Size: Document Number

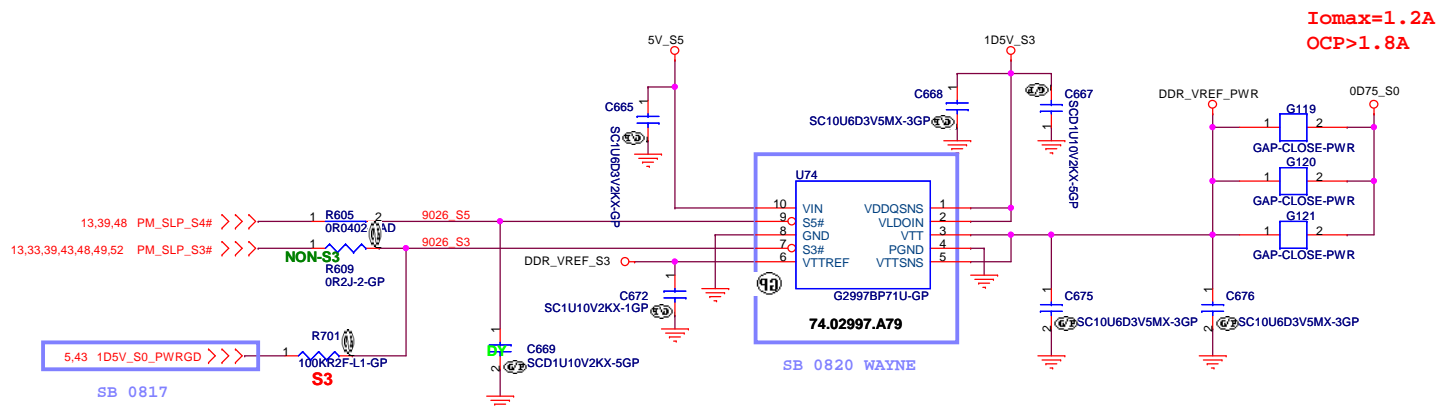
Rev: **-1**

Date: Thursday, October 08, 2009 Sheet 49 of 68

RT9025 for 1D8V_S0



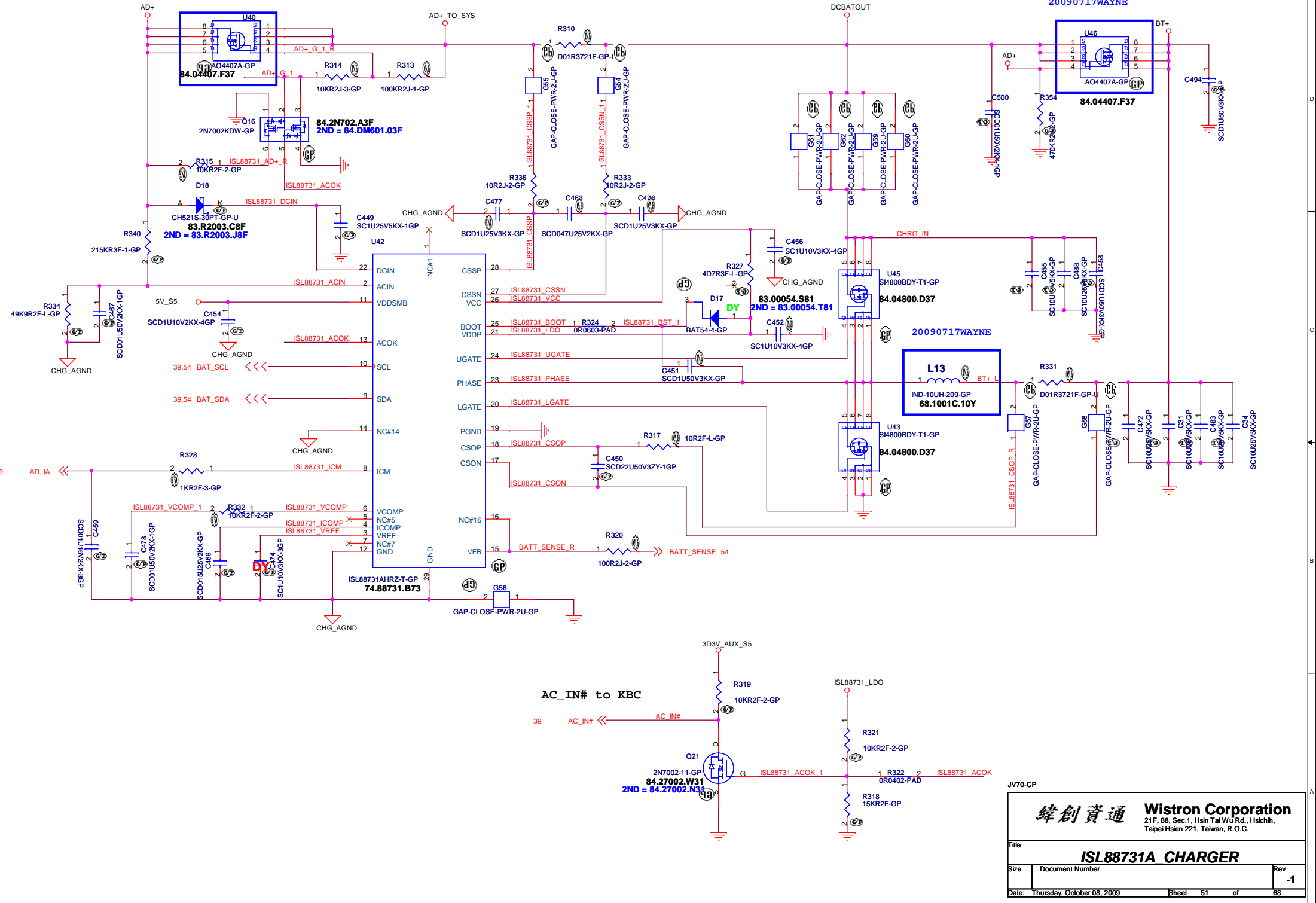
G2997 for 0D75V_S3



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Taipei Hsien 221, Taiwan, R.O.C.

Title		RT9025 1D8V/G2997 0D75	
Size	Document Number	Rev	
JV70-CP		-1	
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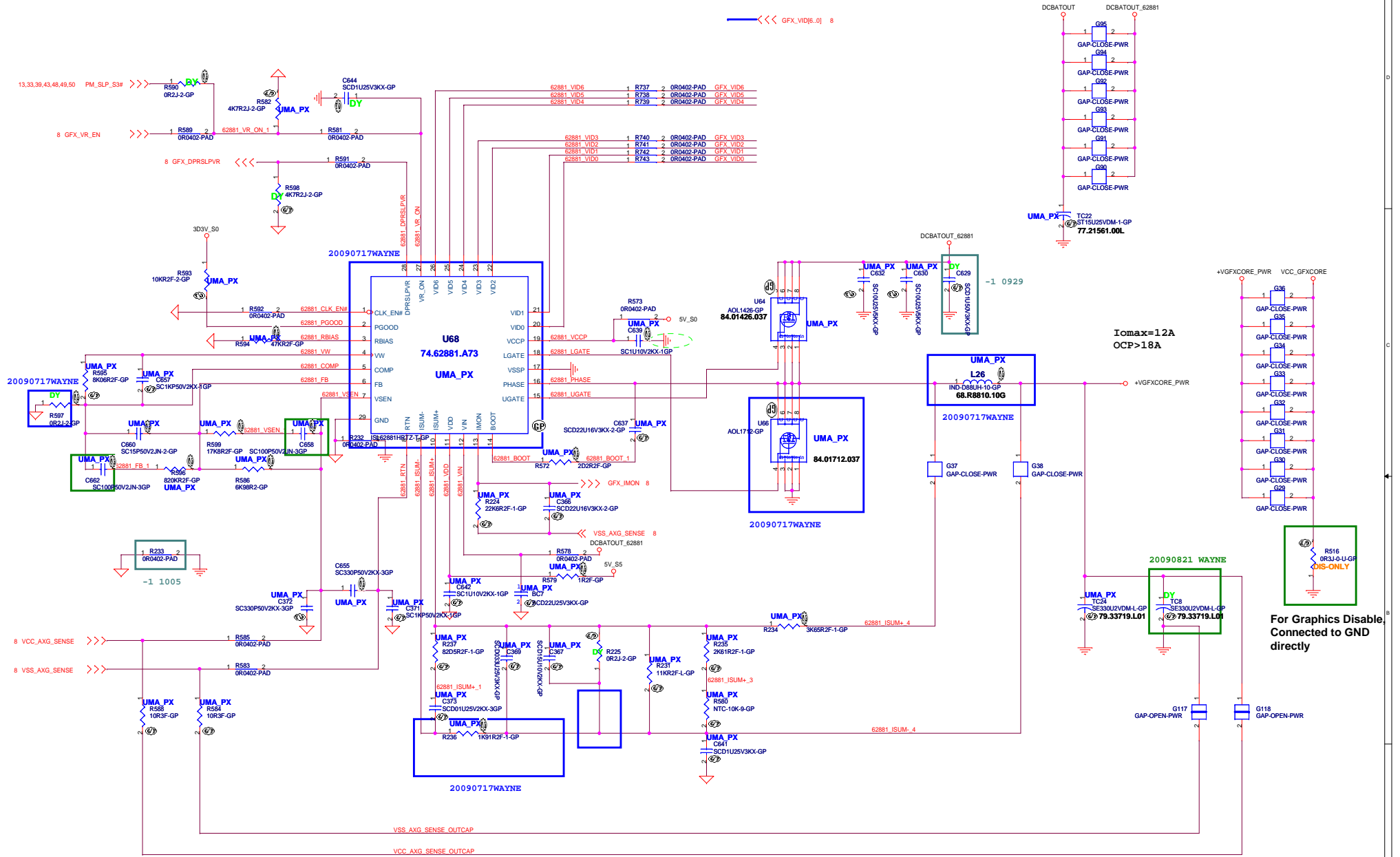
AC_IN# to KBC

AC_IN#

84.27002.W31
2ND = 84.27002.N31

緯創資通 **Wistron Corporation**
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 Taipei Hsien 221, Taiwan, R.O.C.

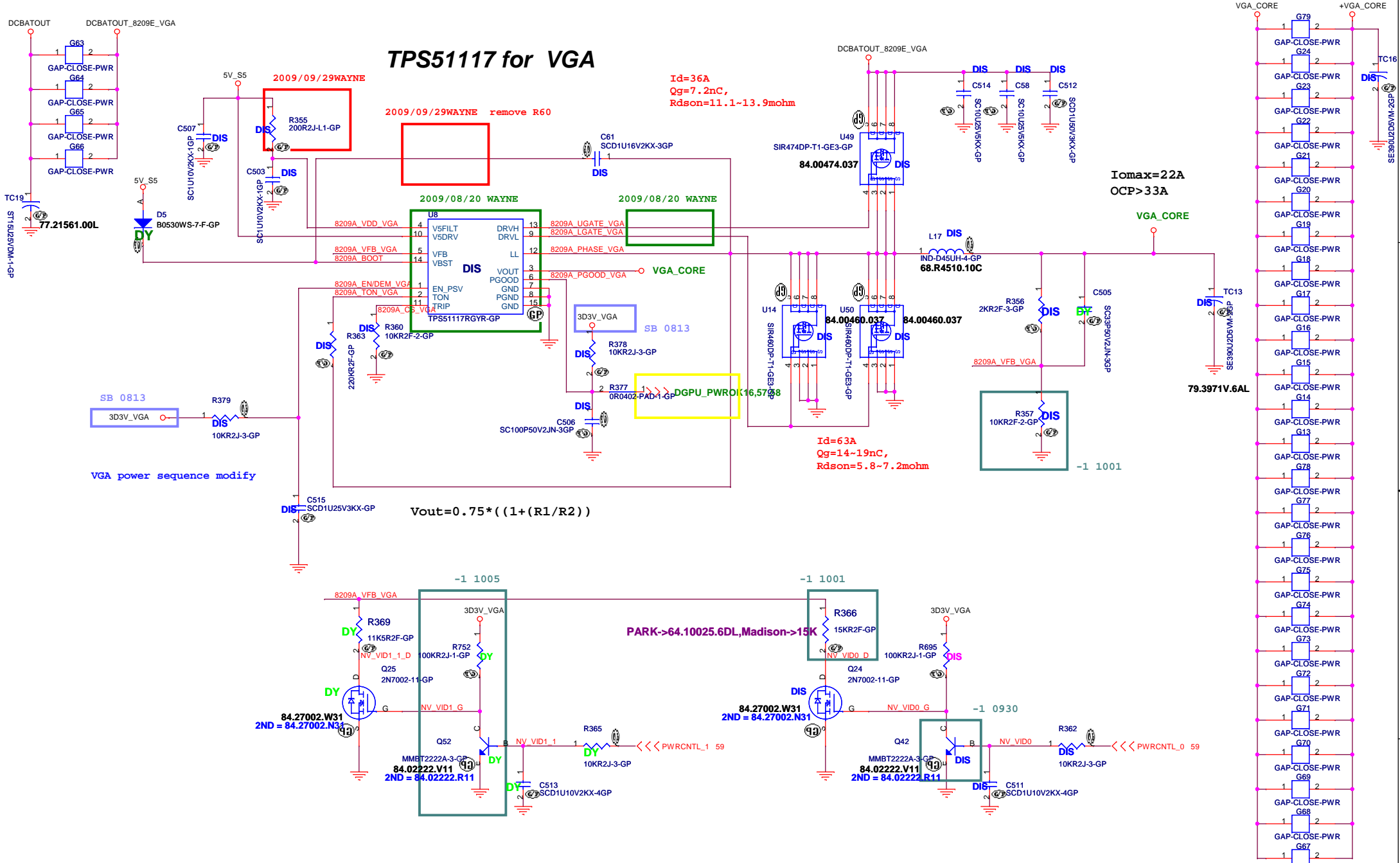
Title		
ISL88731A CHARGER		
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Iomax=1.2A
OCP>1.8A

For Graphics Disable
Connected to GND
directly

TPS51117 for VGA



Madison-Pro	I/O	Inter Pull Low	GPIO TABLE
PWRCNTL_0	O	YES	GPU VOLTAGE L: 1.0V GPU VOLTAGE H: 0.9V

Park-XT	I/O	Inter Pull Low	GPIO TABLE
PWRCNTL_0	O	YES	GPU VOLTAGE L: 1.05V GPU VOLTAGE H: 0.9V

JV70-CP

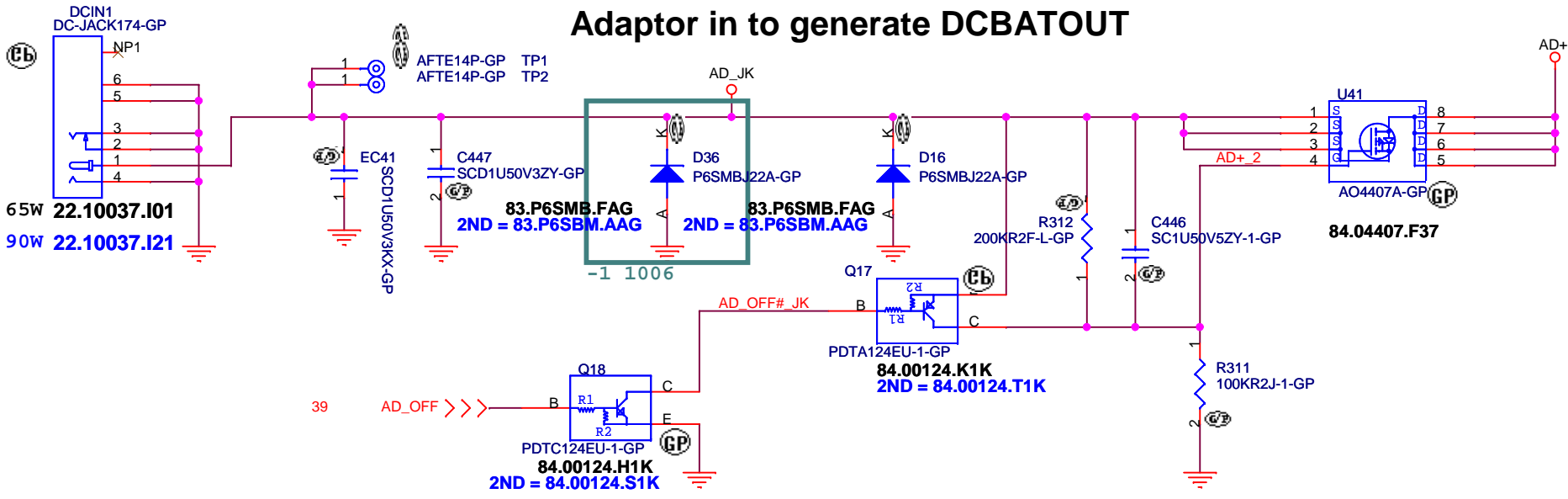
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51117 VGA CORE**

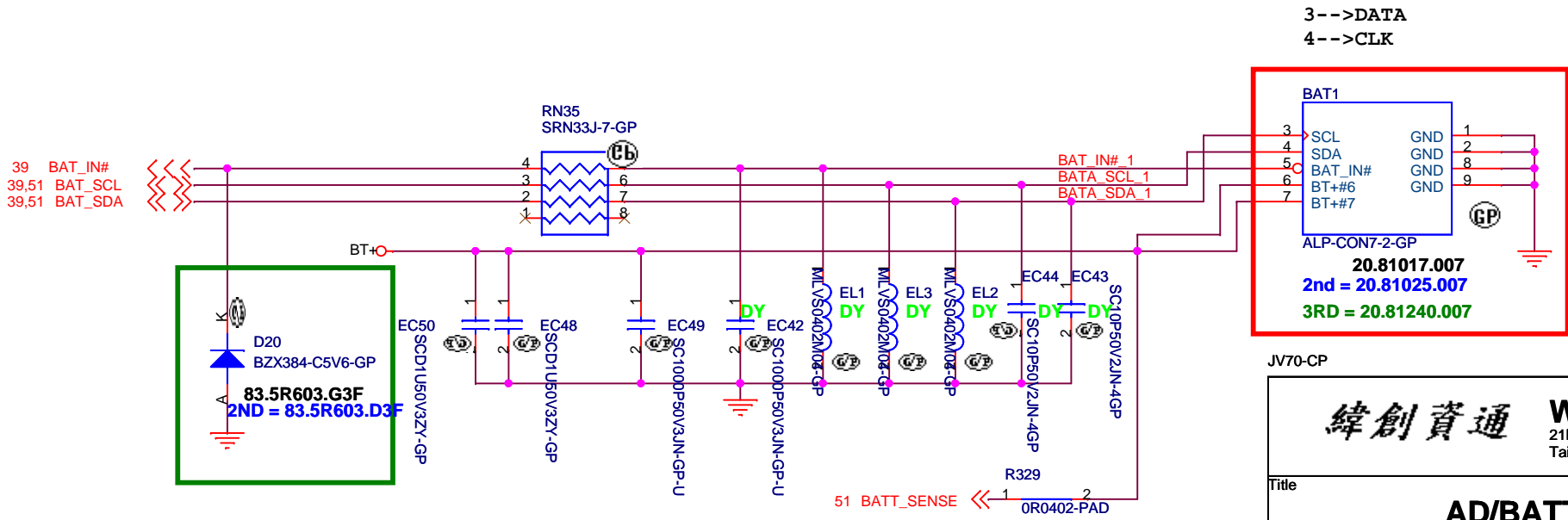
Size A3 Document Number **JV70-CP** Rev

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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



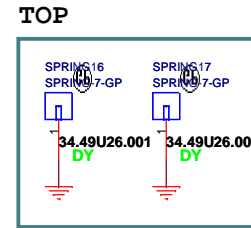
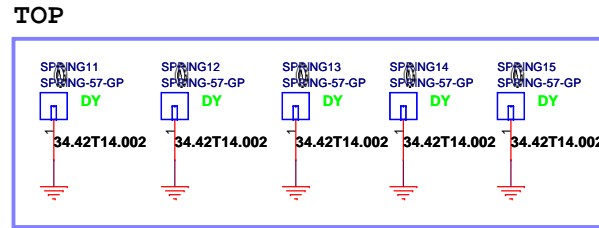
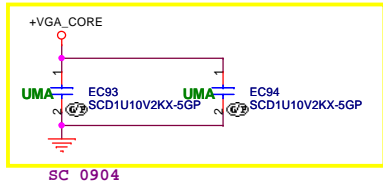
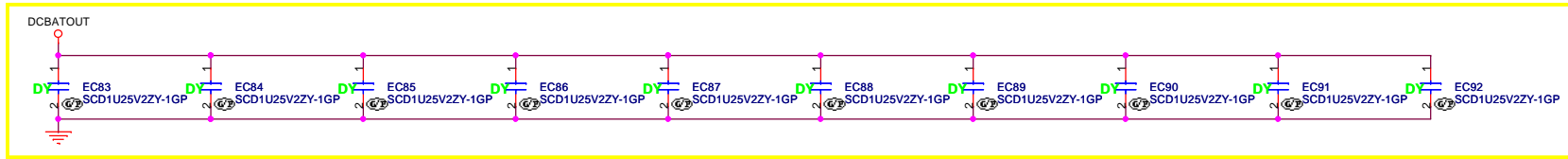
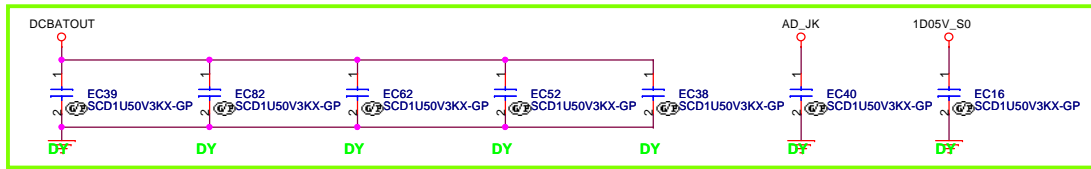
JV70-CP

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
	JV70-CP	-1

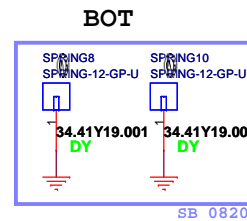
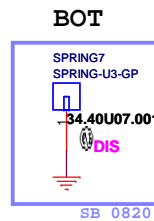
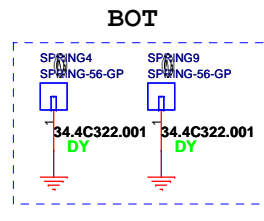
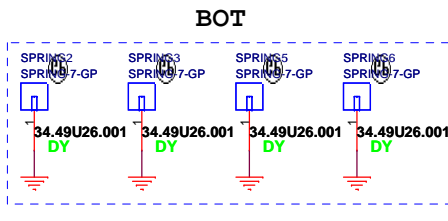
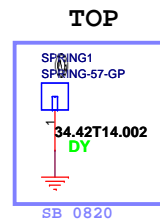
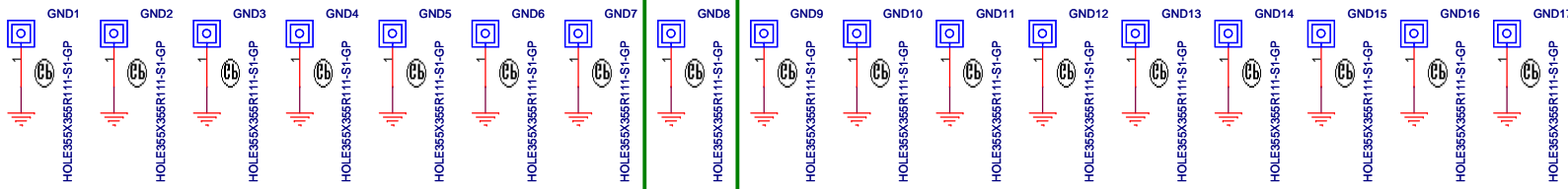
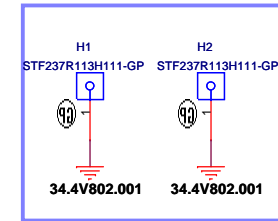
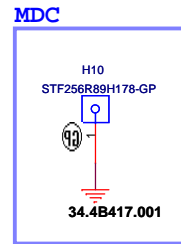
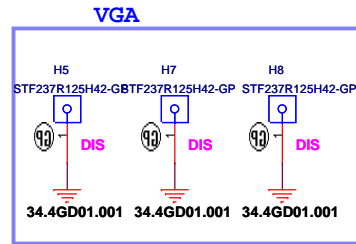
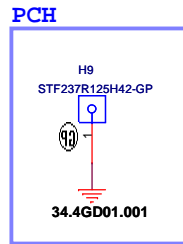
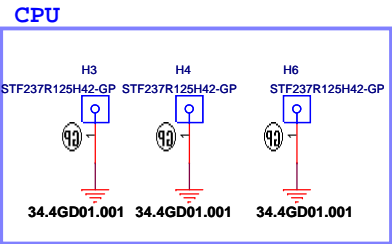
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SB 0819

-1 0930

H1~H10 ALL IN TOP SIDE



SB 0820

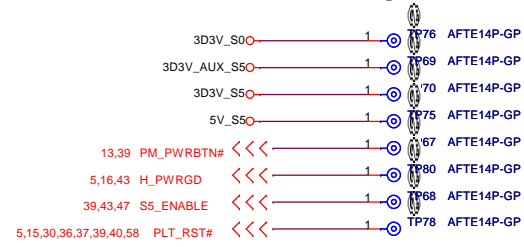
SB 0820

SB 0820

JV70-CP

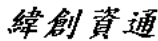
Title: EMI/Spring/Boss	
Size: Document Number	Rev: -1
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Check test point

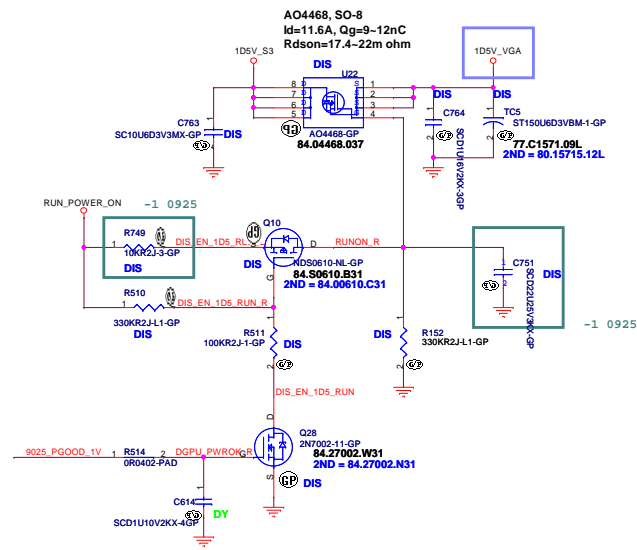
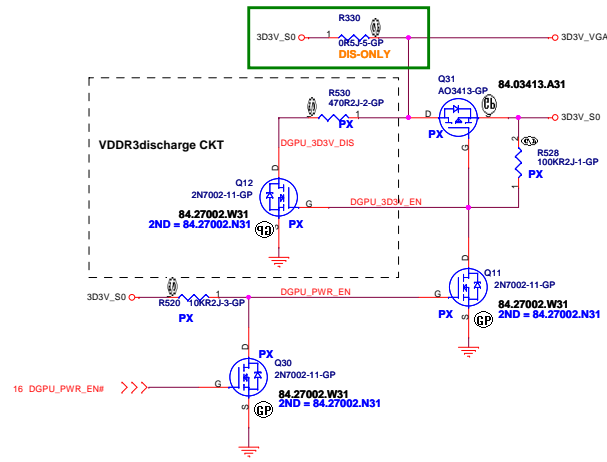


Test Point放在Dimm Door打開可量測處

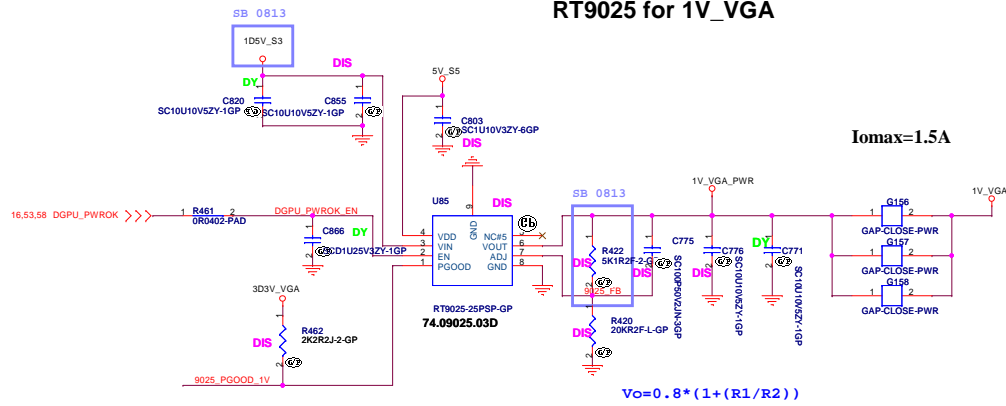
JV70-CP

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
AFTE TP	
Size	Document Number
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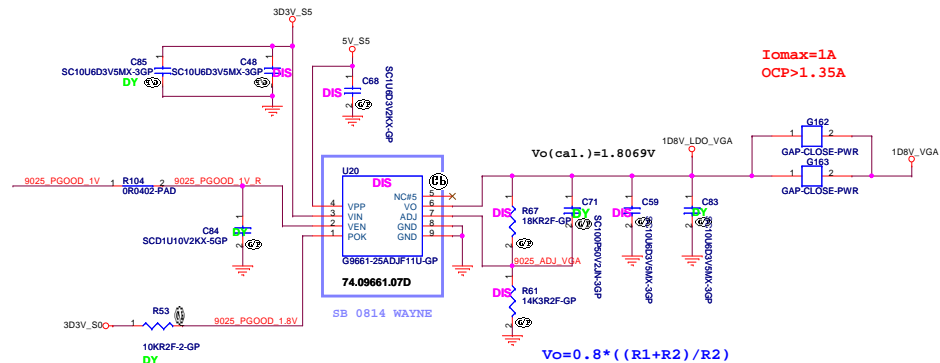
+3VS to 3.3V_DELAY Transfer



RT9025 for 1V_VGA



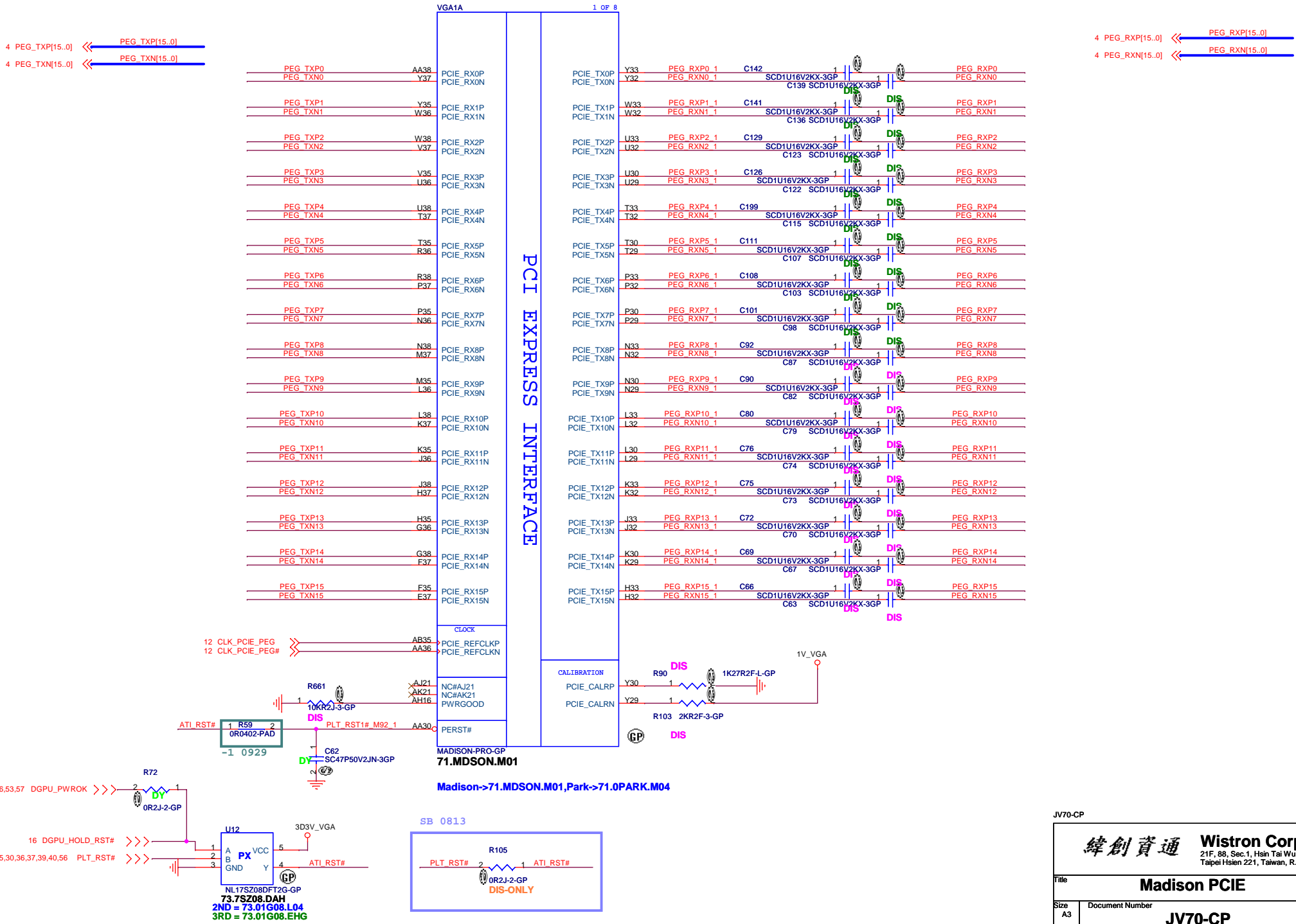
G9661 for 1D8V_VGA



JV70-CP

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Taipei Hsien 221, Taiwan, R.O.C.

Title		ATI POWER	Rev
Size	Document Number	Custom	-1
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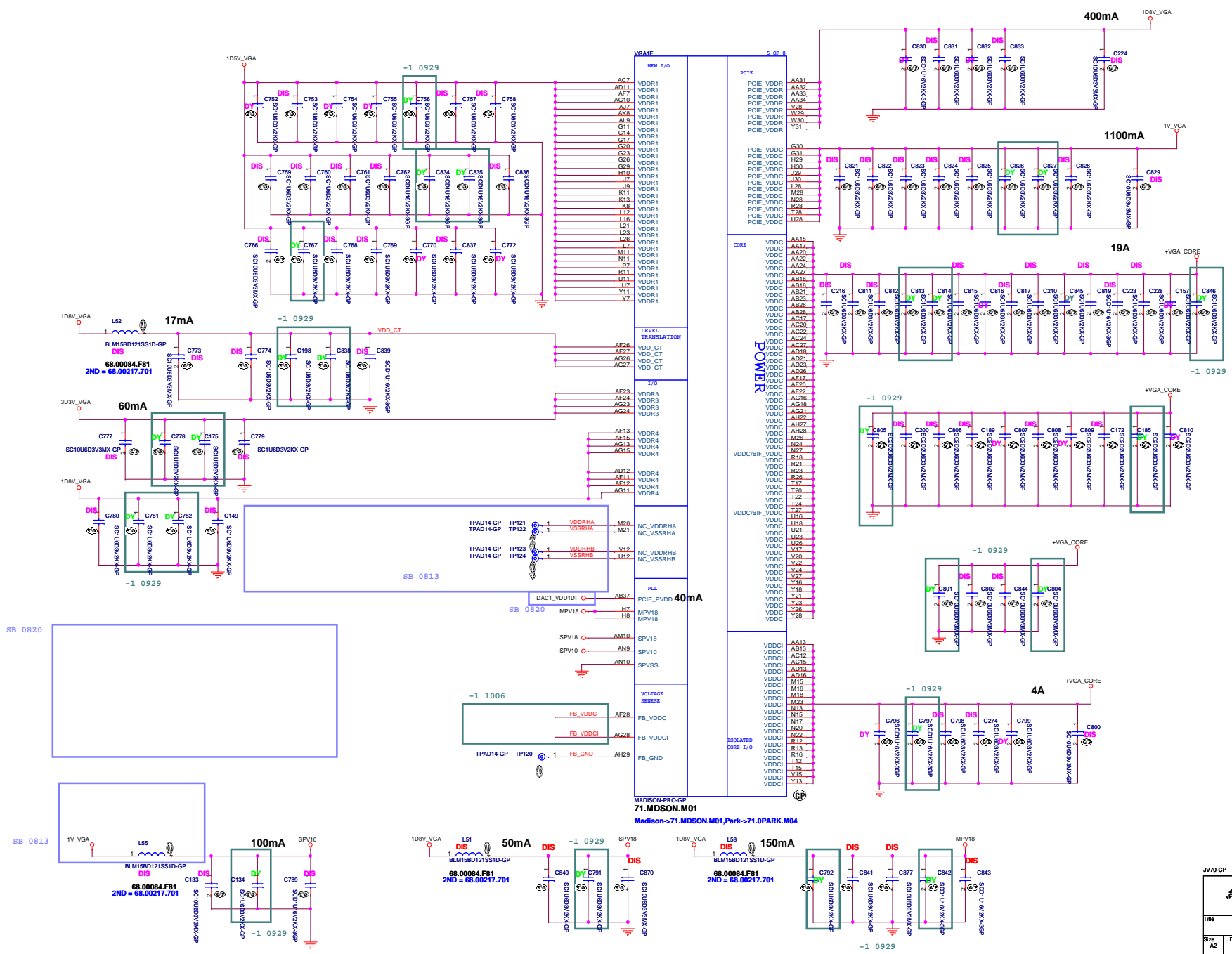
JV70-CP

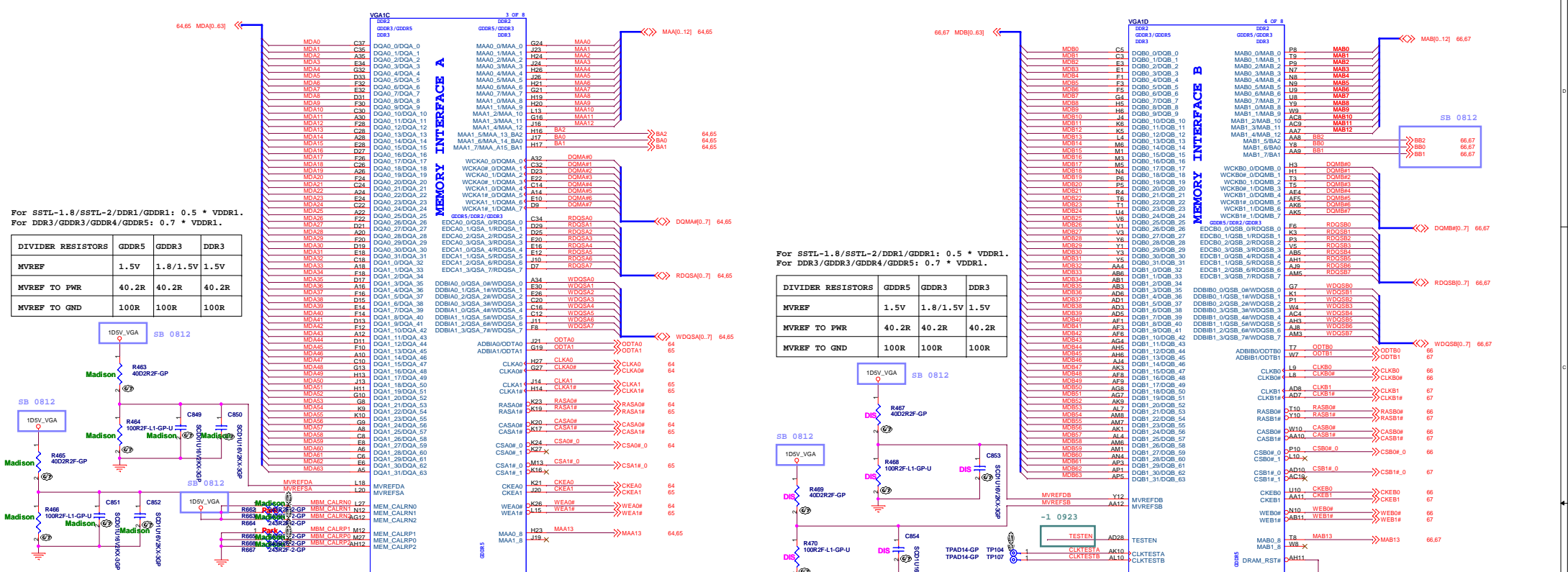
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Madison PCIE**

Size: A3 | Document Number: **JV70-CP** | Rev: **-1**

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For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
 For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
 For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

Madison: MEM_CALRP[0,2] signals are used.
 Park: MEM_CALRP1 and MEM_CALRN1 are used.

71.MDSON.M01
 Madison->71.MDSON.M01, Park->71.PARK.M04

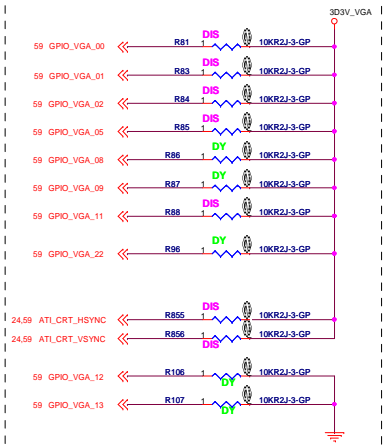
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS
TX_PWRS_ENB (Internal PD)	GPI00	PCIe Full Tx Output Swing Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	x
TX_DEEMPH_EN (Internal PD)	GPI01	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	x
RESERVED	GPI08	RESERVED	0
BIF_VGA_DIS	GPI09	VGA ENABLED	0
RESERVED	GPI021	RESERVED	0
BIOS_ROM_EN	GPI022_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPI0[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	x x x
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00: No audio function 01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI	x x

AMD RESERVED CONFIGURATION STRAPS
 ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

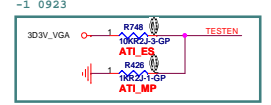
H2SYNC, GENERICCC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1	
Size of the primary memory apertures	SPIO[13,12,11]	Manufacturer	Part Number
128MB	x000	ST	M25P05A
256MB	x001	ST	M25P10A
64MB	x010	ST	M25P20
32MB	x	ST	M25P40
512MB	x	ST	M25P80
1GB	x	Chingis (formerly PWC)	Pm25LV512A
2GB	x	Chingis (formerly PWC)	Pm25LV101A
4GB	x		0101

HW STRAP PIN



Designator	For M97-M2	For Mannheim
R_MEM_1	R471	10K
R_MEM_2	R437	0R/Short
R_MEM_3	DY	DY
C_MEM	C889	2.2nF
		68pF



JV70-CP

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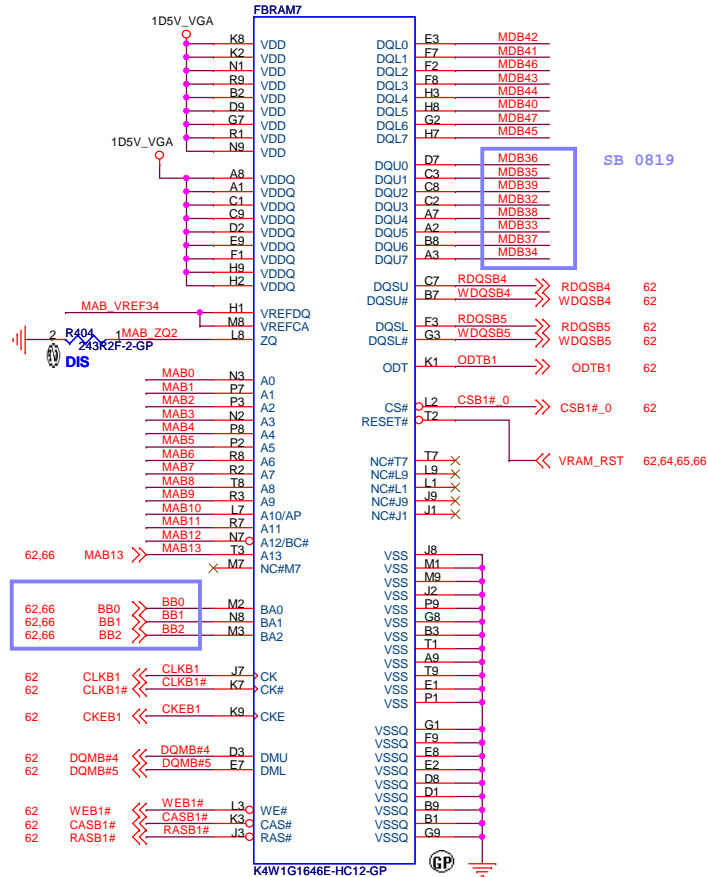
File: **Madison Memory / Straps**

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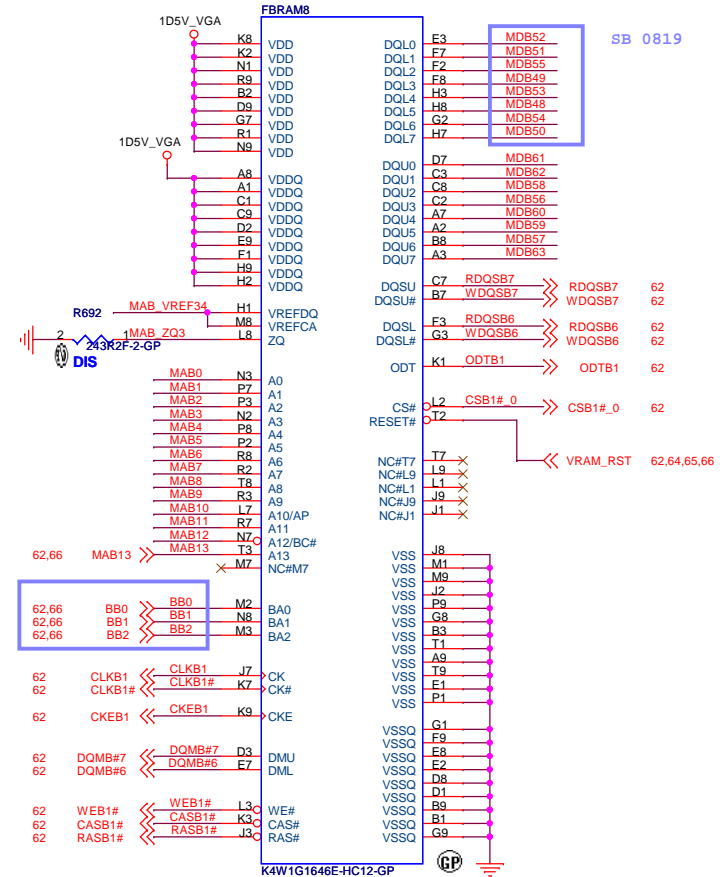
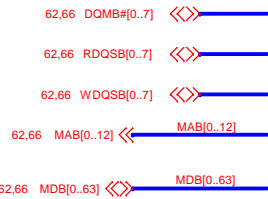
DDR3



72.41164.H0U
HYN-72.51G63.C0U,SAM-72.41164.H0U

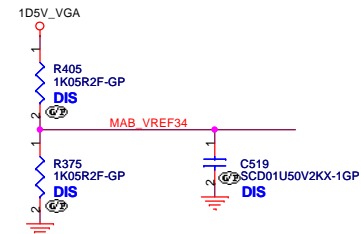
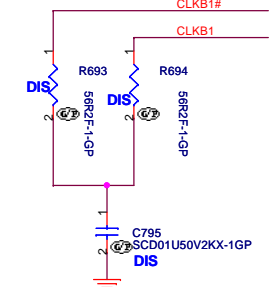
DIS

SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



72.41164.H0U
HYN-72.51G63.C0U,SAM-72.41164.H0U

DIS



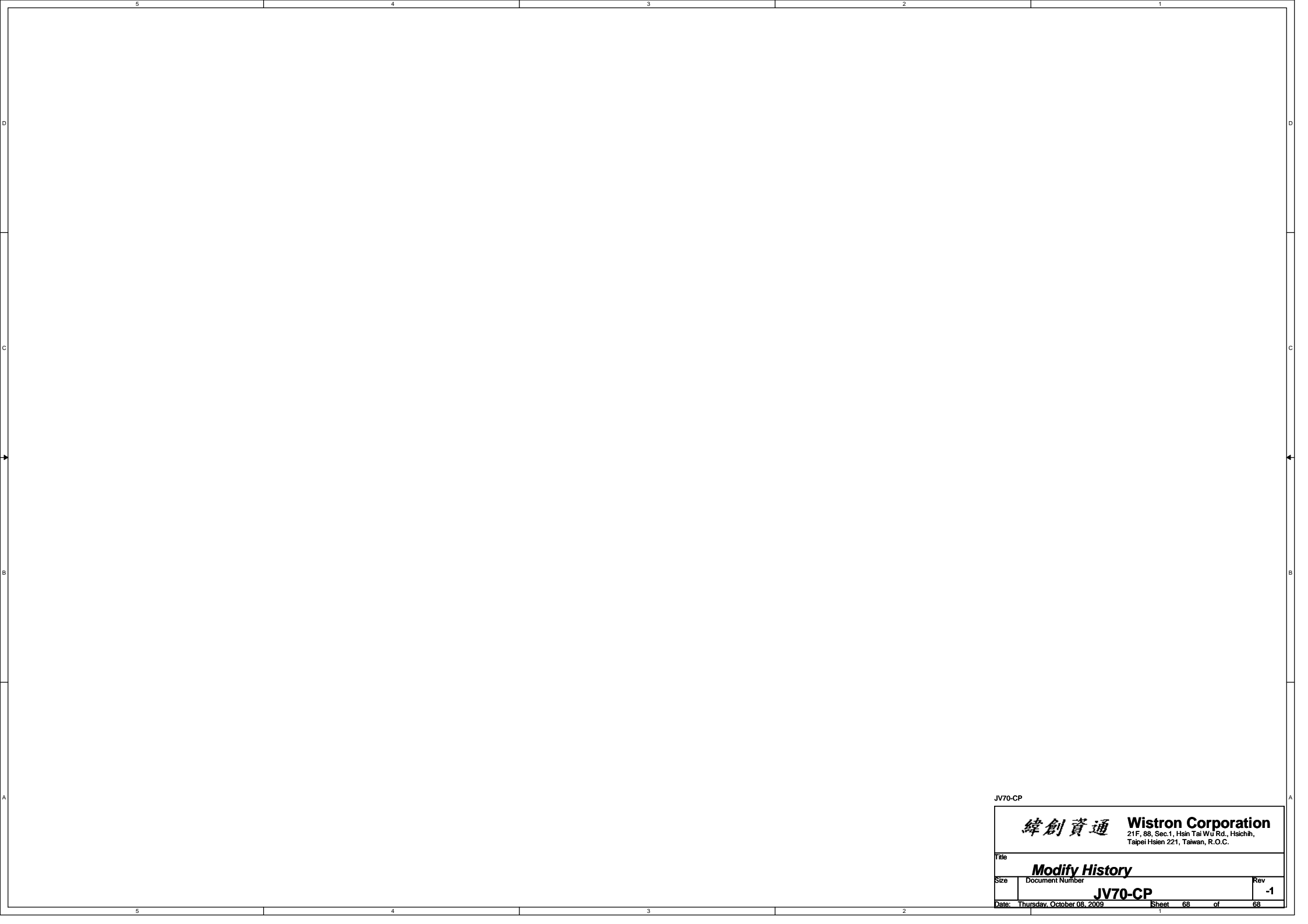
JV70-CP

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Title: **VRAM(4/4)**

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Title

Modify History

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