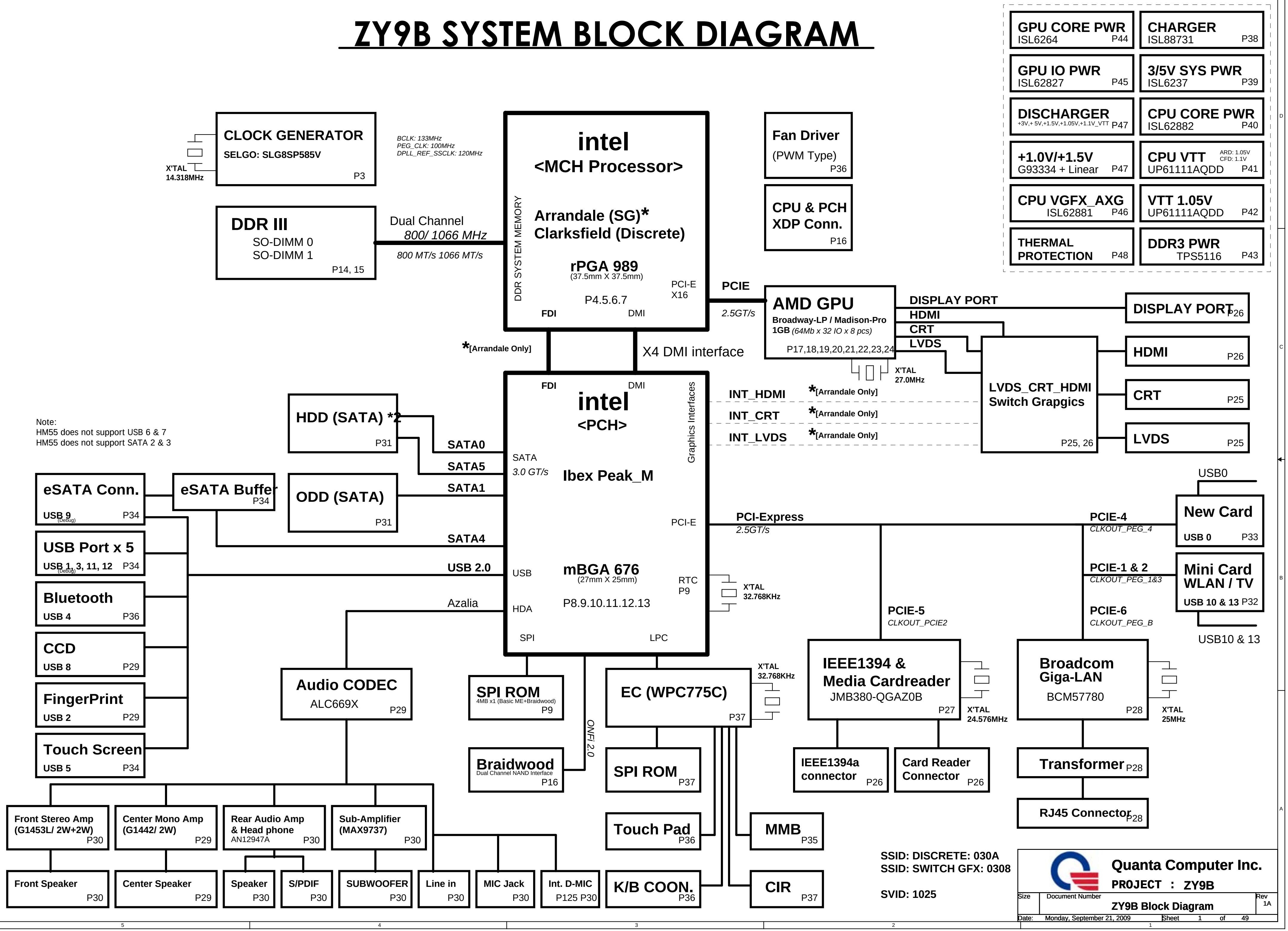
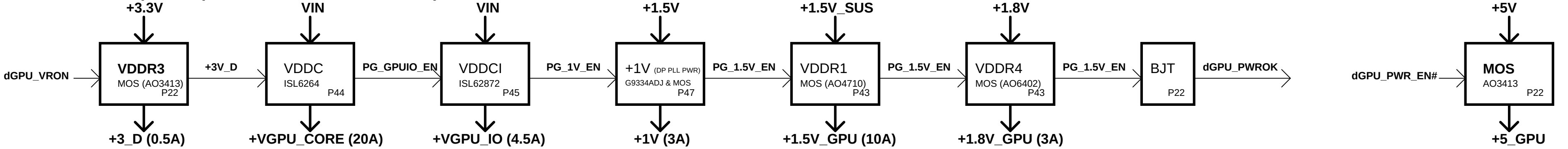
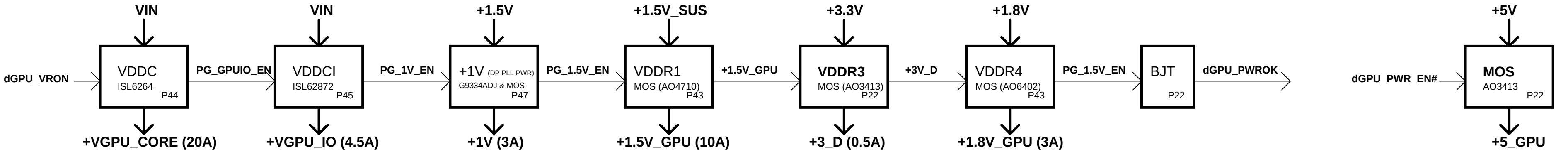
ZY9B SYSTEM BLOCK DIAGRAM



GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



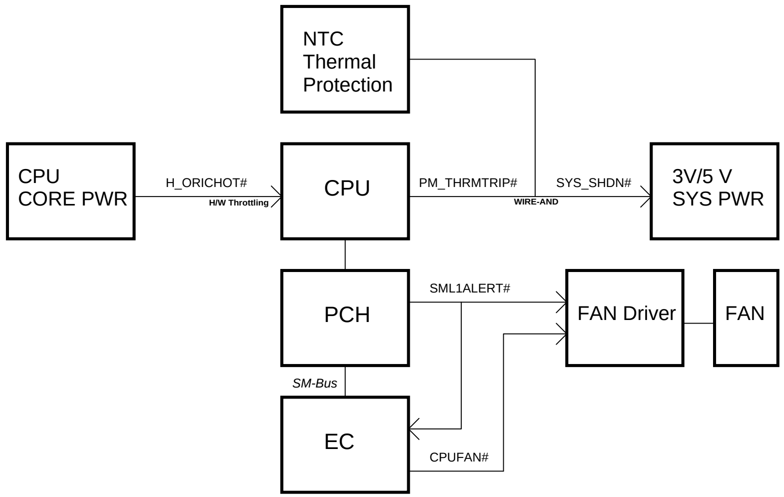
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

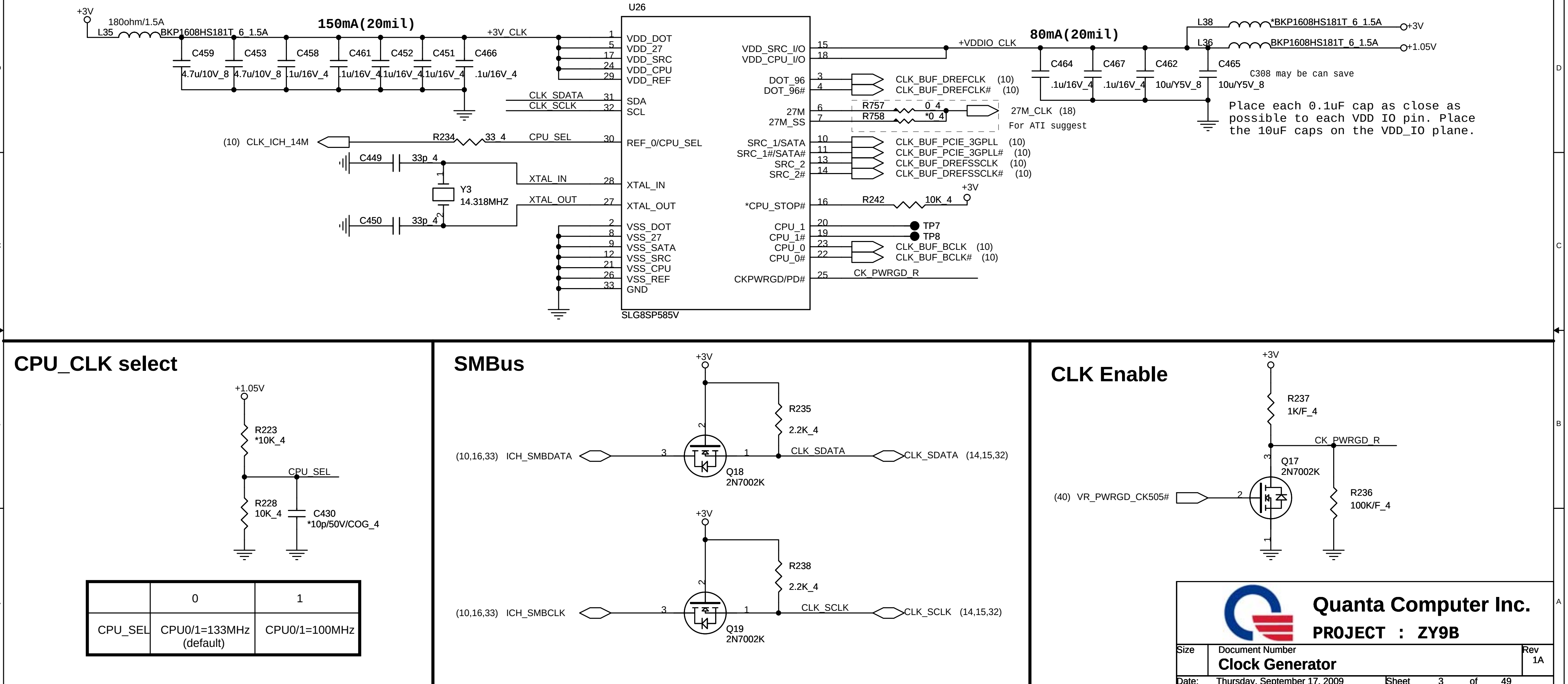


Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart





	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

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Size	Document Number	Rev
	Clock Generator	1A

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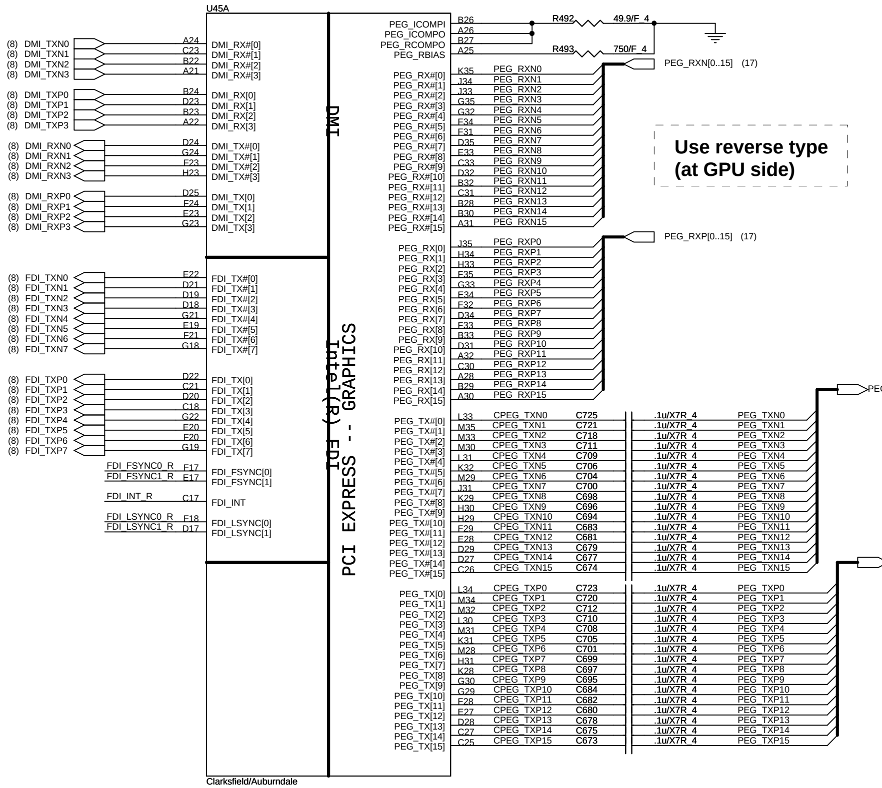
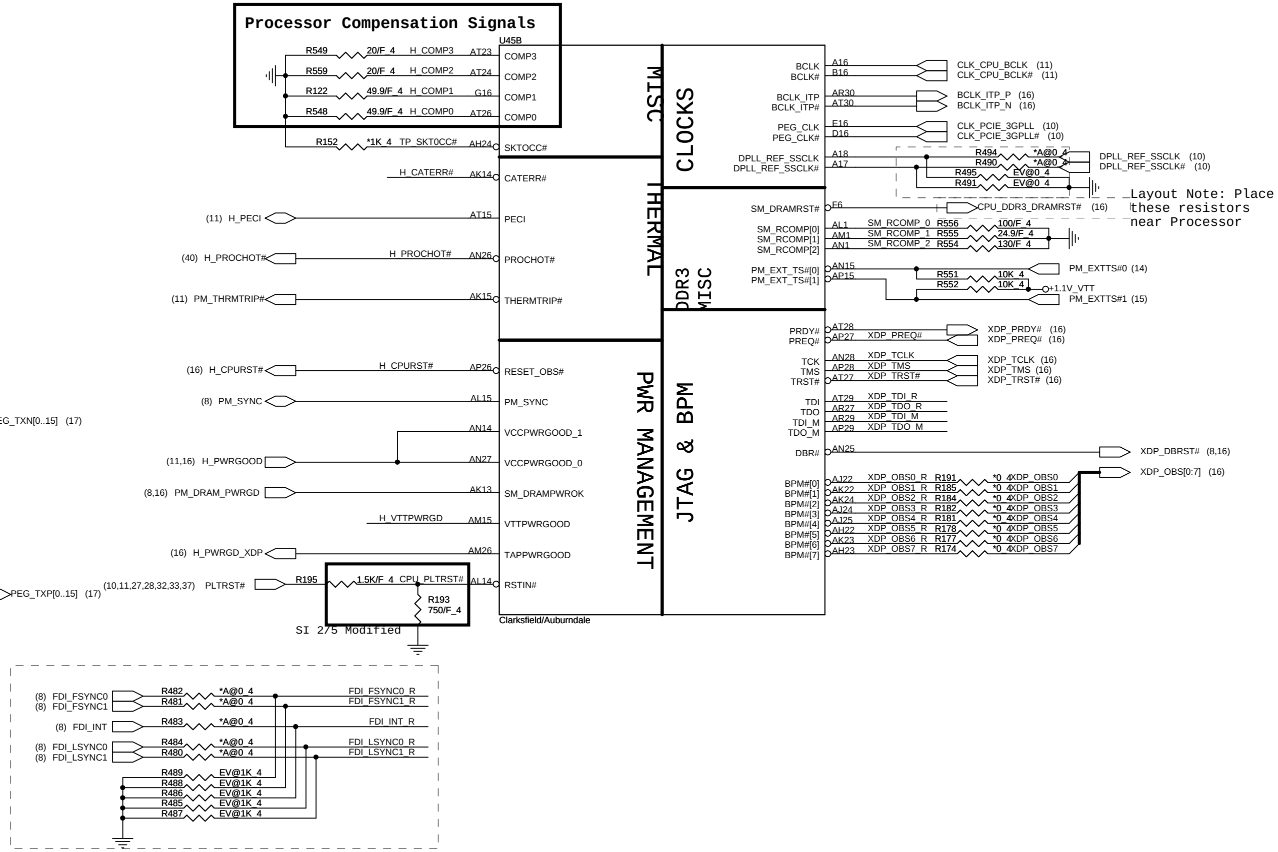
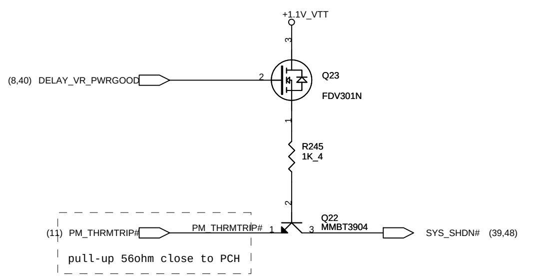
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



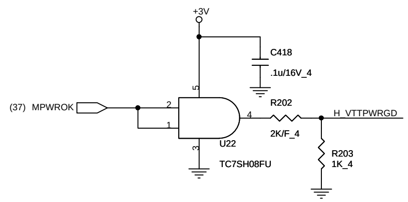
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



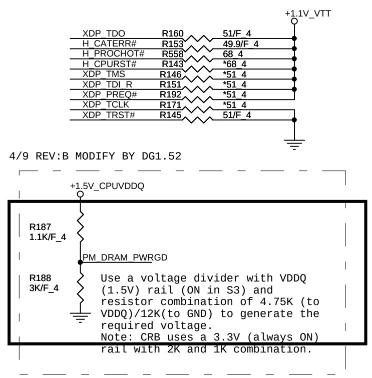
Thermaltrip protect



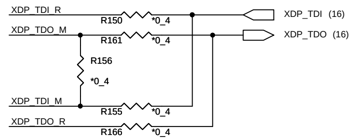
VTT PWR_Good



Processor pull-up



JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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	AUBURNDA 1/4	1A

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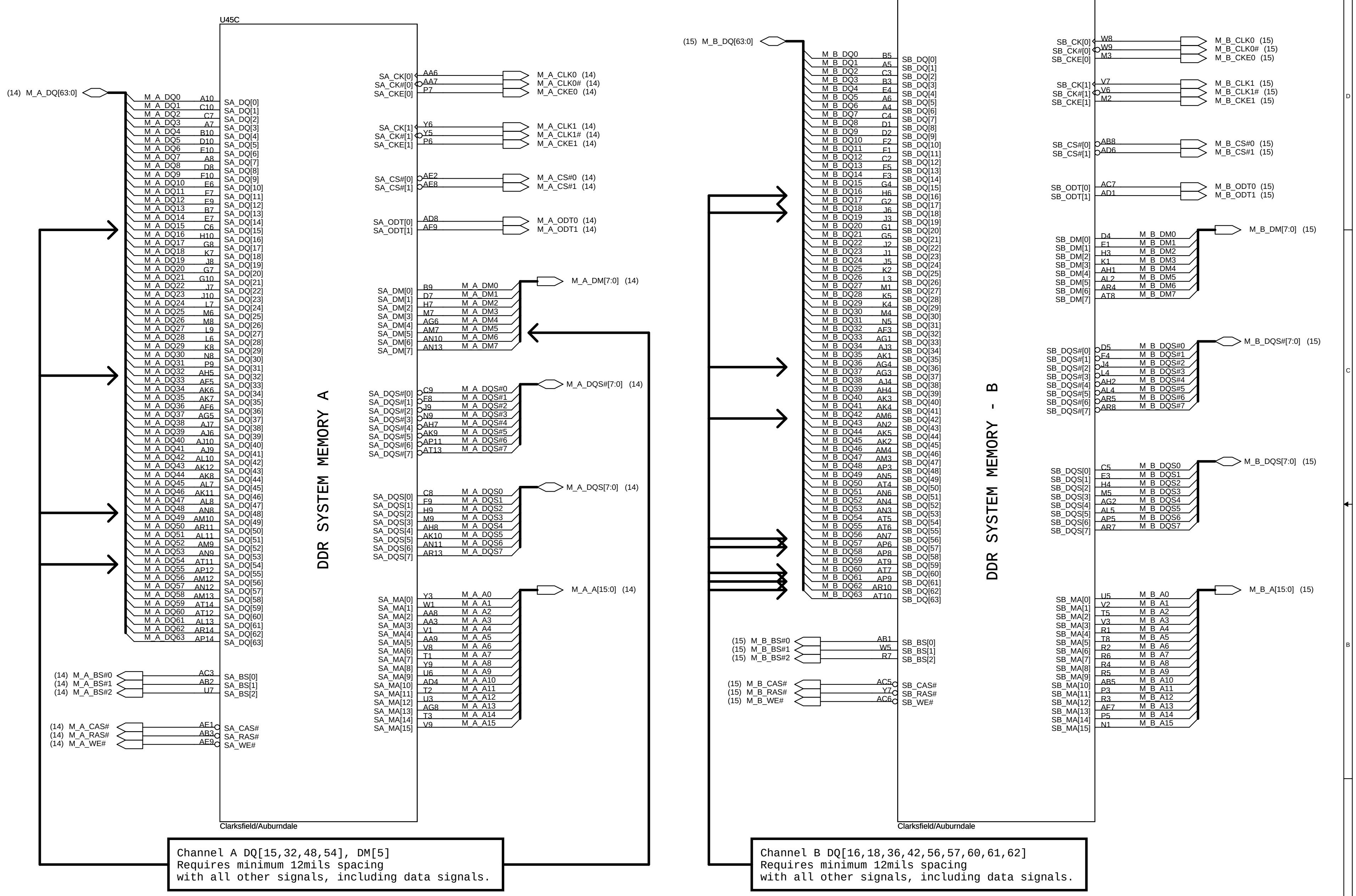
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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	AUBURNDA 2/4	1A

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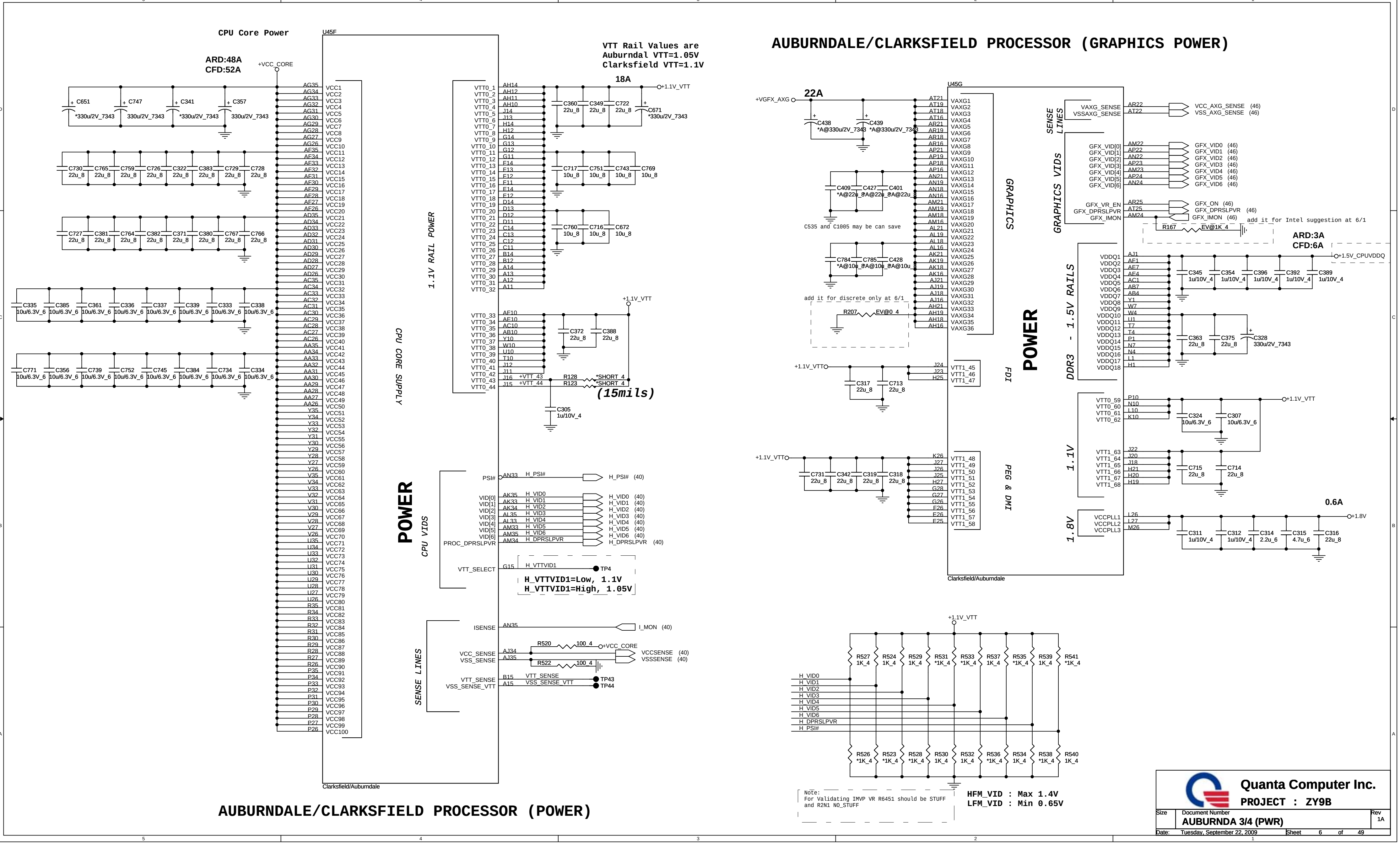

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PROJECT : ZY9B

Size	Document Number	Rev
	AUBURNDA 3/4 (PWR)	1A

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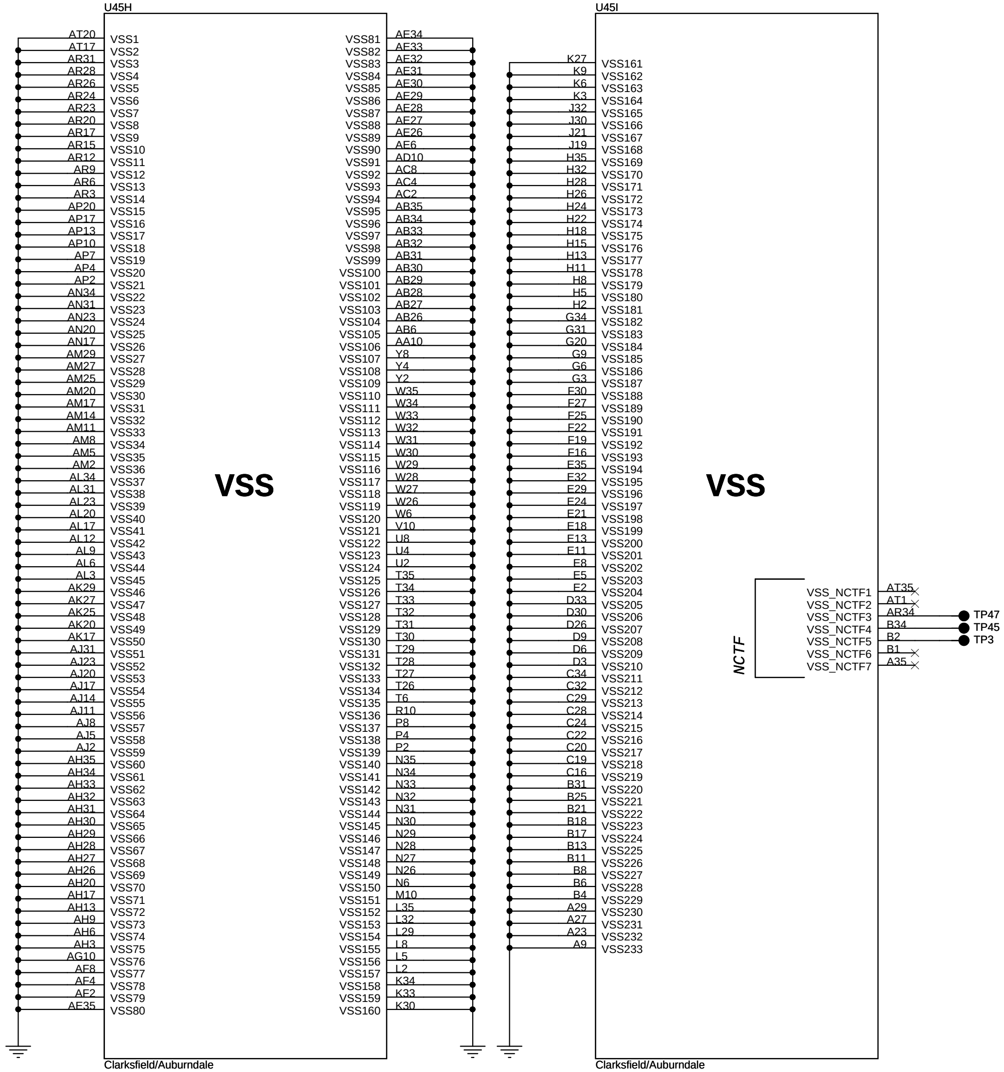
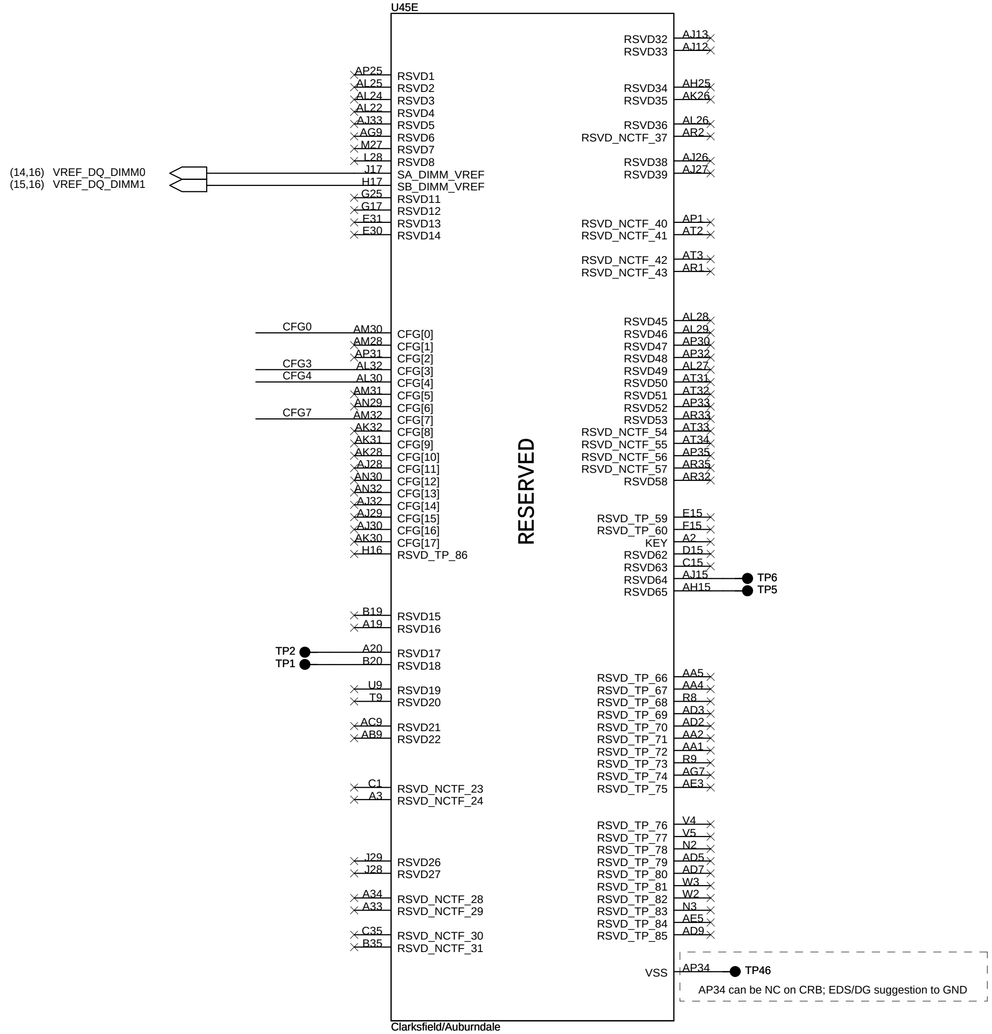
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



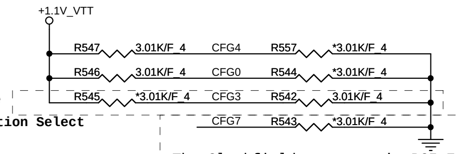
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

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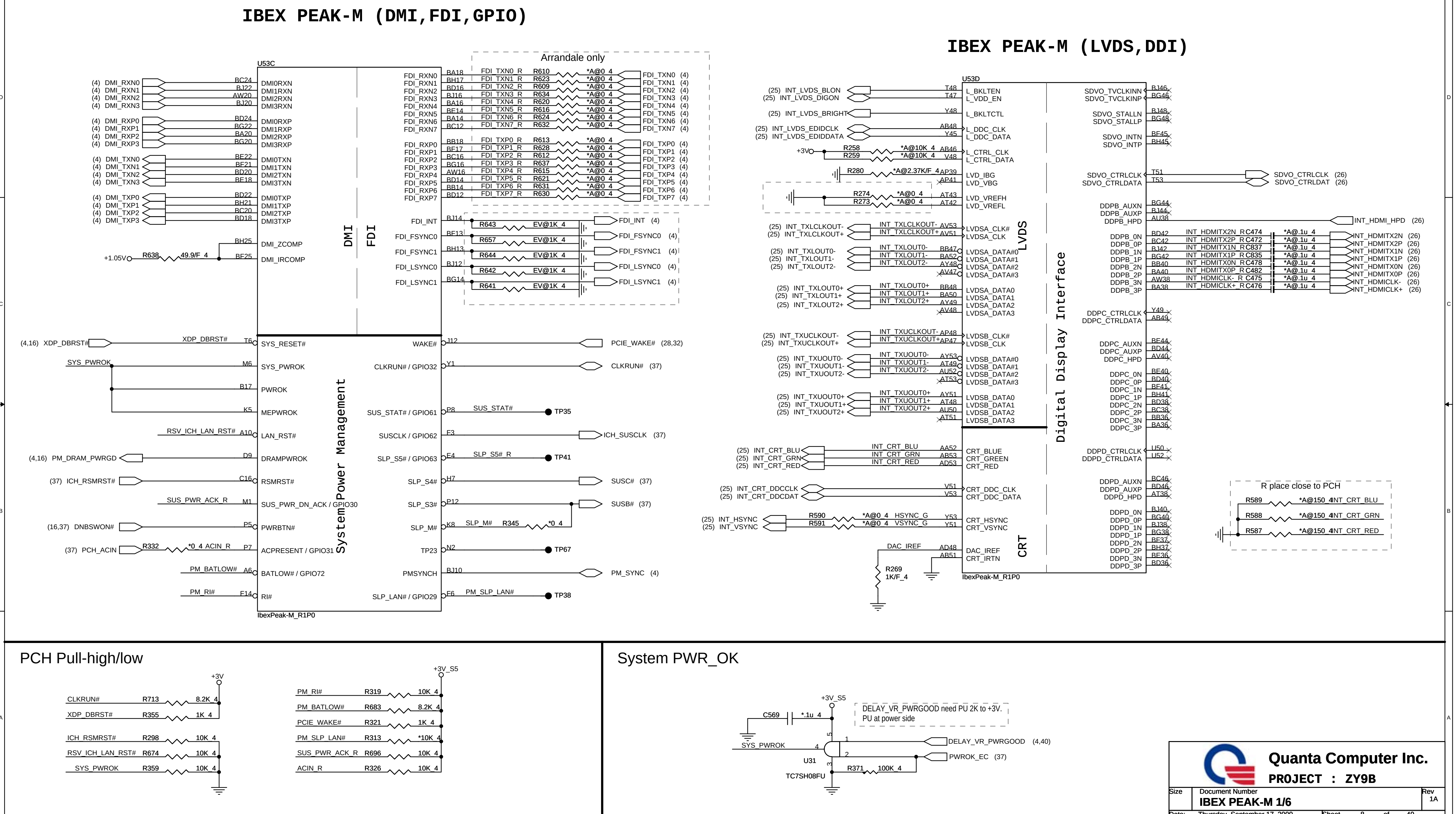

Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	IBEX PEAK-M 1/6	1A
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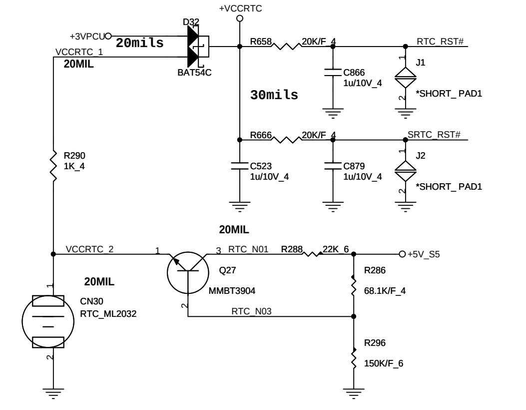
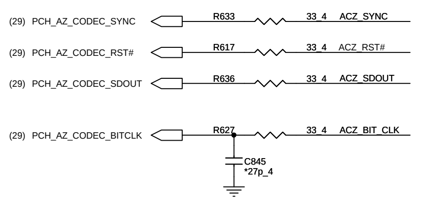
IBEX PEAK-M (HDA,JTAG,SATA)

RTC Circuitry

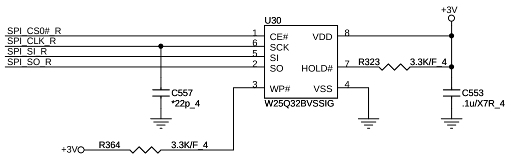


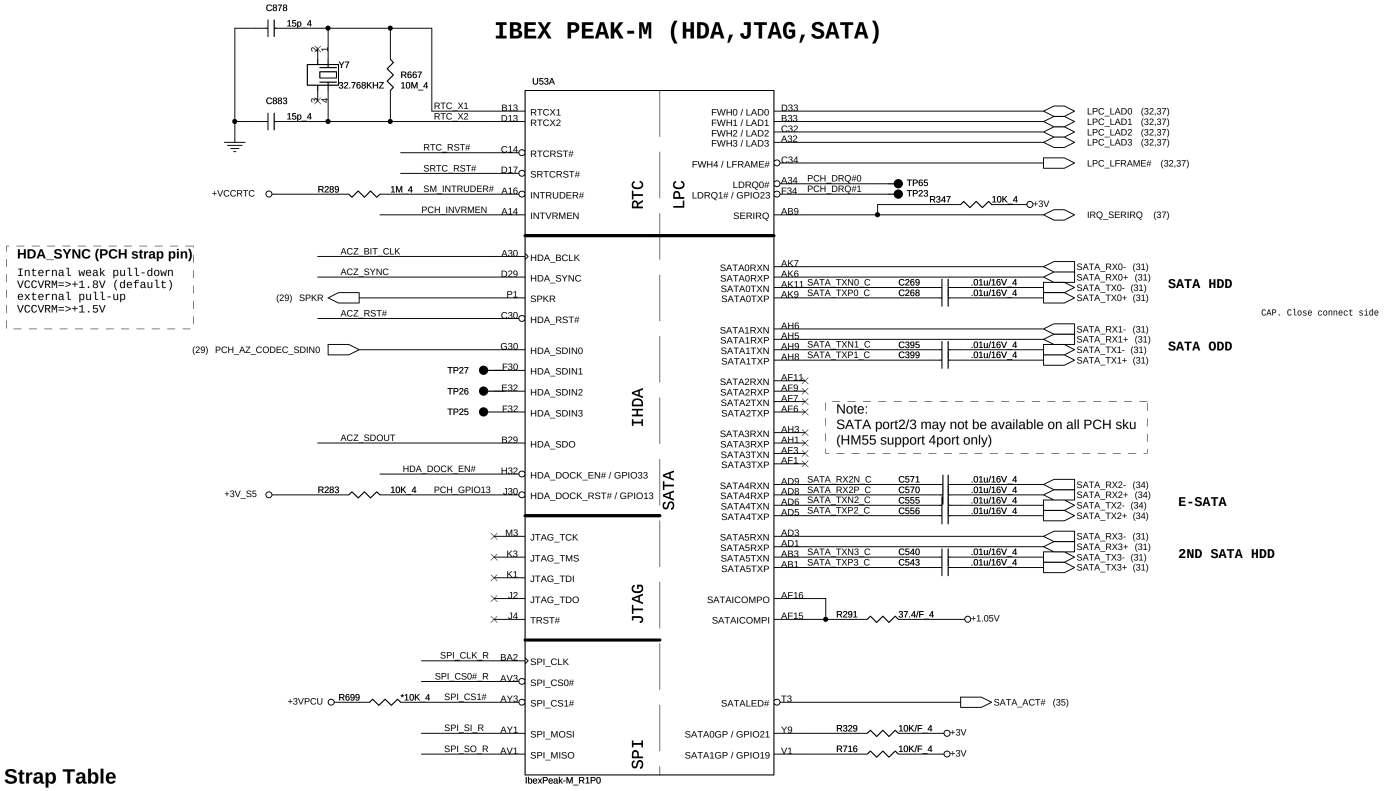
HDA Bus



Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI



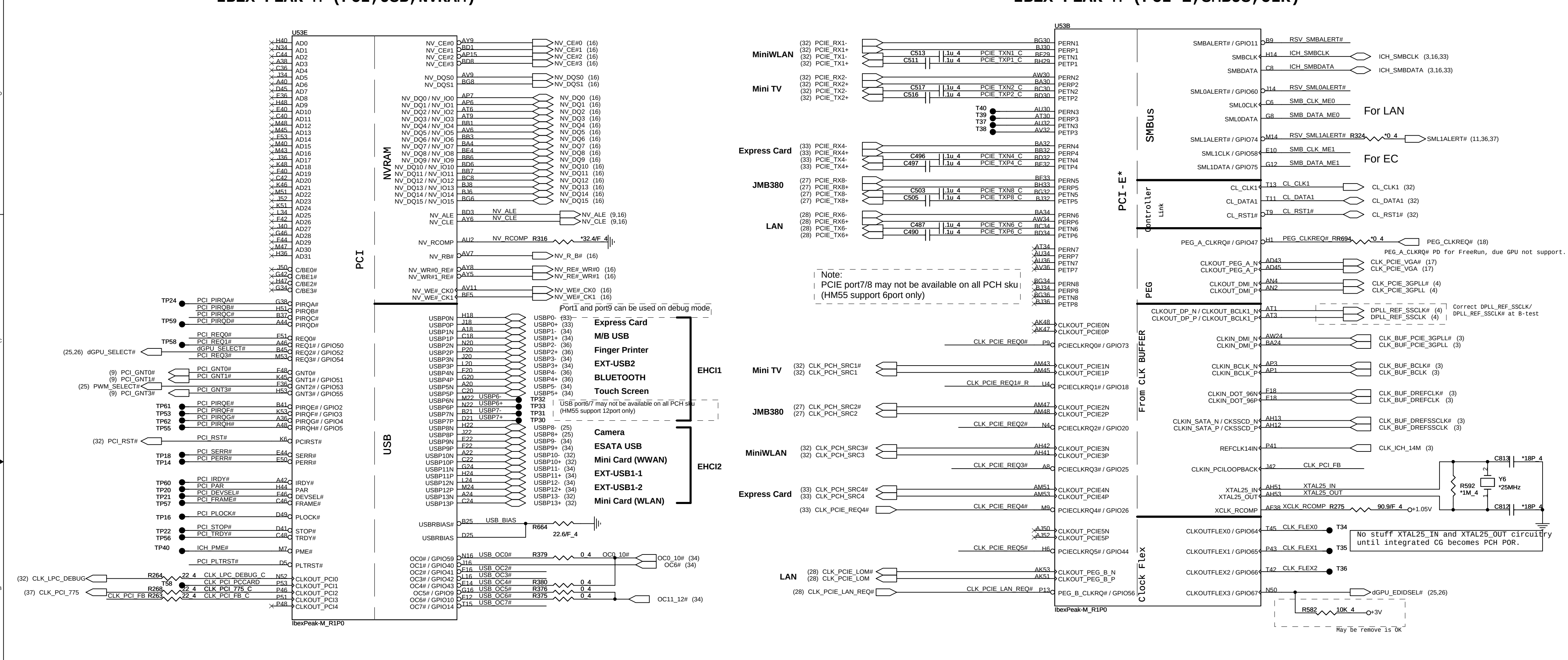


PCH Strap Table

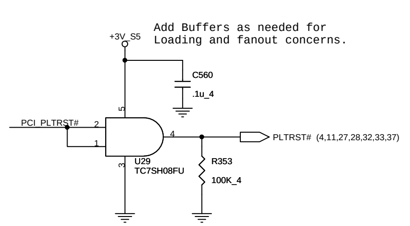
Pin Name	Strap description	Sampled	Configuration	ZY9B note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R702 *10K_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R584 *10K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+VCCRTC R662 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / **LPC**	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]** +3V R270 *1K_4; R256 *1K_4; R272 1K_4; R271 1K_4; PCI_GNT0# (10); PCI_GNT1# (10)
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R698 *1K_4 NV_ALE NV_ALE (10,16)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R697 *1K_4 NV_CLE NV_CLE (10,16)
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	R279 *1K_4; +3V R276 *10K_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R352 *1K_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R340 10K_4 RSV_GPIO8 (11)
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 R330 1K_4 CR_WAKE# (11,27)

IBEX PEAK-M (PCI,USB,NVRAM)

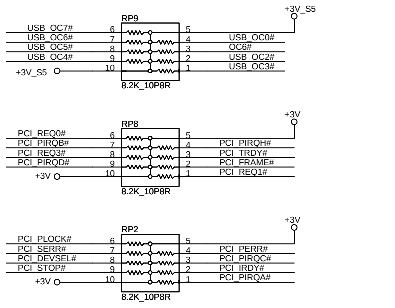
IBEX PEAK-M (PCI-E,SMBUS,CLK)



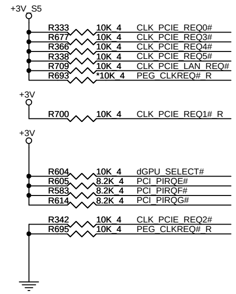
PLTRST#



PCI/USBOC# Pull-up



CLK_REQ/Strap Pin



PEG_A_CLKRQ# PD for FreeRun, due GPU not support.

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

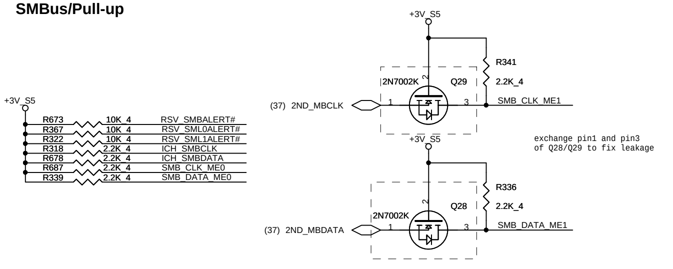
Boot BIOS Strap

GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

SMBus/Pull-up



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	IBEX PEAK-M 3/6	1A
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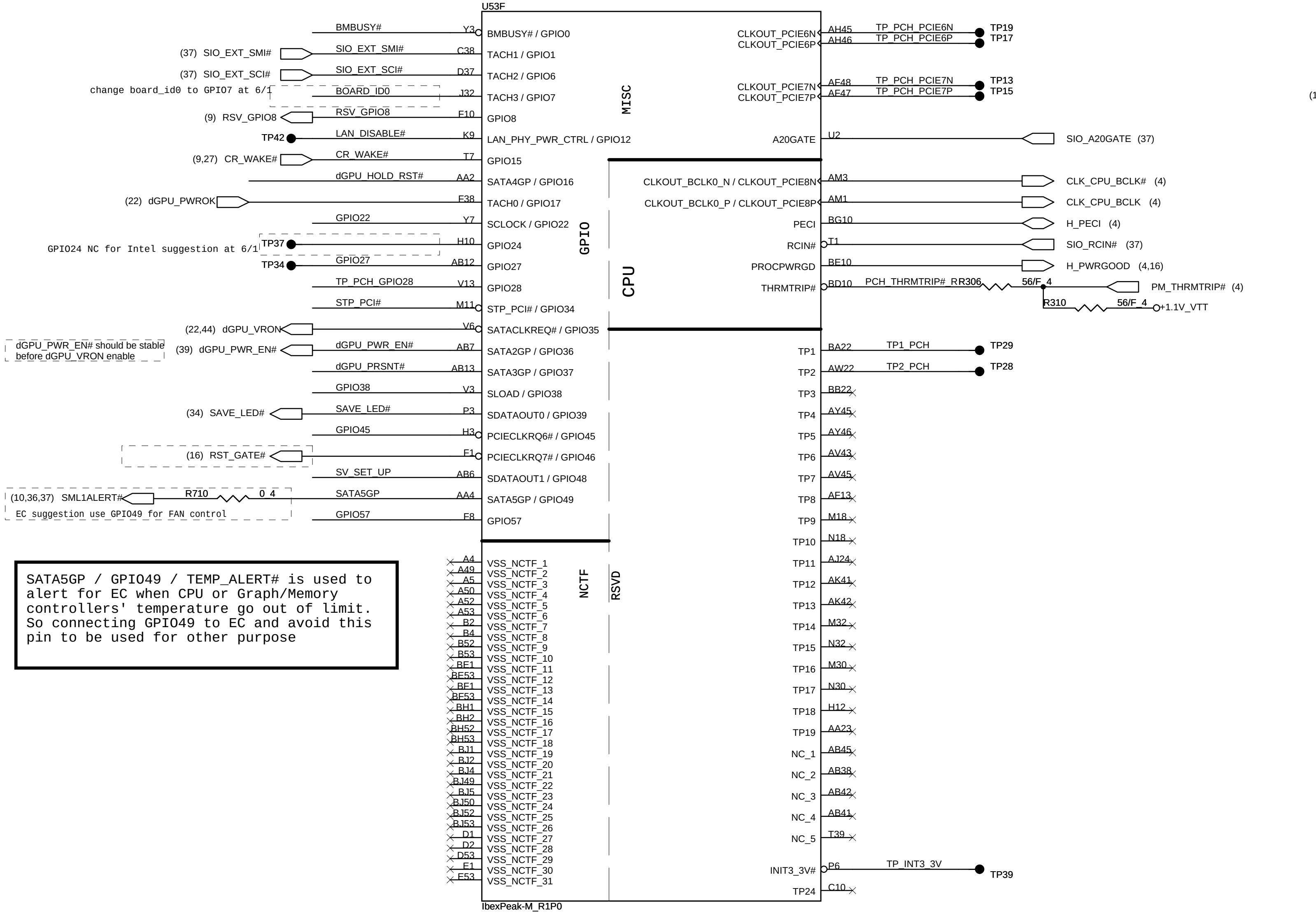
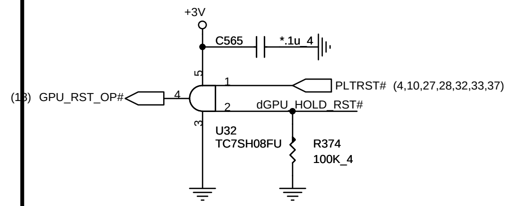
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

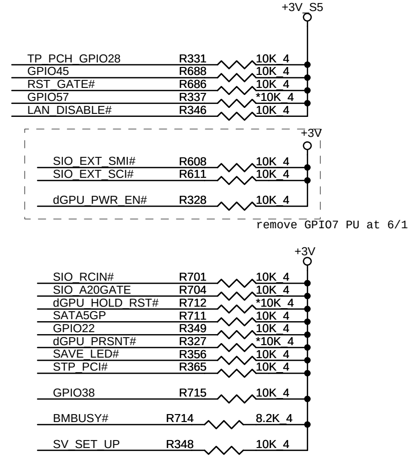


SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

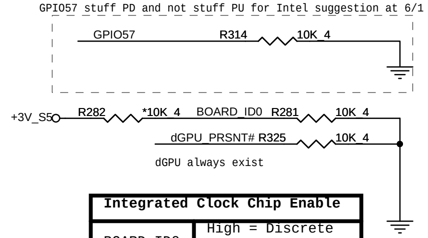
GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)



Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

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	IBEX PEAK-M 4/6	1A

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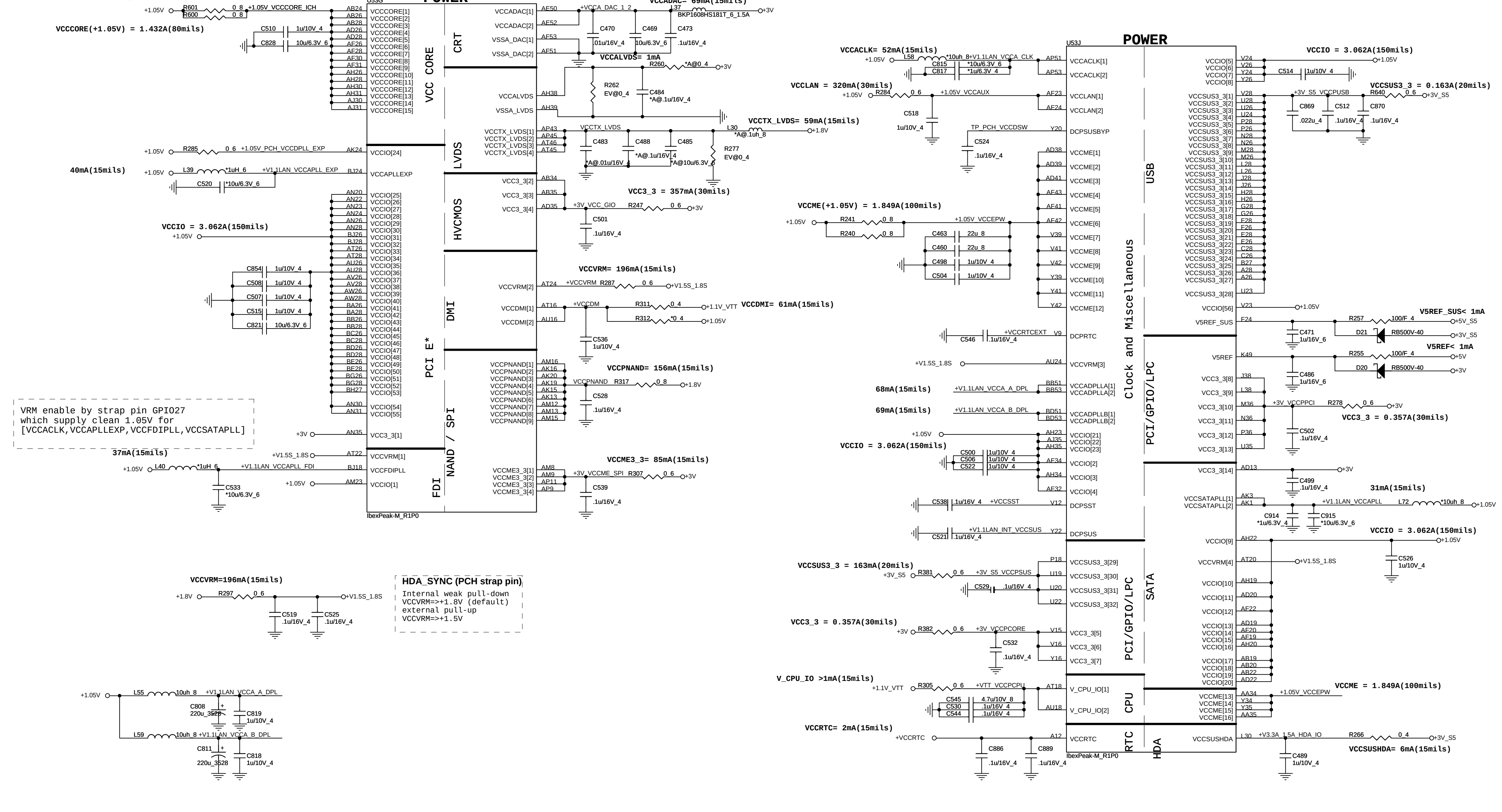
IBEX PEAK-M (POWER)



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	IBEX PEAK-M 5/6	1A

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IBEX PEAK-M (GND)

U53H

Pin	Signal	Signal	Pin
AB16	VSS[0]		
AA19	VSS[1]	VSS[80]	AK30
AA20	VSS[2]	VSS[81]	AK31
AA22	VSS[3]	VSS[82]	AK32
AM19	VSS[4]	VSS[83]	AK34
AA24	VSS[5]	VSS[84]	AK35
AA26	VSS[6]	VSS[85]	AK38
AA28	VSS[7]	VSS[86]	AK43
AA30	VSS[8]	VSS[87]	AK46
AA31	VSS[9]	VSS[88]	AK49
AA32	VSS[10]	VSS[89]	AK5
AB11	VSS[11]	VSS[90]	AK8
AB15	VSS[12]	VSS[91]	AL2
AB23	VSS[13]	VSS[92]	AL52
AB30	VSS[14]	VSS[93]	AM11
AB31	VSS[15]	VSS[94]	BB44
AB32	VSS[16]	VSS[95]	AD24
AB39	VSS[17]	VSS[96]	AM20
AB43	VSS[18]	VSS[97]	AM22
AB47	VSS[19]	VSS[98]	AM24
AB5	VSS[20]	VSS[99]	AM26
AB8	VSS[21]	VSS[100]	AM28
AC2	VSS[22]	VSS[101]	BA42
AC52	VSS[23]	VSS[102]	AM30
AD11	VSS[24]	VSS[103]	AM31
AD12	VSS[25]	VSS[104]	AM32
AD16	VSS[26]	VSS[105]	AM34
AD23	VSS[27]	VSS[106]	AM35
AD30	VSS[28]	VSS[107]	AM38
AD31	VSS[29]	VSS[108]	AM39
AD32	VSS[30]	VSS[109]	AM42
AD34	VSS[31]	VSS[110]	AU20
AU22	VSS[32]	VSS[111]	AM46
AD42	VSS[33]	VSS[112]	AV22
AD46	VSS[34]	VSS[113]	AM49
AD49	VSS[35]	VSS[114]	AM7
AD7	VSS[36]	VSS[115]	AA50
AE2	VSS[37]	VSS[116]	BB10
AE4	VSS[38]	VSS[117]	AN32
AF12	VSS[39]	VSS[118]	AN50
Y13	VSS[40]	VSS[119]	AN52
AH49	VSS[41]	VSS[120]	AP12
AU4	VSS[42]	VSS[121]	AP42
AF35	VSS[43]	VSS[122]	AP46
AP13	VSS[44]	VSS[123]	AP49
AN34	VSS[45]	VSS[124]	AP5
AF45	VSS[46]	VSS[125]	AP8
AF46	VSS[47]	VSS[126]	AR2
AF49	VSS[48]	VSS[127]	AR52
AF5	VSS[49]	VSS[128]	AT11
AF8	VSS[50]	VSS[129]	BA12
AG2	VSS[51]	VSS[130]	AH48
AG52	VSS[52]	VSS[131]	AT32
AH11	VSS[53]	VSS[132]	AT36
AH15	VSS[54]	VSS[133]	AT41
AH16	VSS[55]	VSS[134]	AT47
AH24	VSS[56]	VSS[135]	AT7
AH32	VSS[57]	VSS[136]	AV12
AV18	VSS[58]	VSS[137]	AV16
AH43	VSS[59]	VSS[138]	AV20
AH47	VSS[60]	VSS[139]	AV24
AH7	VSS[61]	VSS[140]	AV30
AJ19	VSS[62]	VSS[141]	AV34
AJ2	VSS[63]	VSS[142]	AV38
AJ20	VSS[64]	VSS[143]	AV42
AJ22	VSS[65]	VSS[144]	AV46
AJ23	VSS[66]	VSS[145]	AV49
AJ26	VSS[67]	VSS[146]	AV5
AJ28	VSS[68]	VSS[147]	AV8
AJ32	VSS[69]	VSS[148]	AW14
AJ34	VSS[70]	VSS[149]	AW18
AT5	VSS[71]	VSS[150]	AW2
AJ4	VSS[72]	VSS[151]	BF9
AK12	VSS[73]	VSS[152]	AW32
AM41	VSS[74]	VSS[153]	AW36
AN19	VSS[75]	VSS[154]	AW40
AK26	VSS[76]	VSS[155]	AW52
AK22	VSS[77]	VSS[156]	AY11
AK23	VSS[78]	VSS[157]	AY43
AK28	VSS[79]	VSS[158]	AY47

IbexPeak-M_R1P0

U53I

Pin	Signal	Signal	Pin
AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH9	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	T8
BE46	VSS[203]	VSS[303]	U30
BE48	VSS[204]	VSS[304]	U31
BE50	VSS[205]	VSS[305]	U32
BE6	VSS[206]	VSS[306]	U34
BE8	VSS[207]	VSS[307]	P38
BF3	VSS[208]	VSS[308]	V11
BF49	VSS[209]	VSS[309]	P16
BF51	VSS[210]	VSS[310]	V19
BG18	VSS[211]	VSS[311]	V20
BG24	VSS[212]	VSS[312]	V22
BG4	VSS[213]	VSS[313]	V30
BG50	VSS[214]	VSS[314]	V31
BH11	VSS[215]	VSS[315]	V32
BH15	VSS[216]	VSS[316]	V34
BH19	VSS[217]	VSS[317]	V35
BH23	VSS[218]	VSS[318]	V38
BH31	VSS[219]	VSS[319]	V43
BH35	VSS[220]	VSS[320]	V45
BH39	VSS[221]	VSS[321]	V46
BH43	VSS[222]	VSS[322]	V47
BH47	VSS[223]	VSS[323]	V49
BH7	VSS[224]	VSS[324]	V5
C12	VSS[225]	VSS[325]	V7
C50	VSS[226]	VSS[326]	V8
D51	VSS[227]	VSS[327]	W2
E12	VSS[228]	VSS[328]	W52
E16	VSS[229]	VSS[329]	Y11
E20	VSS[230]	VSS[330]	Y12
E24	VSS[231]	VSS[331]	Y15
E30	VSS[232]	VSS[332]	Y19
E34	VSS[233]	VSS[333]	Y23
E38	VSS[234]	VSS[334]	Y28
E42	VSS[235]	VSS[335]	Y30
E46	VSS[236]	VSS[336]	Y31
E48	VSS[237]	VSS[337]	Y32
E6	VSS[238]	VSS[338]	Y38
E8	VSS[239]	VSS[339]	Y43
F49	VSS[240]	VSS[340]	Y46
F5	VSS[241]	VSS[341]	P49
G10	VSS[242]	VSS[342]	Y5
G14	VSS[243]	VSS[343]	Y6
G18	VSS[244]	VSS[344]	Y8
G2	VSS[245]	VSS[345]	P24
G22	VSS[246]	VSS[346]	T43
G32	VSS[247]	VSS[347]	AD51
G36	VSS[248]	VSS[348]	AT8
G40	VSS[249]	VSS[349]	AD47
G44	VSS[250]	VSS[350]	Y47
G52	VSS[251]	VSS[351]	AT12
AF39	VSS[252]	VSS[352]	AM6
H16	VSS[253]	VSS[353]	AT13
H20	VSS[254]	VSS[354]	AM5
H30	VSS[255]	VSS[355]	AK45
H34	VSS[256]	VSS[356]	AK39
H38	VSS[257]	VSS[366]	AV14
H42	VSS[258]		

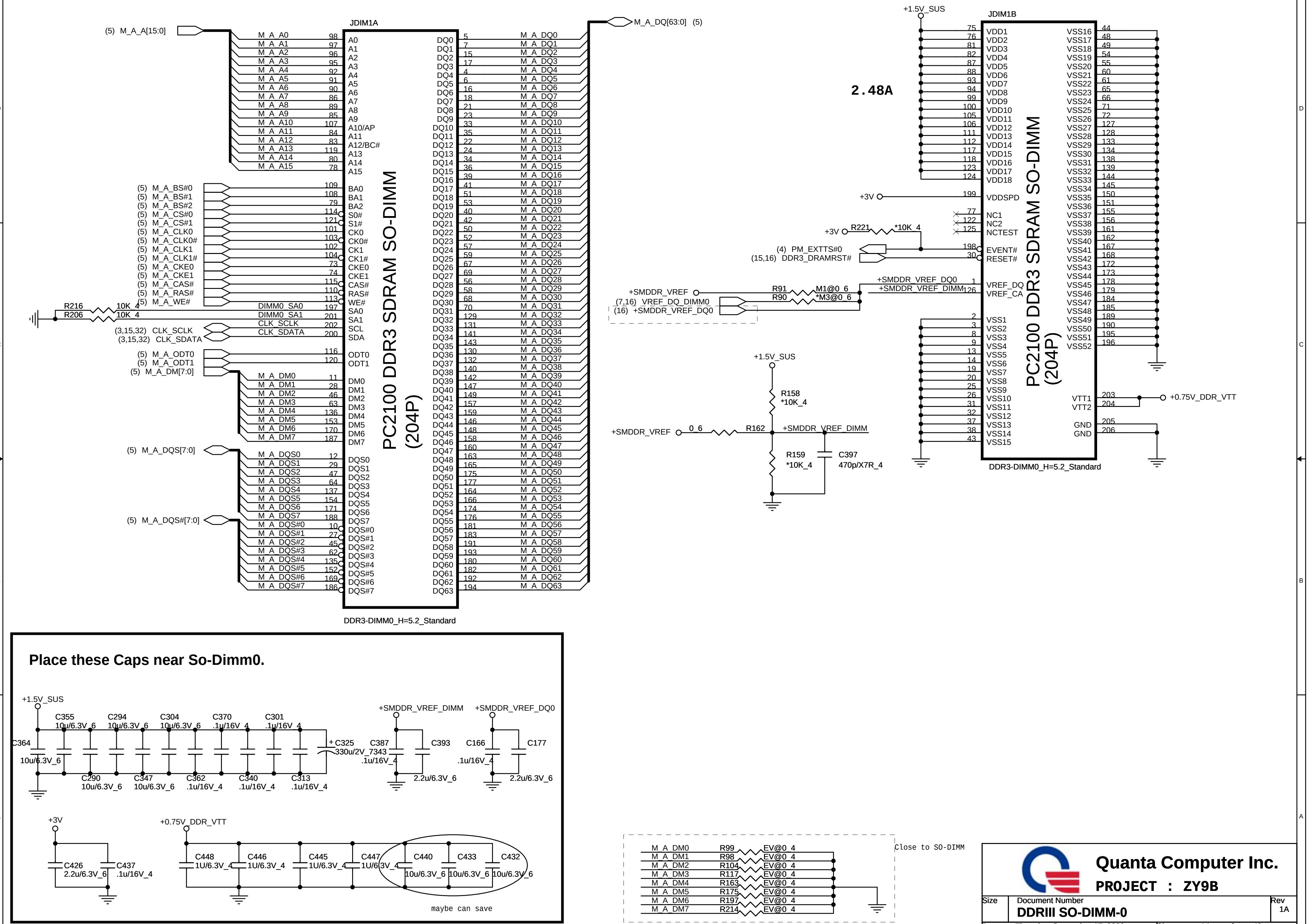
IbexPeak-M_R1P0

Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

Date: Thursday, June 18, 2009 Sheet 13 of 49

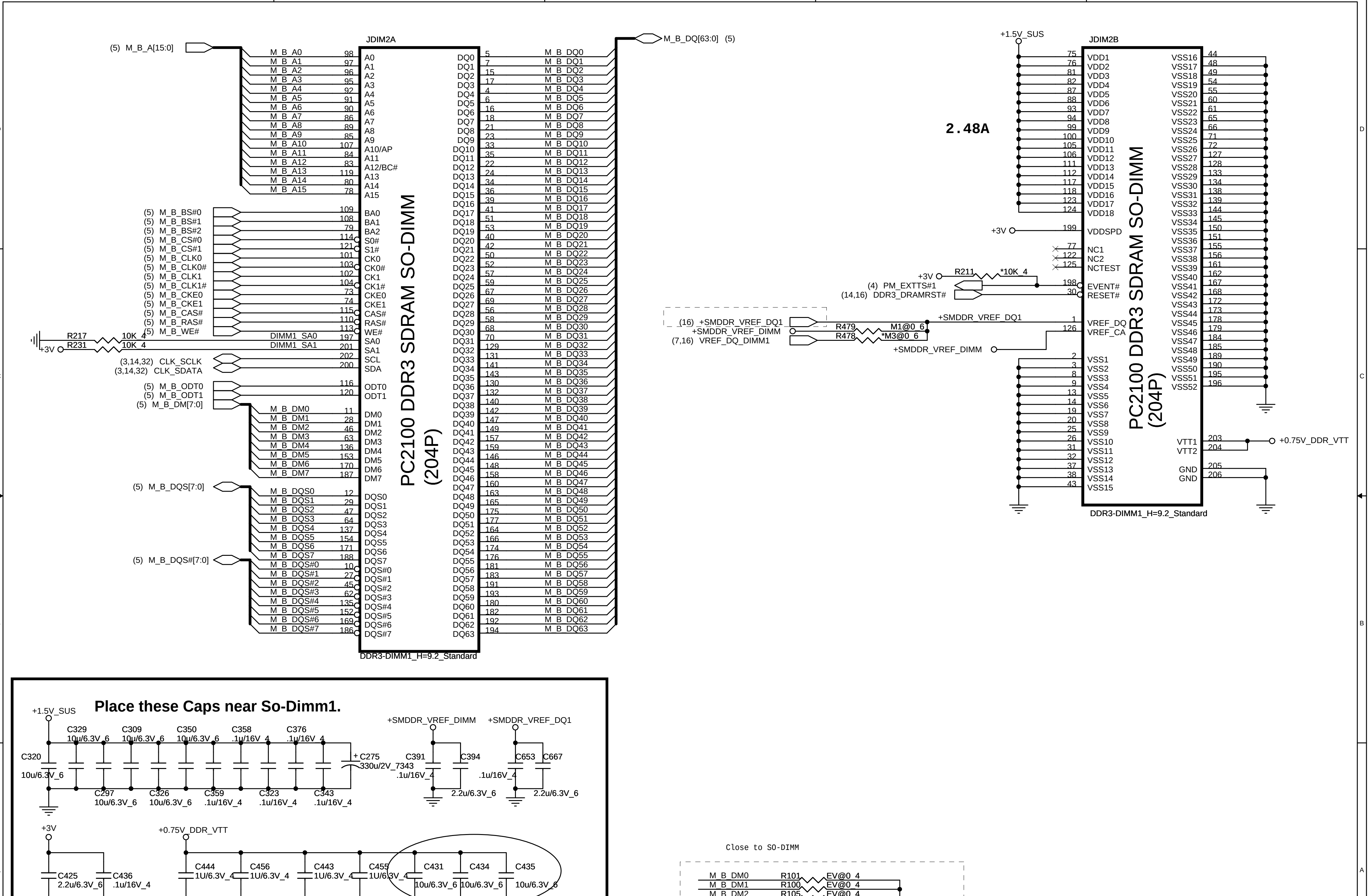


Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A

Date: Thursday, September 17, 2009 Sheet 14 of 49

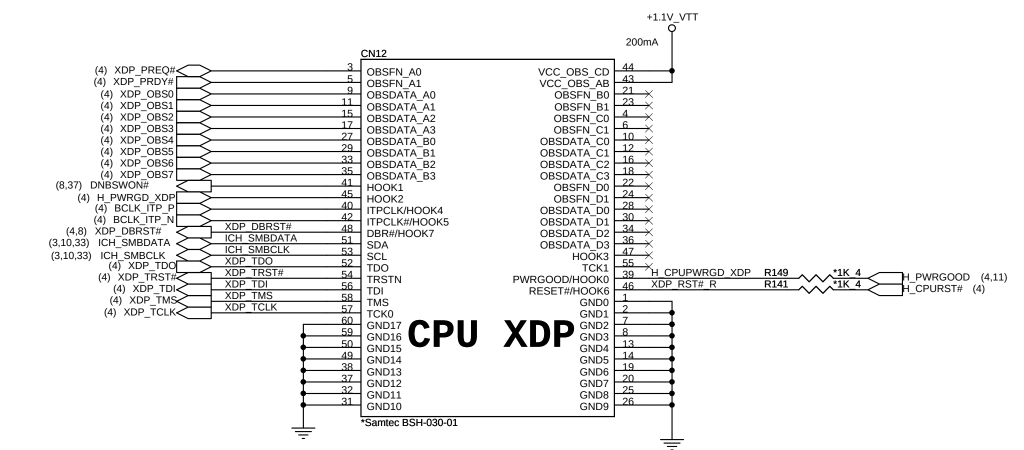


Quanta Computer Inc.

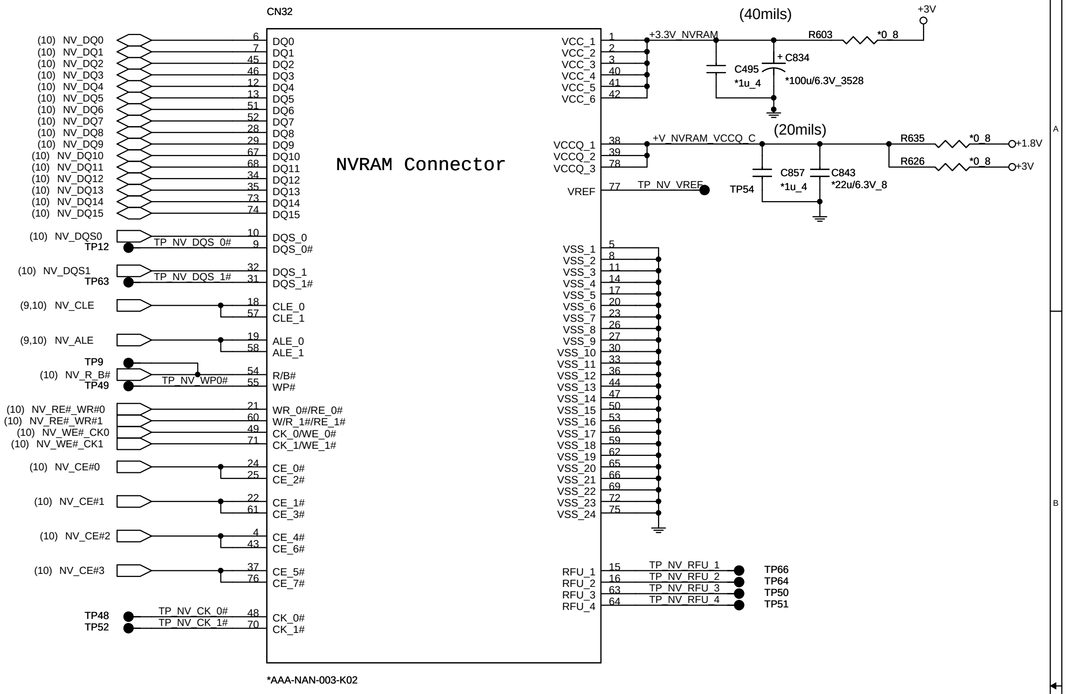
PROJECT : ZY9B

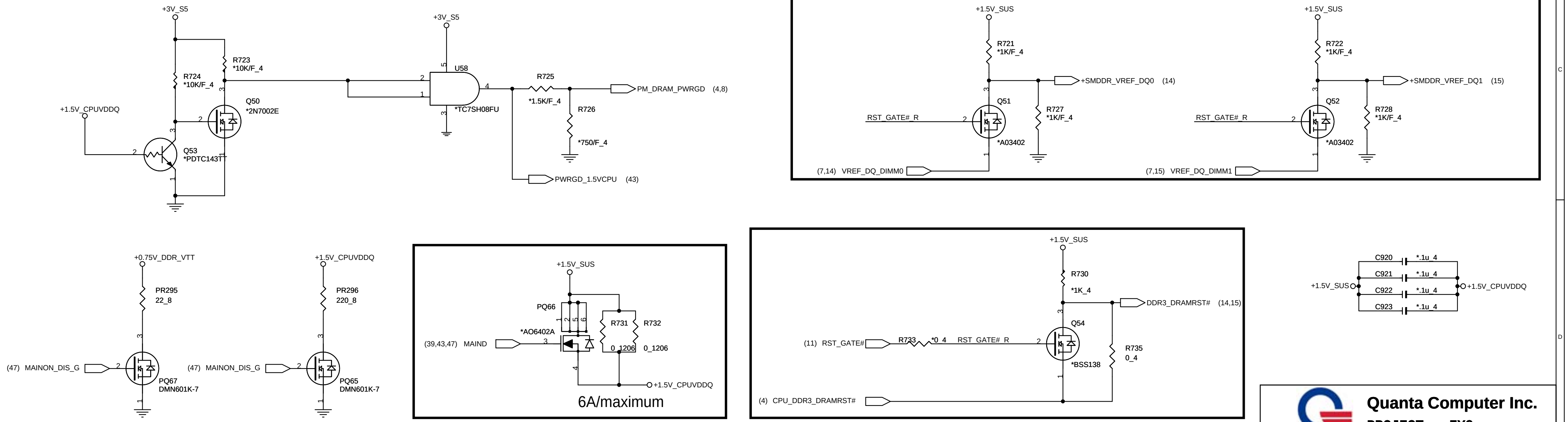
Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date: Thursday, September 17, 2009	Sheet 15 of 49	

CPU XDP Connector



Braidwood



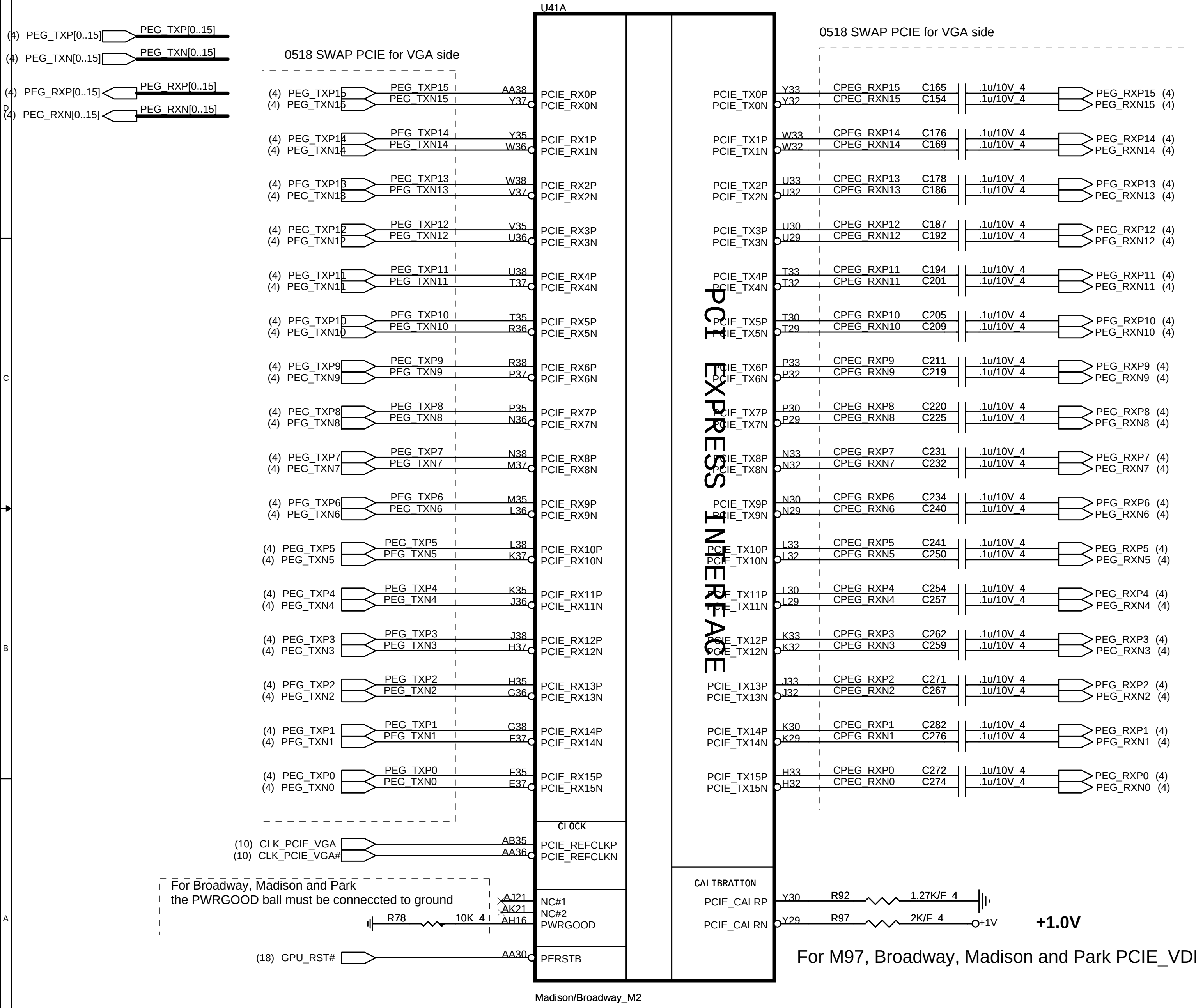


Quanta Computer Inc.

PROJECT : ZY9

Size	Document Number	Rev
	XDP/BRAIDWOOD	1A

Date: Thursday, September 17, 2009 Sheet 16 of 49



For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Quanta Computer Inc.

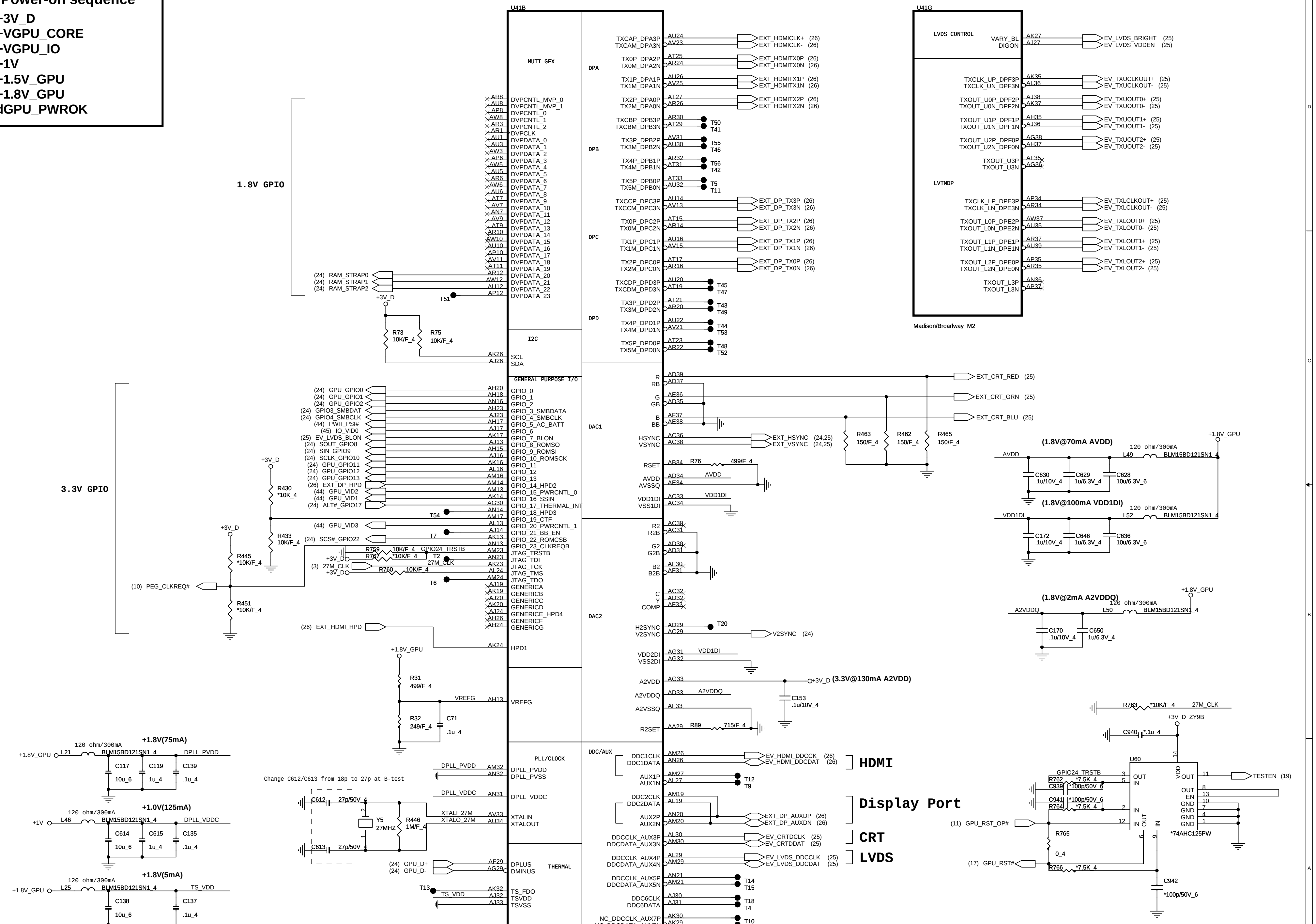
PROJECT : ZY9B

Size	Document Number	Rev
	Madison/Broadway-PCIE I/F	1A

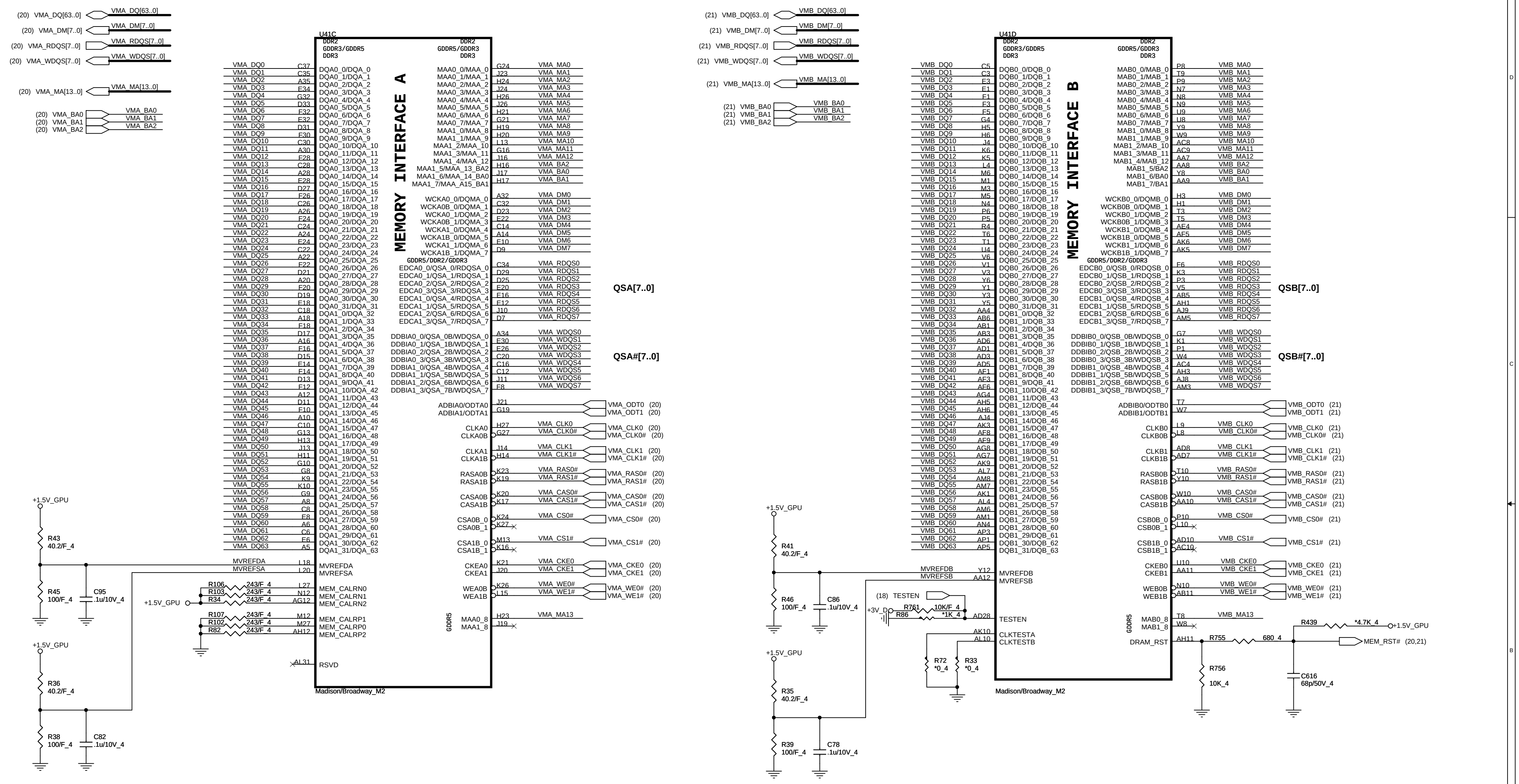
Date: Thursday, September 17, 2009 Sheet 17 of 49

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK



Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: Madison/Broadway-HOST I/F	Rev 1A
Date: Tuesday, September 22, 2009	Sheet 18 of 49	



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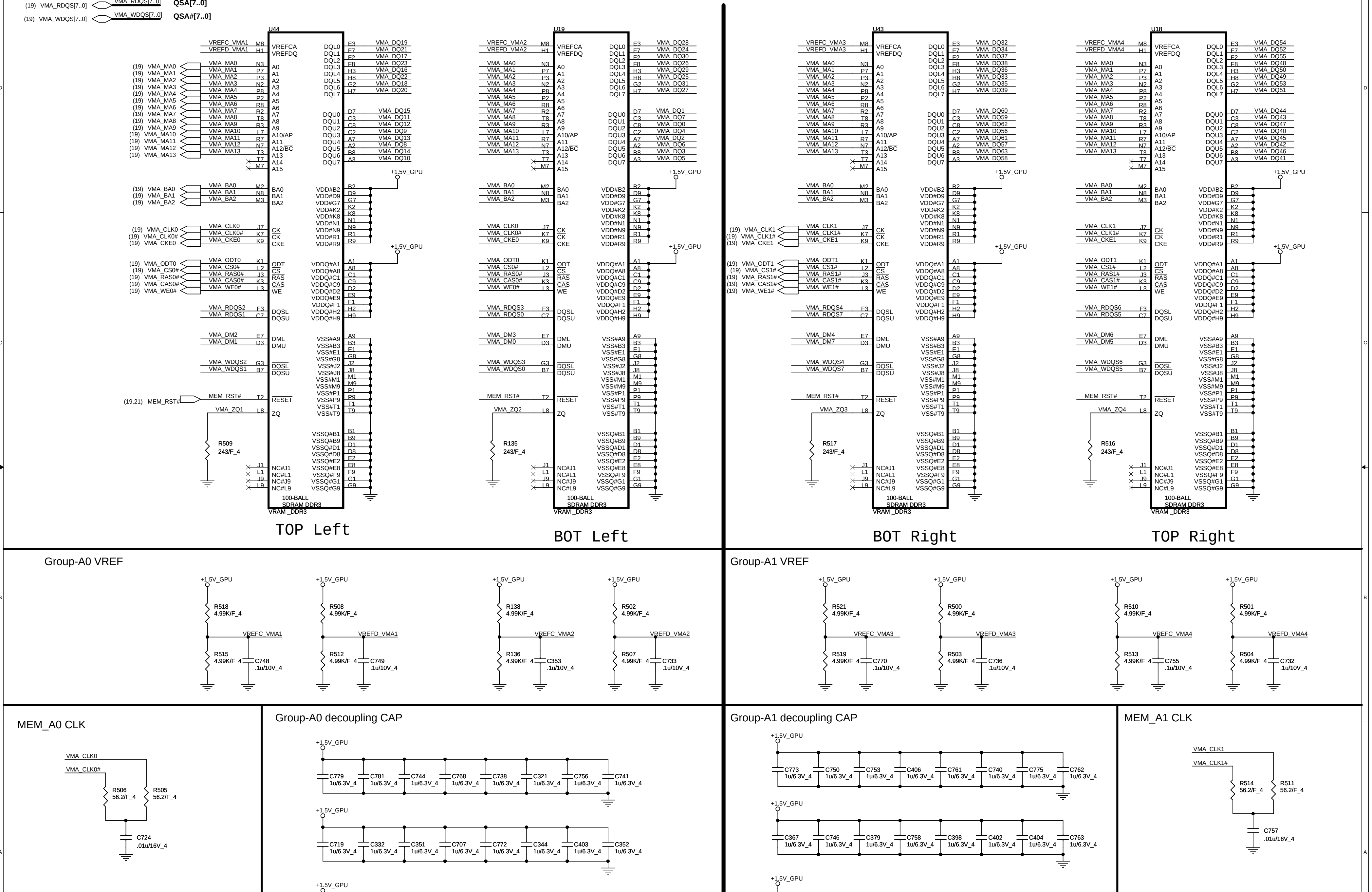
PROJECT : ZY9B

Size	Document Number	Rev
	Madison/Broadway-MEM I/F	1A
Date: Tuesday, September 22, 2009	Sheet 19 of 49	

CHANNEL A: 512MB DDR3 (64M*16*4pcs)



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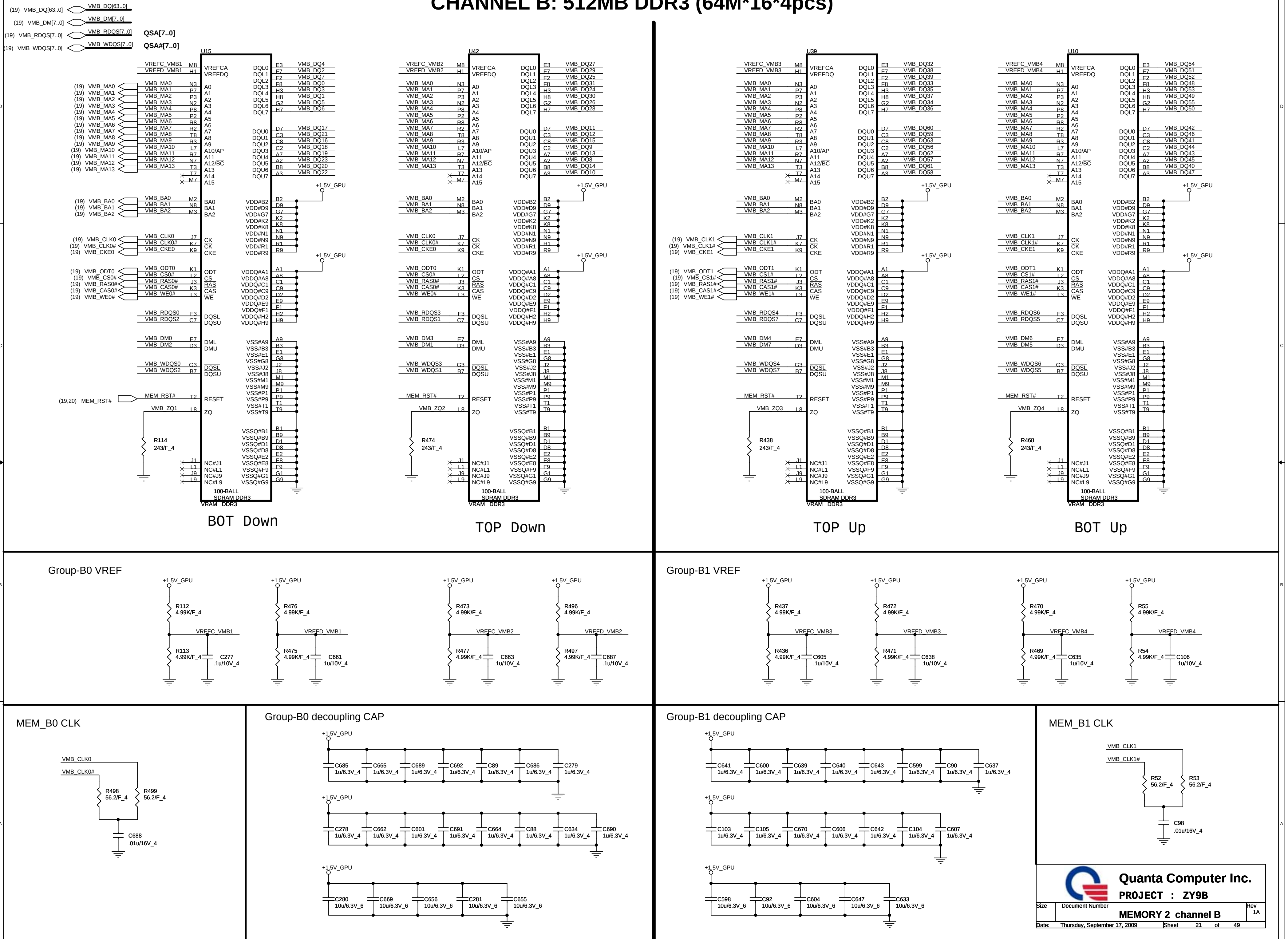
PROJECT : ZY9B

Size	Document Number	Rev
	MEMORY 1 channel A	1A

Date: Thursday, September 17, 2009 Sheet 20 of 49

CHANNEL B: 512MB DDR3 (64M*16*4pcs)

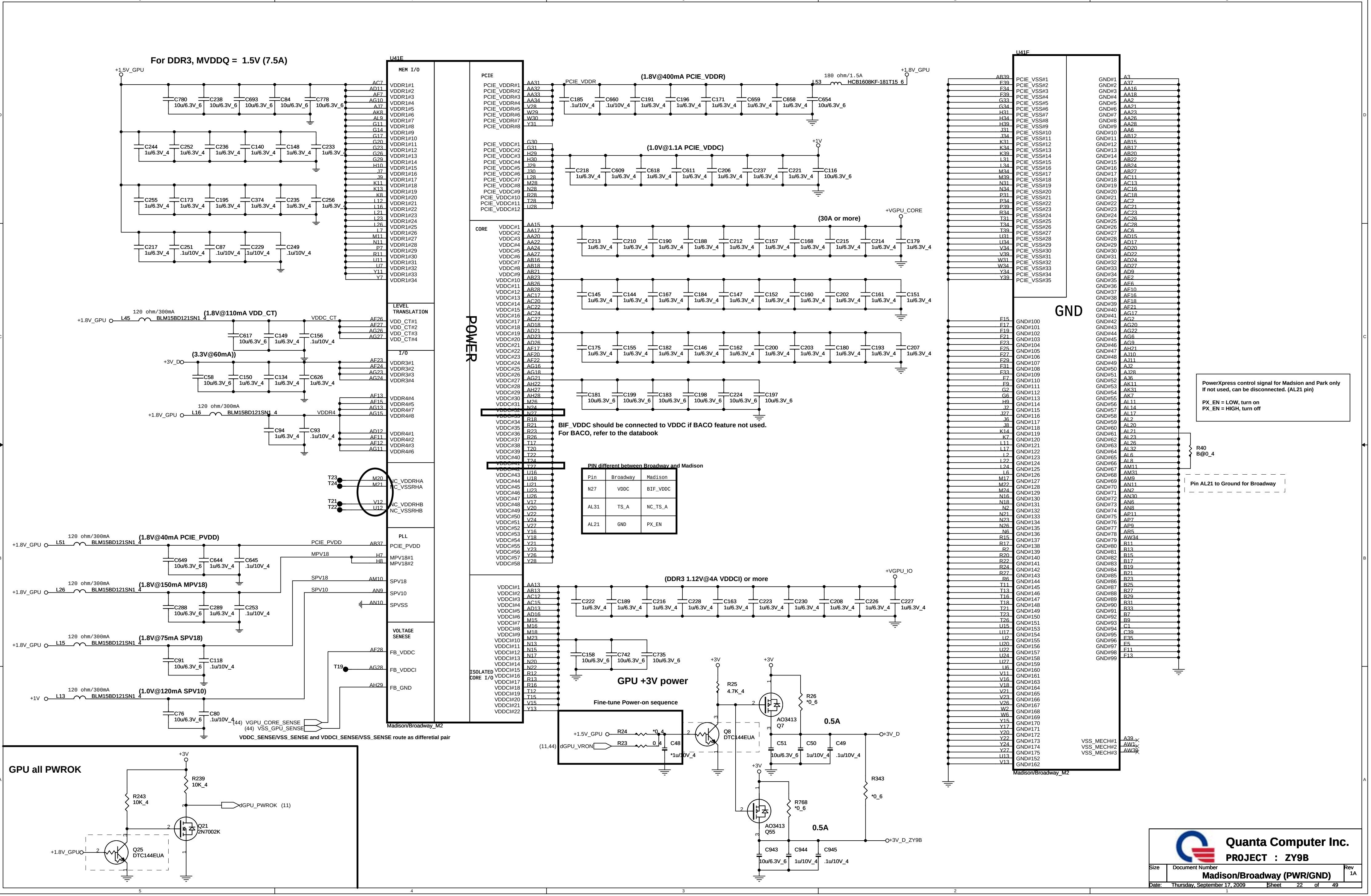


Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	MEMORY 2 channel B	1A

Date: Thursday, September 17, 2009 Sheet 21 of 49



Pin	Broadway	Madison
N27	VDDC	BIF_VDDC
AL31	TS_A	NC_TS_A
AL21	GND	PX_EN

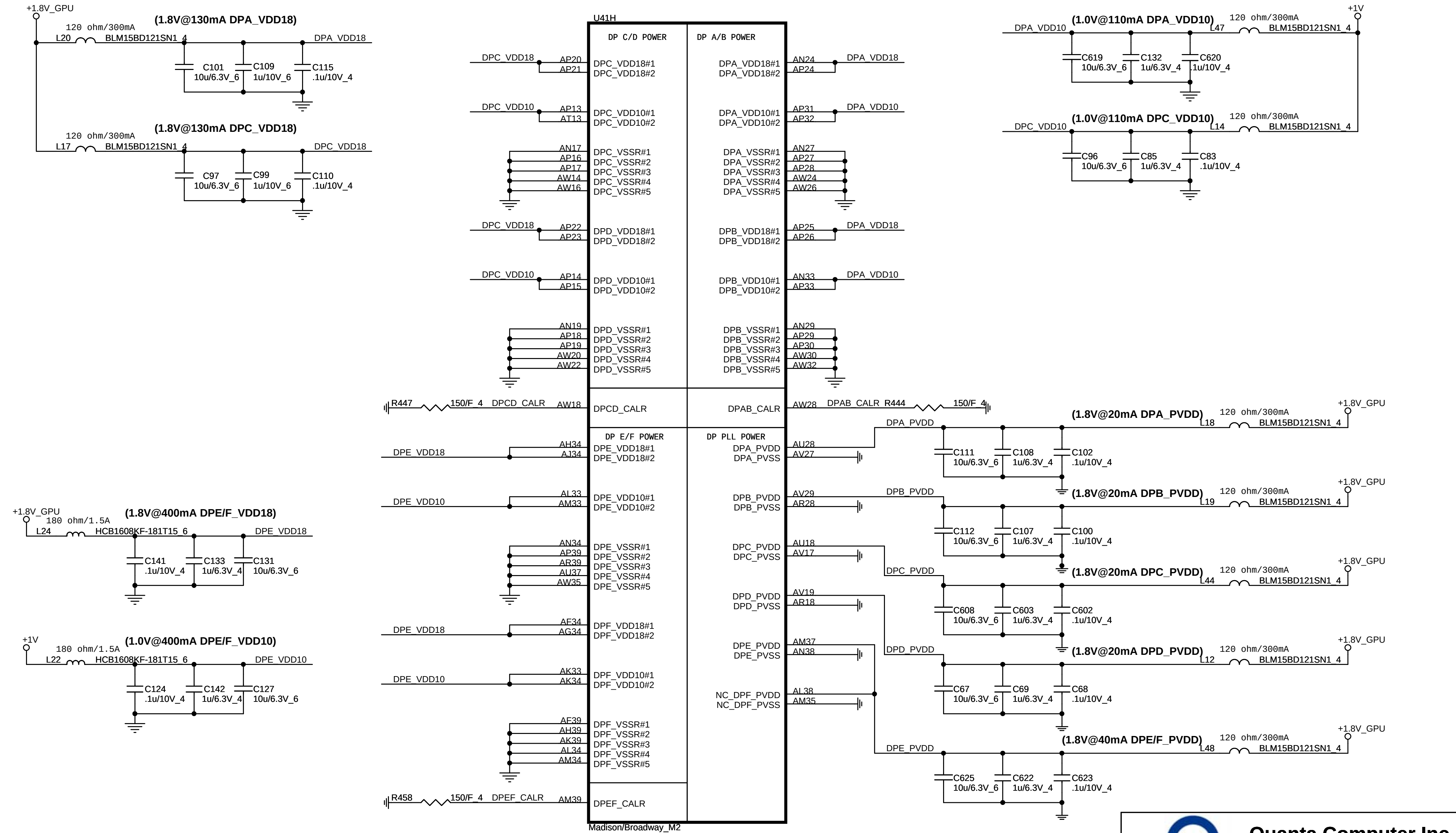
Quanta Computer Inc.

PROJECT : ZY9B

Document Number: Madison/Broadway (PWR/GND)

Rev: 1A

Date: Thursday, September 17, 2009



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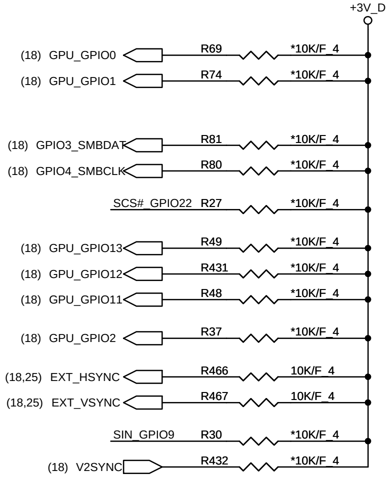
PROJECT : ZY9B

Size	Document Number	Rev
	Madison/Broadway (DP_PWR/GND)	1A
Date: Tuesday, September 15, 2009	Sheet 23 of 49	

PIN STRAPS



Memory Aperture size	
GPIO[13:11]	**Size**
000	**128MB**
001	256MB
010	64MB
011	32MB

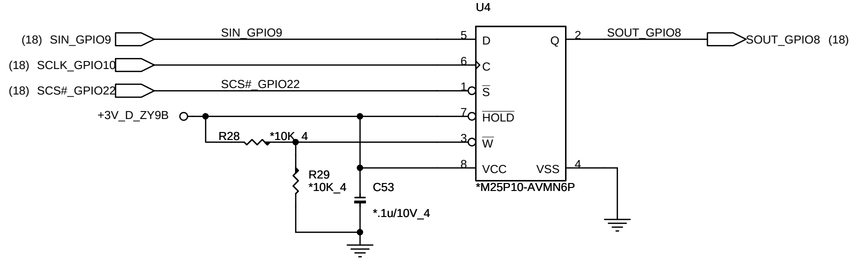
Audio Table		
EXT_HSYNC	**EXT_VSYNC**	**Discription**
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	**Both DP & HDMI**

CONFIGURATION STRAPS

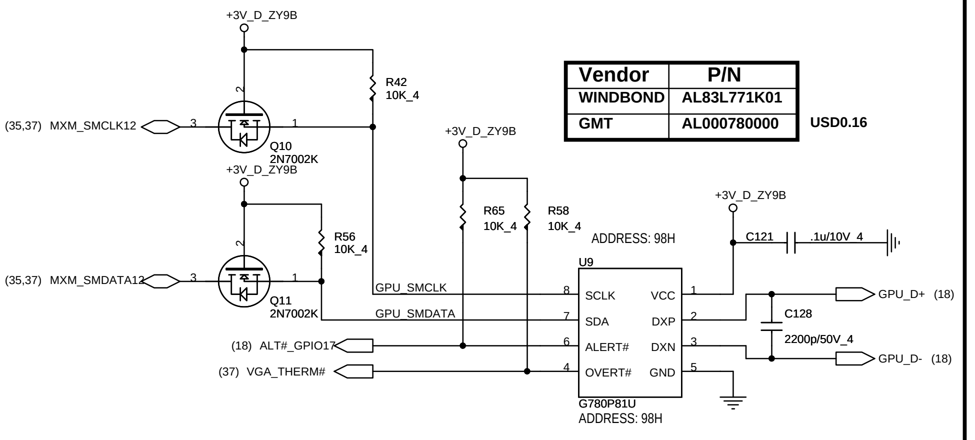
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM



Thermal Sensor



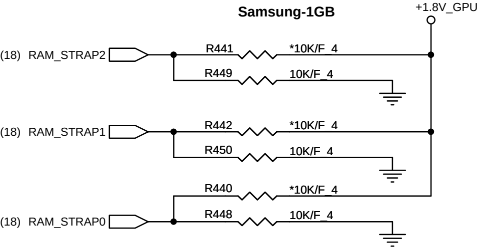
Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16

DDR3 VRAM SIZE Strap

DDR3 VRAM size						
Vendor	**Vendor P/N**	**STN B/S P/N**	**Size**	**RAM_STRAP2** DVPDATA_2	**RAM_STRAP1** DVPDATA_1	**RAM_STRAP0** DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	**512MB**	**1**	**1**	**0**
			1GB	**1**	**0**	**0**
			2GB			
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	**512MB**	**0**	**1**	**0**
			1GB	**0**	**0**	**0**
	K4W2G1646B-HC12	AKD5MGGT500	**2GB**	**0**	**0**	**1**

Samsung-1GB



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

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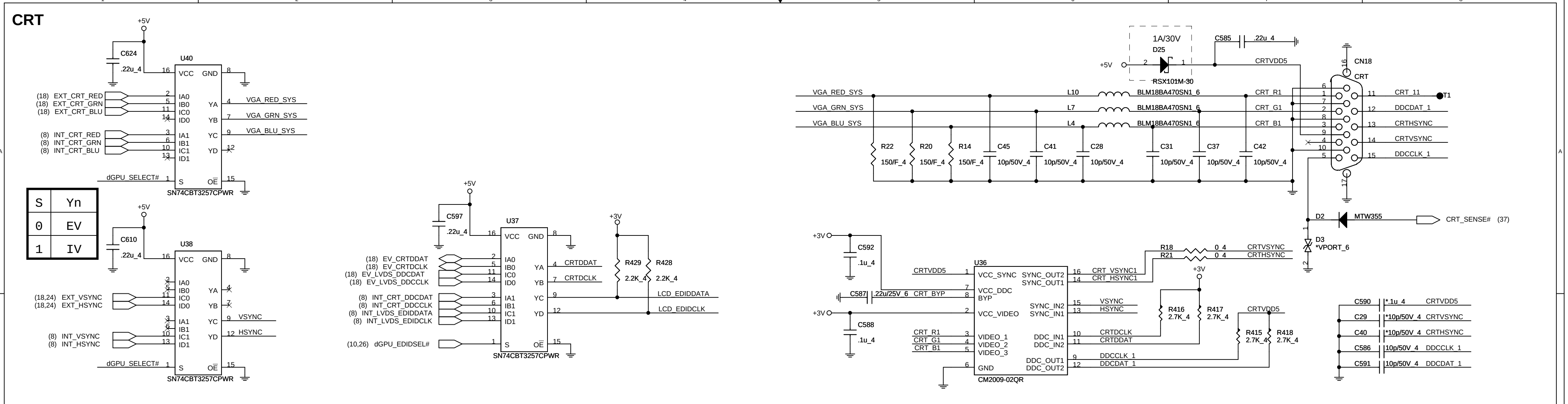
PROJECT : ZY9B

Size	Document Number	Rev
	Strip/Thermal	1A

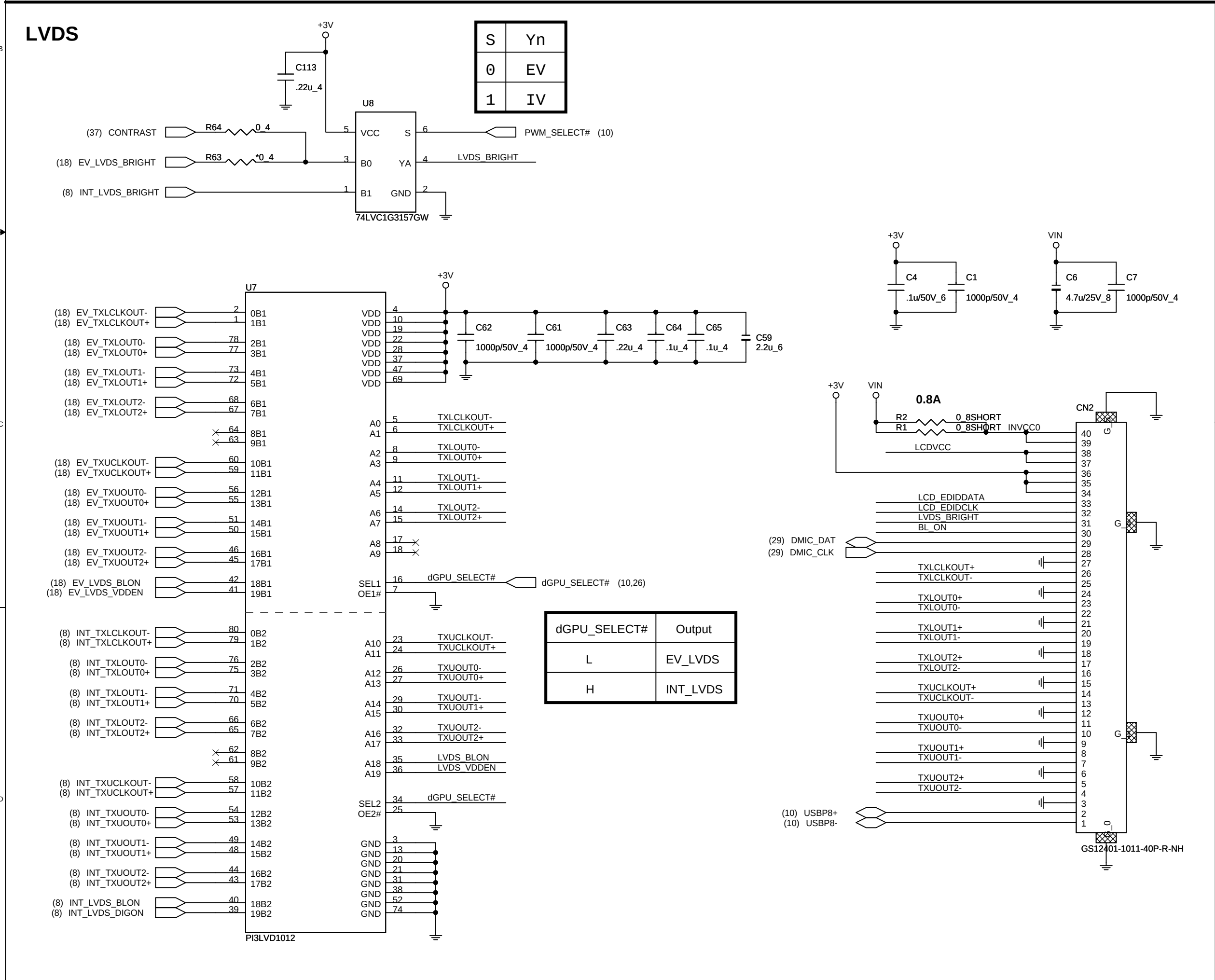
Date: Thursday, September 17, 2009 Sheet 24 of 49

CRT



S	Yn
0	EV
1	IV

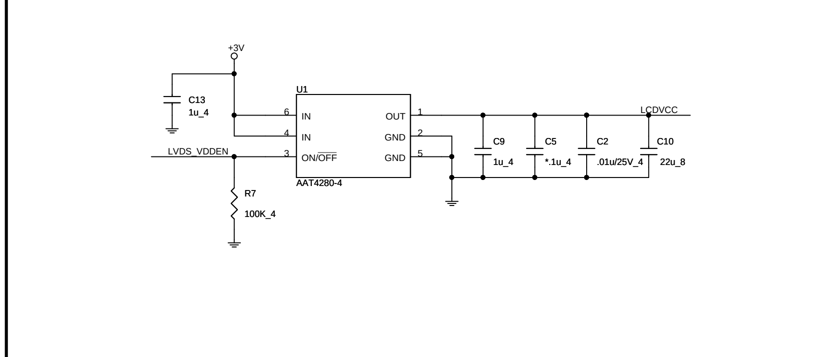
LVDS



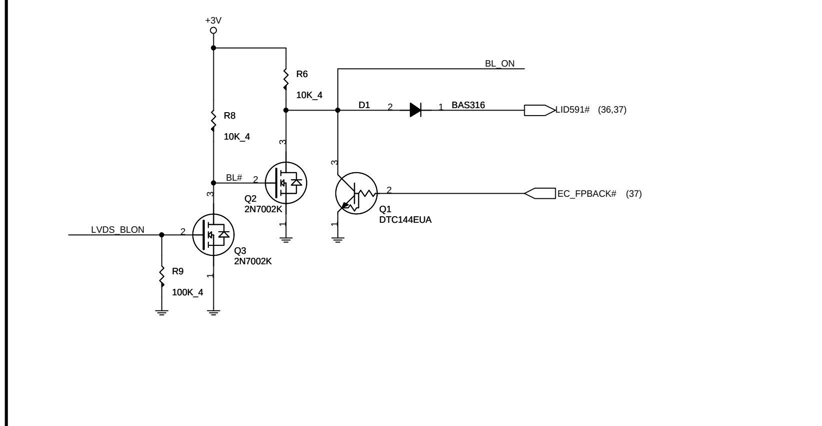
S	Yn
0	EV
1	IV

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

LCD Power



Backlight Control



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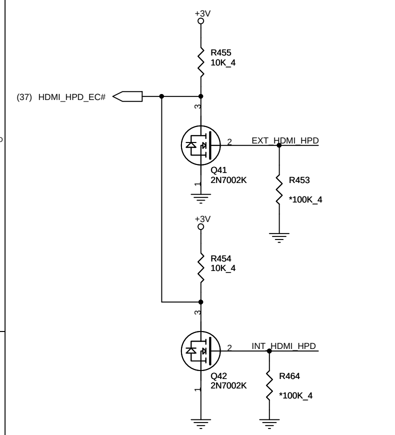
PROJECT : ZY9B

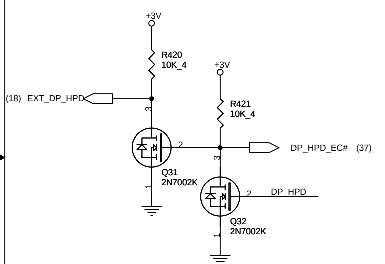
Size	Document Number	Rev
	CRT/LVDS/LID	1A

Date: Thursday, September 17, 2009 Sheet 25 of 49

HDMI Hot-PLUG to EC and GPU



DP Hot-PLUG to EC and GPU



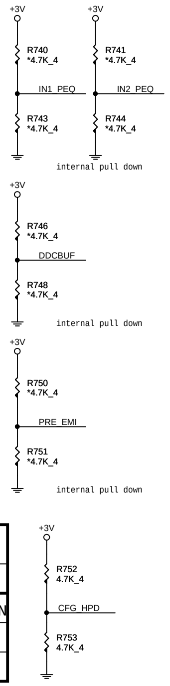
HDMI

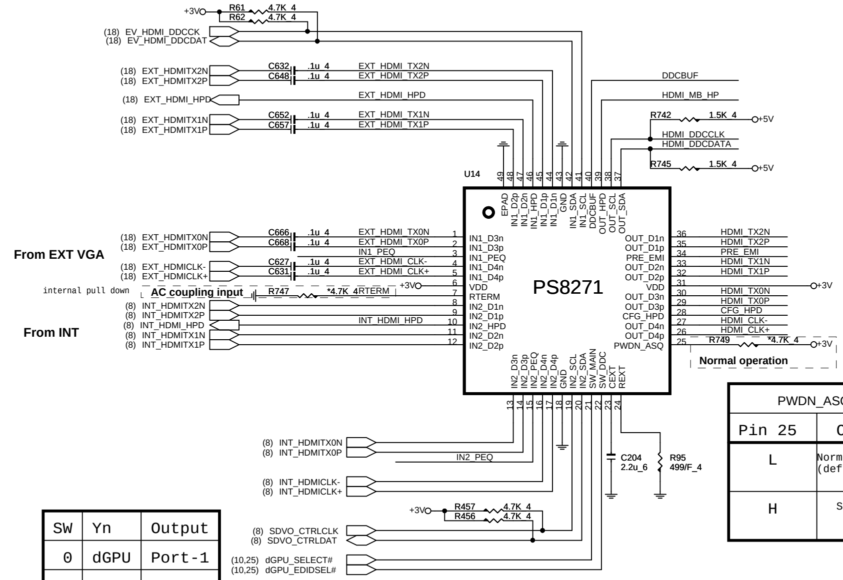
Input EQ setting	
INn_PEQ	Output
L	Middle EQ
H	High EQ
M	Low EQ

DDC Buffer setting	
DDC_BUF	Output
L	Passive DDC
H	Active Set-1
M	Active Set-2

Pre-emphasis and EMI setting	
PRE_EMI	Output
L	No_PRE&EMI
H	PRE enable
M	EMI control

Hot-plug detect	
CFG_HPD	Output
L	Follow SW_MAIN
H	Follow SW_DDC
M	SW or DDC

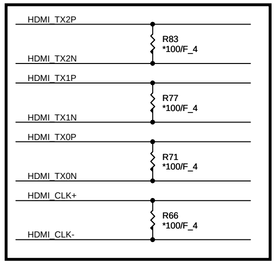




SW	Yn	Output
0	dGPU	Port-1
1	UMA	Port-2

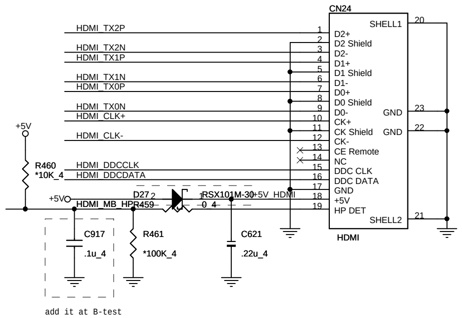
PWDN_ASQ setting	
Pin 25	Output
L	Normal operation (defult)
H	Shut down

EMI reserve for HDMI

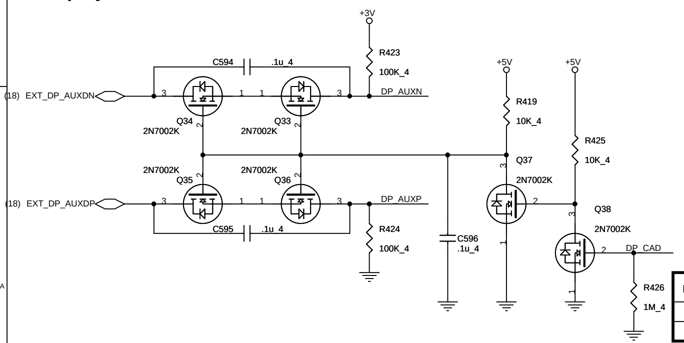


Close CN24

HDMI connector



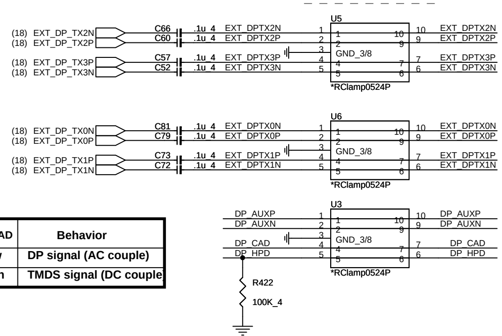
DisplayPort



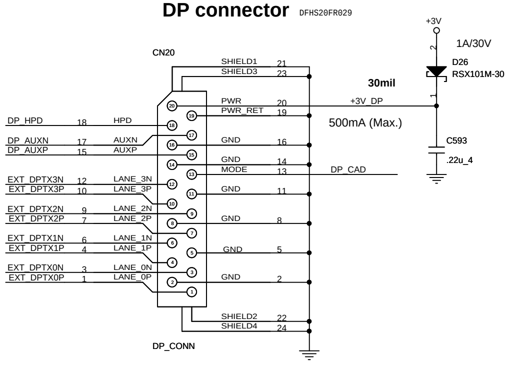
DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple

ESD Protect

close to DP connector



DP connector DFHS20FR029



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PROJECT : ZY9B

Size	Document Number	Rev
	HDMI/DP	1A

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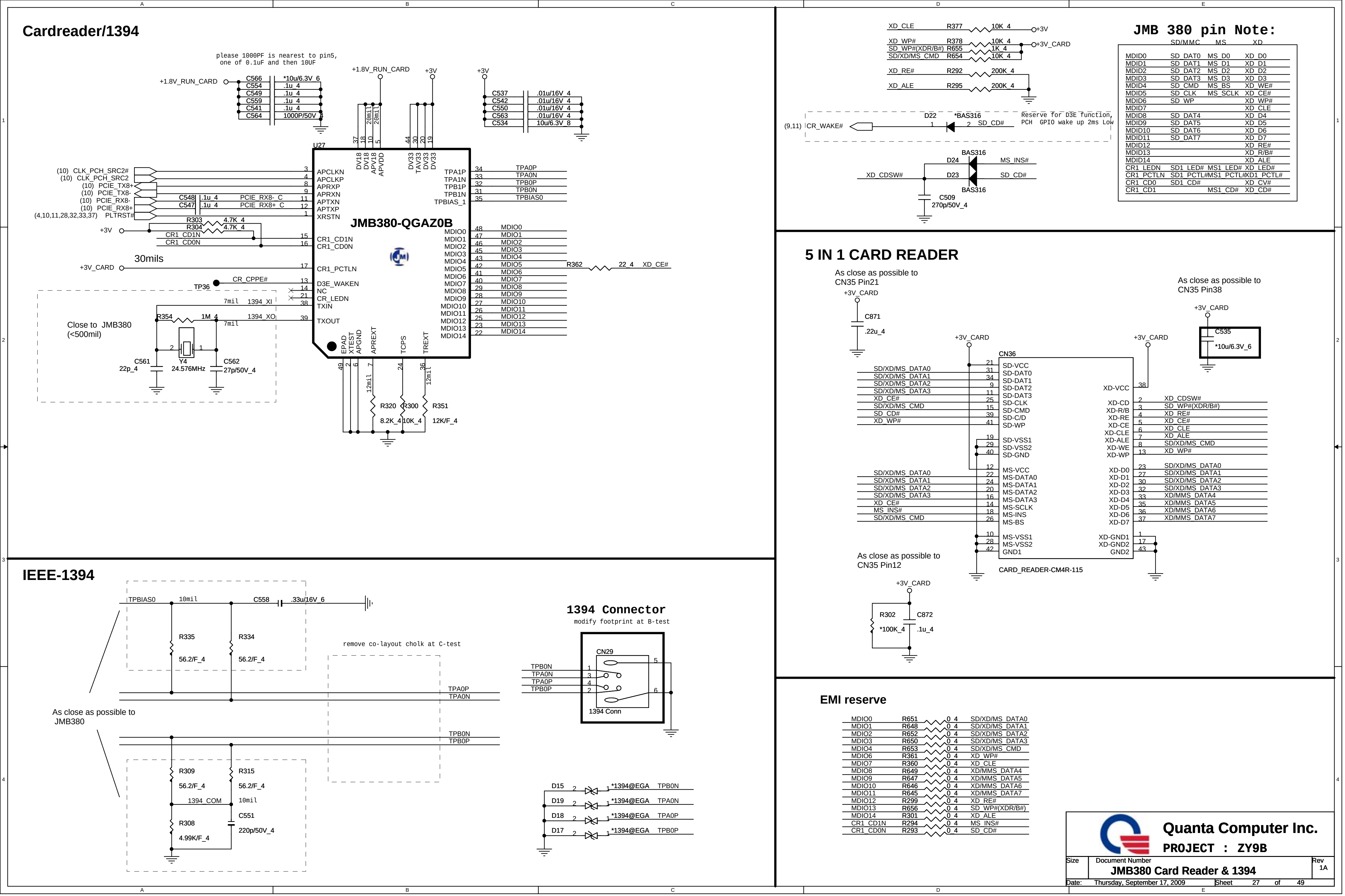

JMB 380 pin Note:

	SD/MMC	MS	XD
MDIO0	SD_DAT0	MS_D0	XD_D0
MDIO1	SD_DAT1	MS_D1	XD_D1
MDIO2	SD_DAT2	MS_D2	XD_D2
MDIO3	SD_DAT3	MS_D3	XD_D3
MDIO4	SD_CMD	MS_BS	XD_WE#
MDIO5	SD_CLK	MS_SCLK	XD_CE#
MDIO6	SD_WP		XD_WP#
MDIO7			XD_CLE
MDIO8	SD_DAT4		XD_D4
MDIO9	SD_DAT5		XD_D5
MDIO10	SD_DAT6		XD_D6
MDIO11	SD_DAT7		XD_D7
MDIO12			XD_RE#
MDIO13			XD_R/B#
MDIO14			XD_ALE
CR1_LEDN	SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0	SD1_CD#		XD_CV#
CR1_CD1		MS1_CD#	XD_CD#

EMI reserve

MDIO0	R651	0_4	SD/XD/MS_DATA0
MDIO1	R648	0_4	SD/XD/MS_DATA1
MDIO2	R652	0_4	SD/XD/MS_DATA2
MDIO3	R650	0_4	SD/XD/MS_DATA3
MDIO4	R653	0_4	SD/XD/MS_CMD
MDIO6	R361	0_4	XD_WP#
MDIO7	R360	0_4	XD_CLE
MDIO8	R649	0_4	XD/MMS_DATA4
MDIO9	R647	0_4	XD/MMS_DATA5
MDIO10	R646	0_4	XD/MMS_DATA6
MDIO11	R645	0_4	XD/MMS_DATA7
MDIO12	R299	0_4	XD_RE#
MDIO13	R656	0_4	SD_WP#(XDR/B#)
MDIO14	R301	0_4	XD_ALE
CR1_CD1N	R294	0_4	MS_INS#
CR1_CD0N	R293	0_4	SD_CD#

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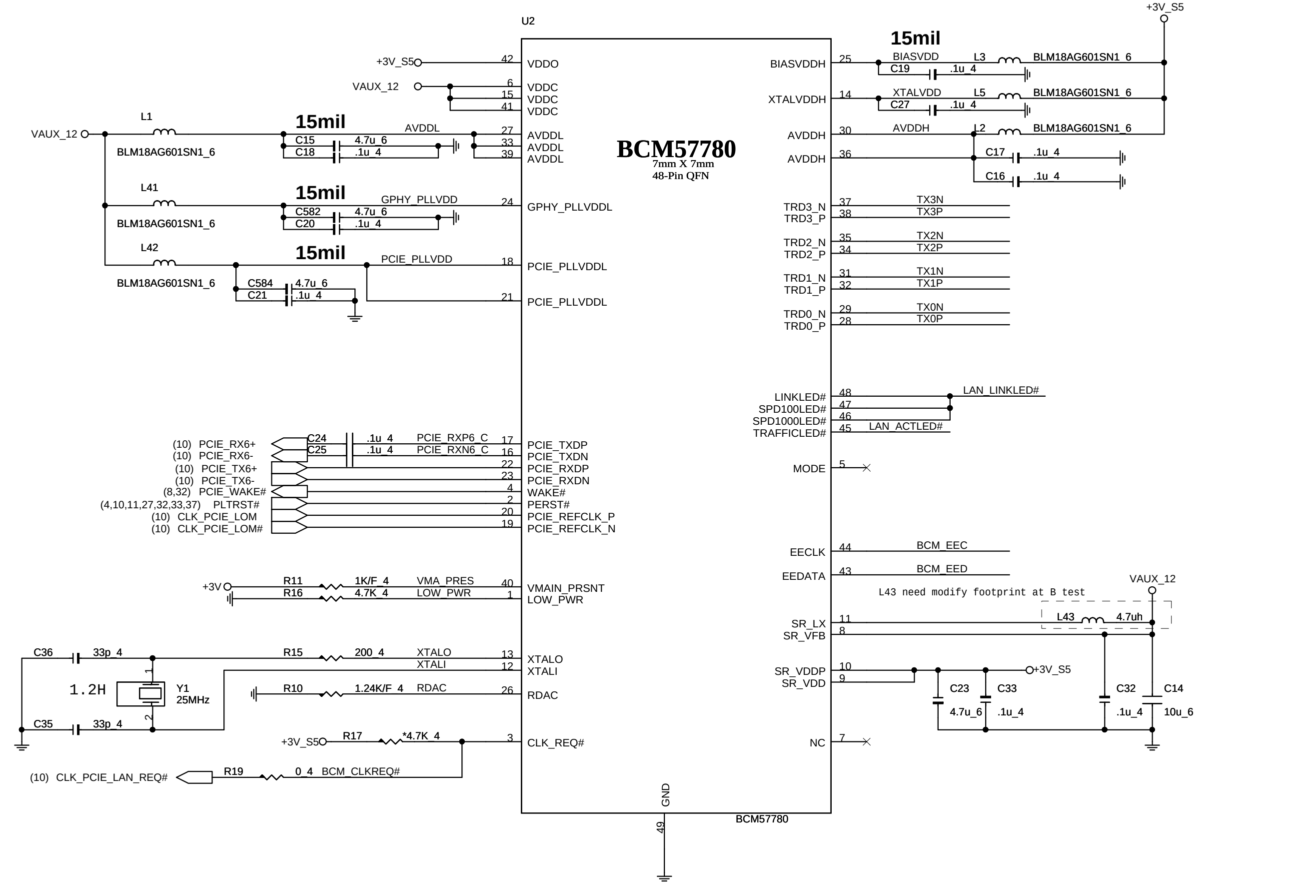
PROJECT : ZY9B

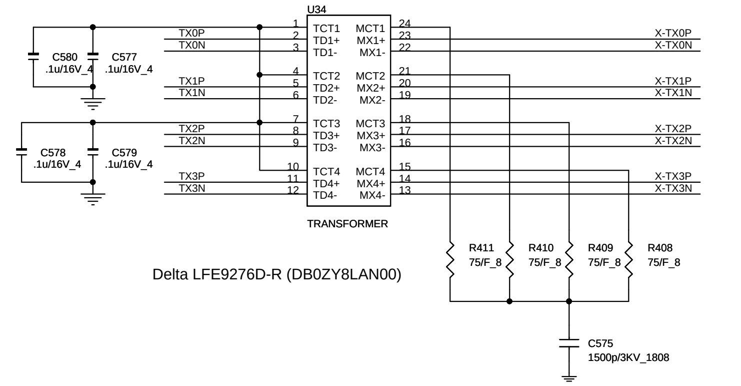
Size | Document Number: JMB380 Card Reader & 1394 | Rev 1A

Date: Thursday, September 17, 2009 | Sheet 27 of 49

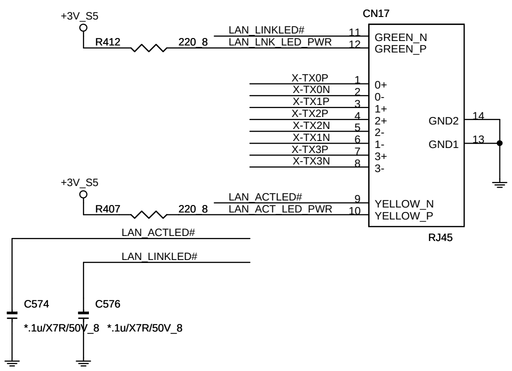
Giga-LAN BCM57780



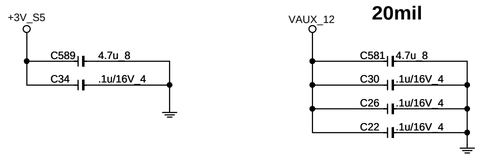
TRANSFORMER



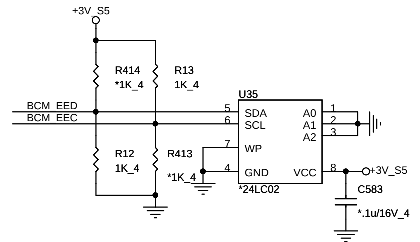
RJ45



LAN POWER



EEPROM



EEPROM Strapping

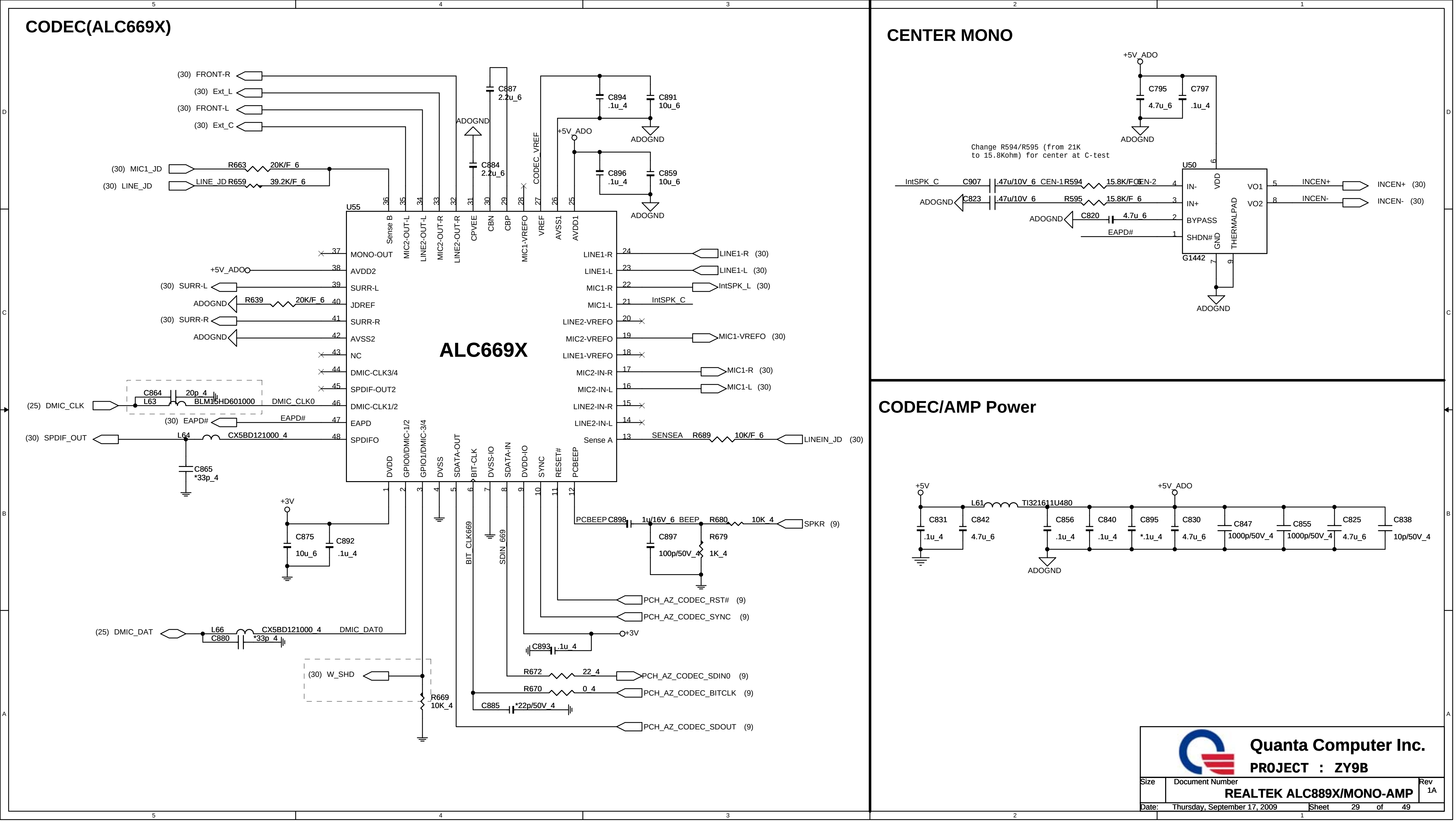
EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

Quanta Computer Inc.

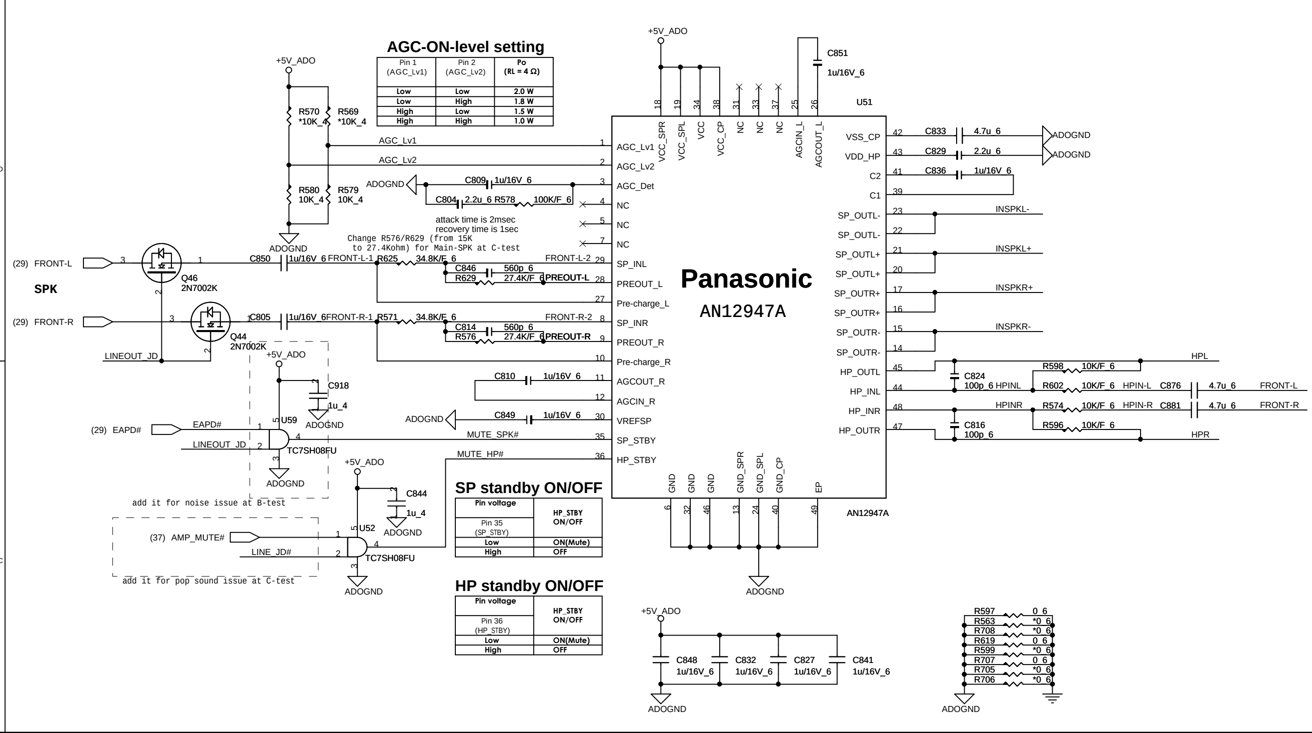
PROJECT : ZY9B

Size	Document Number	Rev
	LAN (BCM57780)	1A

Date: Thursday, September 17, 2009 Sheet 28 of 49


CODEC(ALC669X)
ALC669X
U55
(30) FRONT-R
(30) Ext_L
(30) FRONT-L
(30) Ext_C
(30) MIC1_JD
(30) LINE_JD
R663 20K/F_6
LINE_JD R659 39.2K/F_6
C887 2.2u_6
C884 2.2u_6
ADOGND
CODEC_VREF
+5V_ADO
C894 .1u_4
C891 10u_6
C896 .1u_4
C859 10u_6
Sense B
MIC2-OUT-L
LINE2-OUT-L
MIC2-OUT-R
LINE2-OUT-R
CPVEE
CBN
CBP
MIC1-VREFO
VREF
AVSS1
AVDD1
MONO-OUT
AVDD2
SURR-L
JDREF
SURR-R
AVSS2
NC
DMIC-CLK3/4
SPDIF-OUT2
DMIC-CLK1/2
EAPD
SPDIFO
(30) SURR-L
R639 20K/F_6
(30) SURR-R
C864 20p_4
L63 BLM15HD601000
DMIC_CLK0
(25) DMIC_CLK
(30) EAPD#
EAPD#
(30) SPDIF_OUT
L64 CX5BD121000_4
C865 *33p_4
LINE1-R
LINE1-L
MIC1-R
MIC1-L
LINE2-VREFO
MIC2-VREFO
LINE1-VREFO
MIC2-IN-R
MIC2-IN-L
LINE2-IN-R
LINE2-IN-L
Sense A
LINE1-R (30)
LINE1-L (30)
IntSPK_L (30)
IntSPK_C
MIC1-VREFO (30)
MIC1-R (30)
MIC1-L (30)
SENSEA R689 10K/F_6
LINEIN_JD (30)
DVDD
GPIO0/DMIC-1/2
GPIO1/DMIC-3/4
DVSS
SDATA-OUT
BIT-CLK
DVSS-IO
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP
+3V
C875 10u_6
C892 .1u_4
BIT_CLK669
SDIN_669
PCBEEP C898 1u/16V_6 BEEP R680 10K_4
SPKR (9)
C897 100p/50V_4
R679 1K_4
PCH_AZ_CODEC_RST# (9)
PCH_AZ_CODEC_SYNC (9)
C893 .1u_4
(25) DMIC_DAT
L66 CX5BD121000_4
C880 *33p_4
DMIC_DAT0
(30) W_SHD
R669 10K_4
R672 22_4
PCH_AZ_CODEC_SDIN0 (9)
R670 0_4
PCH_AZ_CODEC_BITCLK (9)
C885 *22p/50V_4
PCH_AZ_CODEC_SDOUT (9)
CENTER MONO
C795 4.7u_6
C797 .1u_4
Change R594/R595 (from 21K
to 15.8Kohm) for center at C-test
U50
G1442
IntSPK_C C907 .47u/10V_6 CEN-1 R594 15.8K/F_6 CEN-2
C823 .47u/10V_6 R595 15.8K/F_6
C820 4.7u_6
EAPD#
IN-
IN+
BYPASS
SHDN#
VDD
GND
THERMALPAD
VO1
VO2
INCEN+
INCEN-
INCEN+ (30)
INCEN- (30)
CODEC/AMP Power
+5V
L61 TI321611U480
C831 .1u_4
C842 4.7u_6
C856 .1u_4
C840 .1u_4
C895 *.1u_4
C830 4.7u_6
C847 1000p/50V_4
C855 1000p/50V_4
C825 4.7u_6
C838 10p/50V_4
Quanta Computer Inc.
PROJECT : ZY9B
Size
Document Number
REALTEK ALC889X/MONO-AMP
Rev
1A
Date: Thursday, September 17, 2009

SPEAKER/HP AMP.



AGC-ON-level setting

Pin 1 (AGC_Lv1)	Pin 2 (AGC_Lv2)	Po (RL = 4 Ω)
Low	Low	2.0 W
Low	High	1.8 W
High	Low	1.5 W
High	High	1.0 W

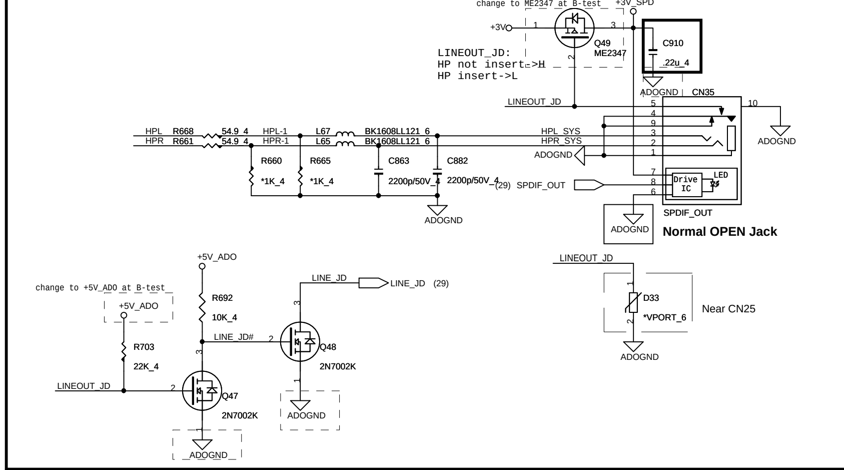
SP standby ON/OFF

Pin voltage Pin 35 (SP_STBY)	HP_STBY ON/OFF
Low	ON(Mute)
High	OFF

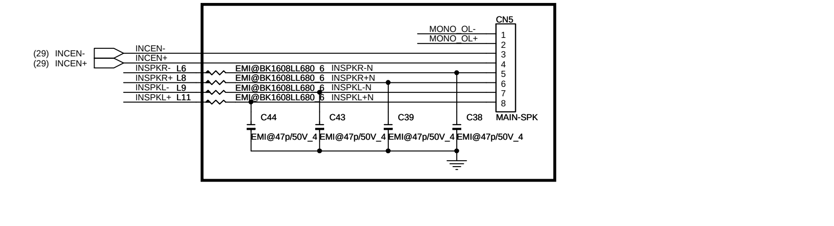
HP standby ON/OFF

Pin voltage Pin 36 (HP_STBY)	HP_STBY ON/OFF
Low	ON(Mute)
High	OFF

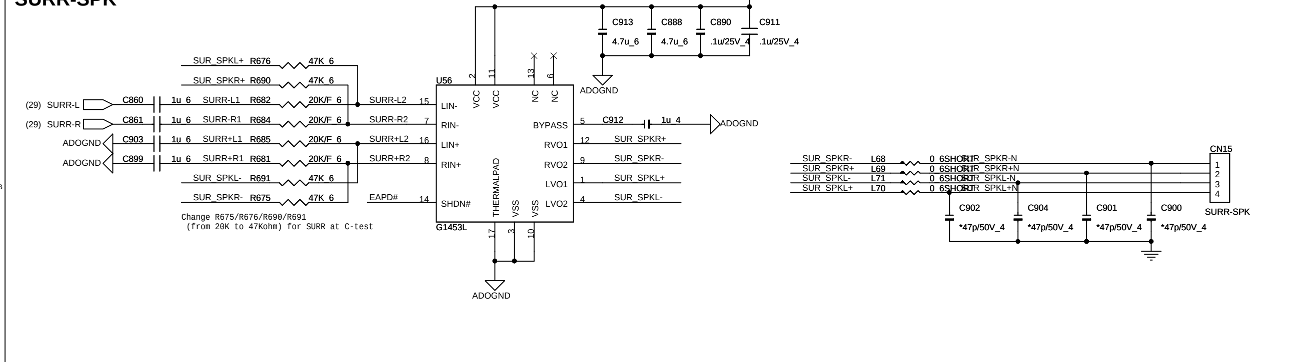
LINE-OUT/SPDIFO



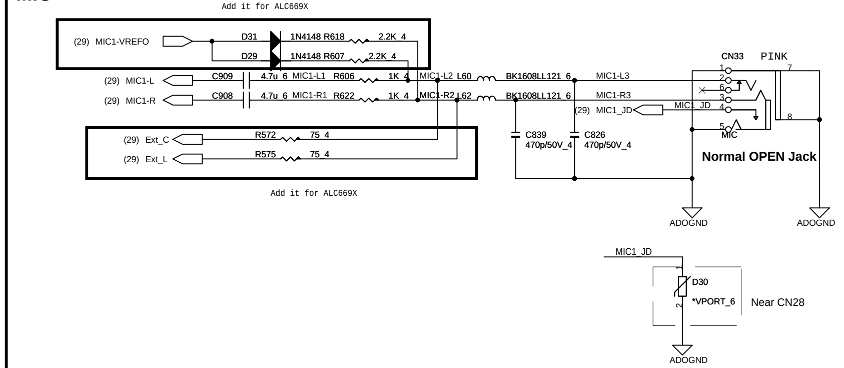
Main SPK/Center/Subwoofer EMI



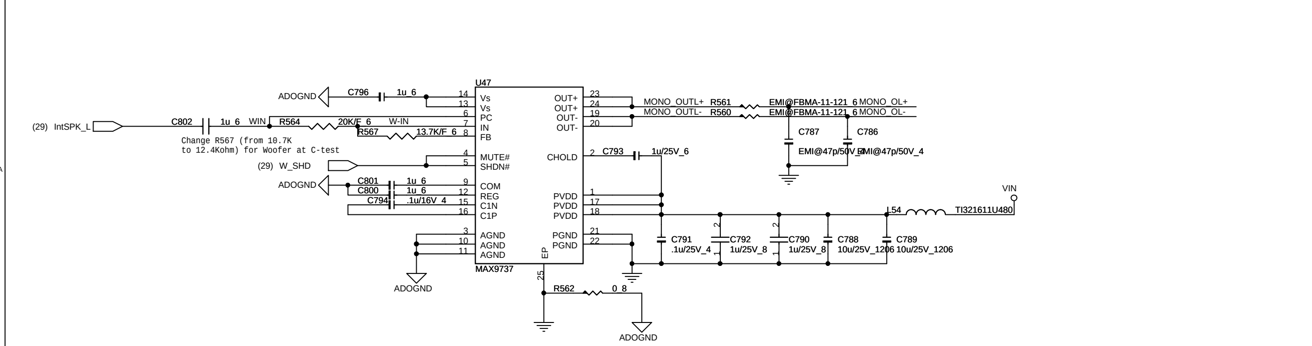
SURR-SPK



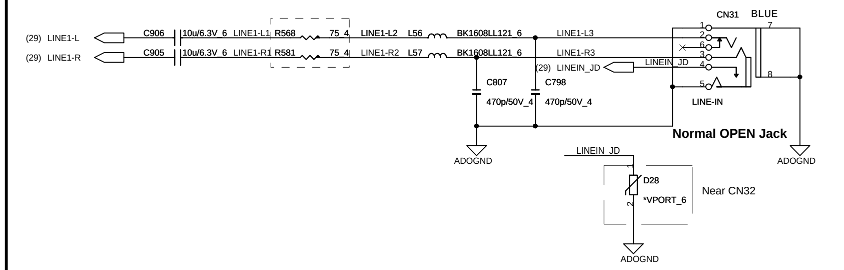
MIC



SUBWOOFER



LINE IN



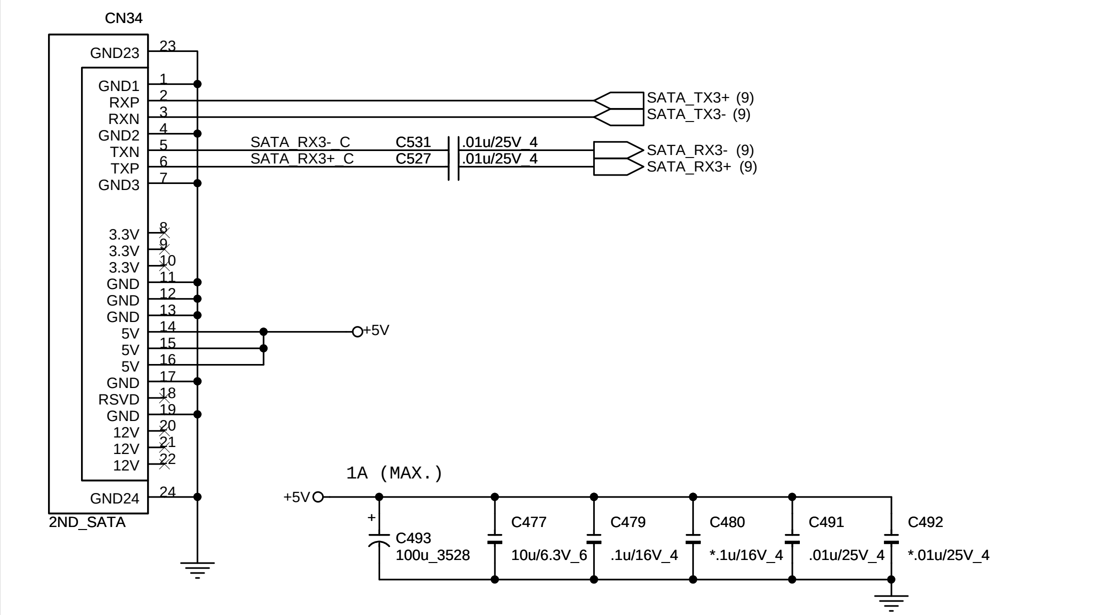
Quanta Computer Inc.

PROJECT : ZY9B

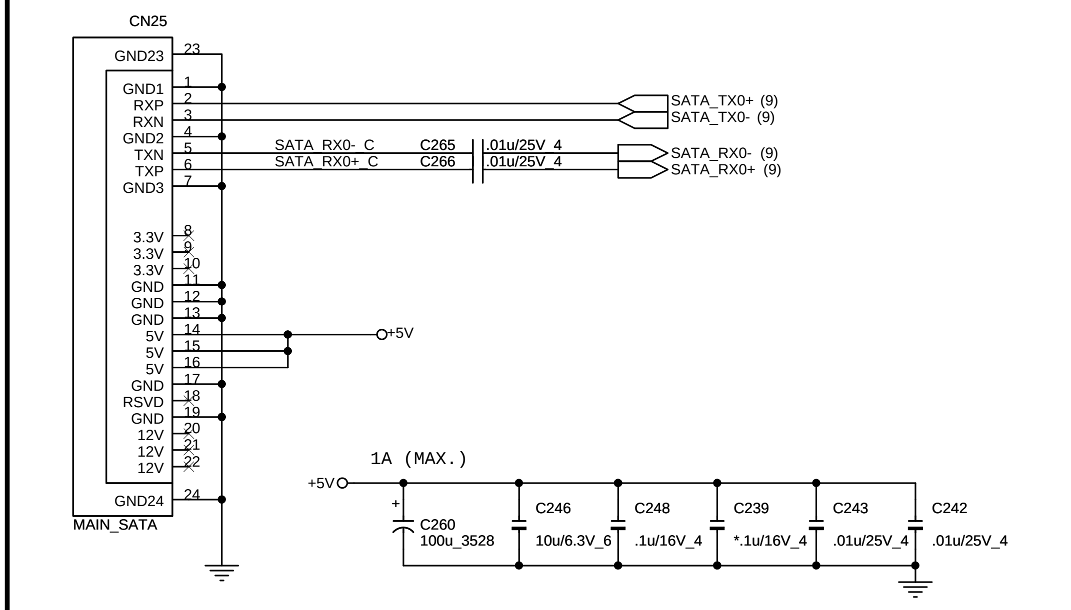
Size	Document Number	Rev
	AMP/AUDIO JACK/WOOFER	1A

Date: Thursday, September 17, 2009 Sheet 30 of 49

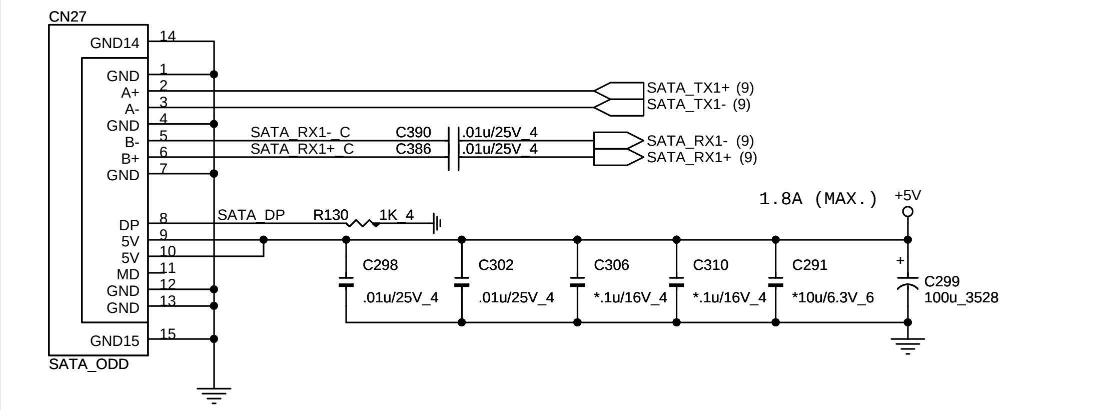
2nd SATA HDD (edge of board)



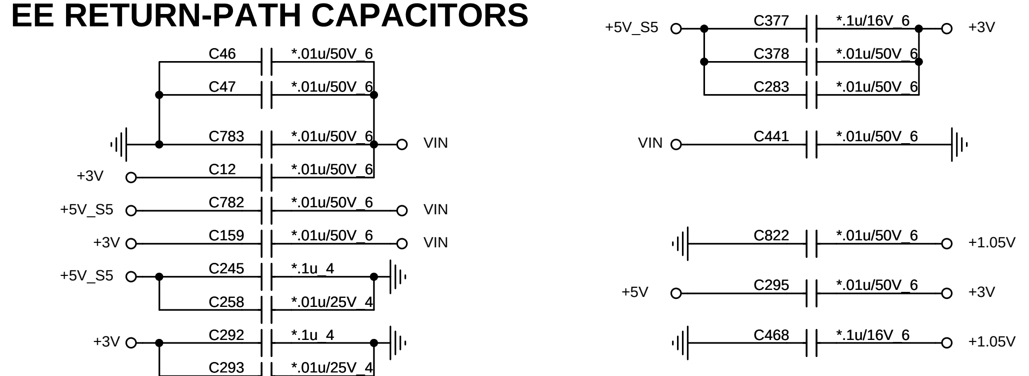
MAIN SATA HDD

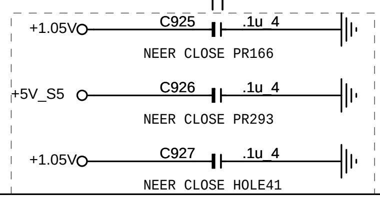


ODD (SATA)



EE RETURN-PATH CAPACITORS





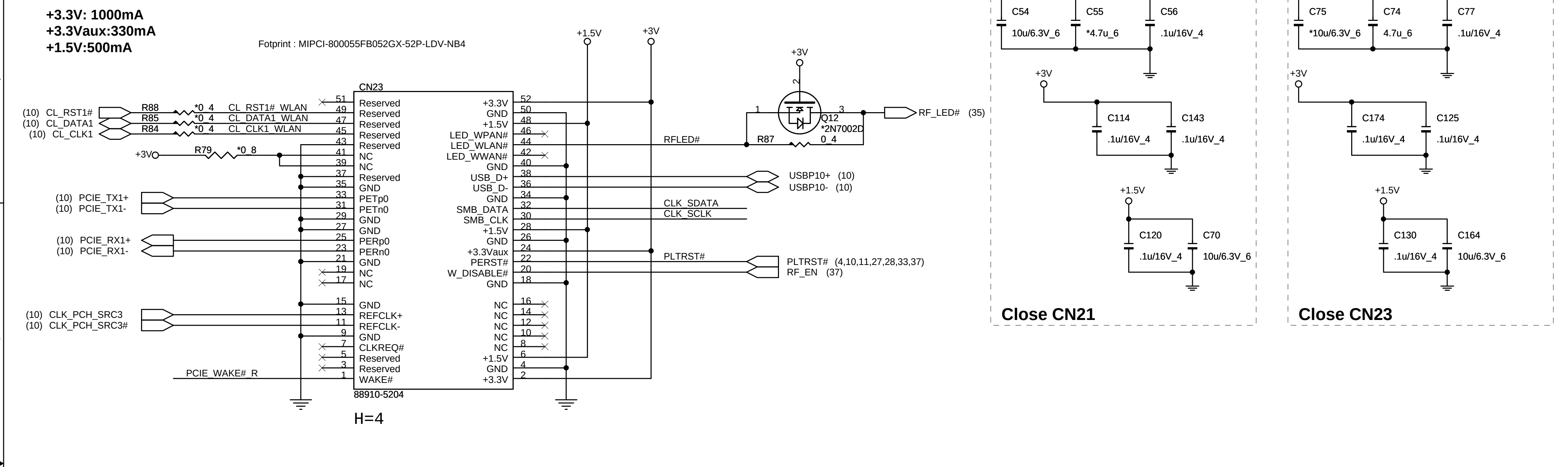
Quanta Computer Inc.

PROJECT : ZY9B

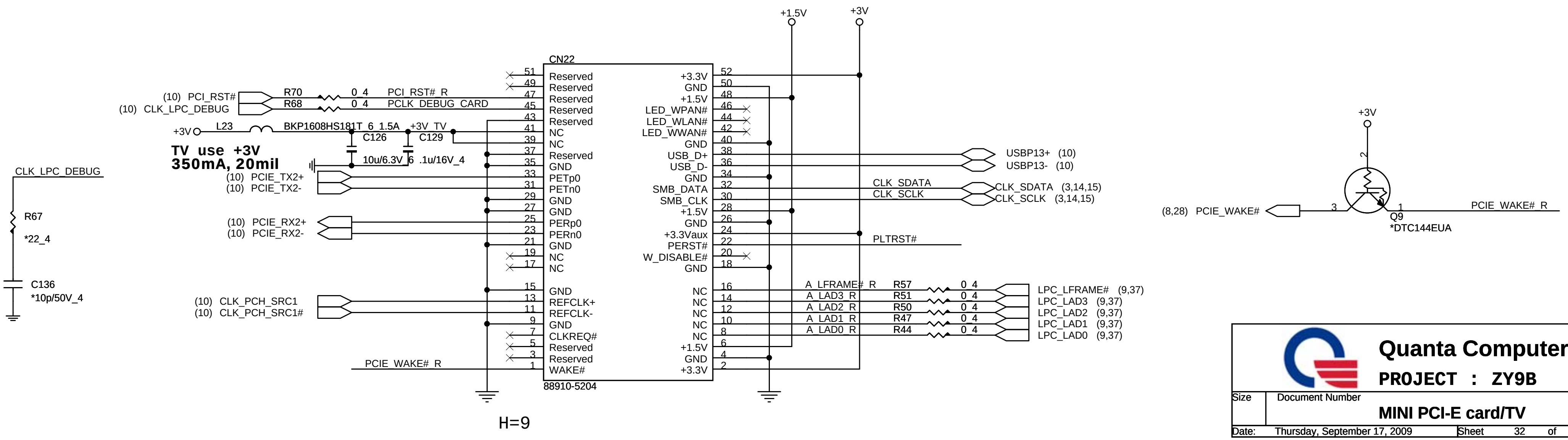
Size	Document Number	Rev
	SATA-HDD/ODD	1A

Date: Thursday, September 17, 2009 | Sheet 31 of 49

Wireless



TV and Debug



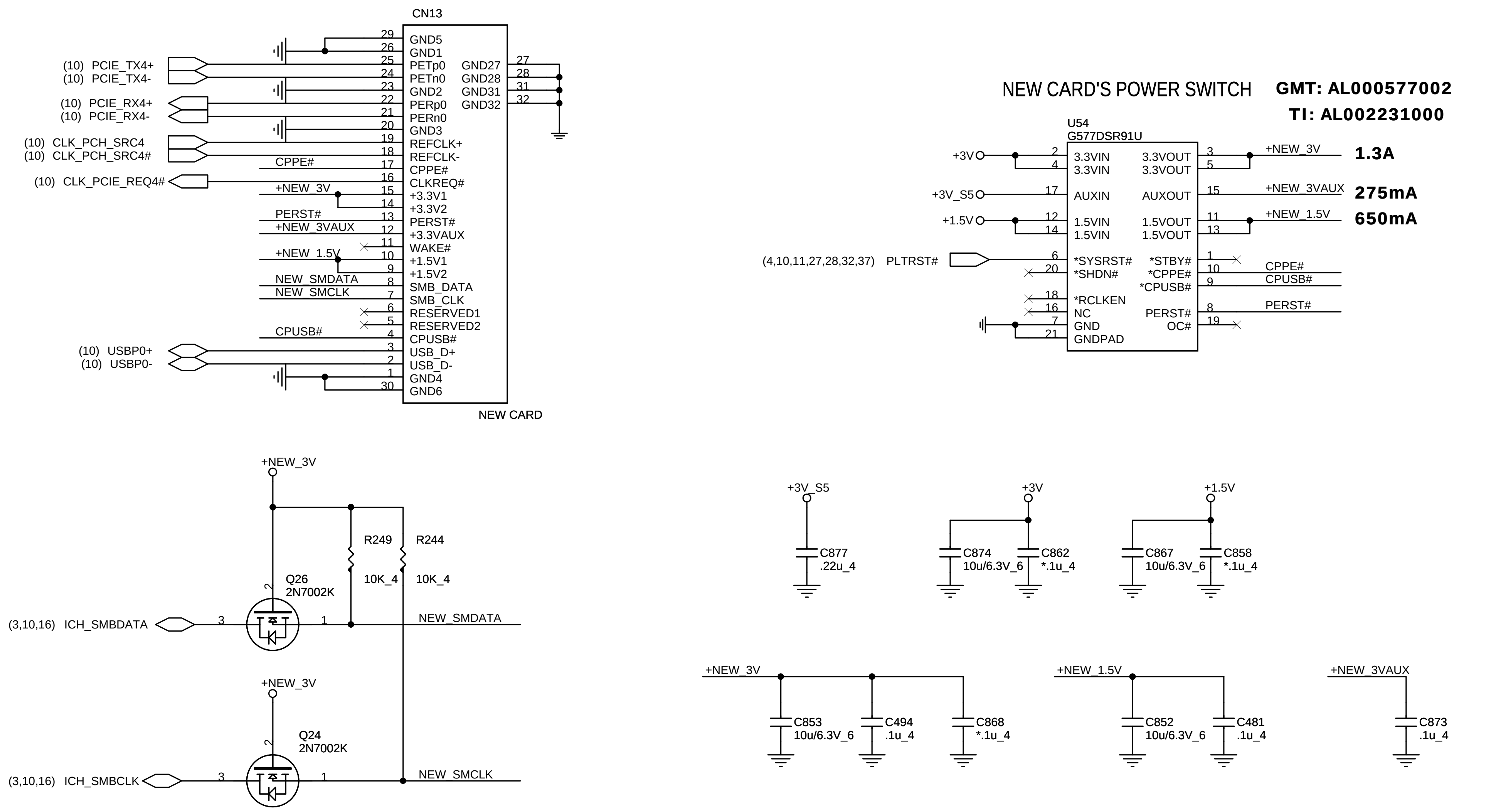
Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	MINI PCI-E card/TV	1A

Date: Thursday, September 17, 2009 Sheet 32 of 49

NEW CARD



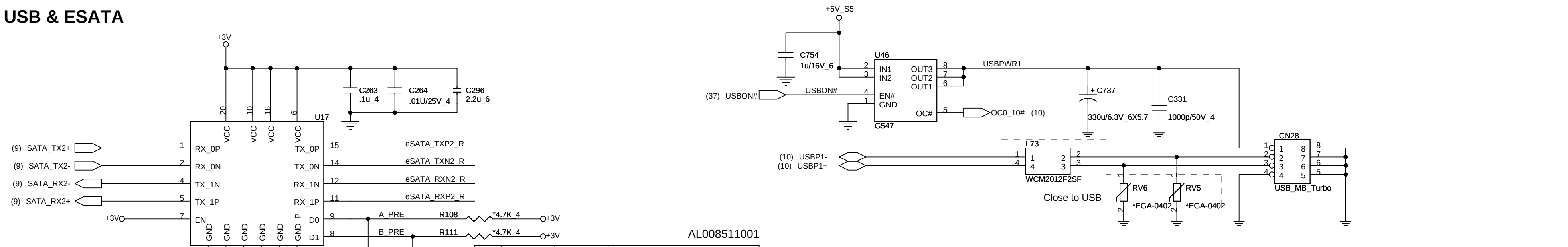
Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	NEW CARD	1A

Date: Thursday, September 17, 2009 Sheet 33 of 49

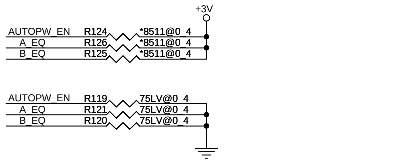
USB & ESATA

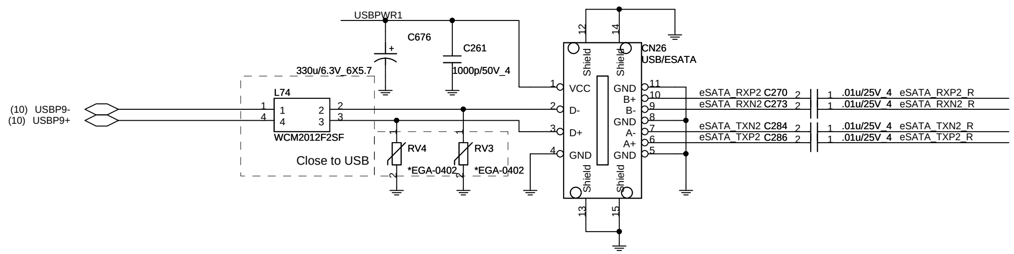


EN	A_PRE	B_PRE	dB
0	X	X	Power down mode
1	0	0	Pre-emphasis disable
1	1	1	Pre-emphasis enable

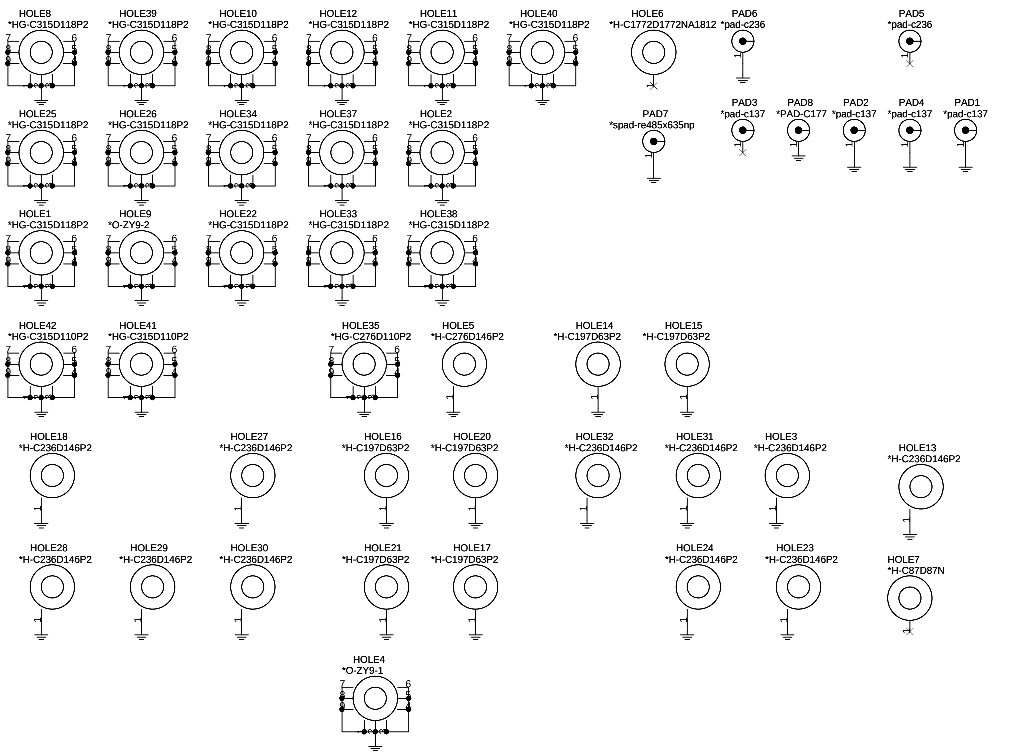
ALLVC412000

EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

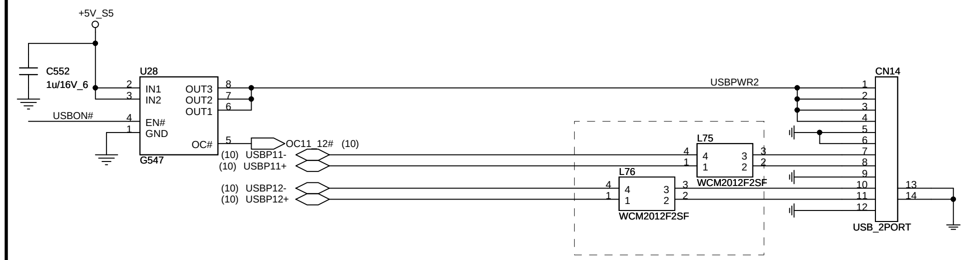




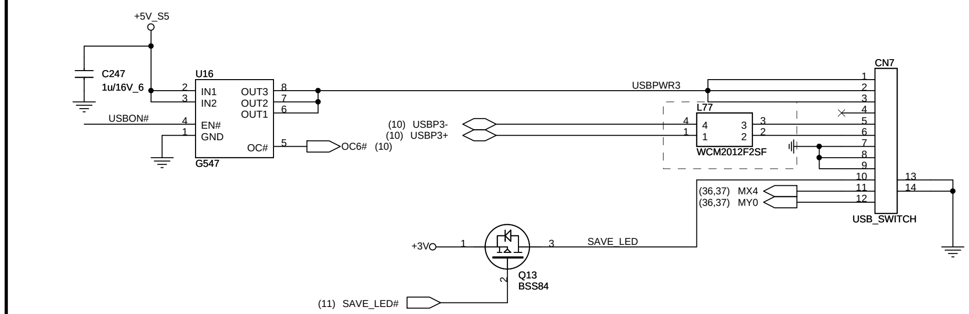
HOLES



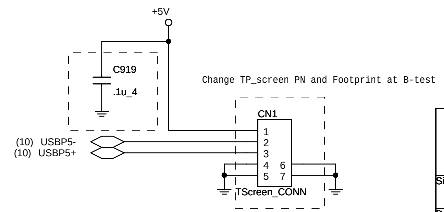
USB_2PORT/B



USB_SWITCH/B



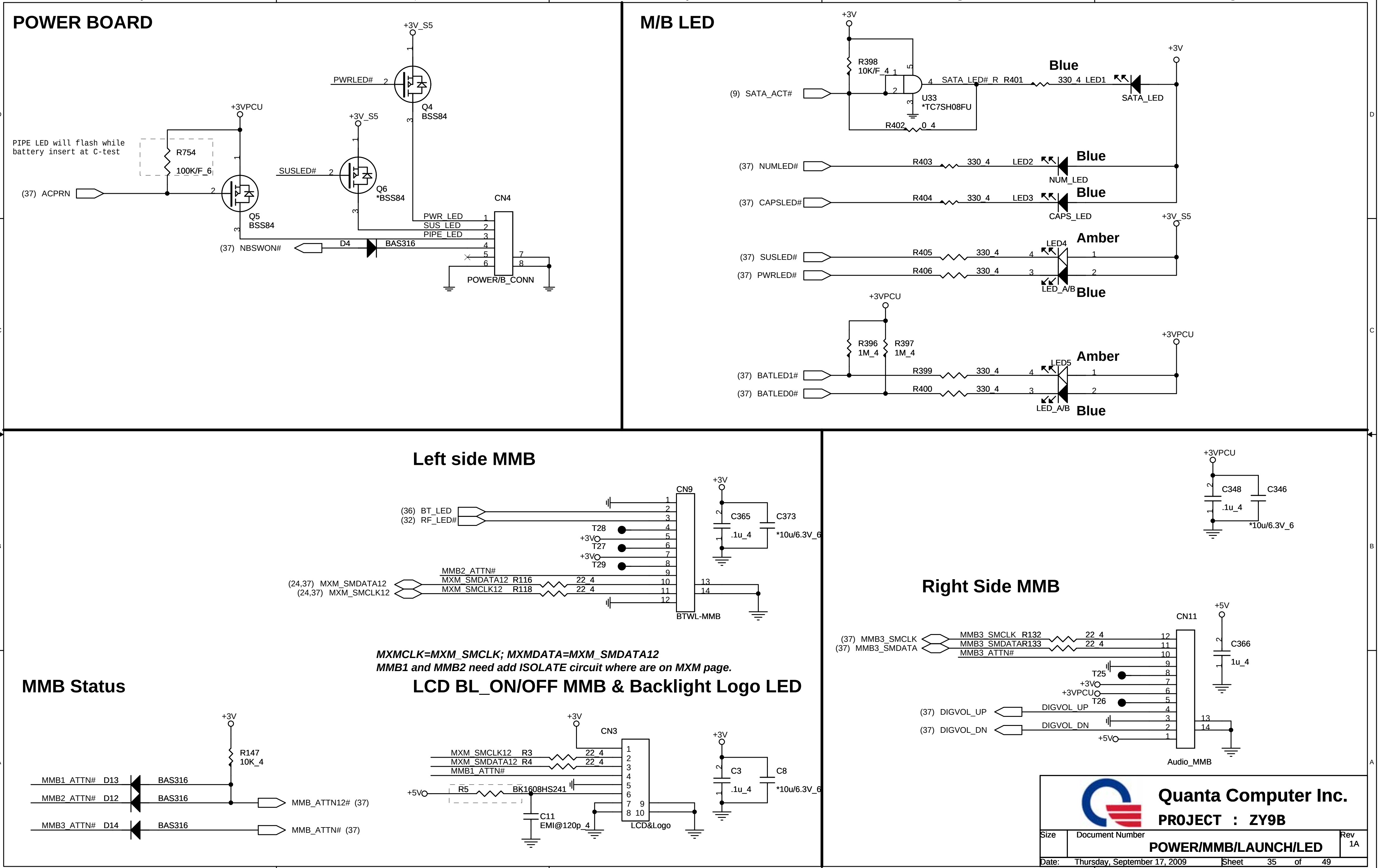
TP_Screen



Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	USB/eSATA/TP_Screen	1A
Date: Thursday, September 17, 2009	Sheet 34 of 49	



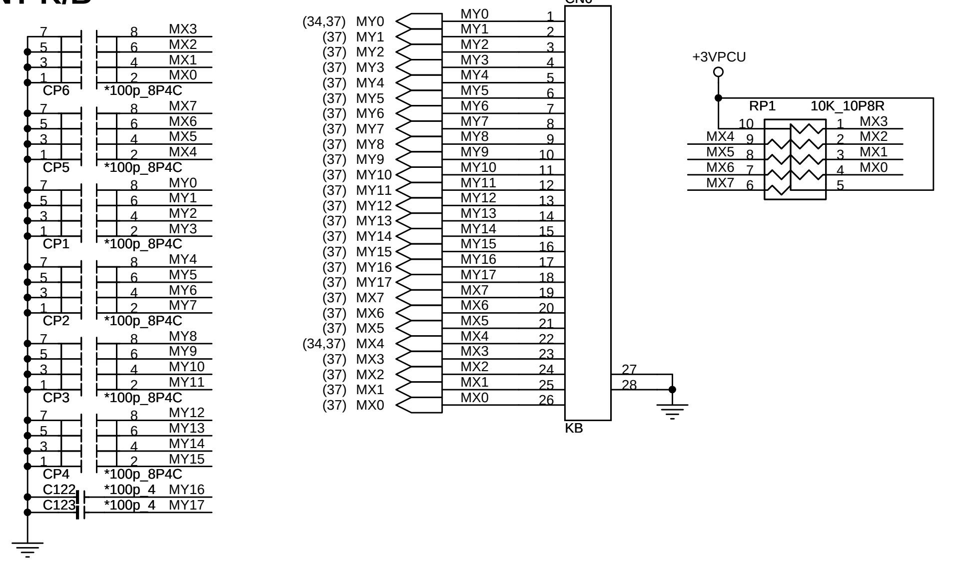
Quanta Computer Inc.

PROJECT : ZY9B

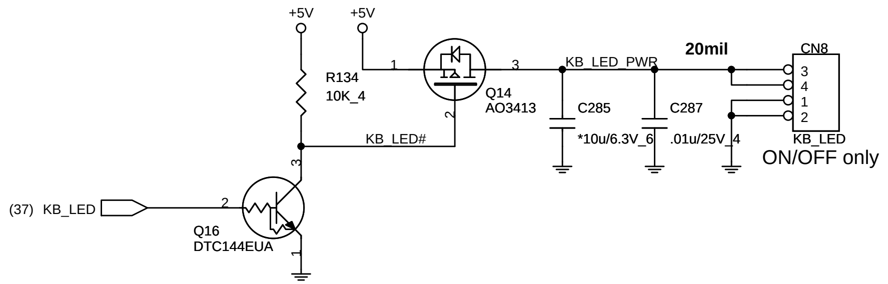
Size | Document Number: POWER/MMB/LAUNCH/LED | Rev 1A

Date: Thursday, September 17, 2009 | Sheet 35 of 49

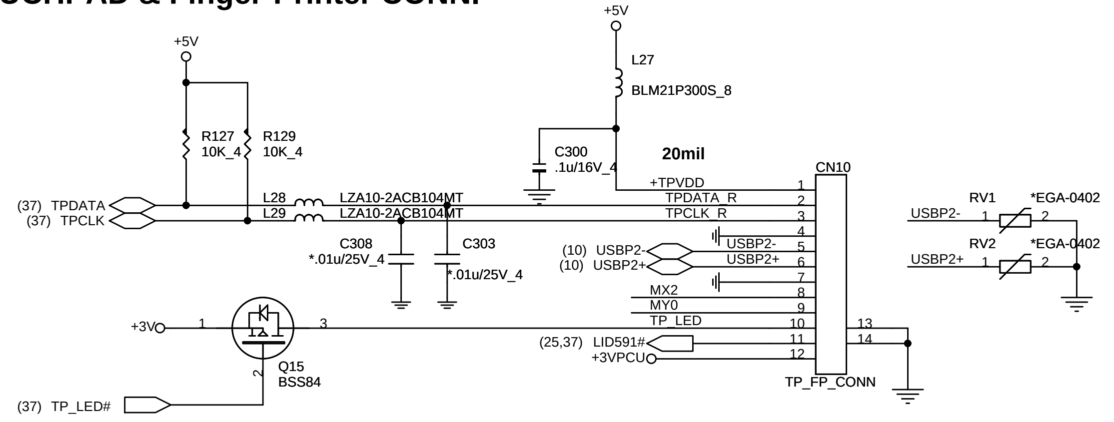
INT K/B



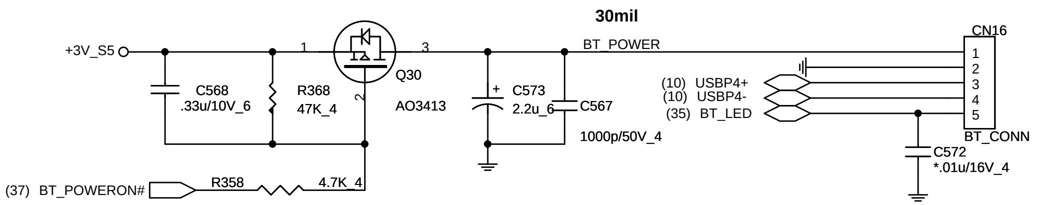
Keyboard LED control



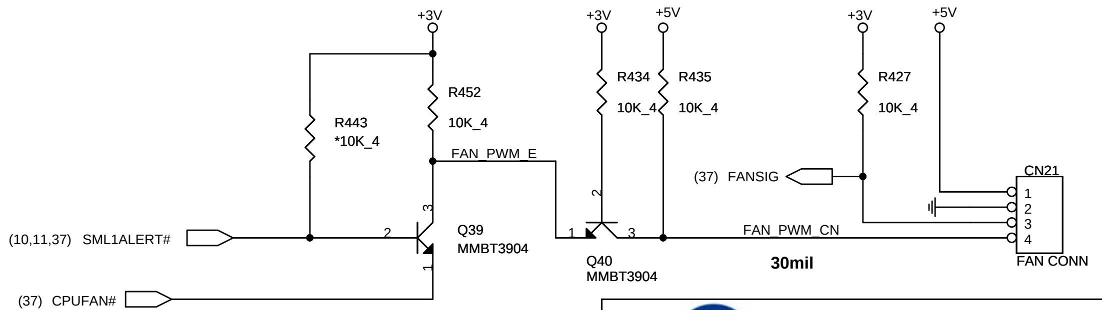
TOUCHPAD & Finger-Printer CONN.



BLUETOOTH CONNECTOR



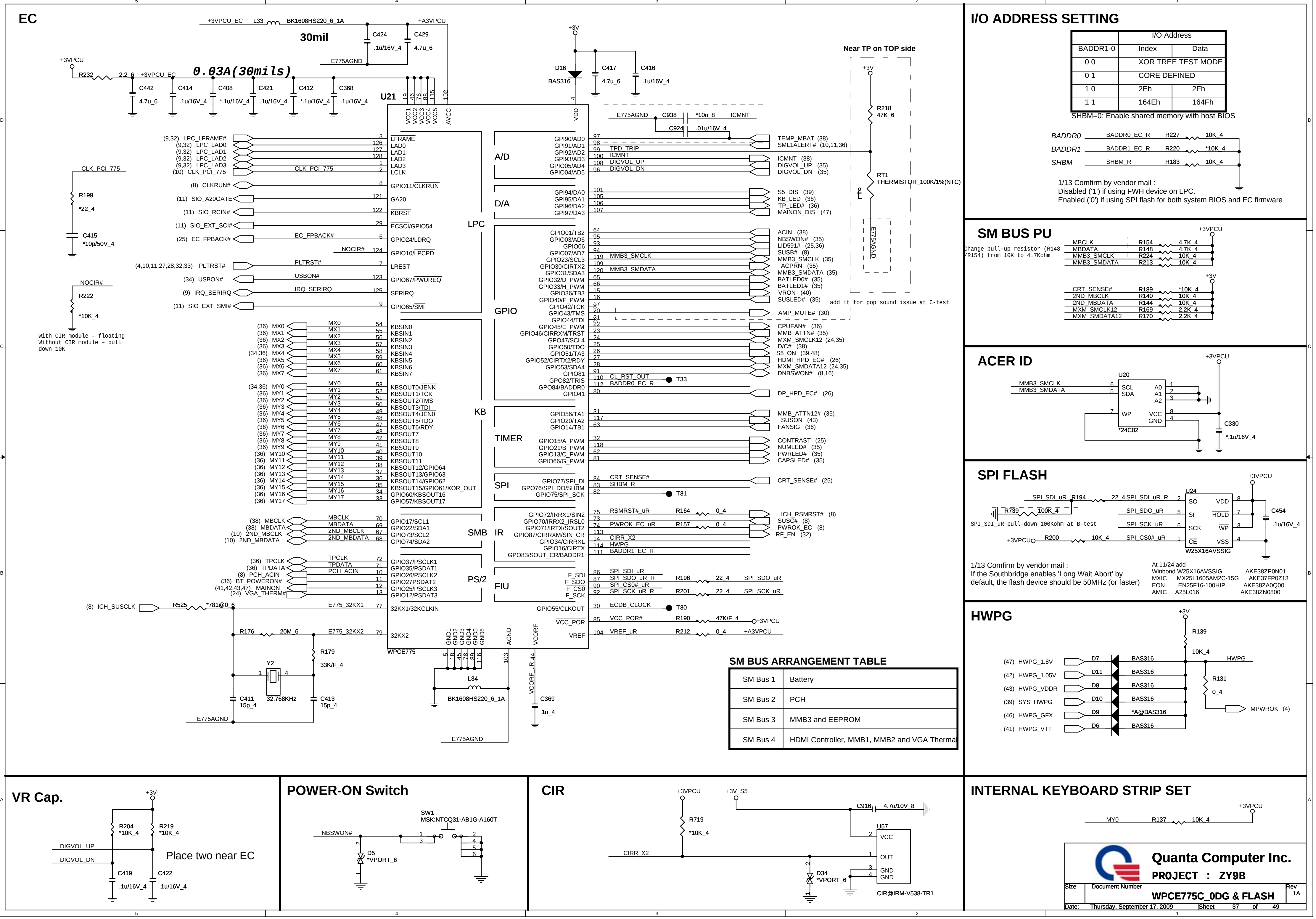
CPU FAN



Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	KB/FAN/TP+FP/BT	1A
Date: Tuesday, September 22, 2009	Sheet 36 of 49	



I/O ADDRESS SETTING

BADDR1-0	I/O Address Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

SM BUS ARRANGEMENT TABLE

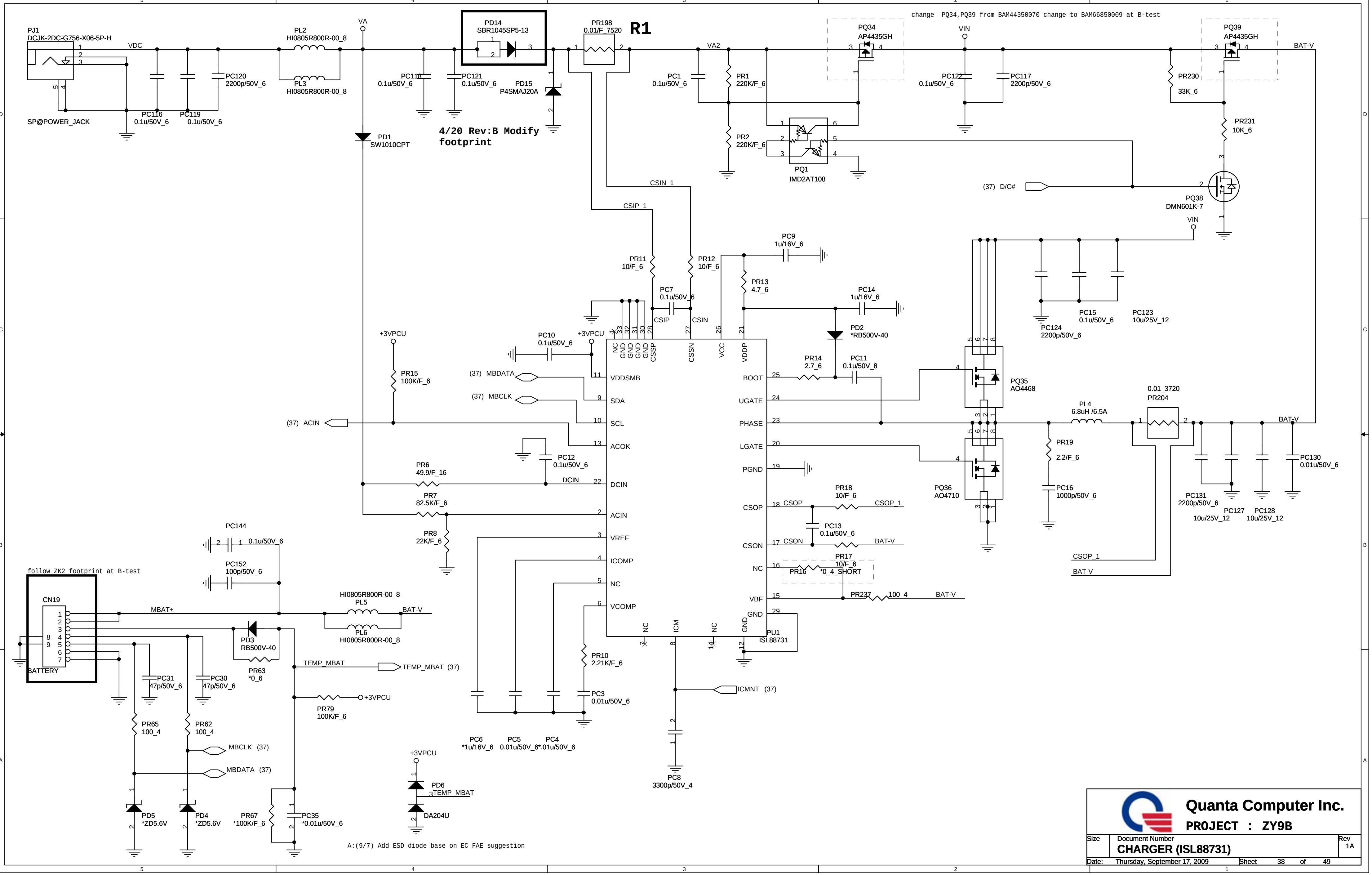
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Therma

Quanta Computer Inc.

PROJECT : ZY9B

Size | Document Number: WPCE775C_0DG & FLASH | Rev 1A

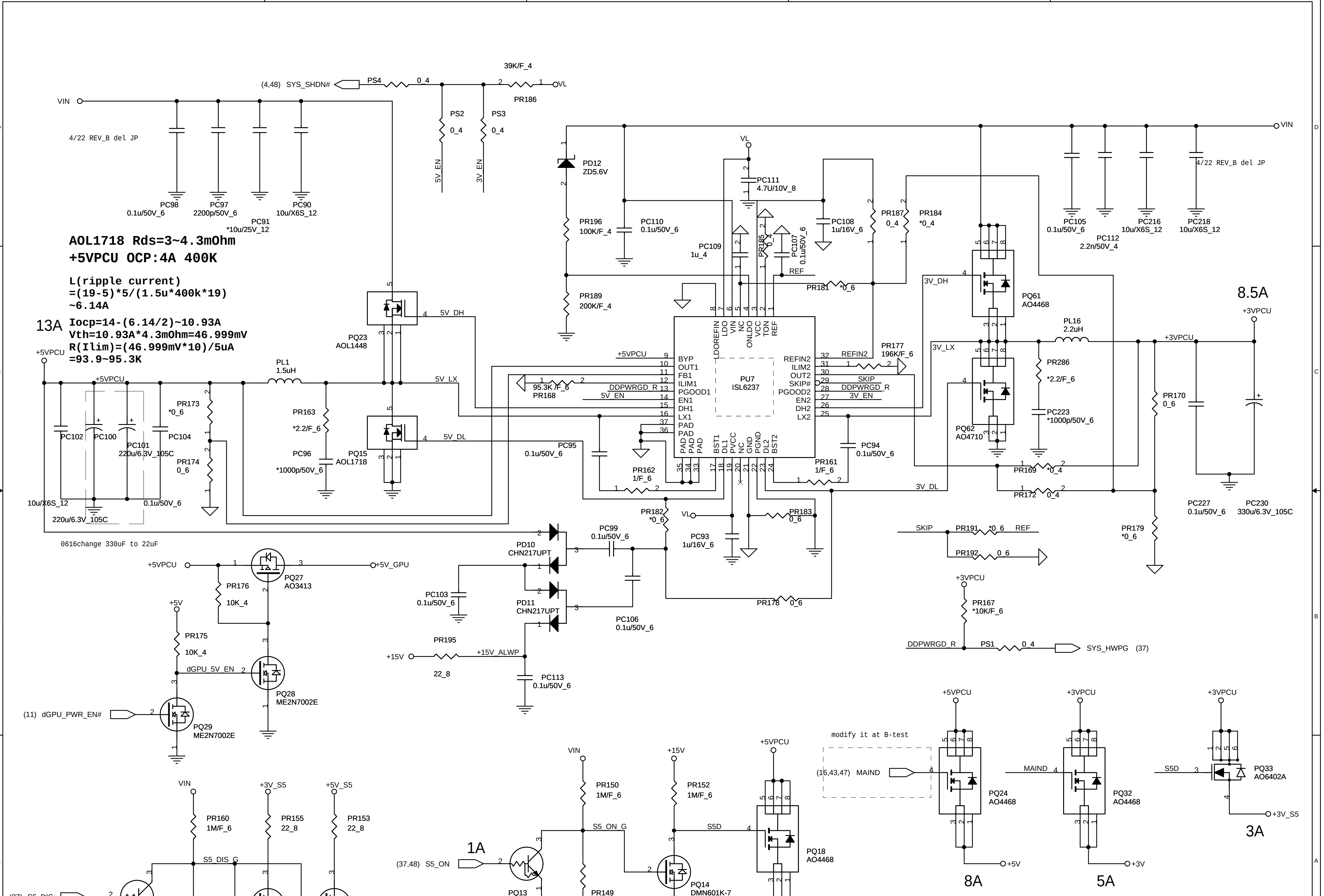
Date: Thursday, September 17, 2009 | Sheet 37 of 49



Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	CHARGER (ISL88731)	1A
Date: Thursday, September 17, 2009	Sheet 38 of 49	



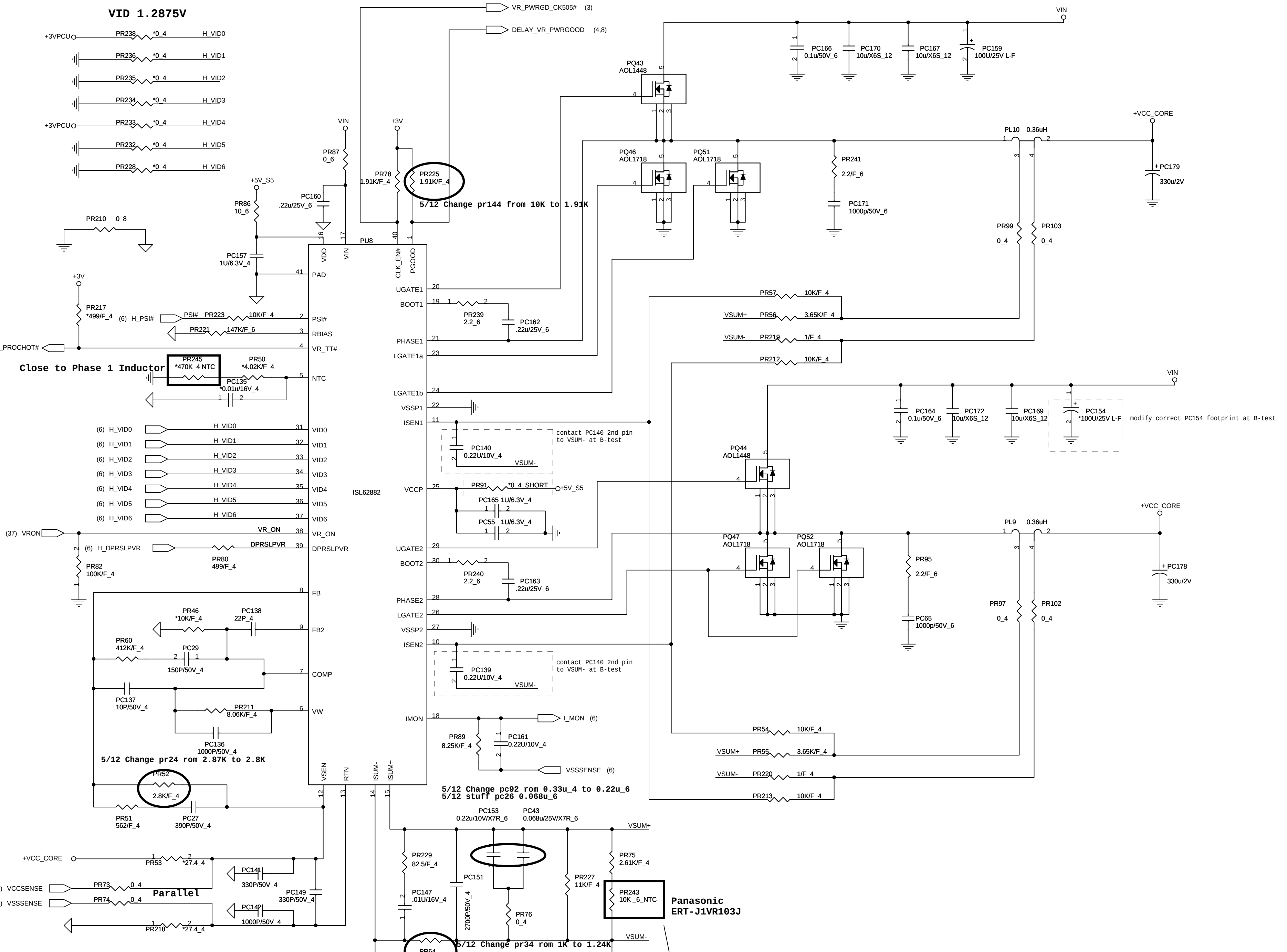
Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	SYSTEM 5V/3V (ISL6237)	1A

Date: Tuesday, September 22, 2009 Sheet 39 of 49

[PWM]



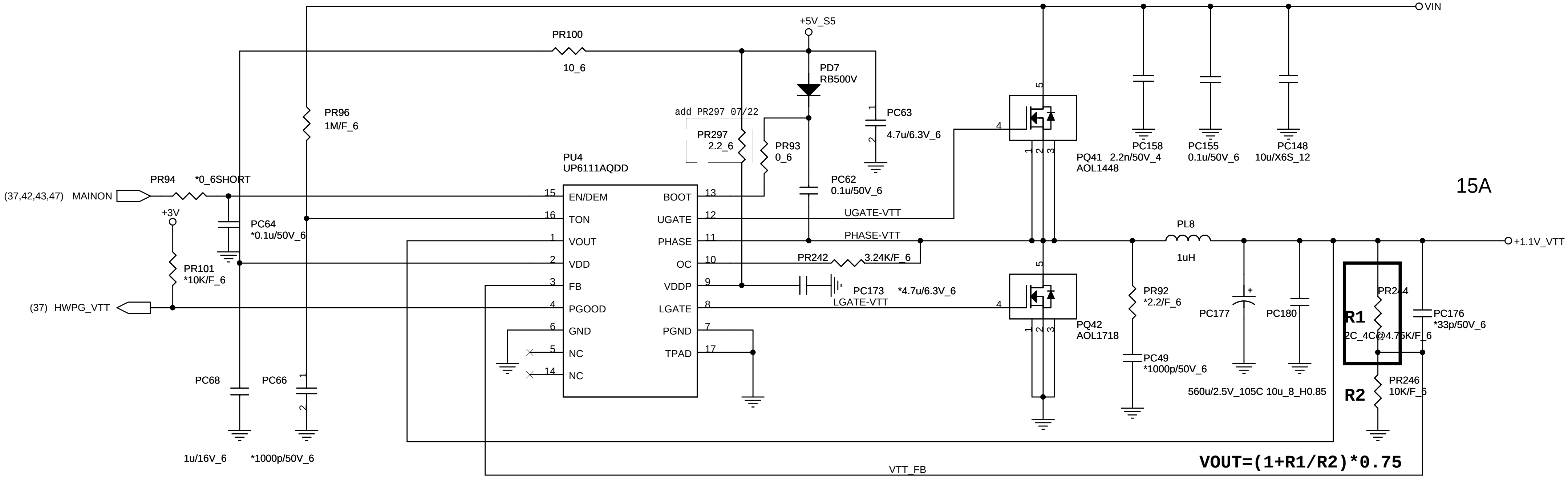
Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	CPU Core (ISL62882)	1A

Date: Thursday, September 17, 2009 Sheet 40 of 49

[PWM]



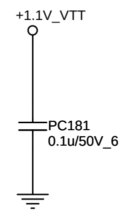
5/4
PR157 change to 4.75K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

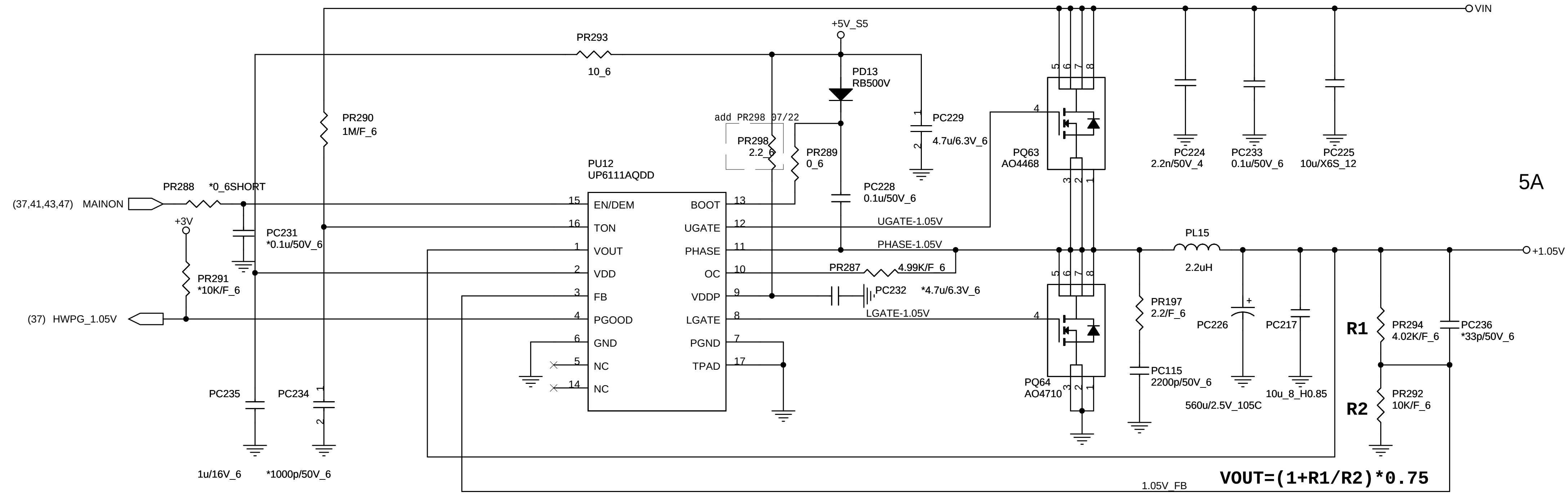
4.3m*15=RILIM*20uA
RILIM=3.24K(3.22K)

BOM change notice
Arrandale (1.05V) R1 = 4.02K (CS24023F928)
Clarksfield(1.1V) R1 = 4.75K (CS24753F919)



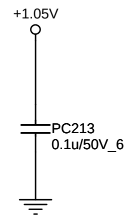
Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: +VTT (UP6111A)	Rev: 1A
Date: Thursday, September 17, 2009		Sheet 41 of 49

[PWM]



AO4710 Rdson=11.8~14.2mOhm
OCP=7.2-0.8A
L(ripple current)
=(19-1.05)*1.05/(2.2u*272k*19)
~1.6577A

14.2m*7=RILIM*20uA
RILIM=4.99K(4.97K)

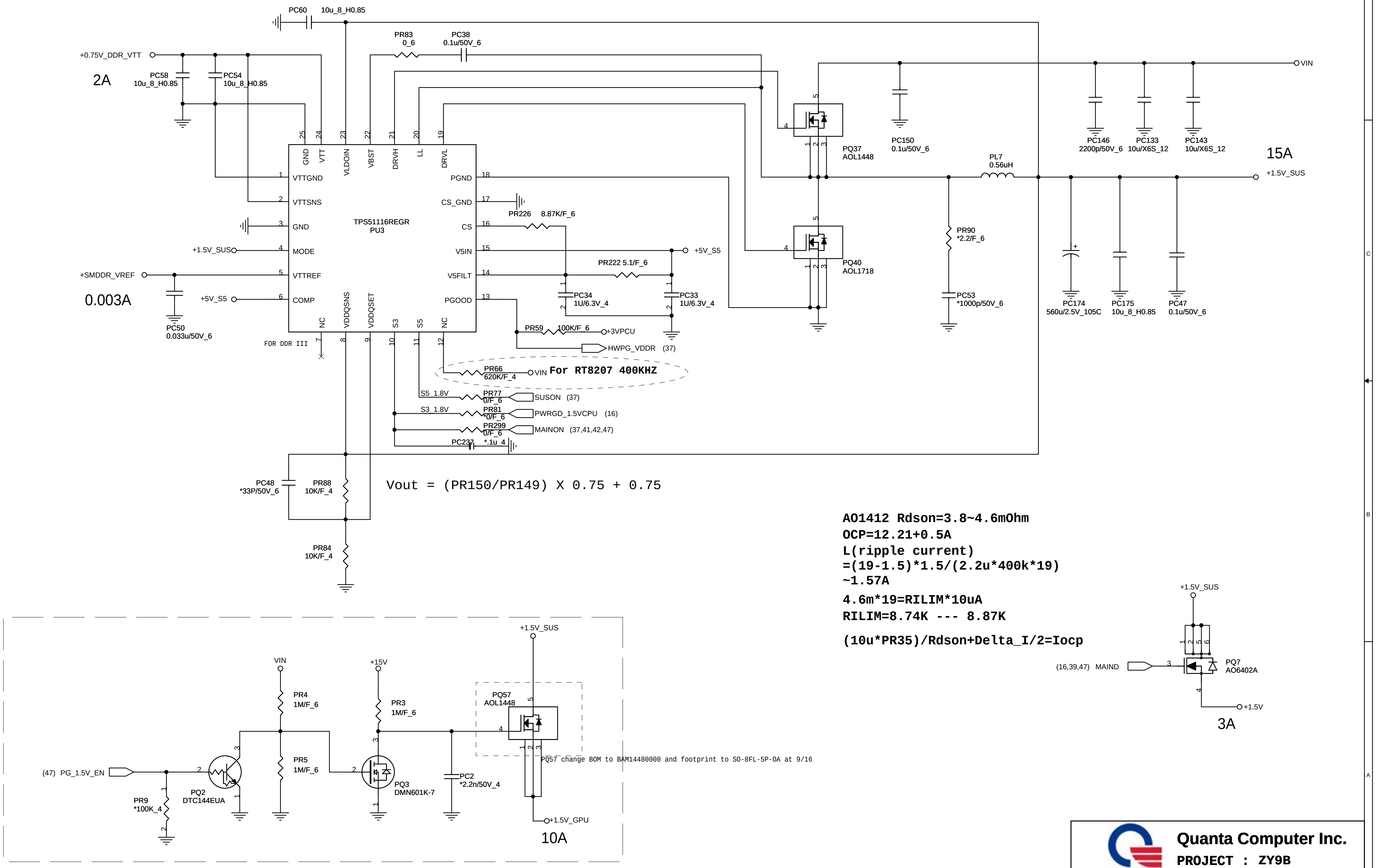


Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	+1.05V(UP6111AQDD)	1A
Date: Monday, September 21, 2009	Sheet 42 of 49	

[PWM]

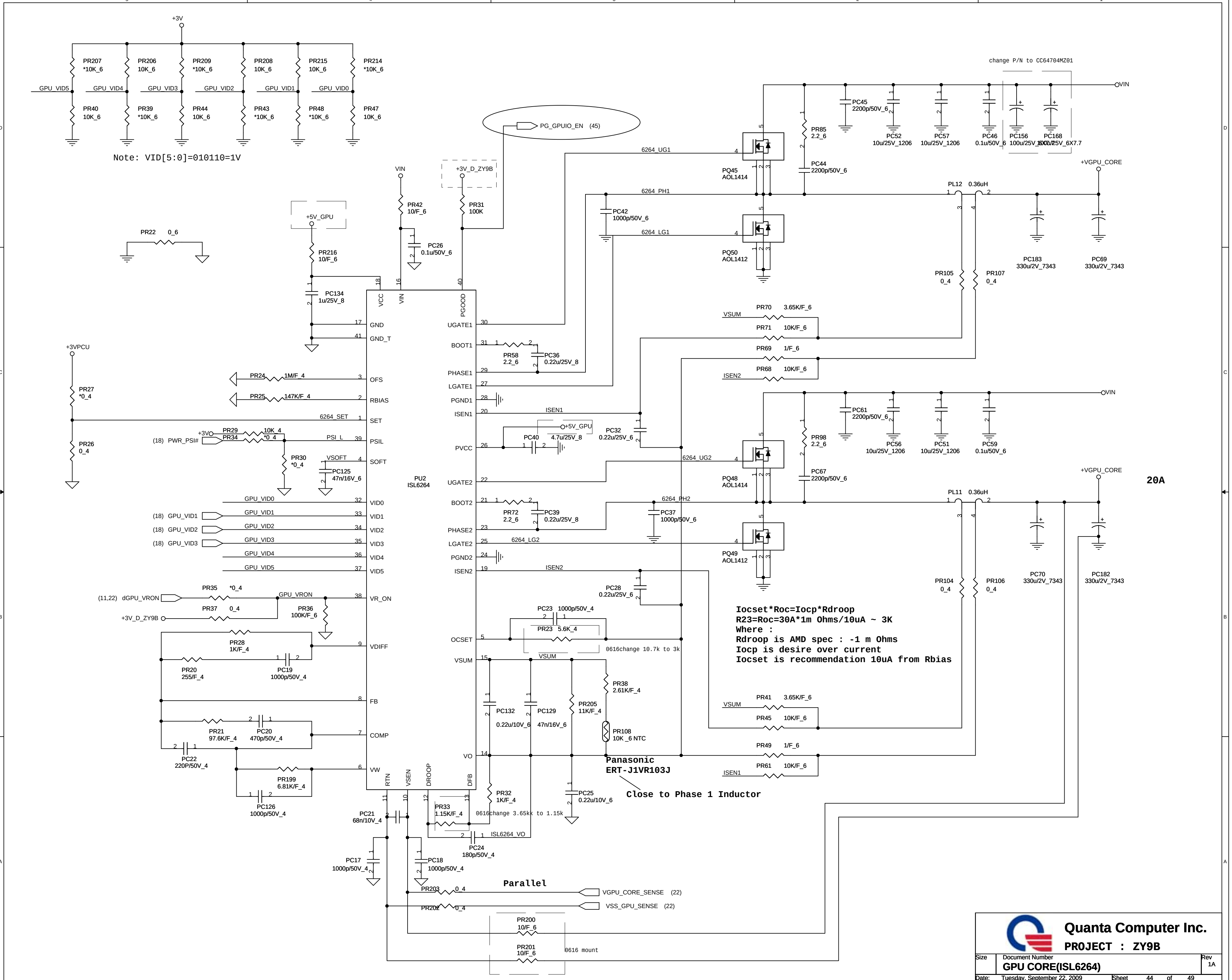


Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

Date: Thursday, September 17, 2009 Sheet 43 of 49

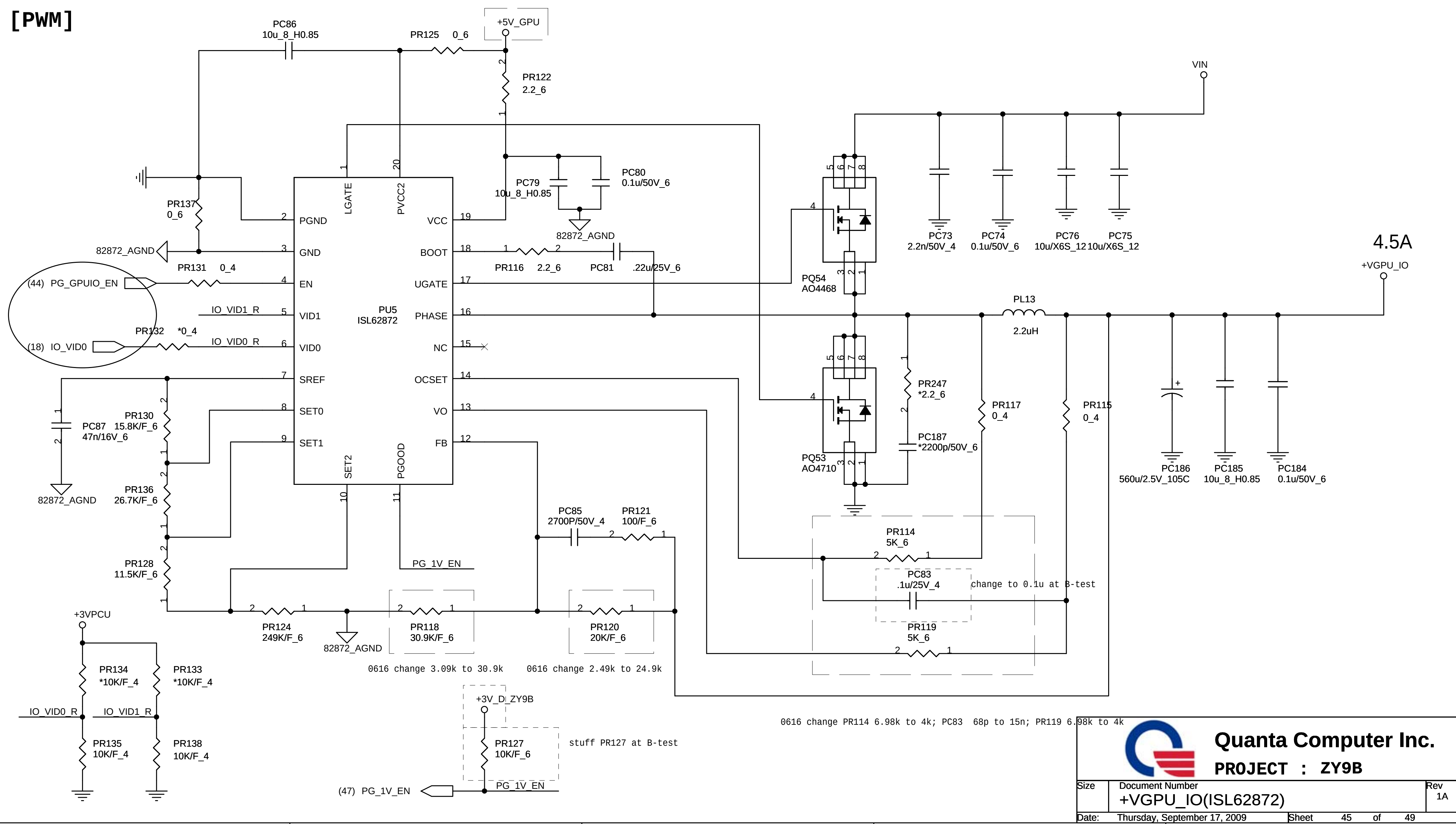


Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	GPU CORE(ISL6264)	1A
Date: Tuesday, September 22, 2009	Sheet 44 of 49	

[PWM]



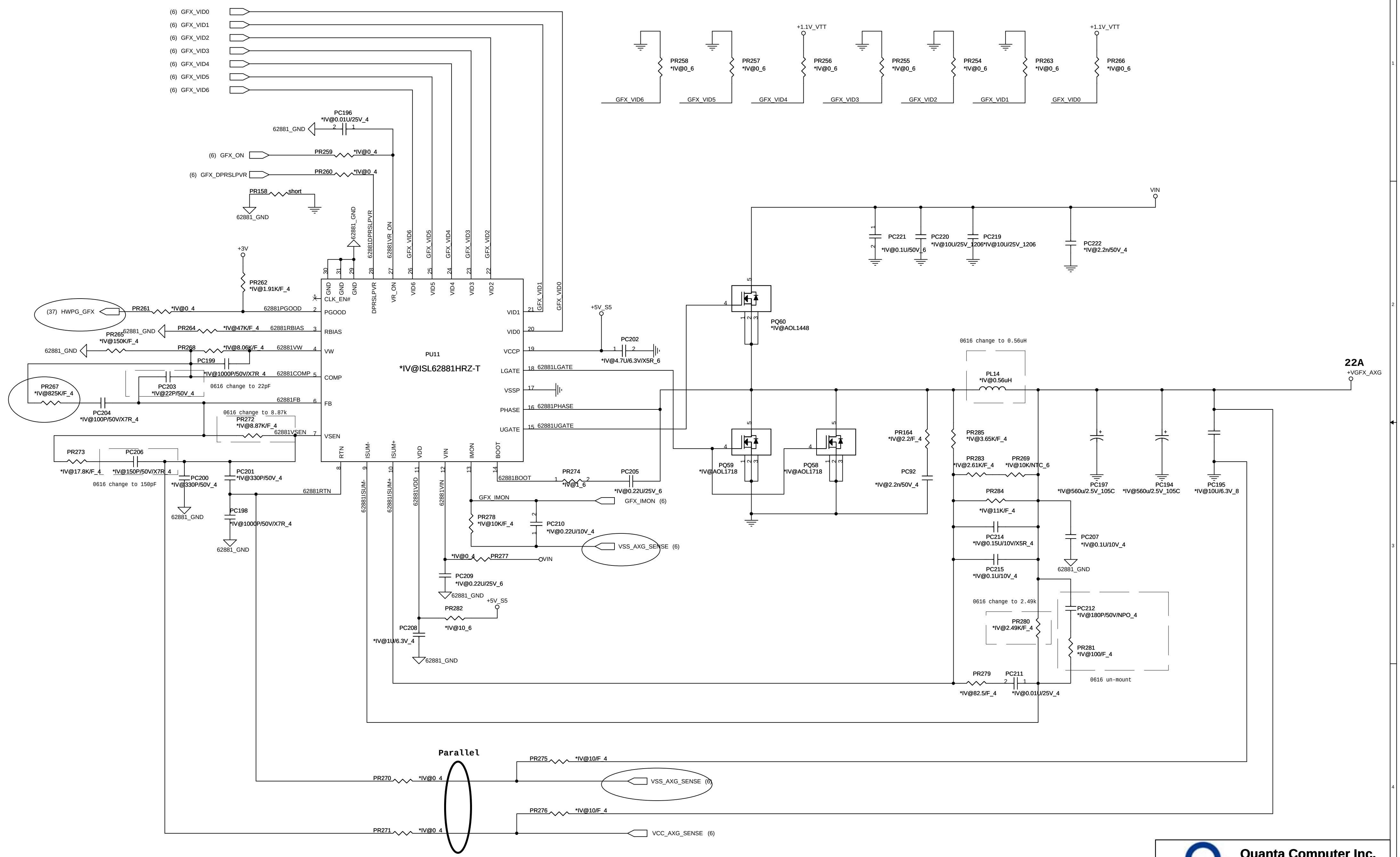
Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	+VGPU_IO(ISL62872)	1A

Date: Thursday, September 17, 2009 Sheet 45 of 49

Int_VGA [PWM]

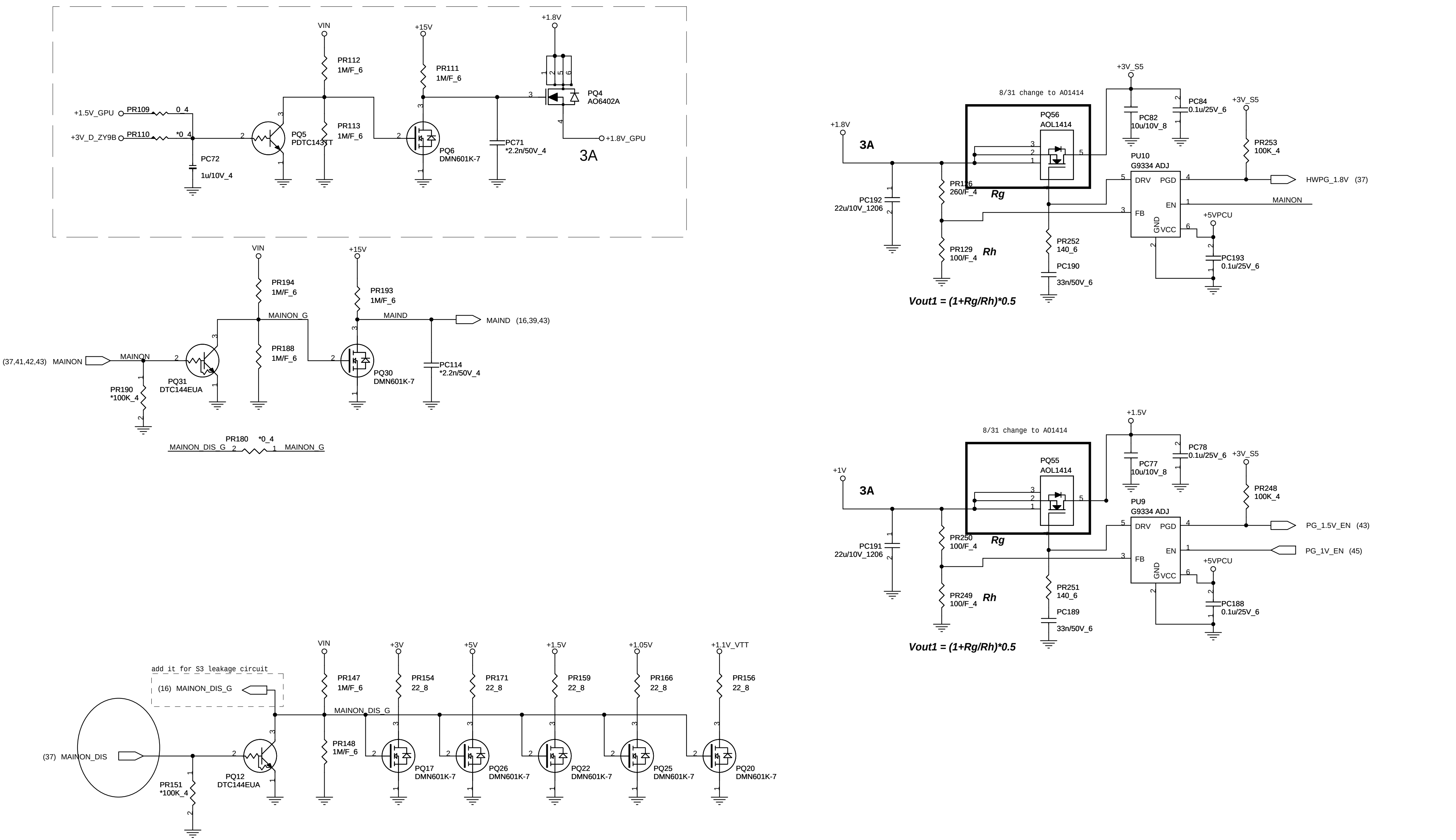


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	1A
Date:	Tuesday, September 22, 2009	Sheet 46 of 49

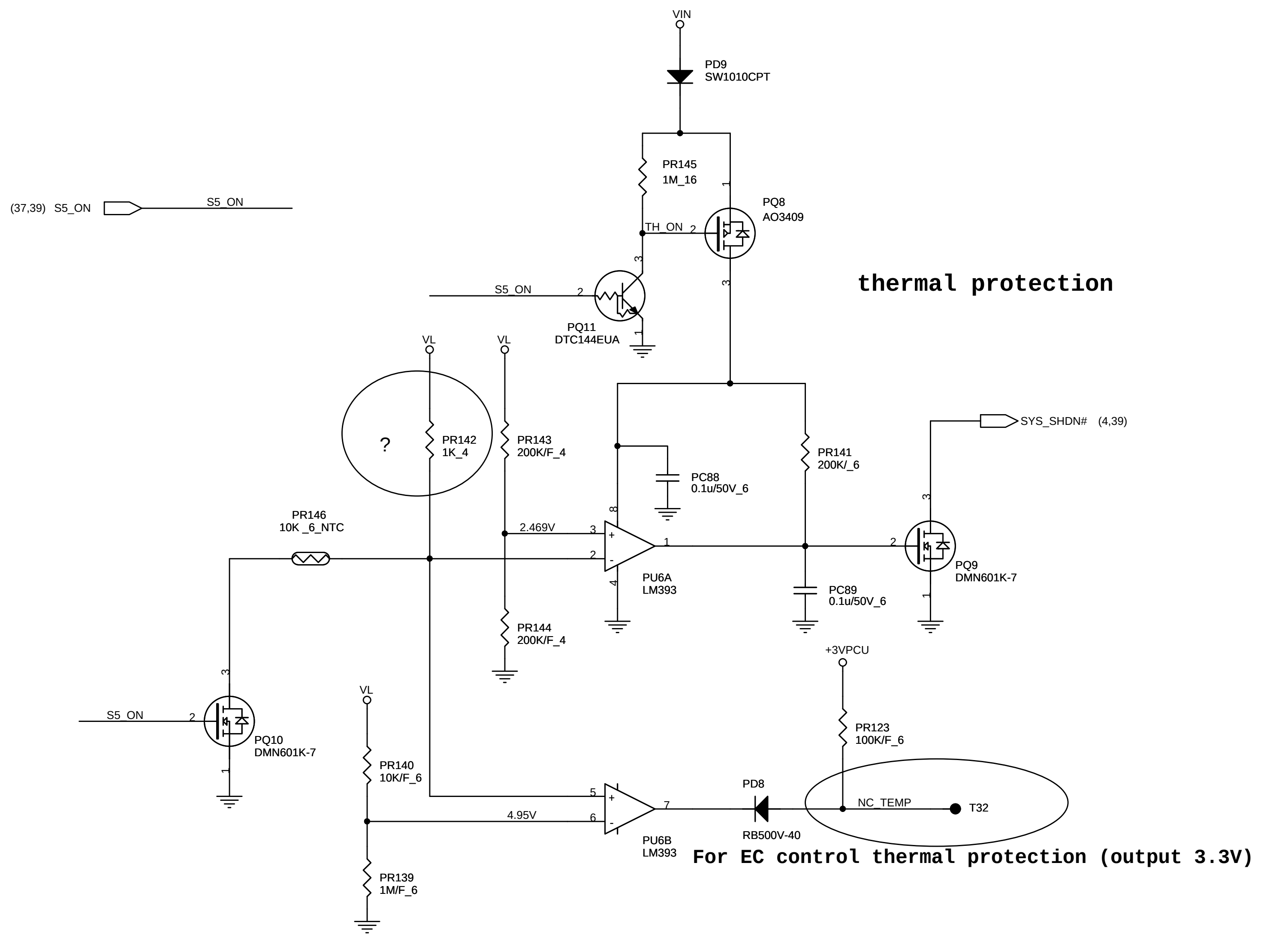
[PWM]



Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	Discharge/1V/1.8V)	1A
Date: Thursday, September 17, 2009	Sheet 47 of 49	



Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	Thermal Protection	1A

Date: Thursday, September 17, 2009 | Sheet 48 of 49

CHANGE LIST

Model	REV	CHANGE LIST
ZY9B MB	1A	FIRST RELEASED: E20080?-???? (PCB: DA0ZY9MB8A0)
	2A	Page4 :
	3A	
	3C	

MODEL: ZY9B

FROM	To
X	1A
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2A	3A
2A	3A
3A	3B
3A	3B
3A	3B
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