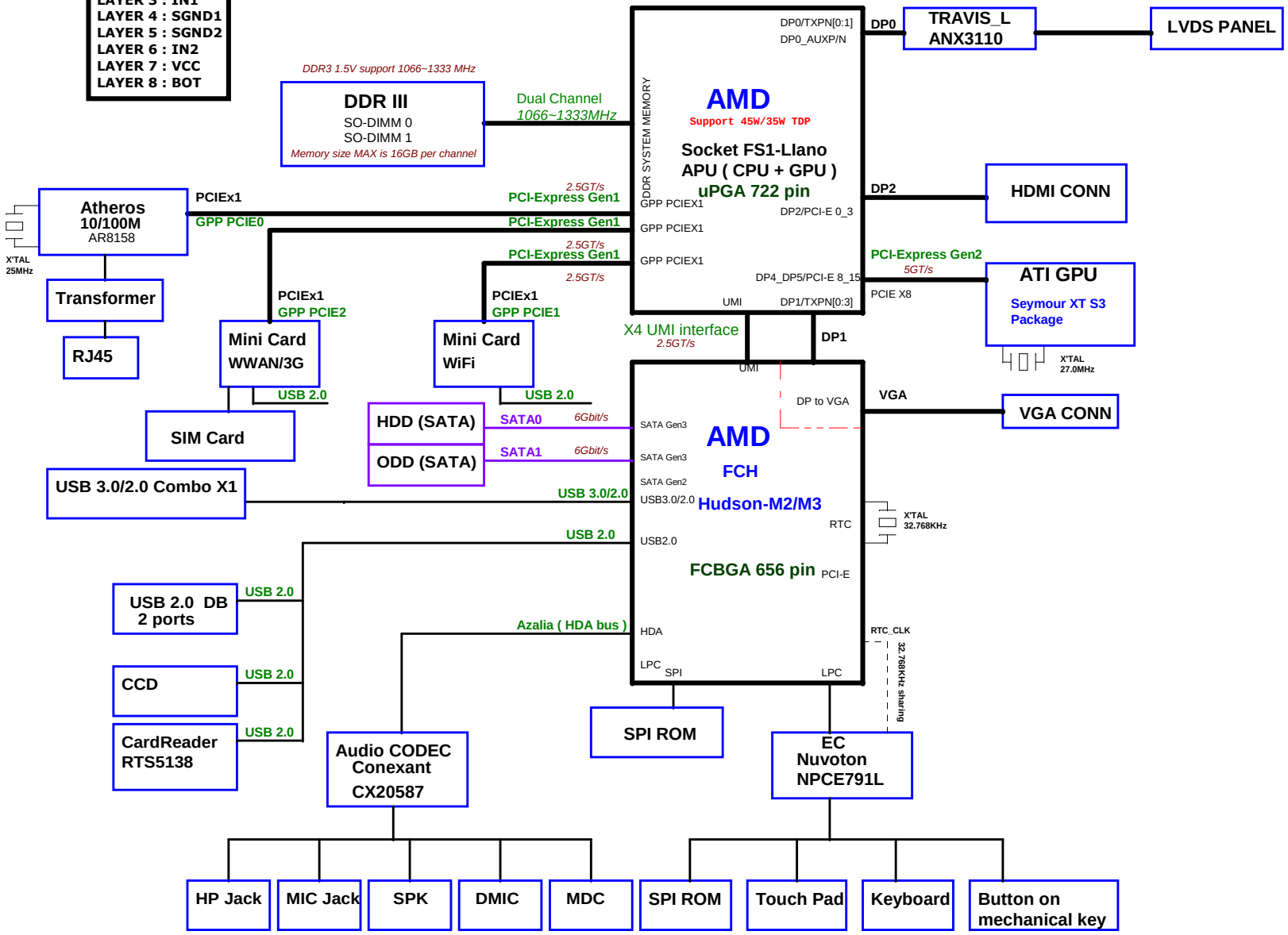
BLOCK DIAGRAM

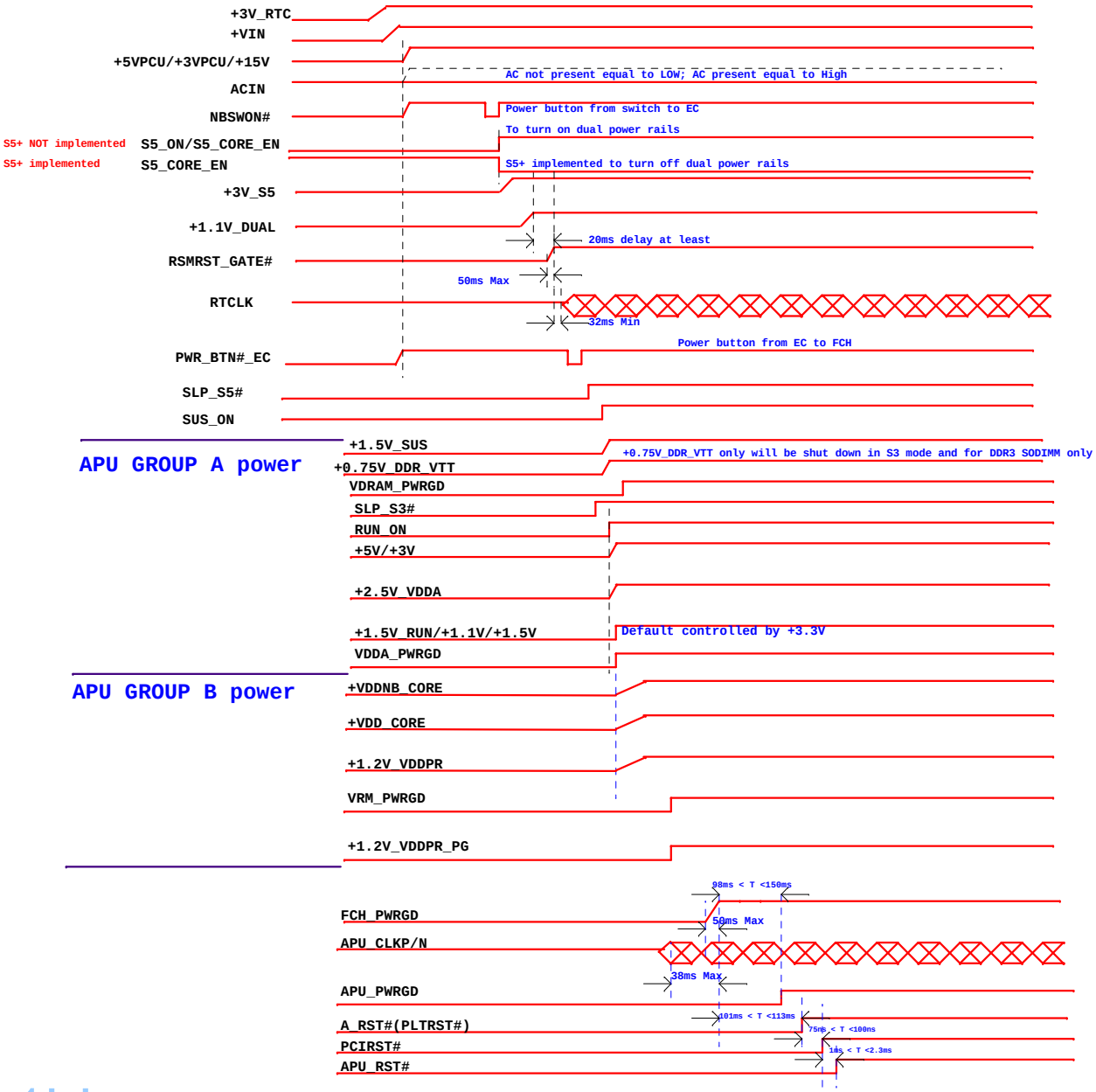
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : SGND1
LAYER 5 : SGND2
LAYER 6 : IN2
LAYER 7 : VCC
LAYER 8 : BOT



Quanta Computer Inc.
PROJECT : BLF_BLFD
Size | Document Number: System Block Diagram | Rev 1C
Date: Tuesday, April 19, 2011 | Sheet 1 of 53

BLF/BLFD Power On Sequence: S5 > S0



APU Power on sequence required:

Llano APU:
1.Group A (+1.5V_SUS, +2.5V_VDDA) ramp before Group B (+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M2/M3:
1.+3V_S5 ramp before +1.1V_DUAL
2.+3V ramp before +1.1V
3.+3V_RTC must ramp at least 5 secs before the +3V_S5

Seymour XT S3 package Power-on sequence

All power rails reach nominal within 20ms

1 => +3V_GPU
2 => +VGPU_CORE/+1V_GPU
3 => +VGPU_CORE PWRGD to enable +1.5V_GPU
4.=> +1V_GPU PWRGD to enable +1.8V_GPU

NOTE

1.+3V to turn on +3V_GPU

2.+3V_GPU ready to enable +VGPU_CORE/+1V_GPU
(+1V_GPU will ramp up before +VGPU_CORE)

3.+VGPU_CORE PWRGD to enable +1.5V_GPU

3.+1V_GPU PWRGD to enable +1.8V_GPU

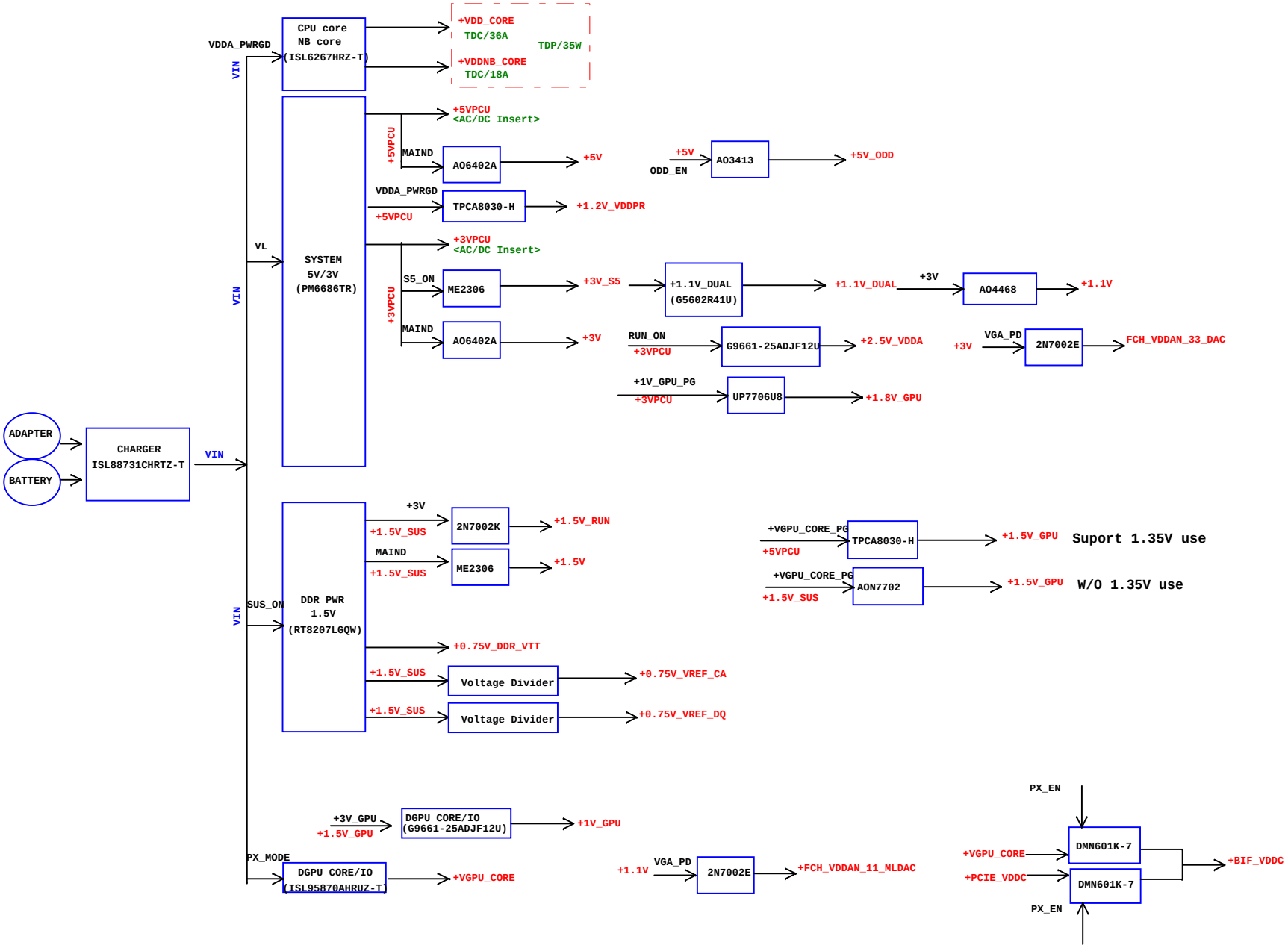
TRAVIS_L ANX3110 power on sequecne

1.+3V must lead +1.2V_TRAVIS

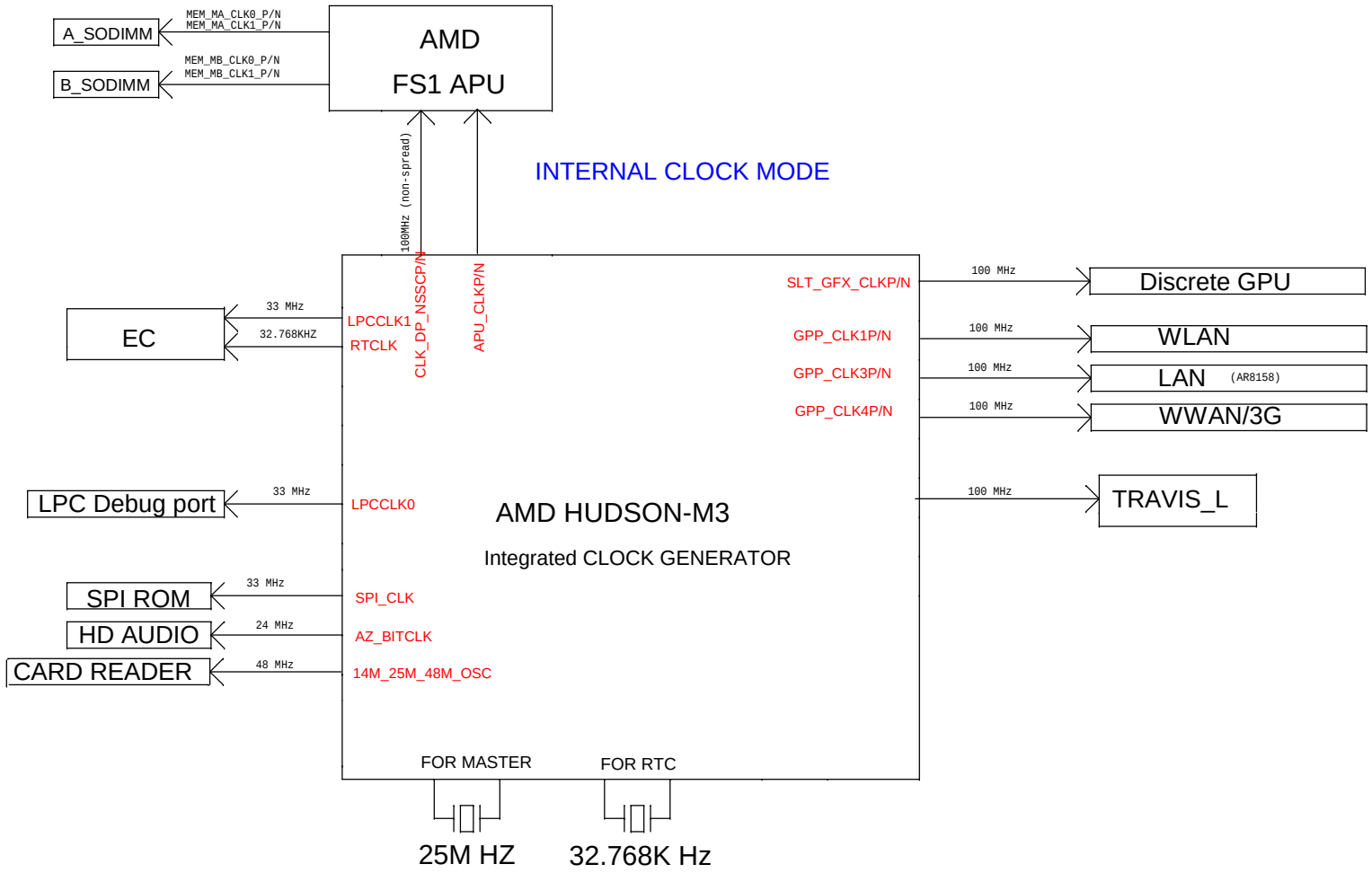
2.+1.2V_TRAVIS must lead TRAVIS_RST#

NOTE: FCH must output PCIE_RST#_TRAVIS or APU_PCIE_RST# after +1.2V_TRAVIS ready

Quanta Computer Inc.
PROJECT : BLF_BLFD
Size | Document Number | Rev 1C
POWER SEQUENCE
Date: Tuesday, April 19, 2011 | Sheet 2 of 53



Quanta Computer Inc.
PROJECT : BLF_BLFD
Power Tree

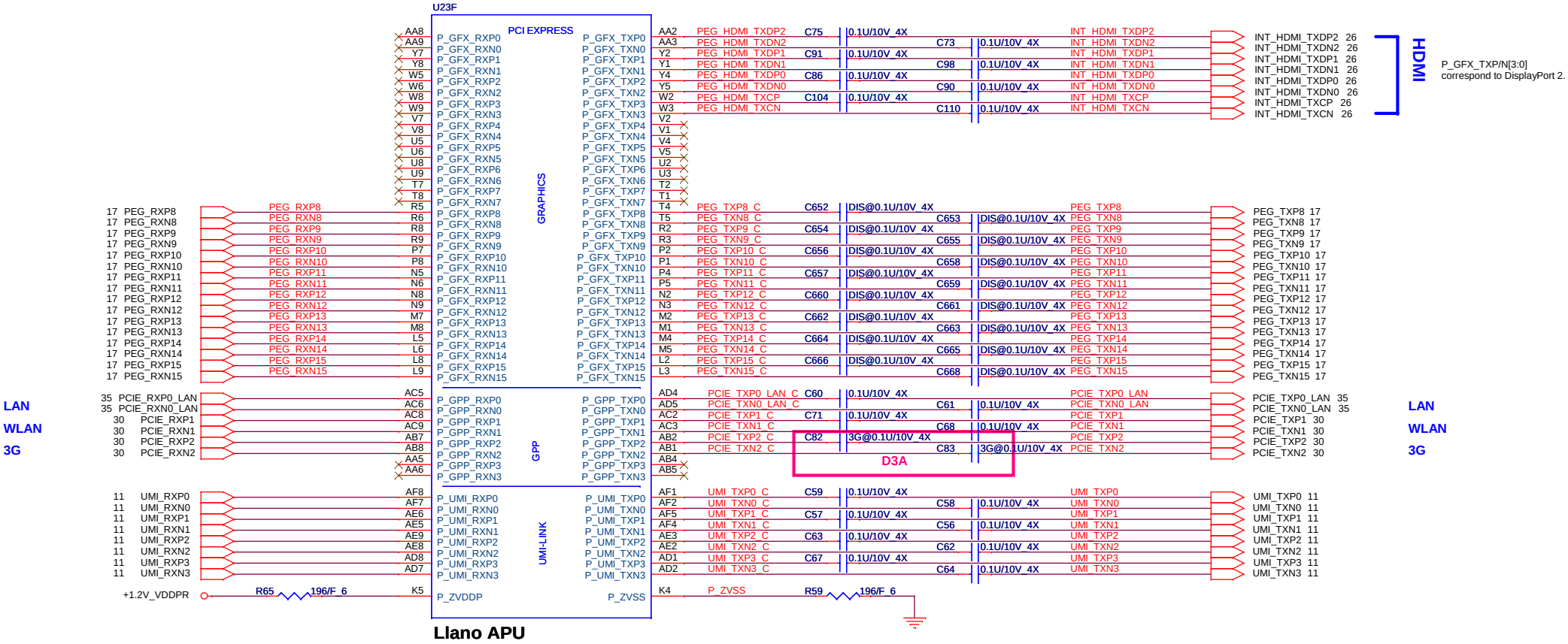


Quanta Computer Inc.

PROJECT : BLF_BLFD

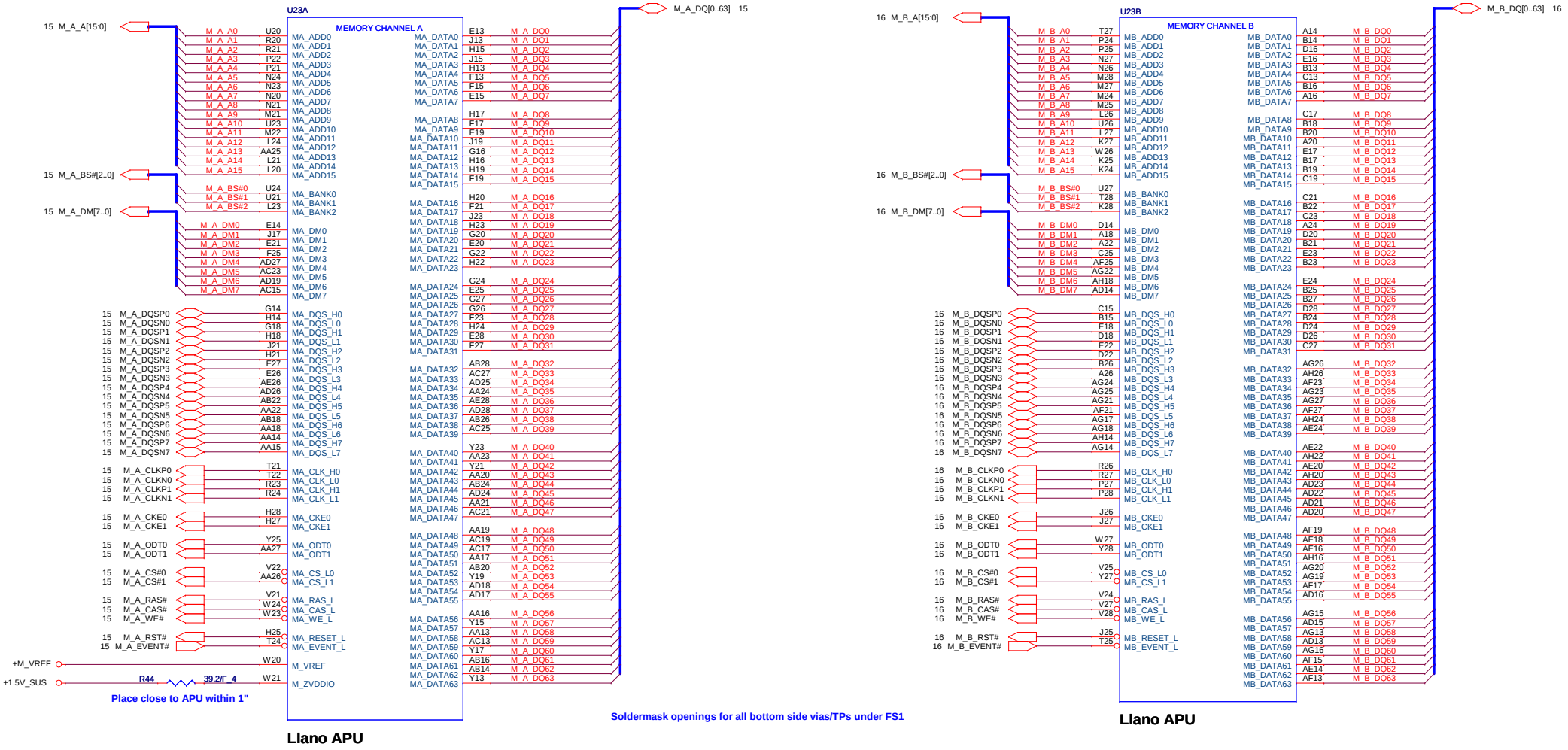
Size	Document Number	Rev
	Clock Distribution Diagram	1C

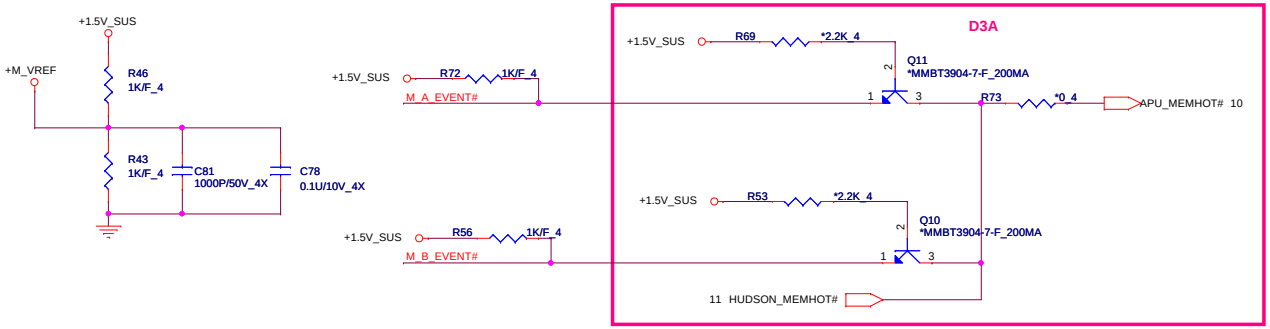
Date: Tuesday, April 19, 2011 Sheet 4 of 53



Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Llano PCIE/UMI/GPP	1C
Date: Tuesday, April 19, 2011	Sheet 5 of 53	





Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Llano DDR3 MEM I/F	1C
Date: Tuesday, April 19, 2011	Sheet 6 of 53	

DP0 to LVDS

DP1 to Hudson-M3 VGA output

Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

LVDS VGA HDMI

LVDS Hot-plug

CRT Hot-plug

Llano APU

These TP near the APU

Debug only

NEAR CPU

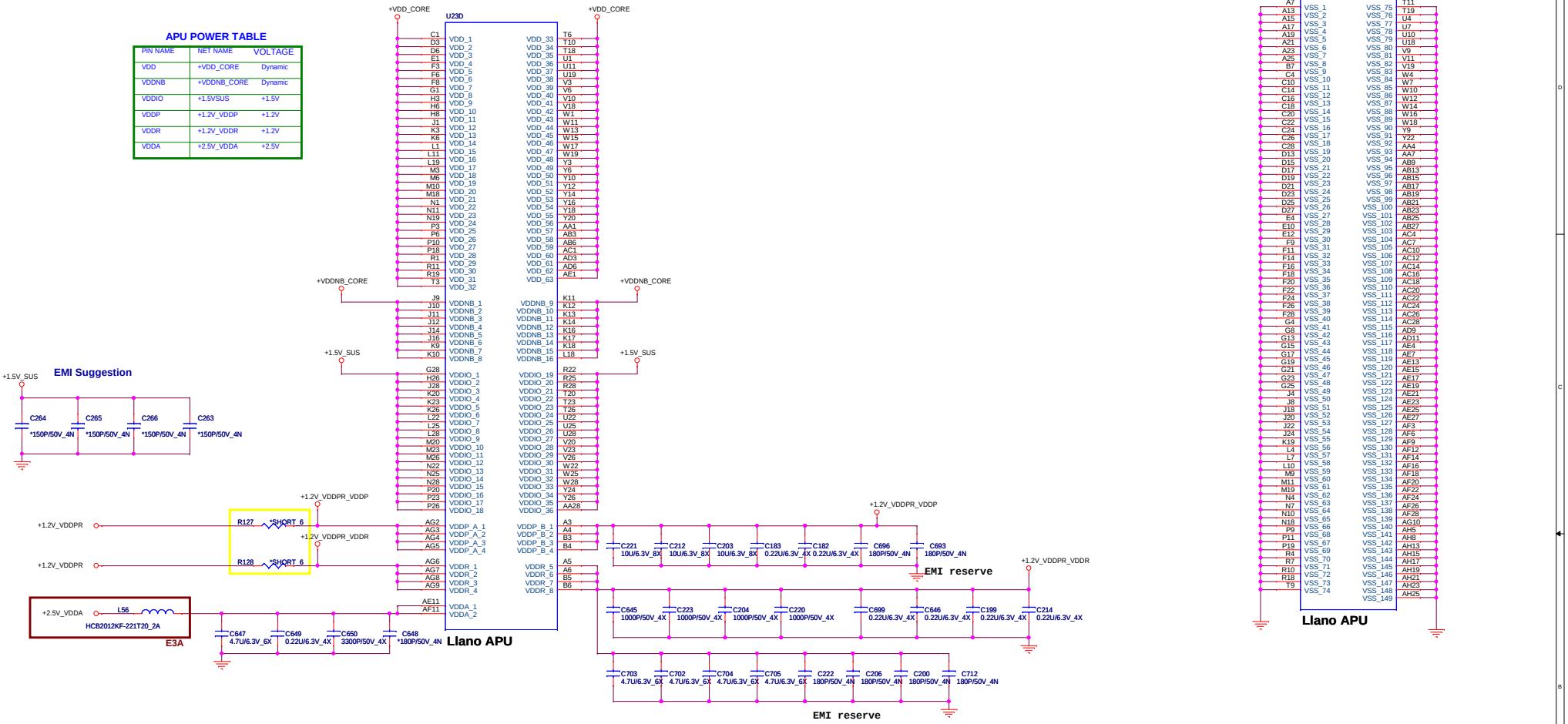
67dgree

Rset(Kohm)=0.0012T*T-0.9308T+96.147,
Shut down on 67dgree (Follow thermal team report)
Hysteresis is 30C

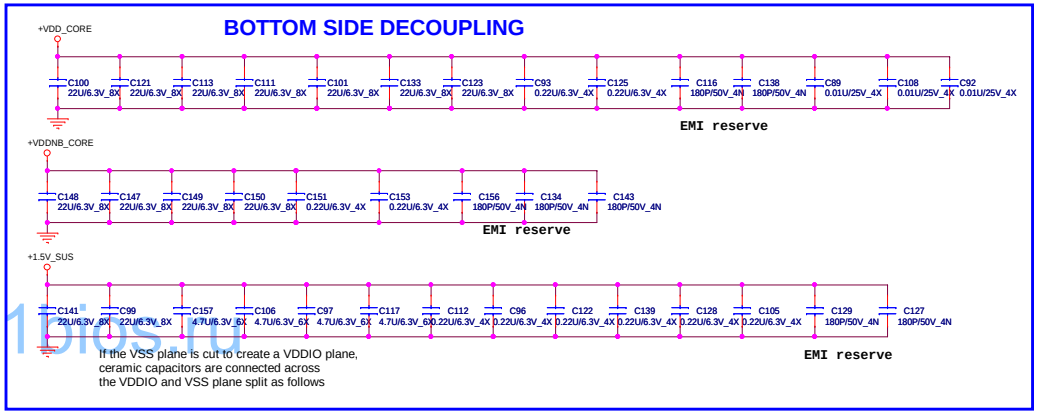
Quanta Computer Inc.
PROJECT : BLF_BLFD
Size | Document Number: Llano Display/Misc | Rev: 1C
Date: Tuesday, April 19, 2011 | Sheet 7 of 53

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	Dynamic
VDDNB	+VDDNB_CORE	Dynamic
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



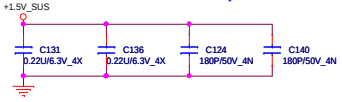
BOTTOM SIDE DECOUPLING



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

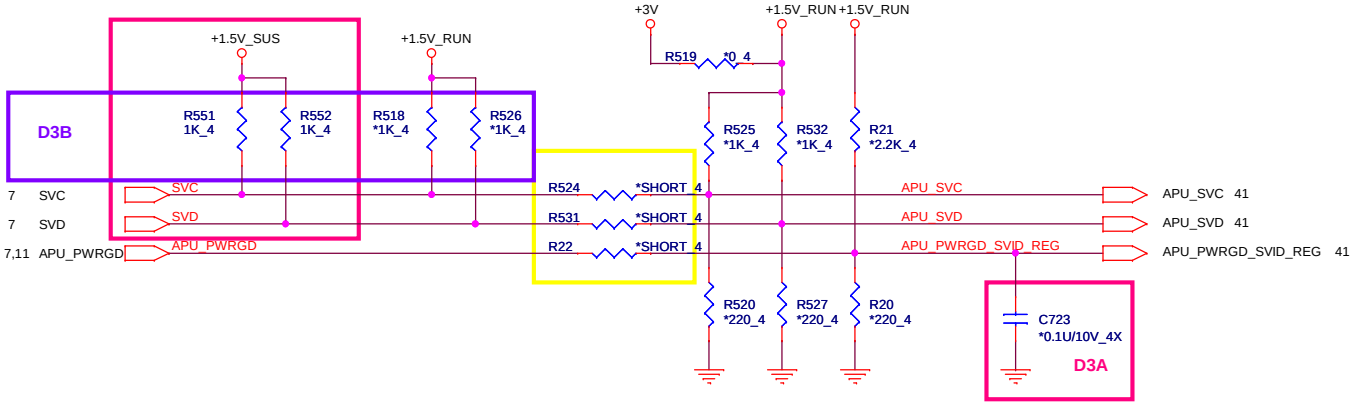
DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split



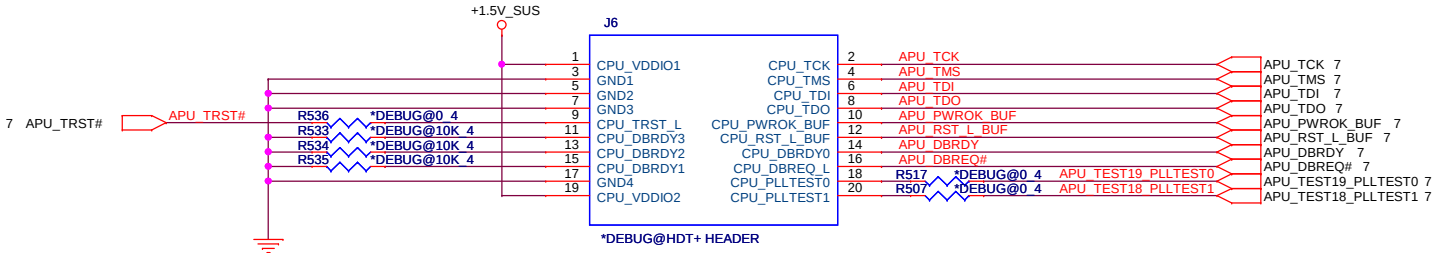
Quanta Computer Inc.
PROJECT : BLF_BLFD
Size | Document Number: Llano POWER/GND | Rev 1C
Date: Tuesday, April 19, 2011 | Sheet 8 of 53

VID Override Circuit



HDT+ Connector

Debug only



Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: Llano DEBUG&OTHER	Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 9 of 53	

NC,no install by default

remove pull hi (chip internal have pull hi)

HUDSON-M2
Part 4 of 5

HUB3
HUB2
HUB1

Reserve USB2.0/3.0 option
3G
SIM Card
WLAN
CCD on LVDS
Card Reader
USB 2.0 x1
TO USB daughter board
TO USB daughter board
USB 3.0 x1

HD audio interface is +3V_S5 voltage

To Azalia

Note:LLB#, WAKE# and PWR_BTN need pull up to +3VPCU only if S5+ mode is supported

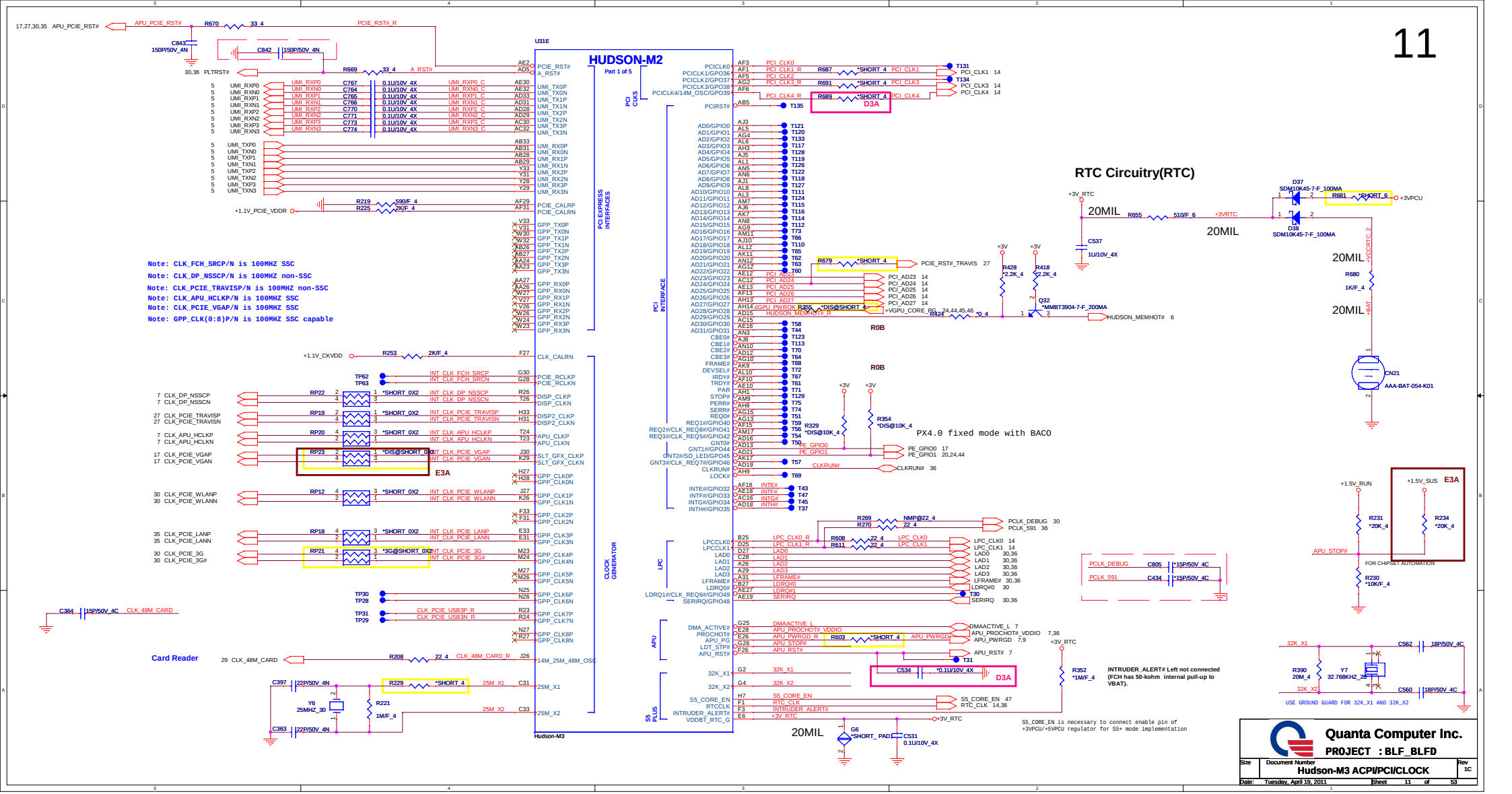
Provided test points from checklist

Hudson-M3

Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Hudson-M3 GPIO/USB/AZ/RGMII	1C

Date: Tuesday, April 19, 2011 Sheet 10 of 53



Quanta Computer Inc.			
PROJECT : BLF_BLFD			
Size	Document Number		Rev
	Hudson-M3 ACPI/PCI/CLOCK		1C
Date: Tuesday, April 19, 2011	Sheet 11 of 53		

PLACE SATA AC COUPLING CAPS CLOSE TO HUDSON-M2/M3

SATA HDD/SSD

SATA ODD

U31B

HUDSON-M2 Part 2 of 5

Hudson-M3

W25Q16BVSSIG: AKE38FP0N01

Socket: DG008000031

PLACE SATA_CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3

Integrated Clock Mode: Leave unconnected.

Remove Zero Power ODD funciton

R place close to PCH

BOARD ID SETTING

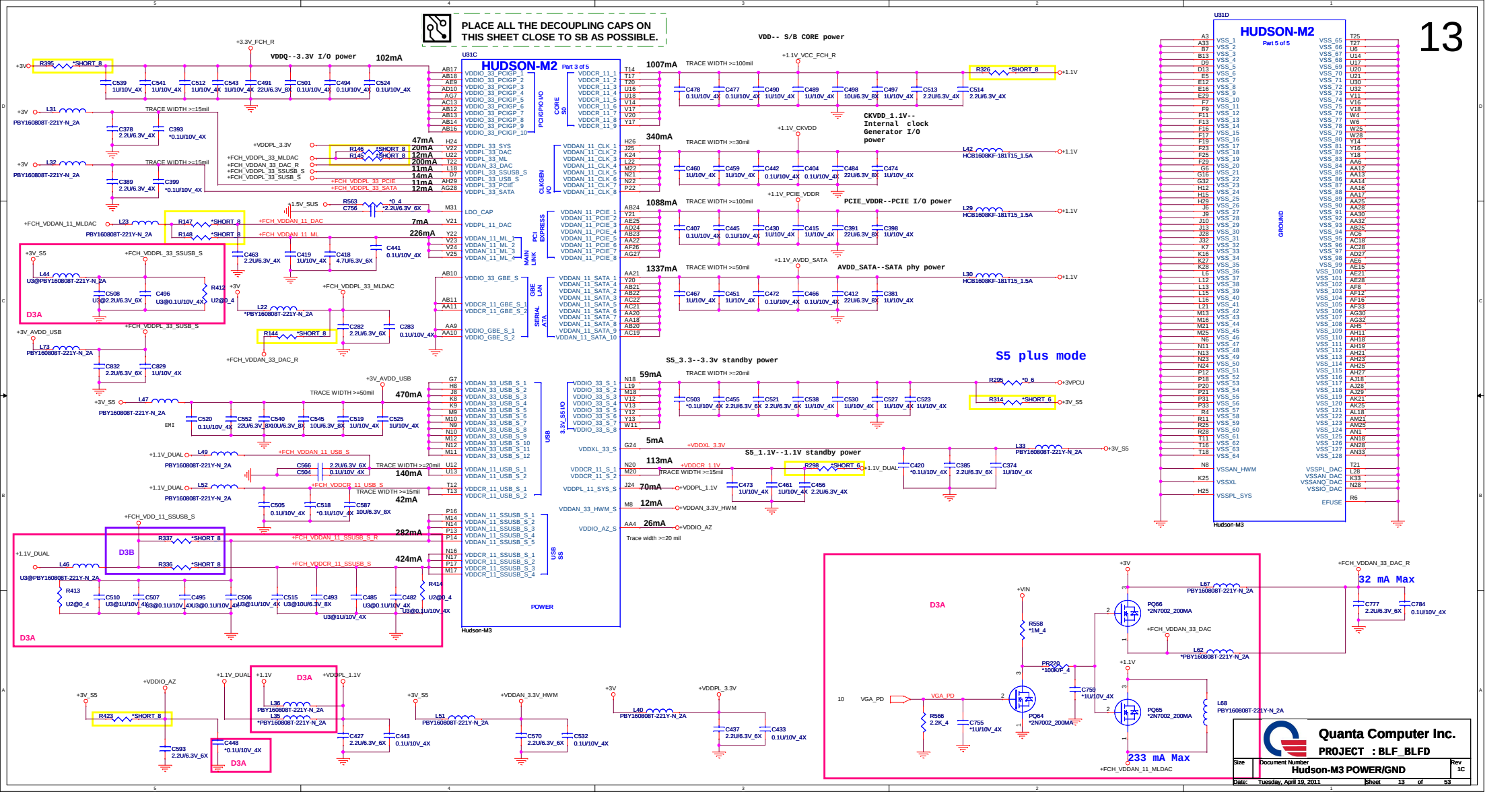
Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
UMA SKU VGA SKU	H L								
W/ MDC W/O MDC		H L							
FCH-M3 FCH-M2			H L						
W/O 3G W/ 3G				H L					
15" 14"					H L				
W/O BT W/ BT						H L			
Reserve							X		
Reserve								X	
Reserve									X

Quanta Computer Inc.

PROJECT : BLF_BLFD

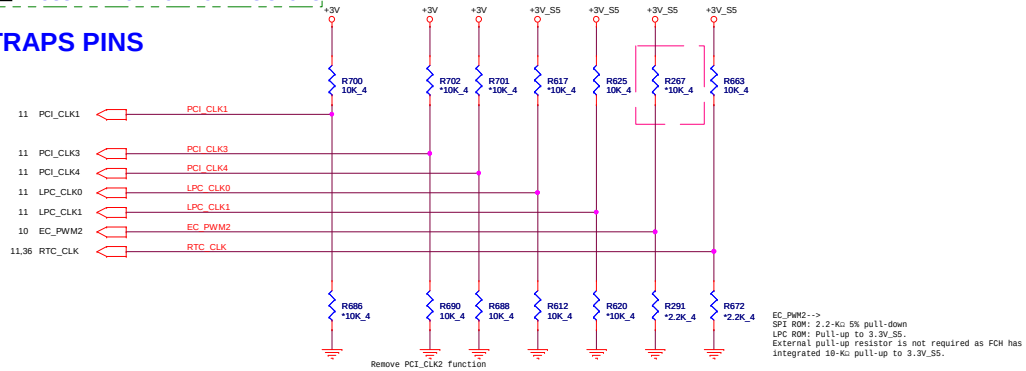
Size | Document Number: Hudson-M3 SATA/HWM/SPI | Rev: 1C

Date: Tuesday, April 19, 2011 | Sheet 12 of 53


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
13
HUDSON-M2
Part 3 of 5
Part 5 of 5
VDDQ--3.3V I/O power
VDD-- S/B CORE power
CKVDD_1.1V-- Internal clock Generator I/O power
PCIE_VDDR--PCIE I/O power
AVDD_SATA--SATA phy power
S5_3.3--3.3v standby power
S5_1.1V--1.1V standby power
S5 plus mode
32 mA Max
233 mA Max
Quanta Computer Inc.
PROJECT : BLF_BLFD
Hudson-M3 POWER/GND
Tuesday, April 19, 2011
Sheet 13 of 53
1bios.ru

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

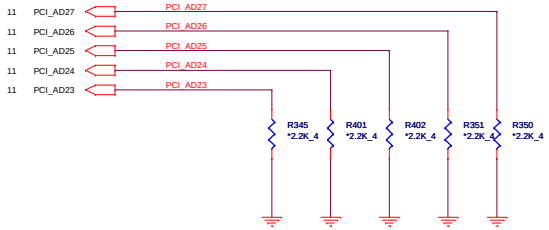


REQUIRED STRAPS

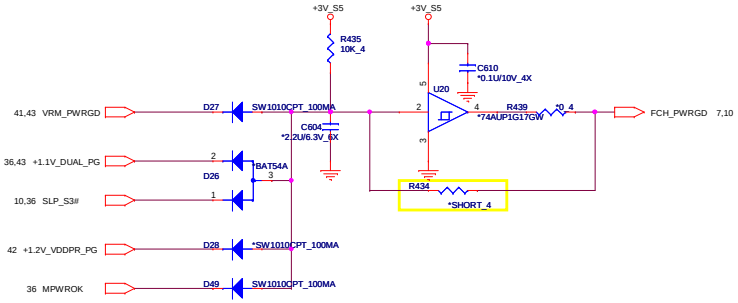
	--------	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



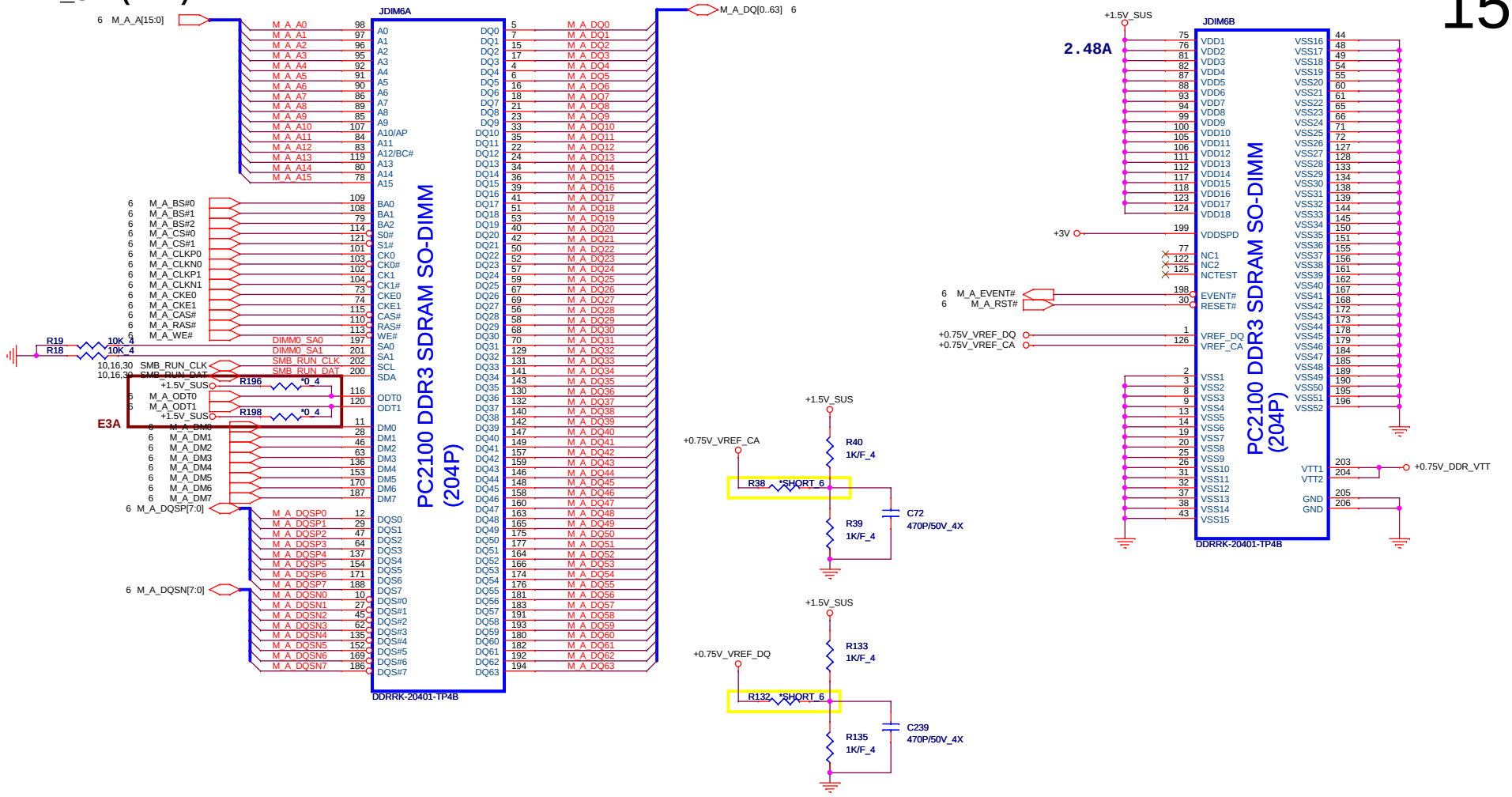
FCH PWRGD CKT

Quanta Computer Inc.
PROJECT : BLF_BLFD

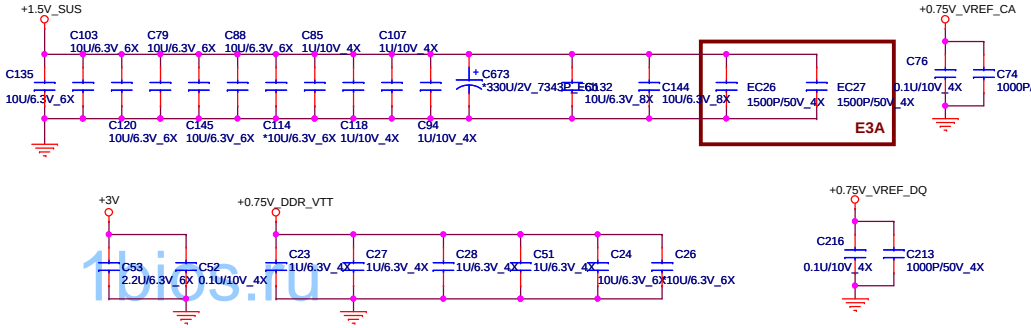
Size	Document Number	Rev
	Hudson-M3 STRAP/PWRGD	1C

Date: Tuesday, April 19, 2011 Sheet 14 of 53

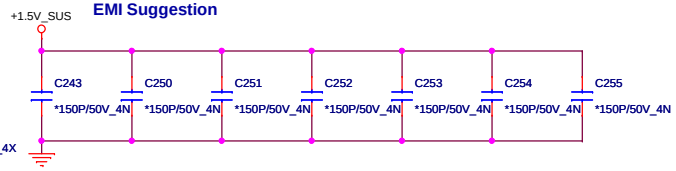
DDR_STD(DDR)



Place these Caps near So-Dimm0.



EMI Suggestion

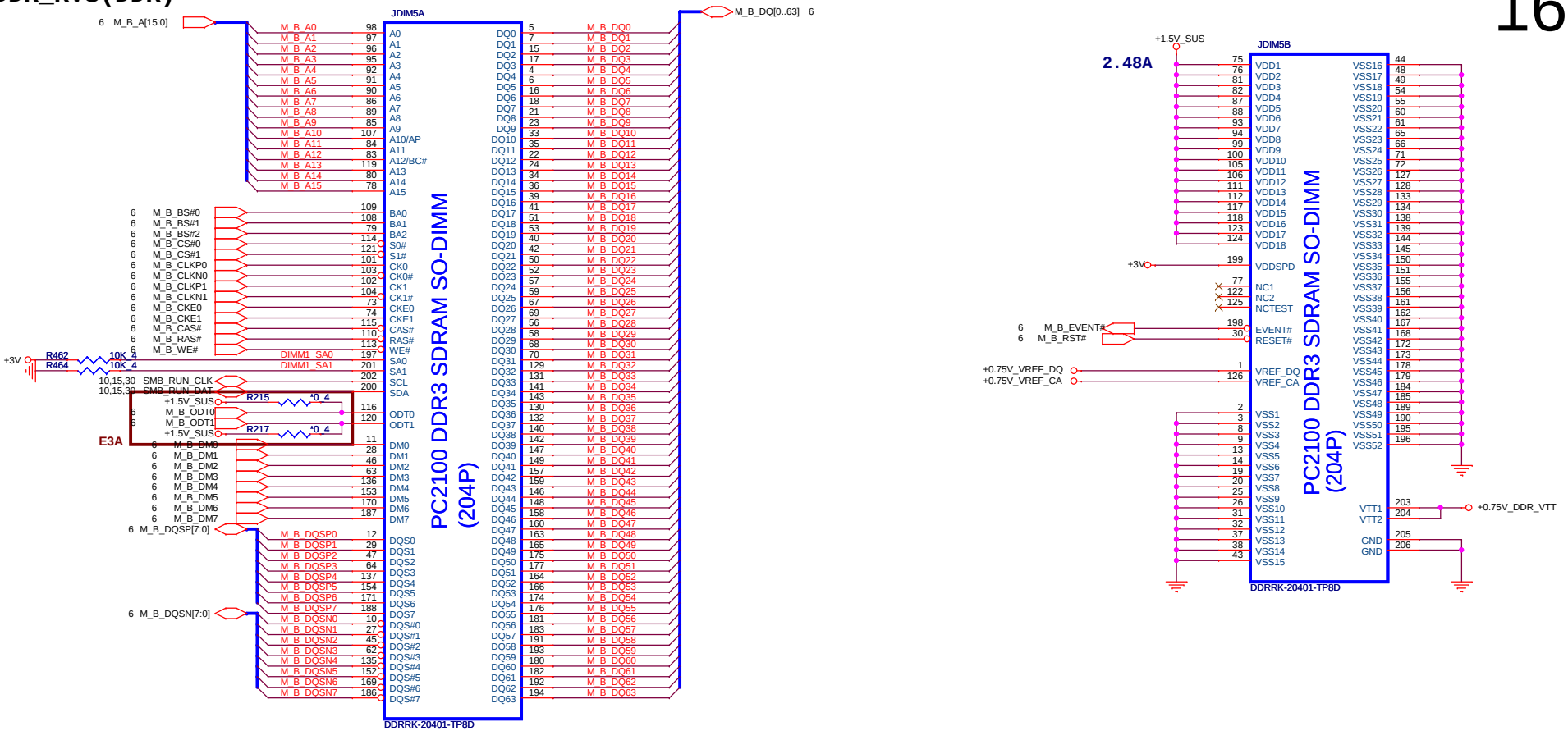


Quanta Computer Inc.

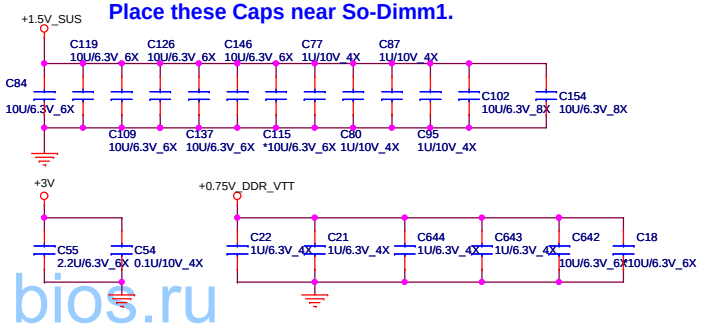
PROJECT : BLF_BLFD

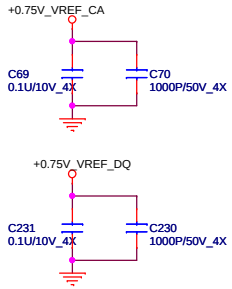
Size	Document Number	Rev
	DDRIII SO-DIMM-0	1C
Date: Tuesday, April 19, 2011	Sheet 15 of 53	

DDR_RVS(DDR)

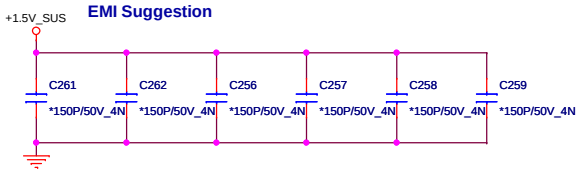


Place these Caps near So-Dimm1.

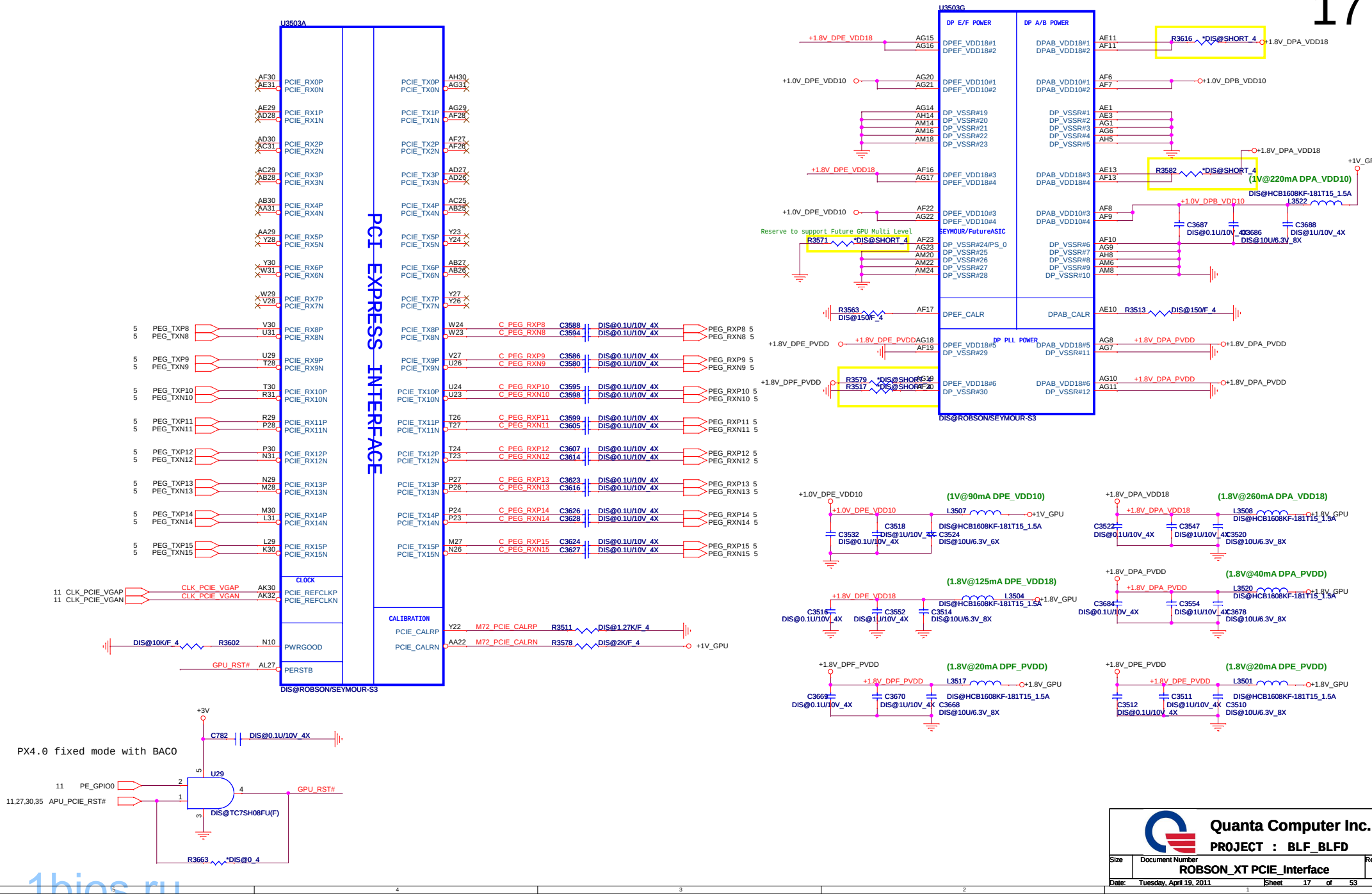




EMI Suggestion



Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: DDRIII SO-DIMM-1	Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 16 of 53	

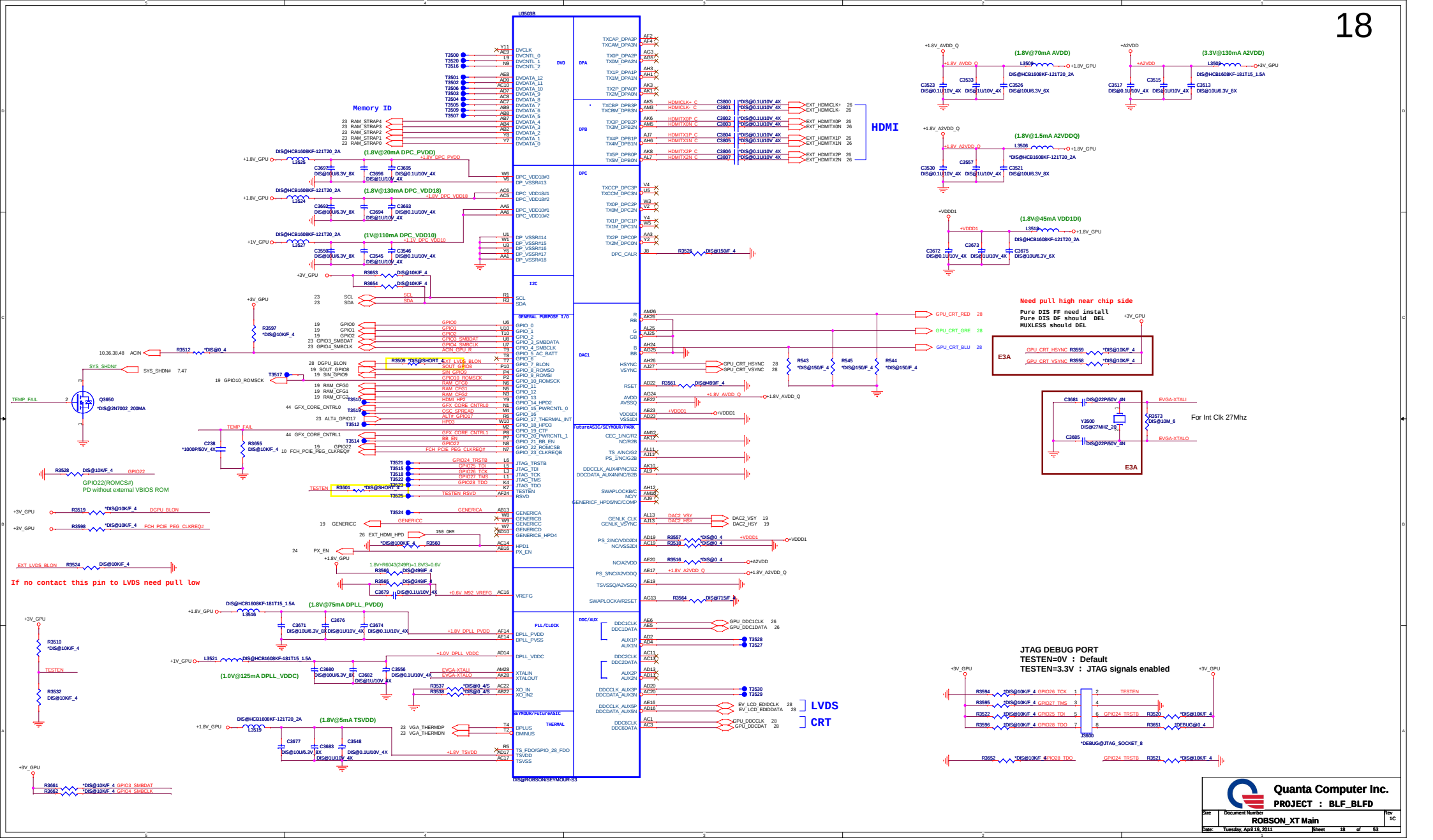


Quanta Computer Inc.

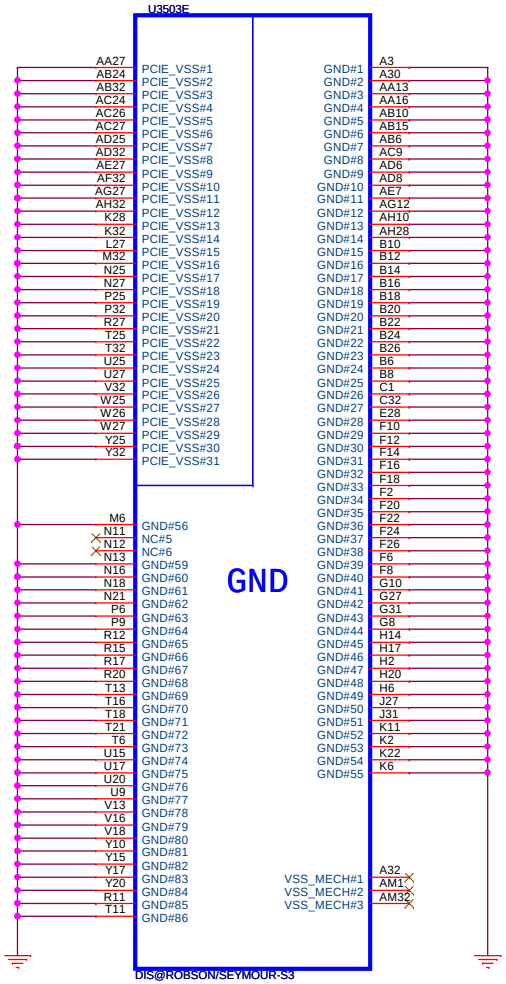
PROJECT : BLF_BLFD

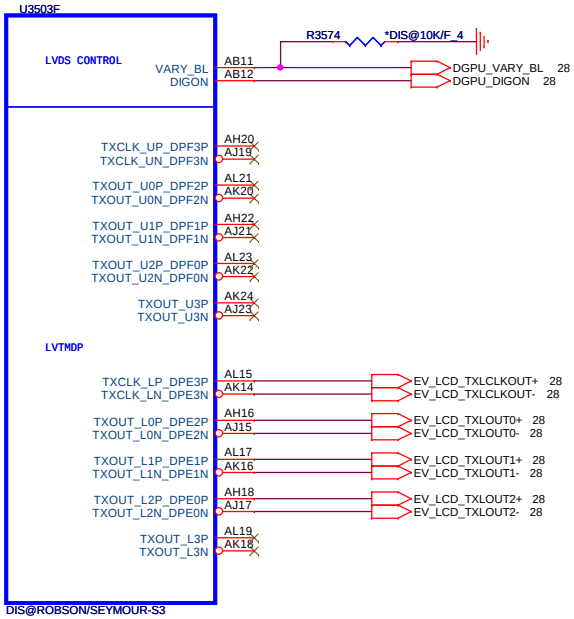
Size	Document Number	Rev
	ROBSON_XT PCIE_Interface	1C

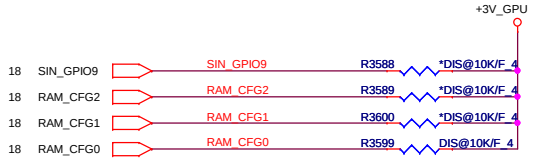
Date: Tuesday, April 19, 2011 Sheet 17 of 53


U3503B
Memory ID
HDMI
LVDS
CRT
(1.8V@20mA DPC_PVDD)
(1.8V@130mA DPC_VDD18)
(1V@110mA DPC_VDD10)
(1.8V@75mA DPLL_PVDD)
(1.0V@125mA DPLL_VDDC)
(1.8V@5mA TSVDD)
(1.8V@70mA AVDD)
(3.3V@130mA A2VDD)
(1.8V@1.5mA A2VDDQ)
(1.8V@45mA VDD1DI)
Need pull high near chip side
Pure DIS FF need install
Pure DIS DF should DEL
MUXLESS should DEL
For Int Clk 27Mhz
JTAG DEBUG PORT
TESTEN=0V : Default
TESTEN=3.3V : JTAG signals enabled
If no contact this pin to LVDS need pull low
GPIO22(ROMCS#)
PD without external VBIOS ROM
Quanta Computer Inc.
PROJECT : BLF_BLFD
ROBSON_XT Main
Tuesday, April 19, 2011
Sheet 18 of 53

Reserve only for MUXLESS







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

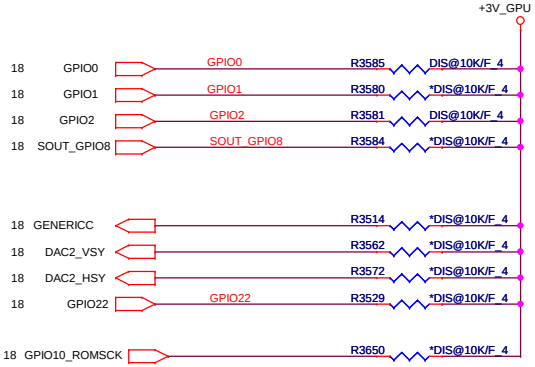
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

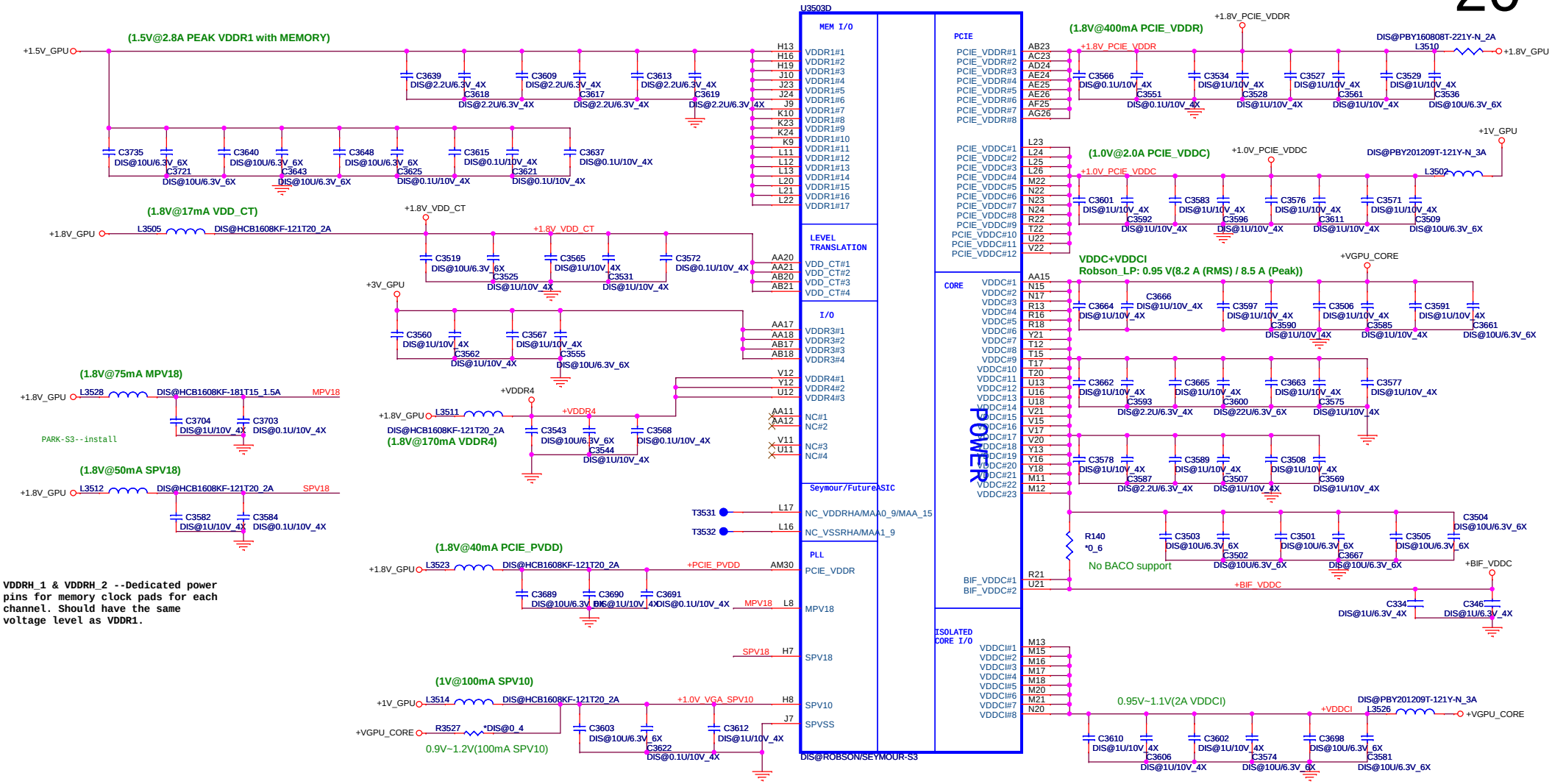
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	ROBSON_XT GND / LVDS/ Straps	1C
Date: Tuesday, April 19, 2011	Sheet 19 of 53	

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

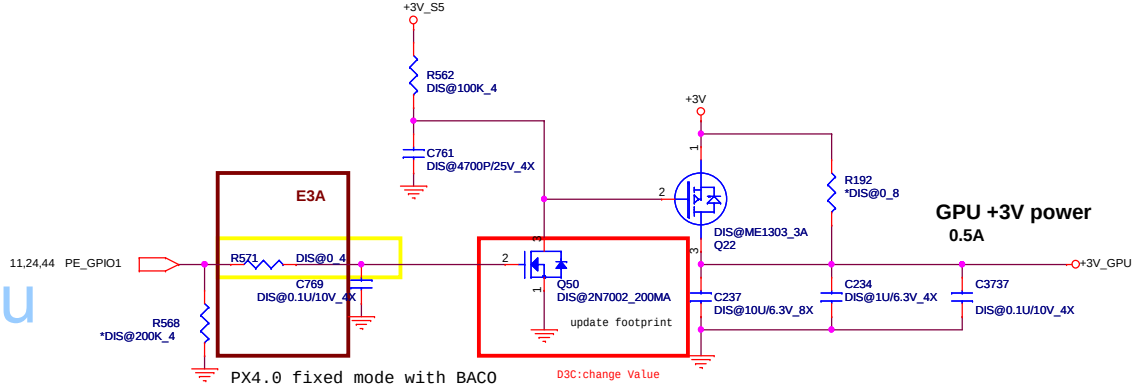


VDDRH_1 & VDDRH_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.

VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

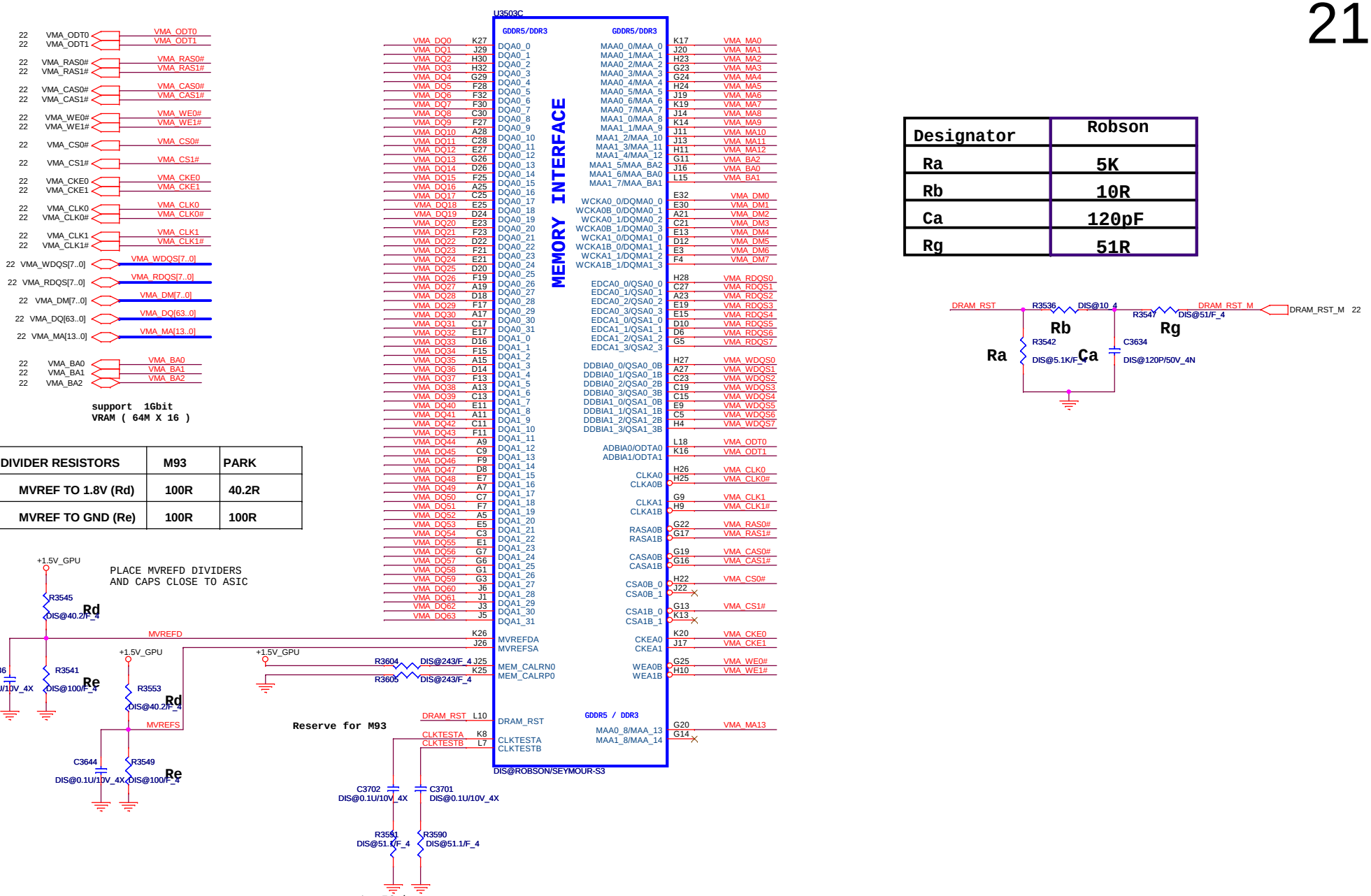
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%



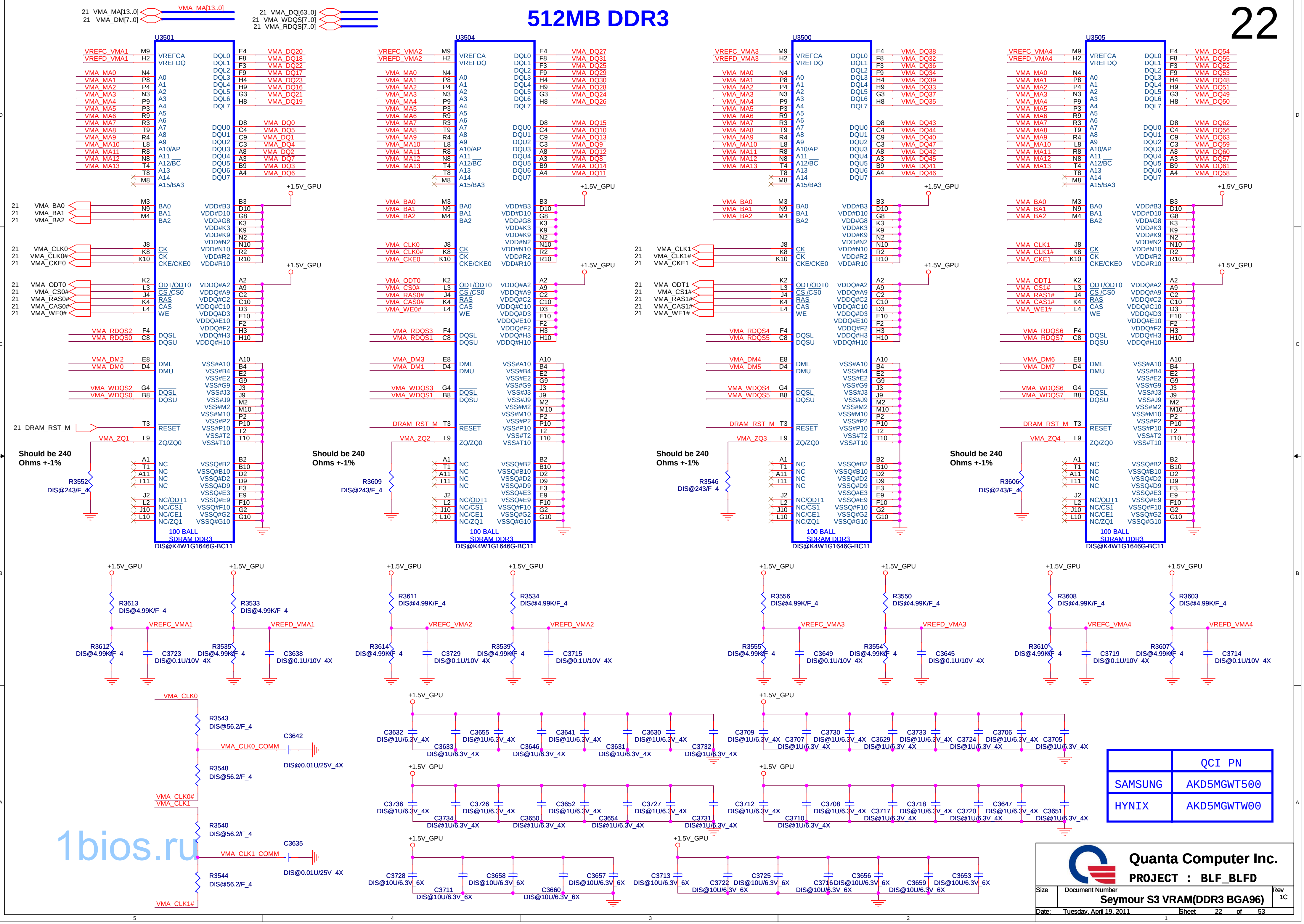
Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	ROBSON_Power_and_NC	1C
Date: Tuesday, April 19, 2011	Sheet 20 of 53	



Quanta Computer Inc.	
PROJECT : BLF_BLFD	
Size	Document Number: ROBSON/MEM_Interface — Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 21 of 53

512MB DDR3



	QCI PN
SAMSUNG	AKD5MGWT500
HYNIX	AKD5MGWTW00

Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	Seymour S3 VRAM(DDR3 BGA96)	1C

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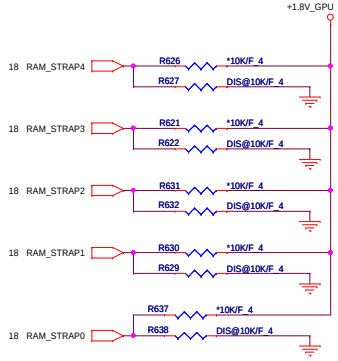
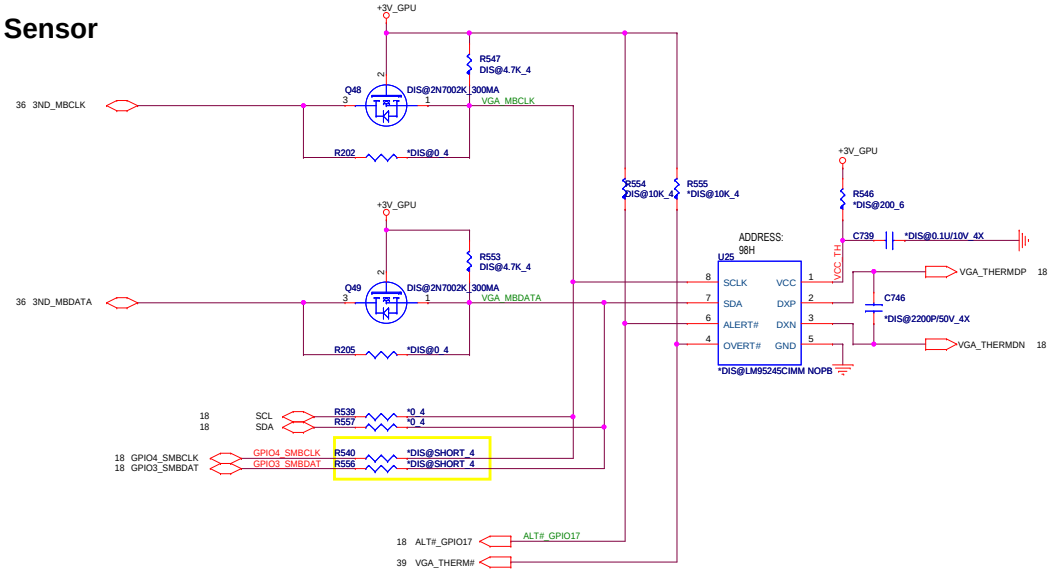
VRAM Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3	RAM_STRAP2	RAM_STRAP1	RAM_STRAP0	RAM_STRAP4	
				DVPDATA_3	DVPDATA_2	DVPDATA_1	DVPDATA_0	15"	14"
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW02 (64M*16-1Gb)	512MB	0	1	0	0	0	1
	H5TQ2G63BFR-11C	AKD5MGWTW00 (128M*16-2Gb)	1GB	0	0	0	0	0	1
Samsung	K4W1G1646G-BC11	AKD5EGGT500 (64M*16-1Gb)	512MB	0	1	0	1	0	1
	K4W2G1646C-HC11	AKD5MGWT500 (128M*16-2Gb)	1GB	0	0	0	1	0	1



Thermal Sensor



Quanta Computer Inc.
PROJECT : BLF_BLFD
Size | Document Number: Blank | Rev: 1C
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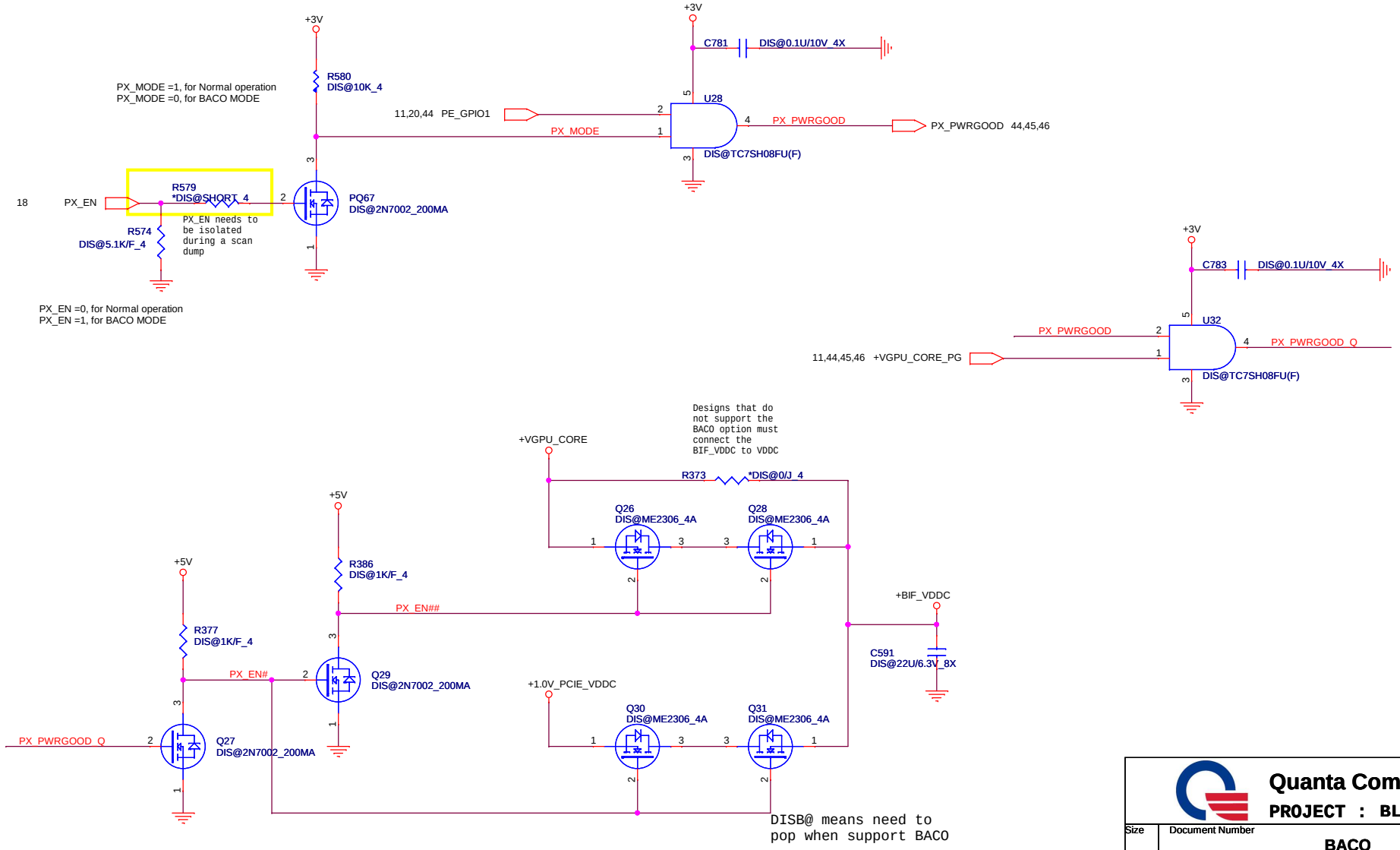

Quanta Computer Inc.		
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Quanta Computer Inc.		
PROJECT : BLF_BLFD		
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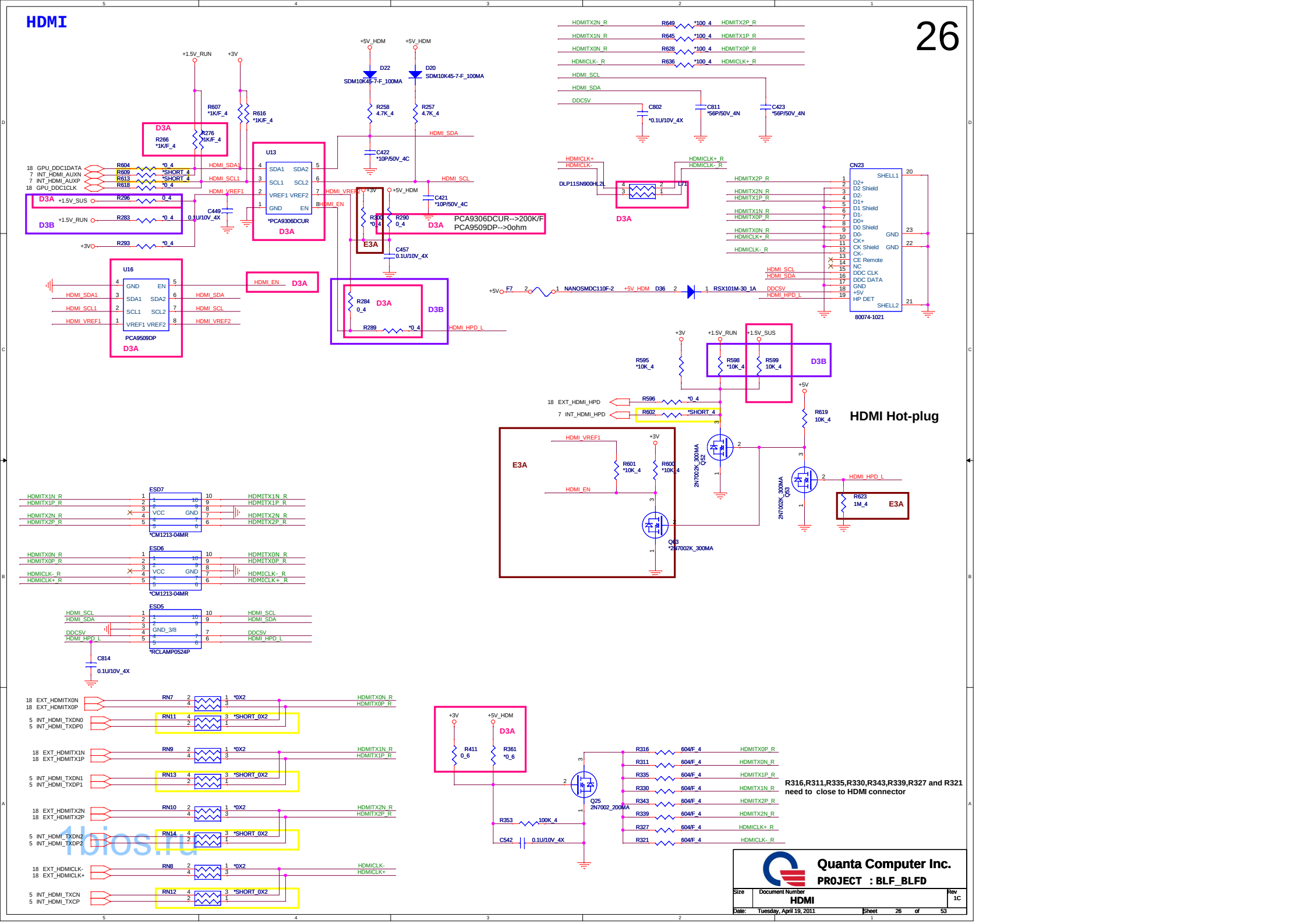
HDMI



Quanta Computer Inc.
PROJECT : BLF_BLFD

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	HDMI	1C
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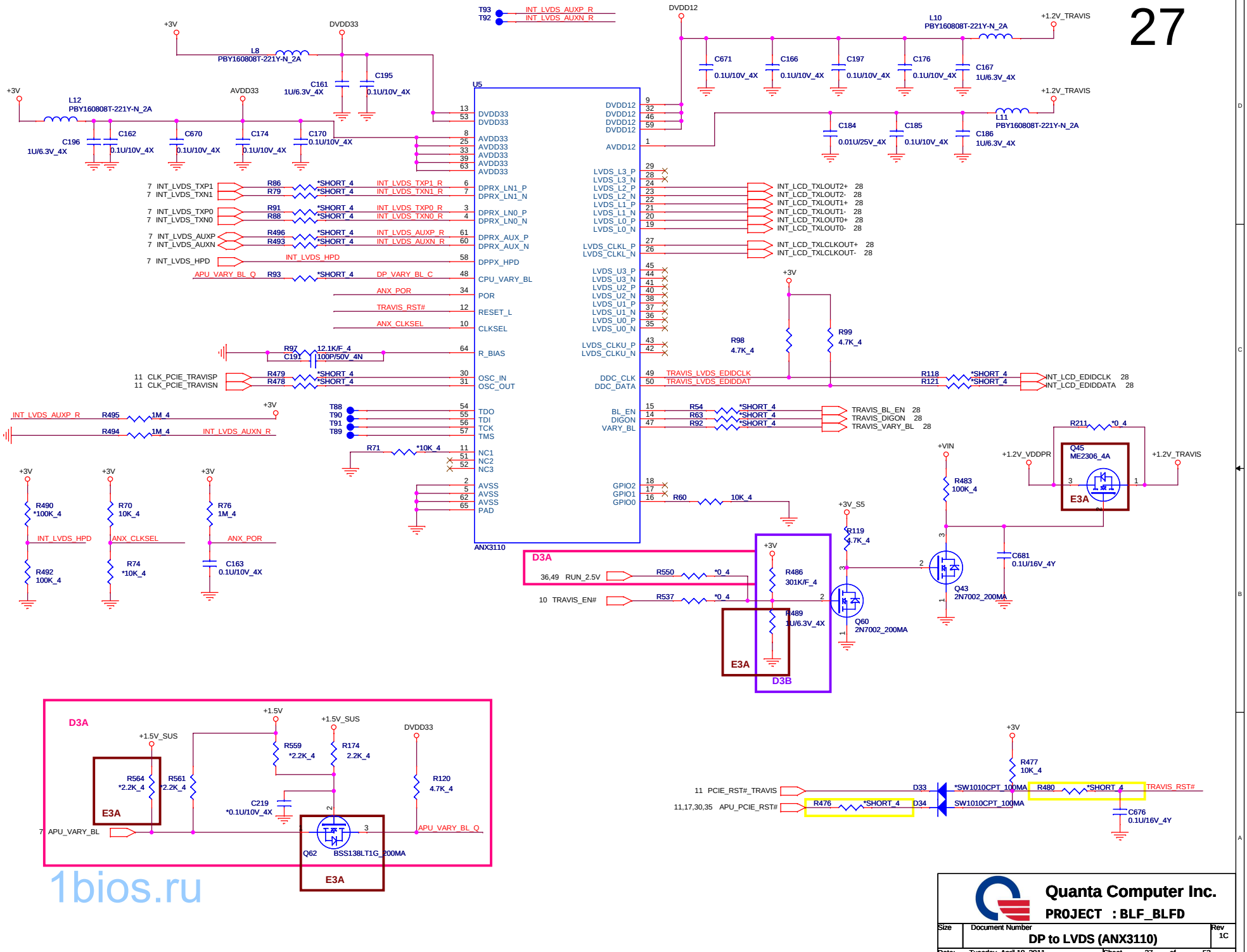
U5
ANX3110
DVDD33
AVDD33
DVDD12
AVDD12
+3V
+1.2V_TRAVIS
+1.5V
+1.5V_SUS
+3V_S5
+VIN
+1.2V_VDDPR
D3A
D3B
E3A
Q43 2N7002_200MA
Q45 ME2306_4A
Q60 2N7002_200MA
Q62 BSS138LT1G_200MA
INT_LVDS_AUXP_R
INT_LVDS_AUXN_R
INT_LVDS_TXP1_R
INT_LVDS_TXN1_R
INT_LVDS_TXP0_R
INT_LVDS_TXN0_R
INT_LVDS_AUXP_R
INT_LVDS_AUXN_R
INT_LVDS_HPD
APU_VARY_BL_Q
DP_VARY_BL_C
ANX_POR
TRAVIS_RST#
ANX_CLKSEL
INT_LCD_TXLOUT2+
INT_LCD_TXLOUT2-
INT_LCD_TXLOUT1+
INT_LCD_TXLOUT1-
INT_LCD_TXLOUT0+
INT_LCD_TXLOUT0-
INT_LCD_TXLCLKOUT+
INT_LCD_TXLCLKOUT-
TRAVIS_LVDS_EDIDCLK
TRAVIS_LVDS_EDIDDAT
INT_LCD_EDIDCLK
INT_LCD_EDIDDATA
TRAVIS_BL_EN
TRAVIS_DIGON
TRAVIS_VARY_BL
CLK_PCIE_TRAVISP
CLK_PCIE_TRAVISN
RUN_2.5V
TRAVIS_EN#
APU_VARY_BL
PCIE_RST#_TRAVIS
APU_PCIE_RST#
SW1010CPT_100MA
SW1010CPT_100MA
R99 4.7K_4
R98 4.7K_4
R119 4.7K_4
R483 100K_4
R486 301K/F_4
R489 1U/6.3V_4X
R211 *0_4
R550 *0_4
R537 *0_4
R60 10K_4
R71 *10K_4
R477 10K_4
R480 *SHORT_4
R476 *SHORT_4
R559 *2.2K_4
R174 2.2K_4
R564 *2.2K_4
R561 *2.2K_4
C219 *0.1U/10V_4X
R120 4.7K_4
C681 0.1U/16V_4Y
C676 0.1U/16V_4Y
R490 *100K_4
R492 100K_4
R70 10K_4
R74 *10K_4
R76 1M_4
C163 0.1U/10V_4X
R495 1M_4
R494 1M_4
Quanta Computer Inc.
PROJECT : BLF_BLFD
DP to LVDS (ANX3110)
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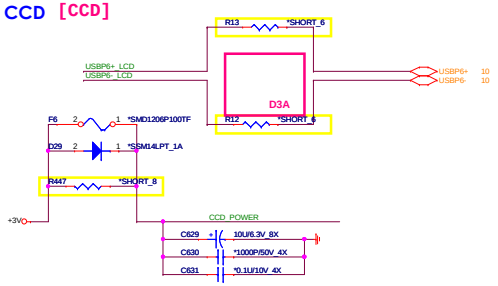
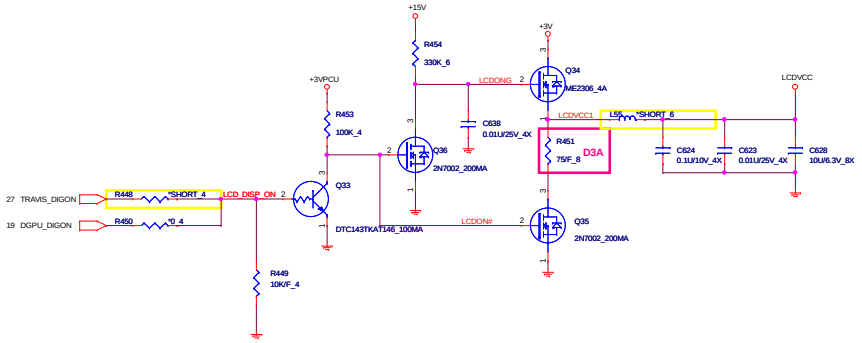
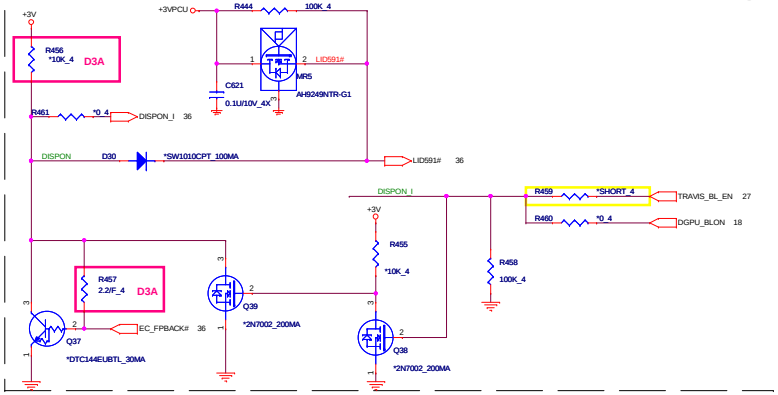
CCD [CCD]



LCD POWER SWITCH [LDS]

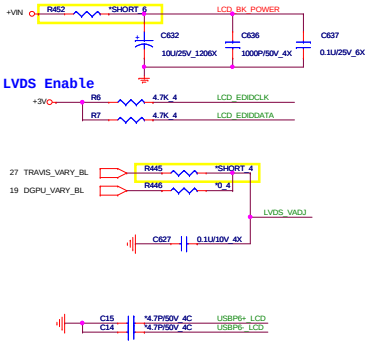


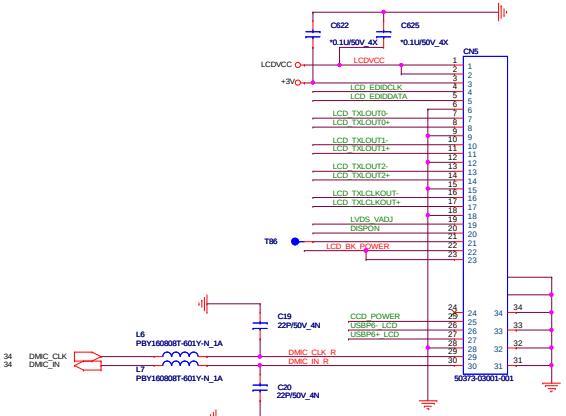
HALL SENSOR&BACK LIGHT SWITCH [HSR]

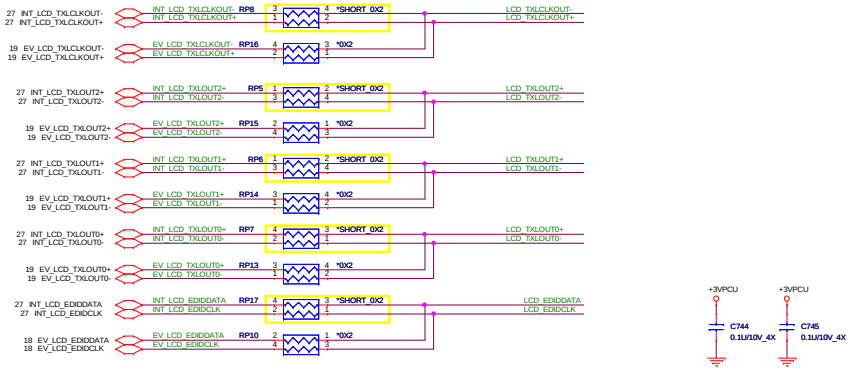


[LDS]

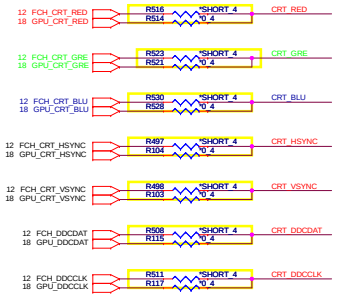
LCD Panel Module

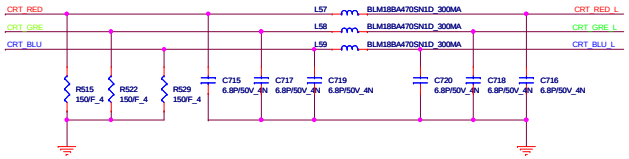


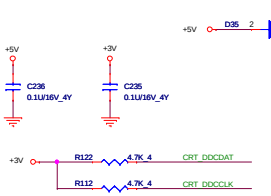


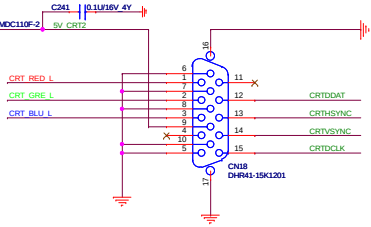


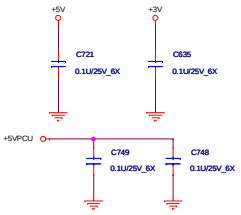
CRT [CRT]

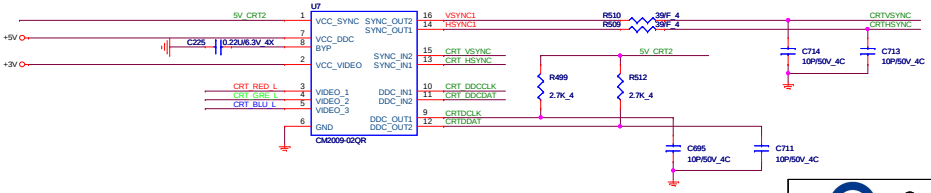












Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	LVDS/CCD/CRT/USB	1C
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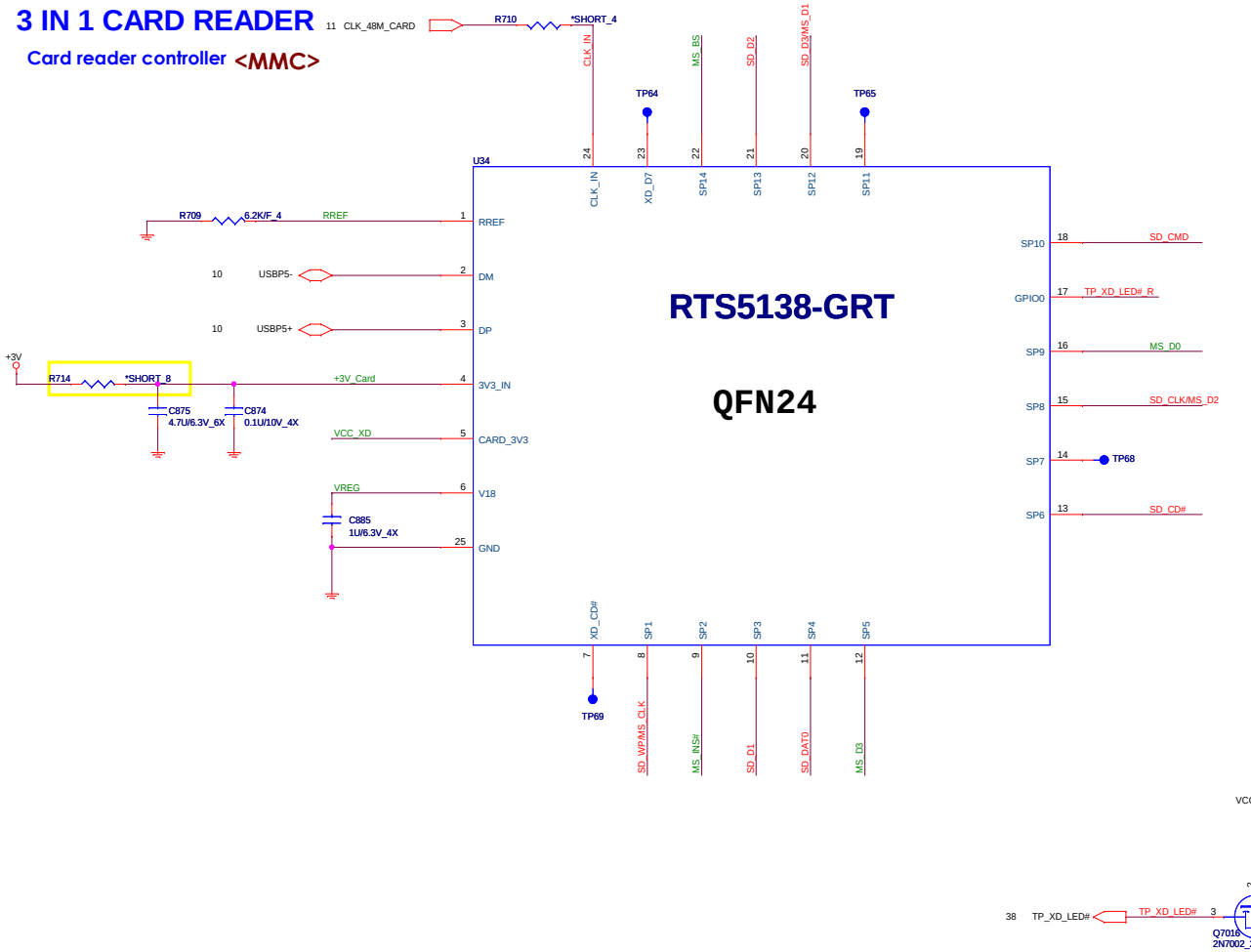
3 IN 1 CARD READER

Card reader controller <MMC>



3 IN 1 CARD READER

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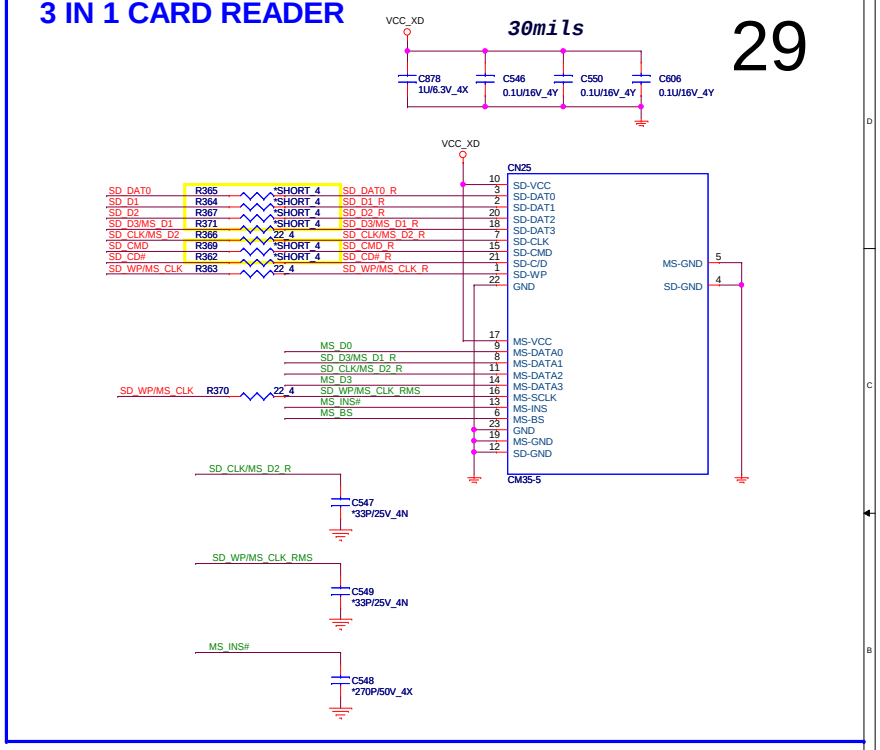

Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	RTS5138 (Card Reader)	1C
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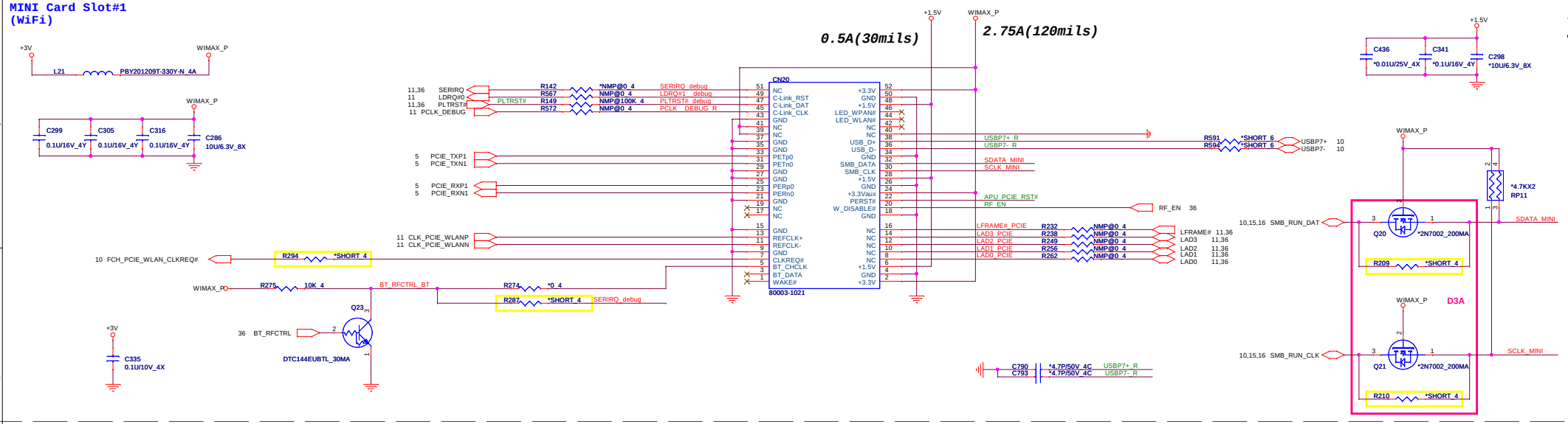
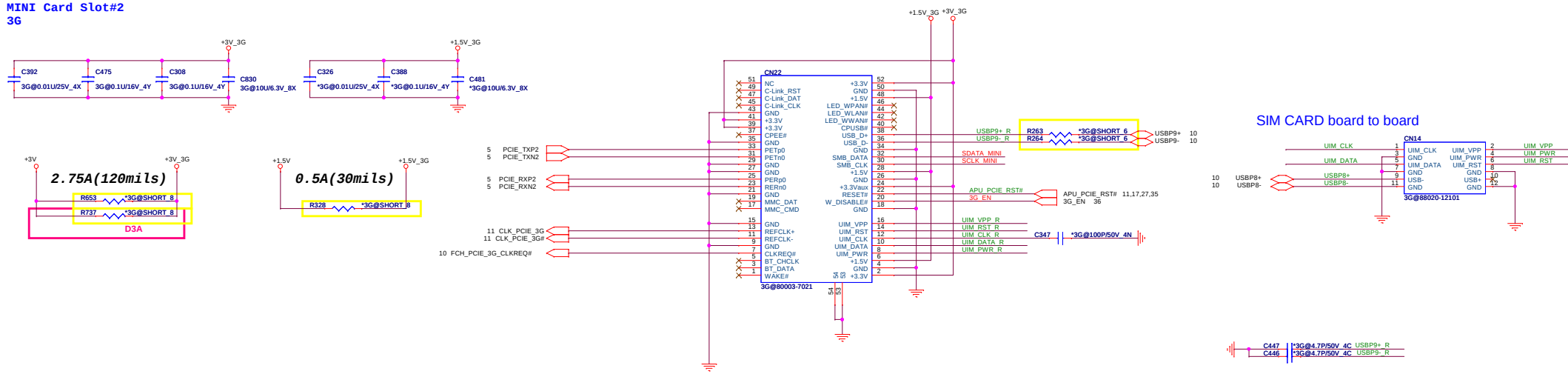
MINI Card Slot#1 (WiFi)



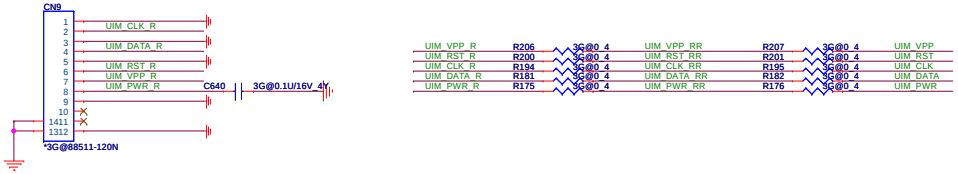
MINI Card Slot#2 3G



SIM CARD board to board

C447 *3G@4.7P/50V_4C
C446 *3G@4.7P/50V_4C
C634 *3G@4.7P/50V_4C
C633 *3G@4.7P/50V_4C

3G CONN



UIM_VPP_R	R206	3G@0_4	UIM_VPP_RR	R207	3G@0_4	UIM_VPP
UIM_RST_R	R200	3G@0_4	UIM_RST_RR	R201	3G@0_4	UIM_RST
UIM_CLK_R	R194	3G@0_4	UIM_CLK_RR	R195	3G@0_4	UIM_CLK
UIM_DATA_R	R181	3G@0_4	UIM_DATA_RR	R182	3G@0_4	UIM_DATA
UIM_PWR_R	R175	3G@0_4	UIM_PWR_RR	R176	3G@0_4	UIM_PWR

Quanta Computer Inc.			
PROJECT : BLF_BLFD			
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	MINI Card(WLAN/3G/SIM)		1C
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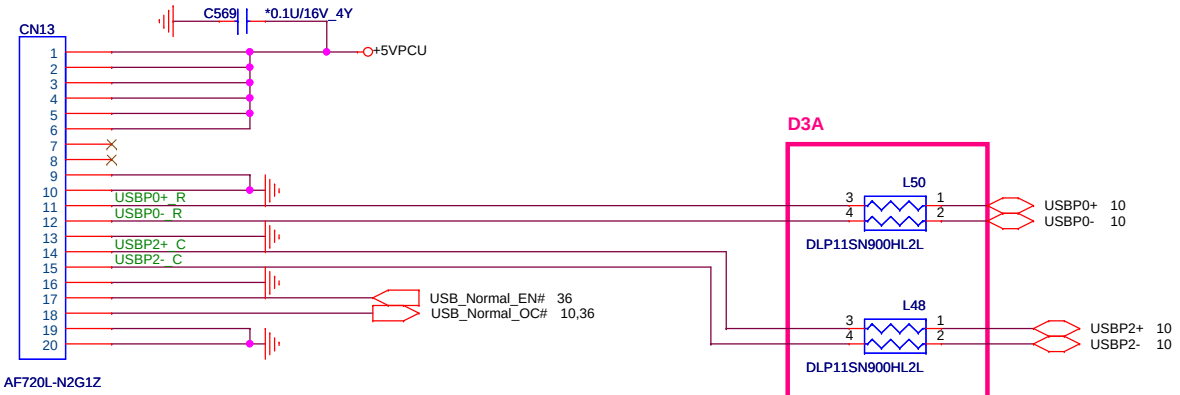
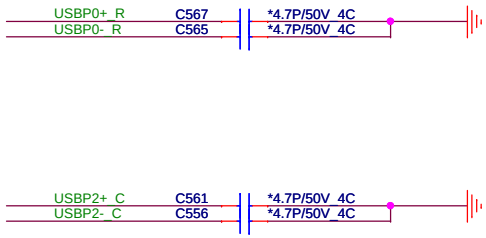
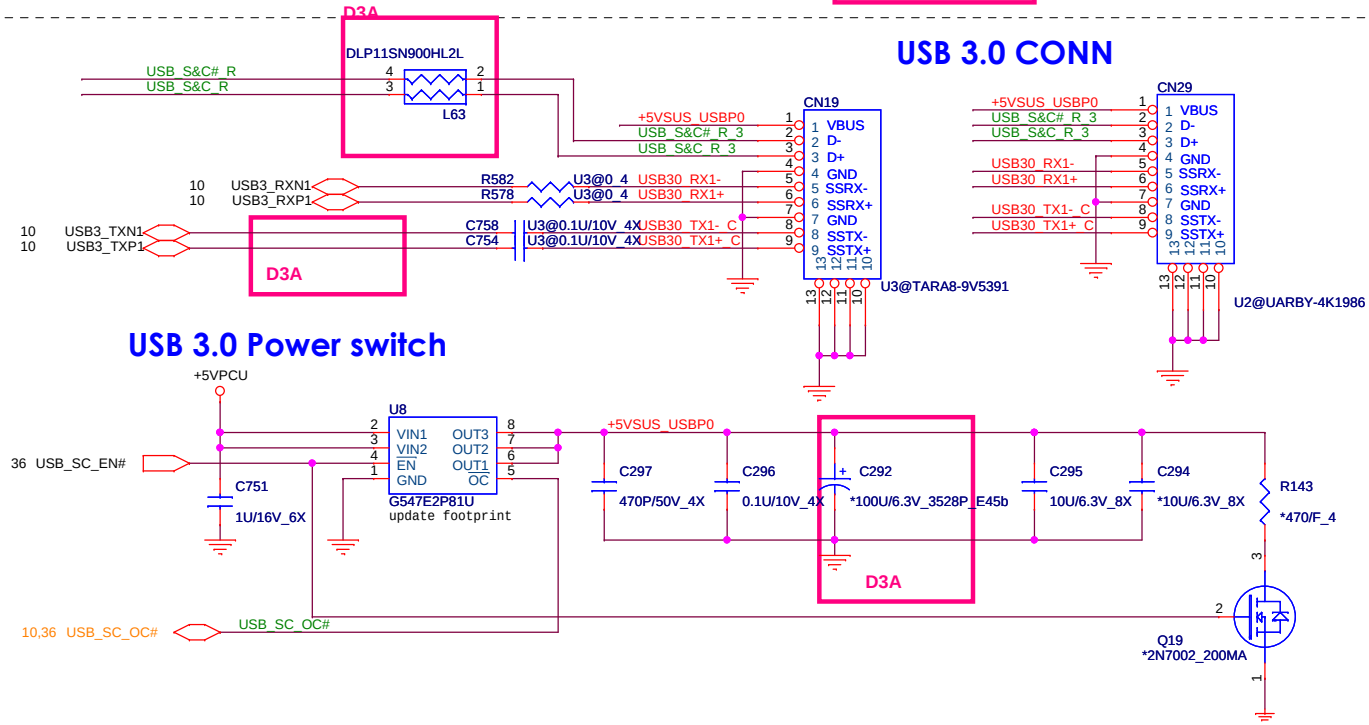
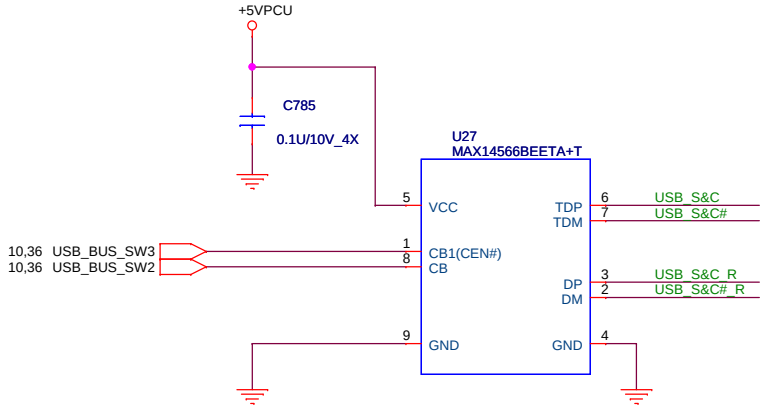
USB board







USB Sleep & Charge MAXIM solution



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

10 USB_S&C# → USB_S&C#
10 USB_S&C → USB_S&C

Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	USB2.0X1+USB3.0X1	1C
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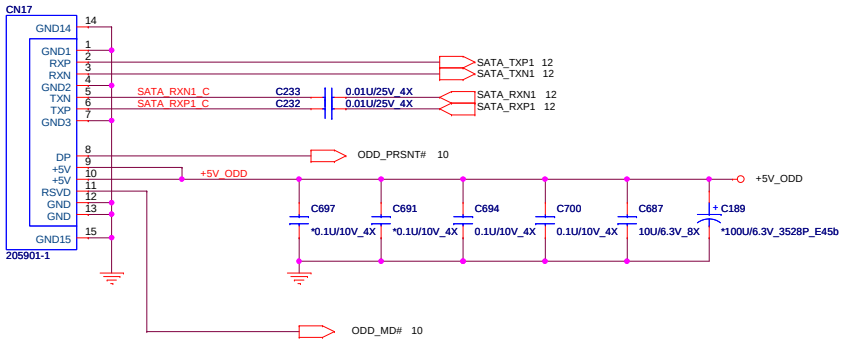
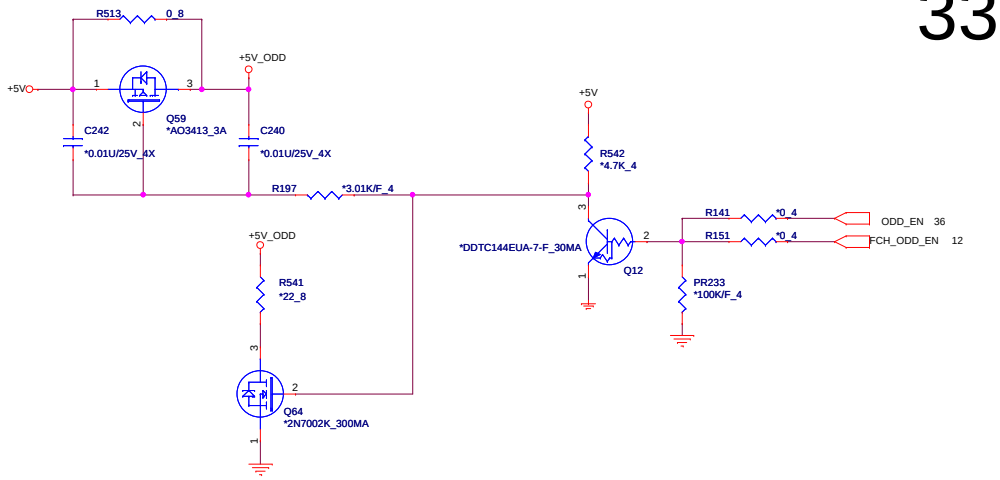
SATA ODD

[ODD]



ODD Zero power .



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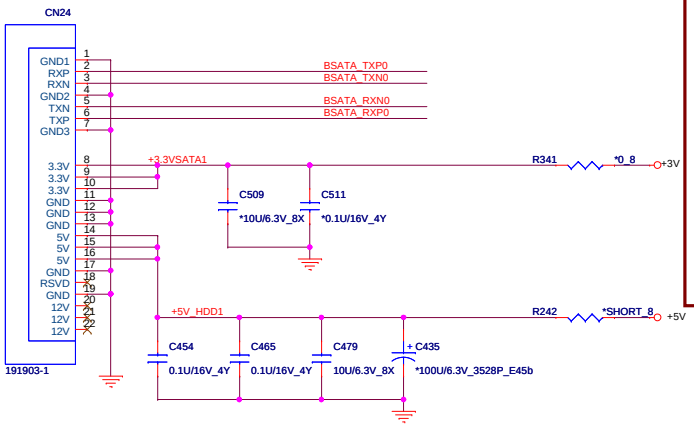
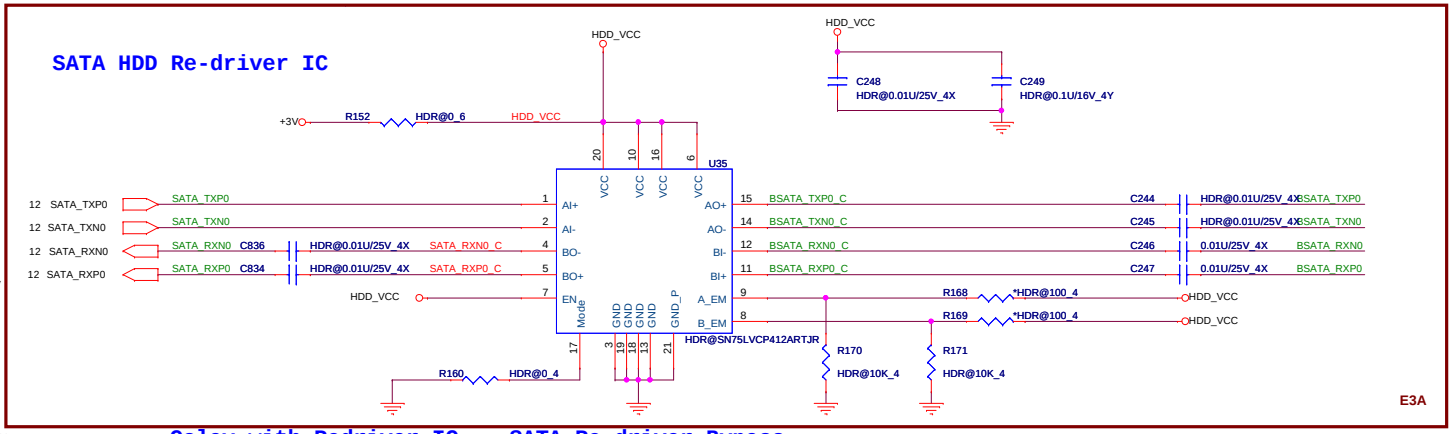
SATA HDD

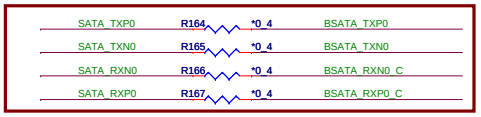
[HDD]



SATA HDD Re-driver IC



Colay with Redriver IC SATA Re-driver Bypass



Quanta Computer Inc.		
PROJECT : BLF_BLFD		
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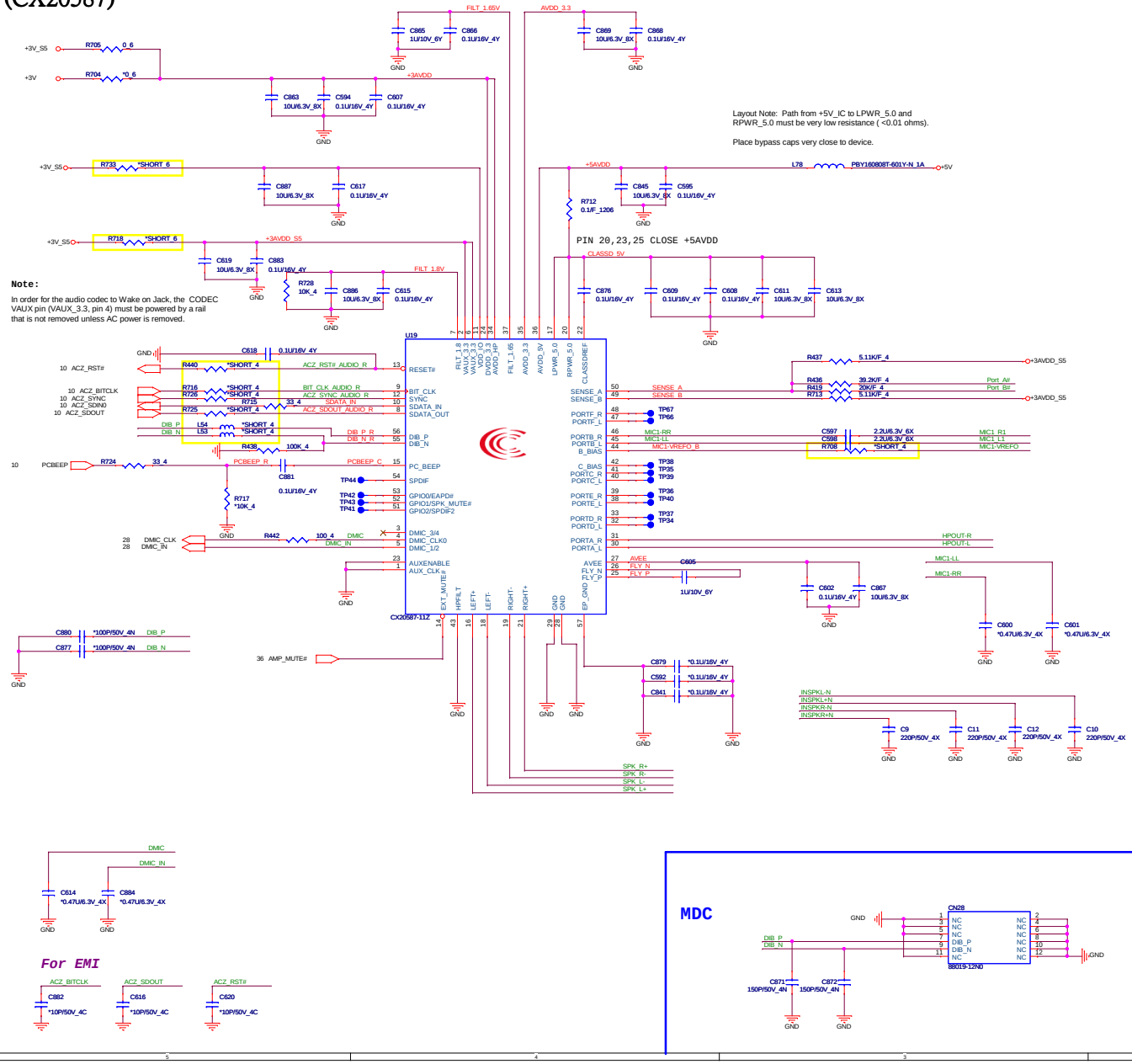
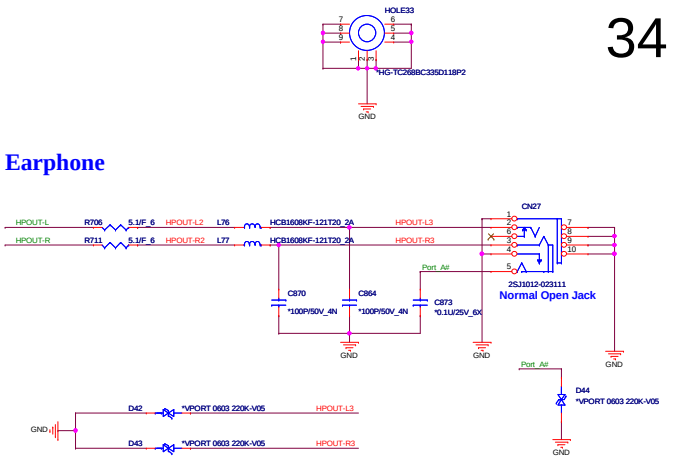
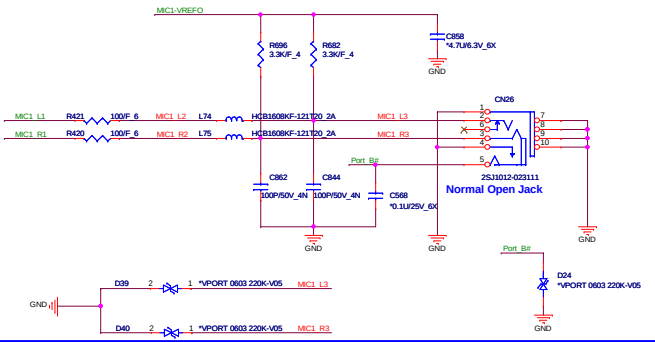
Codec (CX20587)



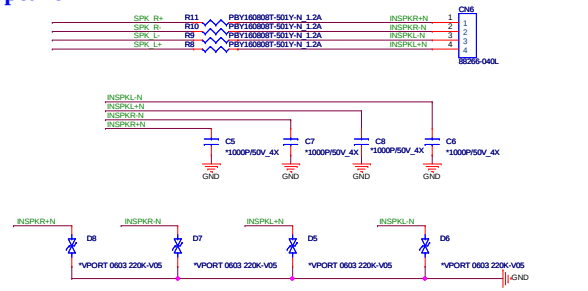
Earphone



External MIC



Internal Speaker



MDC

Quanta Computer Inc.			
PROJECT : BLF_BLFD			
Size	Document Number		Rev
	Audio(CX20587)/MDC		1C
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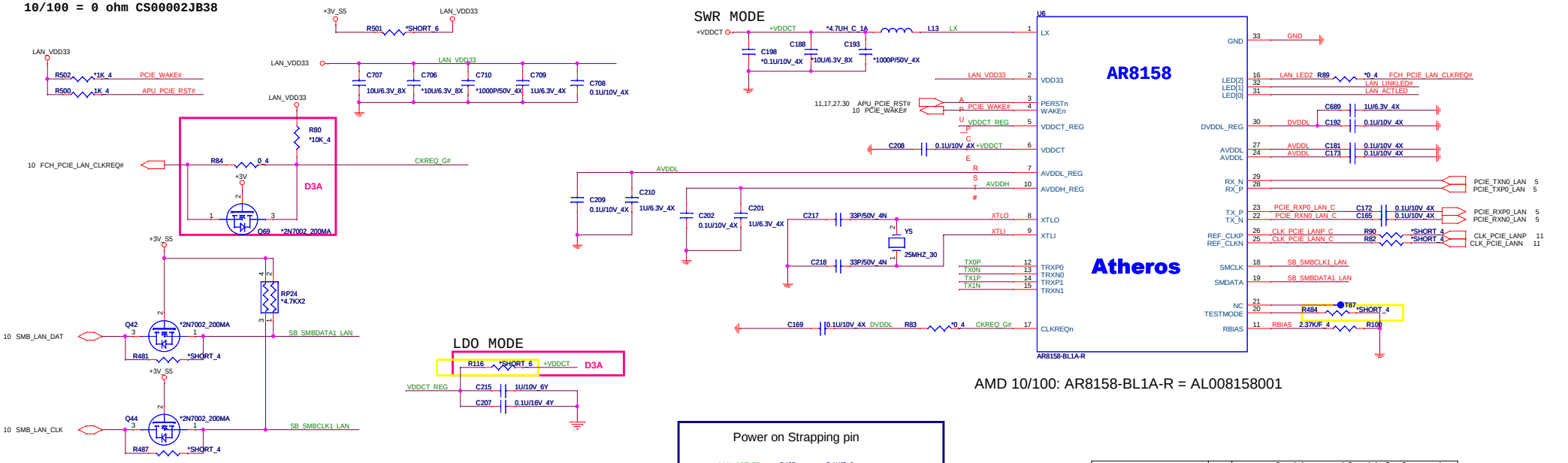
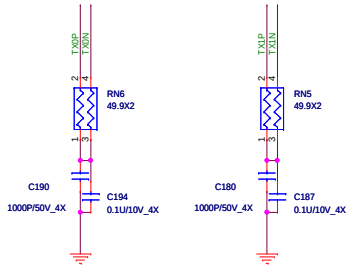
Atheros Lan AR8158

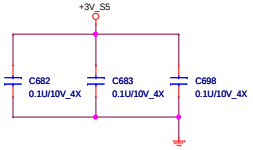
10/100 = 0 ohm CS00002JB38



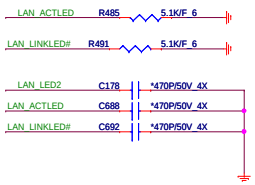
AMD 10/100: AR8158-BL1A-R = AL008158001

PLACE NEAR LAN IC SIDE



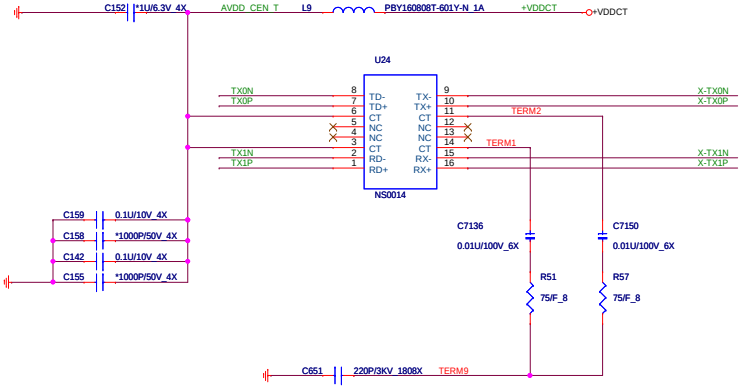


Power on Strapping pin

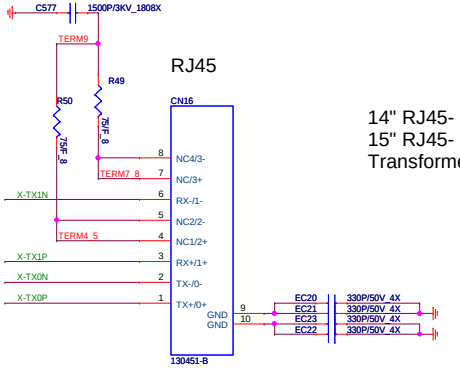


LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low

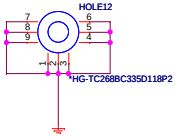
TRANSFORMER



RJ45



14" RJ45- DFTJ08FR164
15" RJ45- DFTJ08FR169
Transformer- DB0EL5LAN02



Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Atheros LAN(AR8158)	1C
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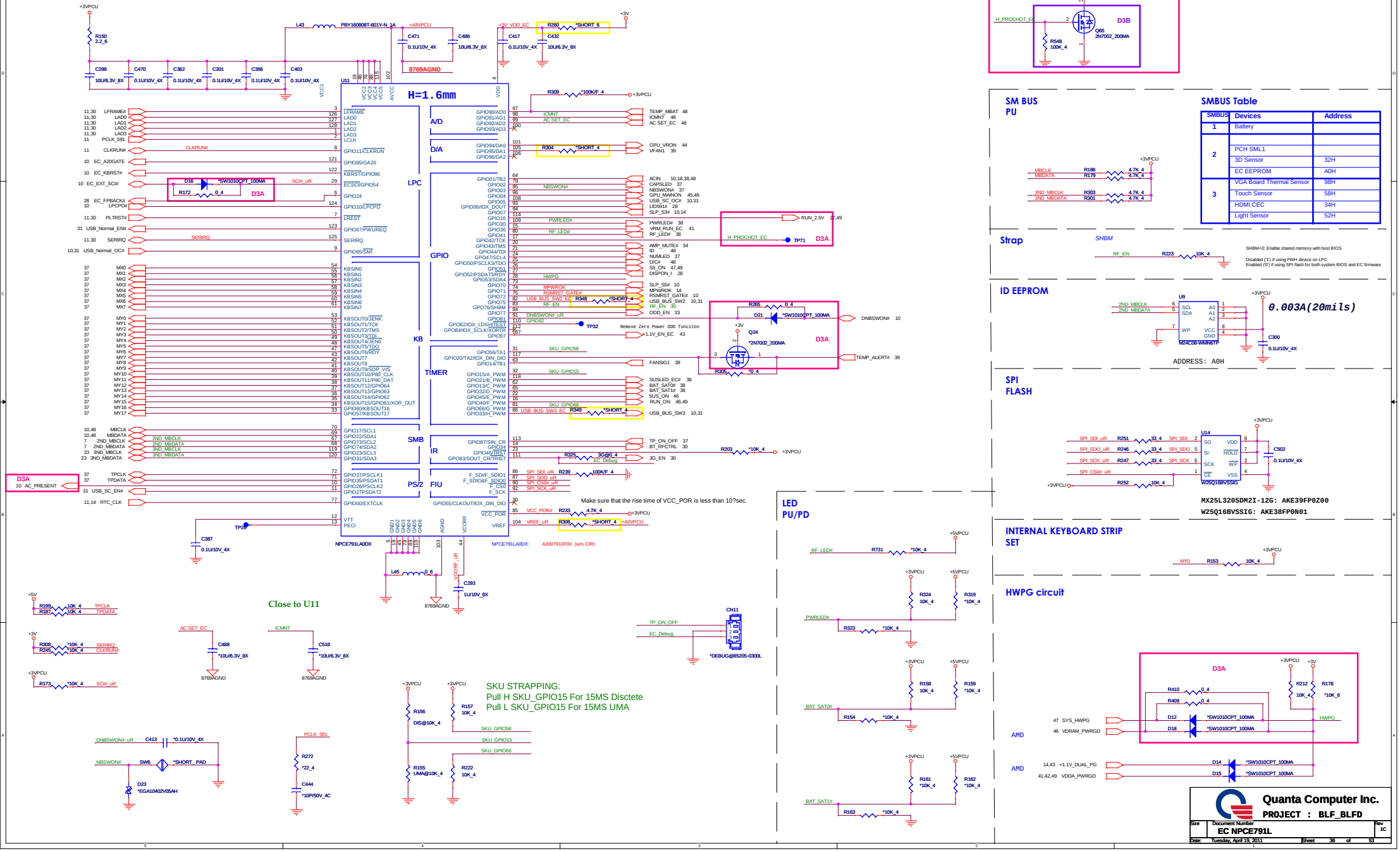
H=1.6mm
LPC
A/D
D/A
GPIO
KB
TIMER
SMB
IR
PS/2
FIU
SM BUS PU
SMBUS Table
SMBUS | Devices | Address
1 | Battery |
2 | PCH SML1 |
2 | 3D Sensor | 32H
2 | EC EEPROM | A0H
3 | VGA Board Thermal Sensor | 98H
3 | Touch Sensor | 58H
3 | HDMI CEC | 34H
3 | Light Sensor | 52H
Strap
SHBM
SHBM=0: Enable shared memory with host BIOS
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
ID EEPROM
0.003A(20mils)
ADDRESS: A0H
SPI FLASH
MX25L3205DM2I-12G: AKE39FP0Z00
W25Q16BVSSIG: AKE38FP0N01
INTERNAL KEYBOARD STRIP SET
HWPG circuit
LED PU/PD
Close to U11
SKU STRAPPING:
Pull H SKU_GPIO15 For 15MS Disctete
Pull L SKU_GPIO15 For 15MS UMA
Make sure that the rise time of VCC_POR is less than 10?sec.
Quanta Computer Inc.
PROJECT : BLF_BLFD
EC NPCE791L
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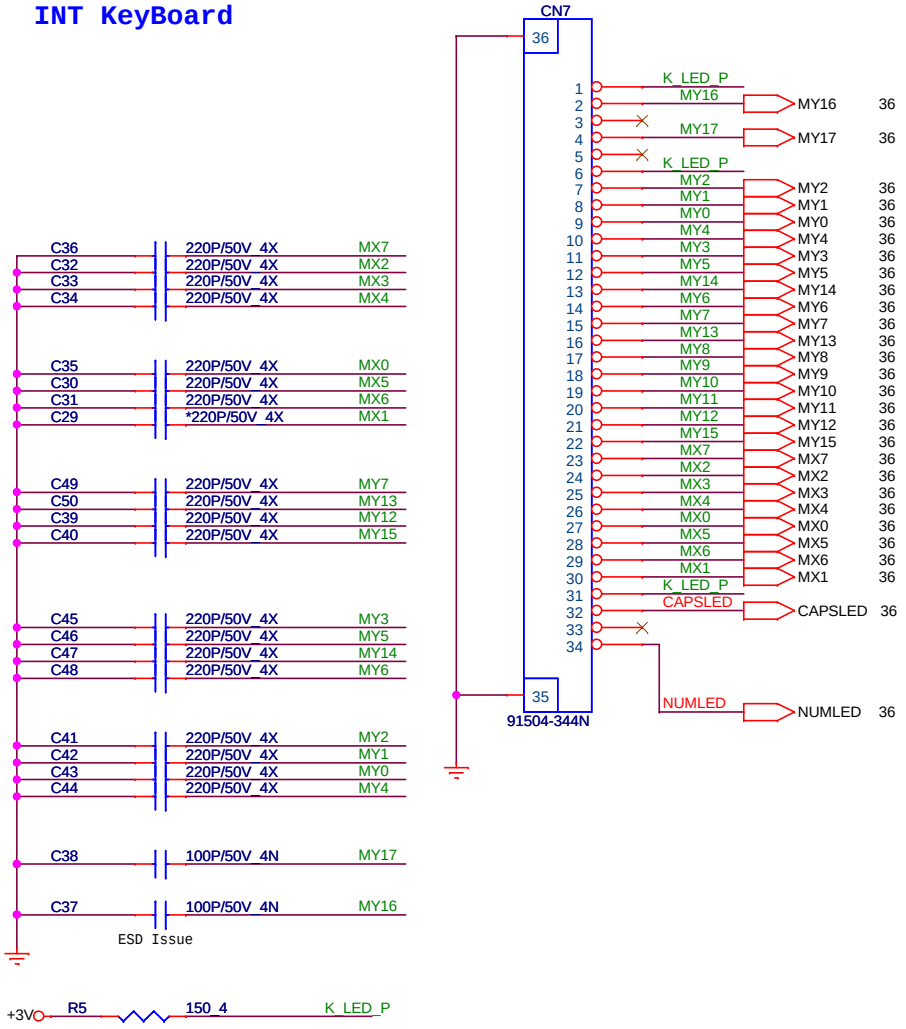
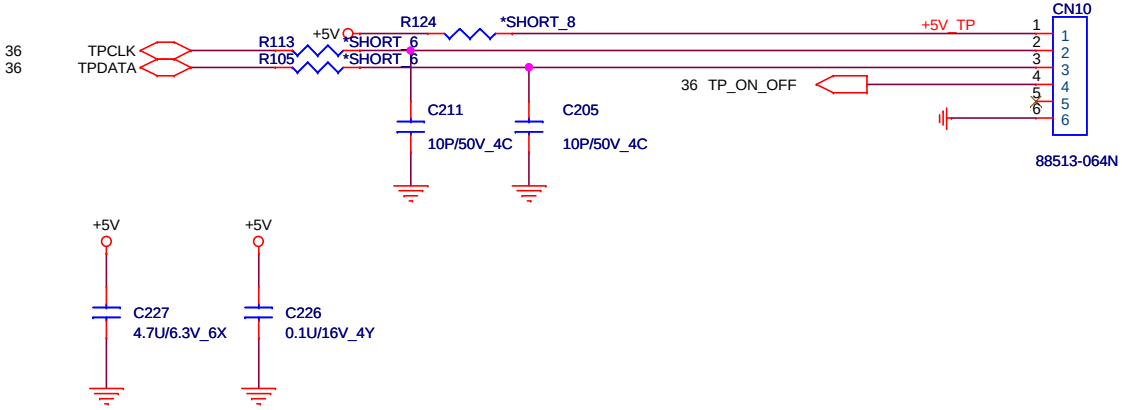
KEY BOARD Connector

INT KeyBoard

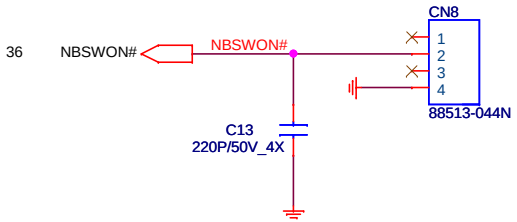


TOUCH PAD BOARD

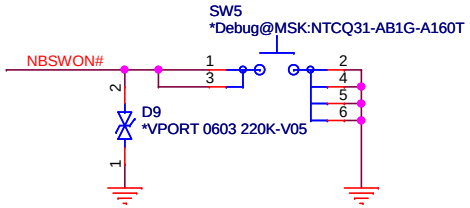
37



Power Board (UIF)



Power Switch (debug only)



Quanta Computer Inc.

PROJECT : BLF_BLFD

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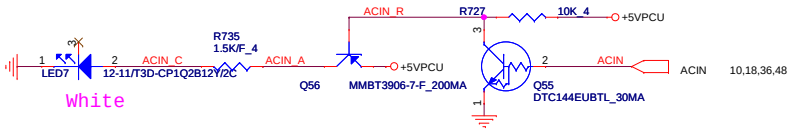
LED

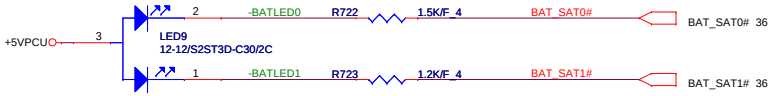
AC-IN



White

BATERRY

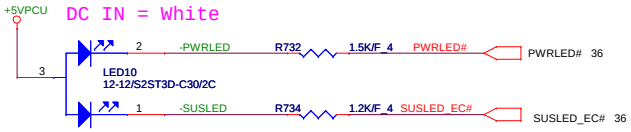
Full Charge = White



Charging = Orange

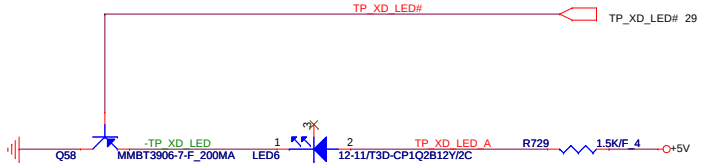
POWER

DC IN = White



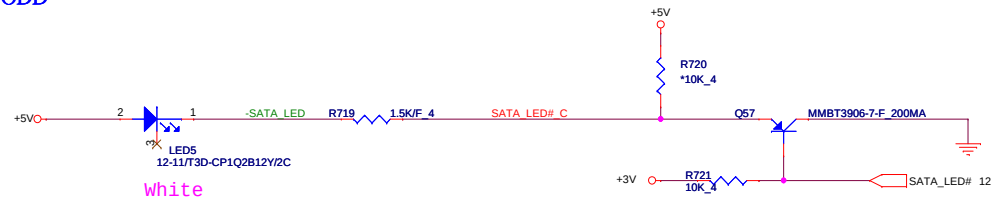
S3 Mode = Orange

CARDREADER



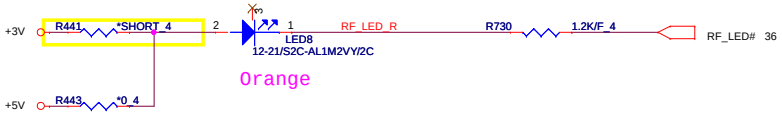
White

HDD/ODD



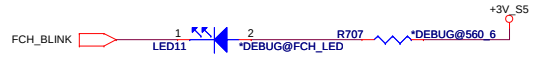
White

RF LED



Orange

When ON, means in S0
When BLINK, means in S3
When OFF, means in S5



Orange

Quanta Computer Inc.
PROJECT : BLF_BLFD

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	LED	1C

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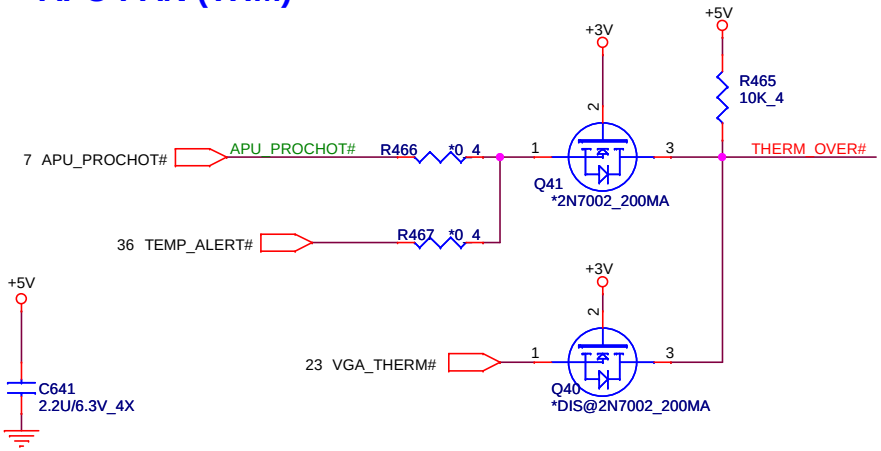
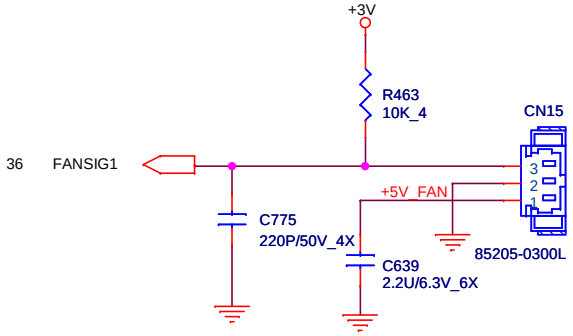
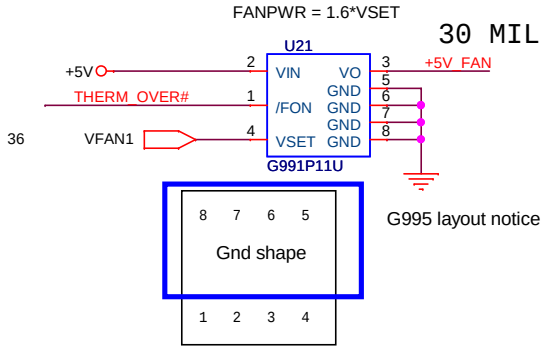
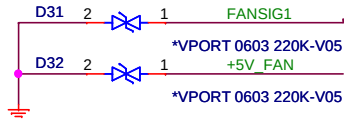
APU FAN (THM)









Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	APU FAN	1C
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Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: BLANK	Rev: 1C
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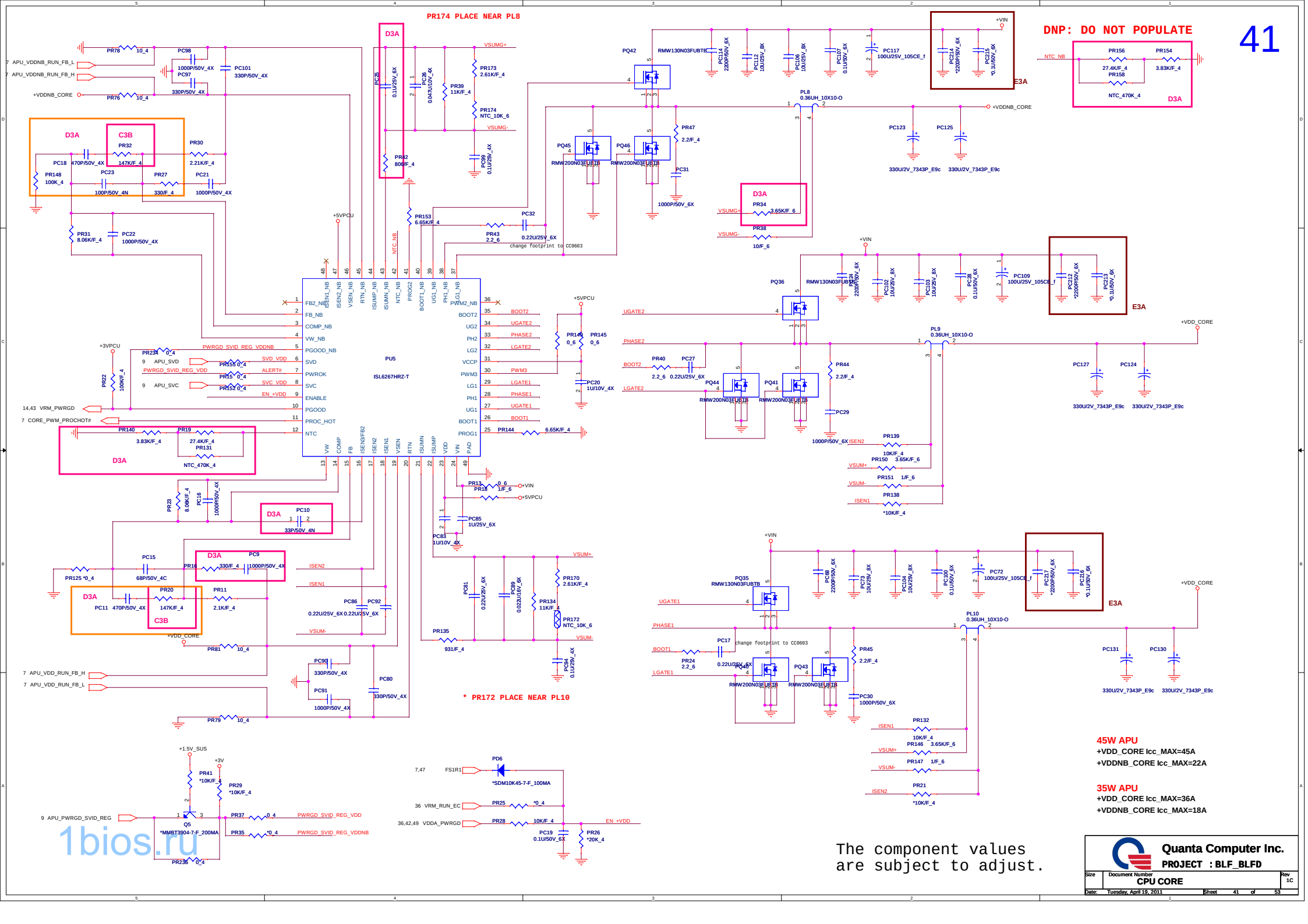
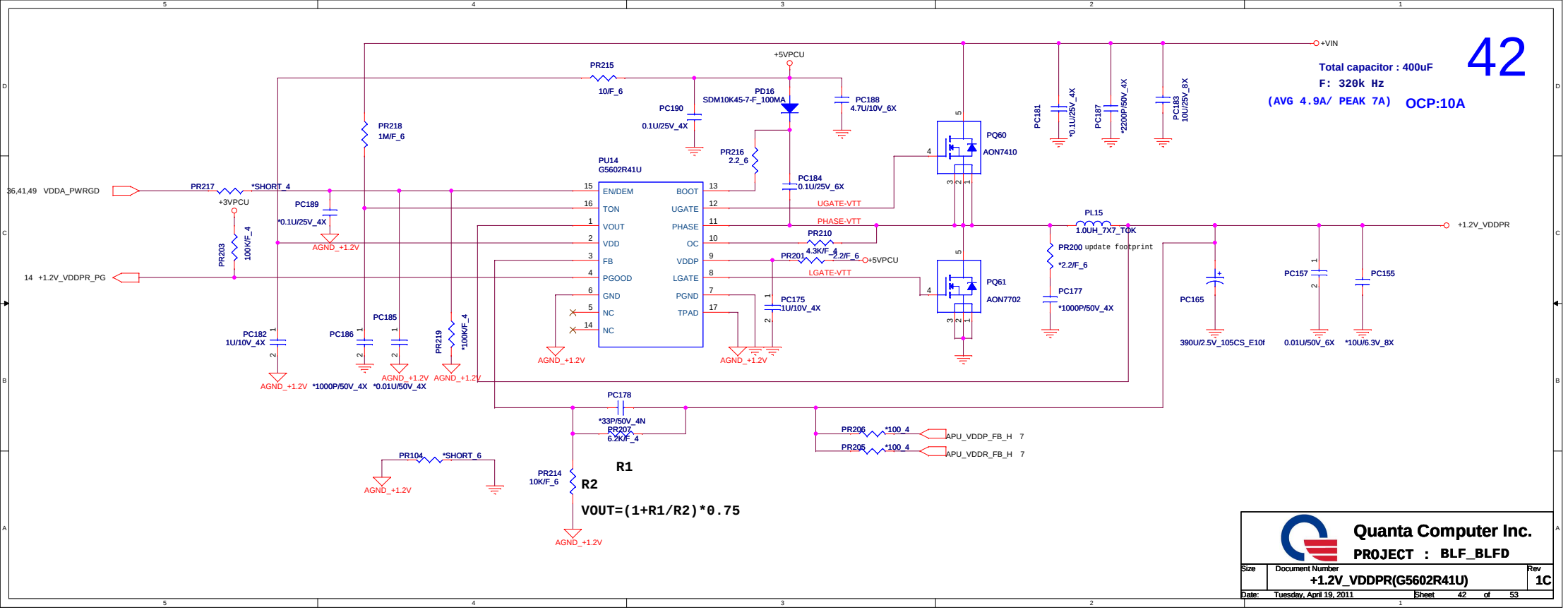

PR174 PLACE NEAR PL8
DNP: DO NOT POPULATE
41
PU5
ISL6267HRZ-T
* PR172 PLACE NEAR PL10
45W APU
+VDD_CORE Icc_MAX=45A
+VDDNB_CORE Icc_MAX=22A
35W APU
+VDD_CORE Icc_MAX=36A
+VDDNB_CORE Icc_MAX=18A
The component values are subject to adjust.
Quanta Computer Inc.
PROJECT : BLF_BLFD
CPU CORE
Tuesday, April 19, 2011
1bios.ru


42
Total capacitor : 400uF
F: 320k Hz
(AVG 4.9A/ PEAK 7A) OCP:10A
+VIN
+5VPCU
PR215
10/F_6
PD16
SDM10K45-7-F_100MA
PC190
0.1U/25V_4X
PC188
4.7U/10V_6X
PR218
1M/F_6
PU14
G5602R41U
PR216
2.2_6
PC184
0.1U/25V_6X
PQ60
AON7410
PC181
*0.1U/25V_4X
PC187
*220P/50V_4X
PC183
10U/25V_8X
36,41,49 VDDA_PWRGD
PR217
*SHORT_4
+3VPCU
PC189
*0.1U/25V_4X
PR203
100K/F_4
AGND_+1.2V
EN/DEM
TON
VOUT
VDD
FB
PGOOD
GND
NC
NC
BOOT
UGATE
PHASE
OC
VDDP
LGATE
PGND
TPAD
UGATE-VTT
PHASE-VTT
PR210
4.3K/F_4
PR201
2.2/F_6
+5VPCU
LGATE-VTT
PC175
1U/10V_4X
PQ61
AON7702
PL15
1.0UH_7X7_T0K
+1.2V_VDDPR
PR200 update footprint
*2.2/F_6
PC177
*1000P/50V_4X
PC165
390U/2.5V_105CS_E10f
PC157
0.01U/50V_6X
PC155
*10U/6.3V_8X
14 +1.2V_VDDPR_PG
PC182
1U/10V_4X
PC186
PC185
*0.01U/50V_4X
PR219
*100K/F_4
AGND_+1.2V
*1000P/50V_4X
PC178
*33P/50V_4N
PR207
6.2K/F_4
PR206
*100_4
PR205
*100_4
APU_VDDP_FB_H 7
APU_VDDR_FB_H 7
PR104
*SHORT_6
PR214
10K/F_6
R1
R2
VOUT=(1+R1/R2)*0.75
Quanta Computer Inc.
PROJECT : BLF_BLFD
Size
Document Number
+1.2V_VDDPR(G5602R41U)
Rev
1C
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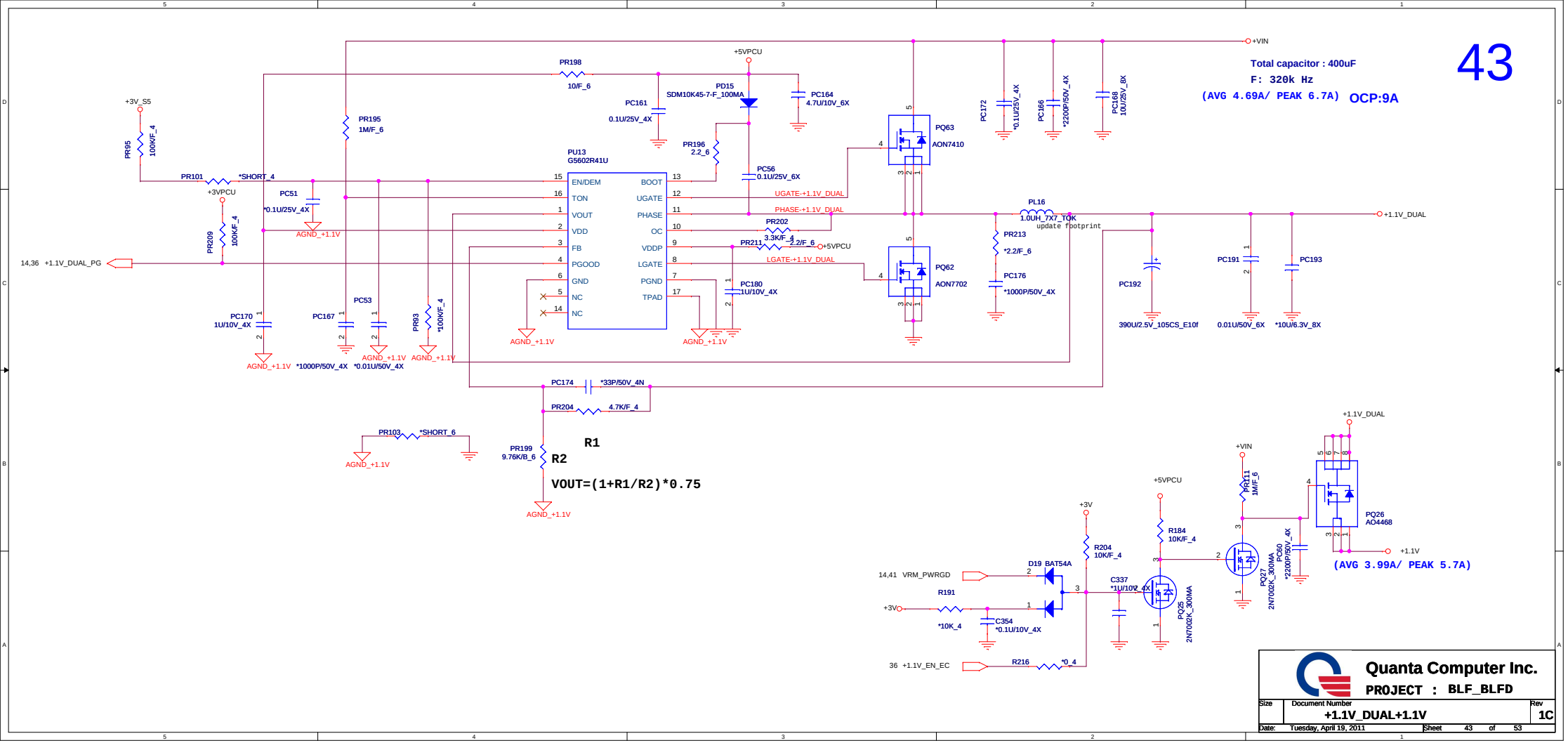
43
Total capacitor : 400uF
F: 320k Hz
(AVG 4.69A/ PEAK 6.7A) OCP:9A
+VIN
+5VPCU
+3V_S5
+3VPCU
PR198 10/F_6
PD15 SDM10K45-7-F_100MA
PC164 4.7U/10V_6X
PC161 0.1U/25V_4X
PR195 1M/F_6
PR95 100K/F_4
PR101 *SHORT_4
PR196 2.2_6
PC56 0.1U/25V_6X
PU13 G5602R41U
EN/DEM
TON
VOUT
VDD
FB
PGOOD
GND
NC
NC
BOOT
UGATE
PHASE
OC
VDDP
LGATE
PGND
TPAD
UGATE-+1.1V_DUAL
PHASE-+1.1V_DUAL
LGATE-+1.1V_DUAL
PQ63 AON7410
PQ62 AON7702
PC172 *0.1U/25V_4X
PC166 *2200P/50V_4X
PC168 10U/25V_8X
PL16 1.0UH_7X7_TOK update footprint
PR213 *2.2/F_6
PC176 *1000P/50V_4X
PC192 390U/2.5V_105CS_E10f
PC191 0.01U/50V_6X
PC193 *10U/6.3V_8X
+1.1V_DUAL
PR202 3.3K/F_4
PR211 2.2/F_6
PC180 1U/10V_4X
PR209 100K/F_4
PC51 *0.1U/25V_4X
PC53 *0.01U/50V_4X
PR93 *100K/F_4
PC170 1U/10V_4X
PC167 *1000P/50V_4X
14,36 +1.1V_DUAL_PG
AGND_+1.1V
PC174 *33P/50V_4N
PR204 4.7K/F_4
PR103 *SHORT_6
PR199 9.76K/B_6
R1
R2
VOUT=(1+R1/R2)*0.75
14,41 VRM_PWRGD
D19 BAT54A
R191 *10K_4
C354 *0.1U/10V_4X
R204 10K/F_4
C337 *1U/10V_4X
R184 10K/F_4
PQ25 2N7002K_300MA
36 +1.1V_EN_EC
R216 *0_4
PR211 1M/F_6
PQ27 2N7002K_300MA
PC60 *2200P/50V_4X
PQ26 AO4468
(AVG 3.99A/ PEAK 5.7A)
Quanta Computer Inc.
PROJECT : BLF_BLFD
Size
Document Number
+1.1V_DUAL+1.1V
Rev
1C
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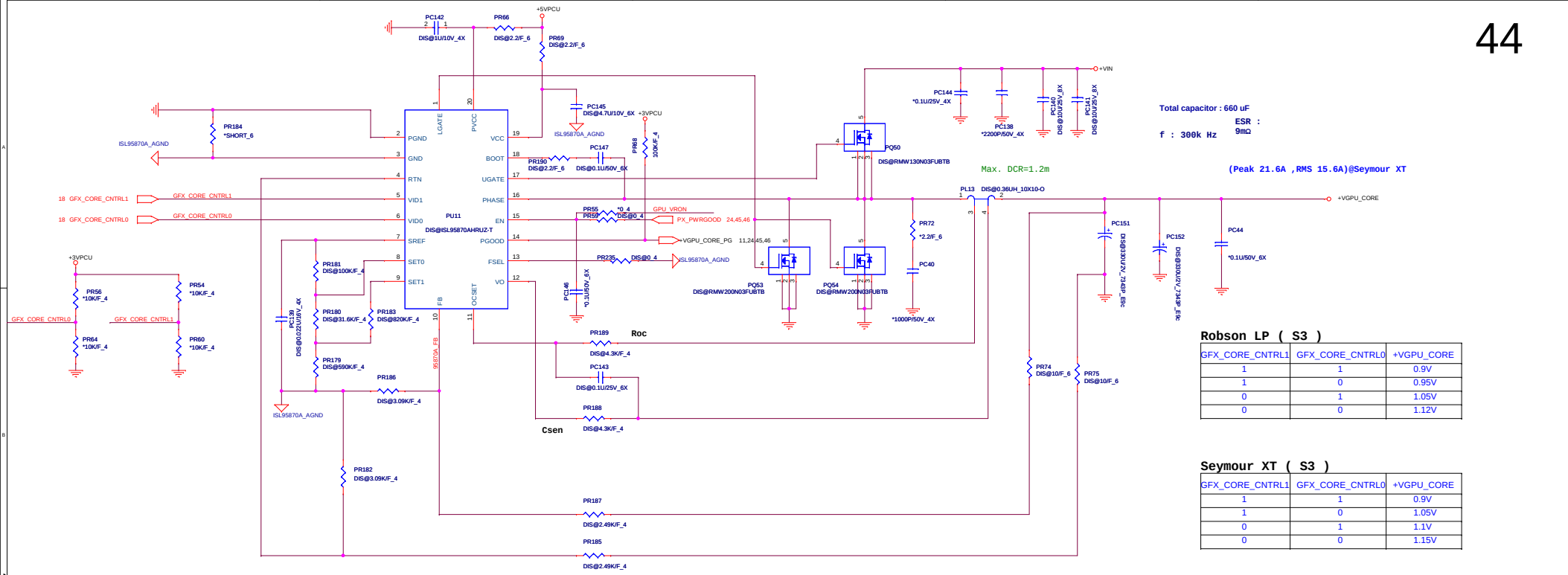
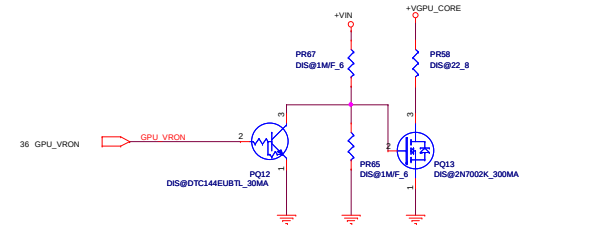


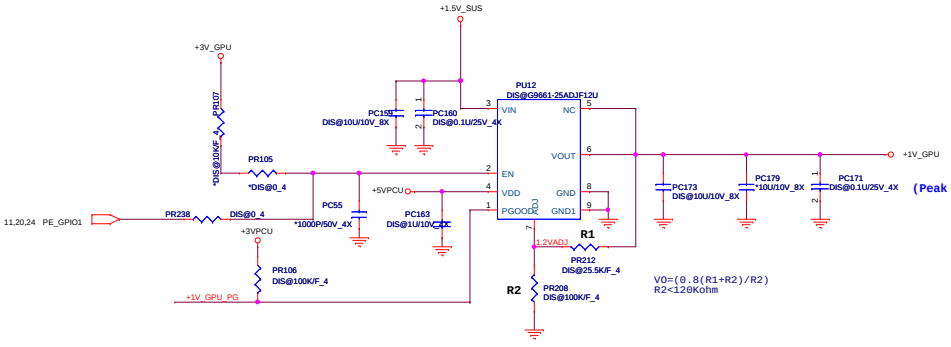
Robson LP (S3)

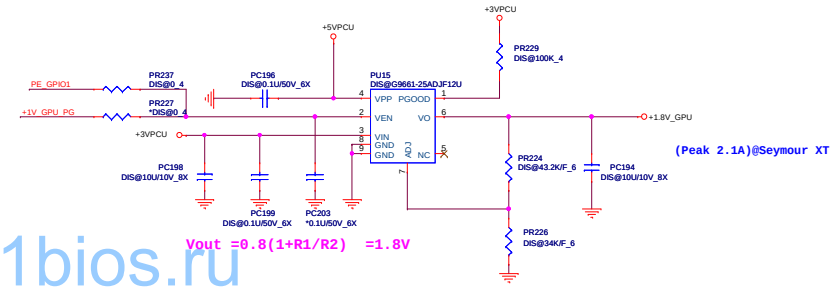
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.12V

Seymour XT (S3)

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	1.05V
0	1	1.1V
0	0	1.15V







PCIE_VDDC

Madison,Park-->1.0V

	Madison,Park
R1	25.5K/F_4 (CS32552FB11)
R2	100K/F_4 (CS41002FB28)

Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	GPU	1C
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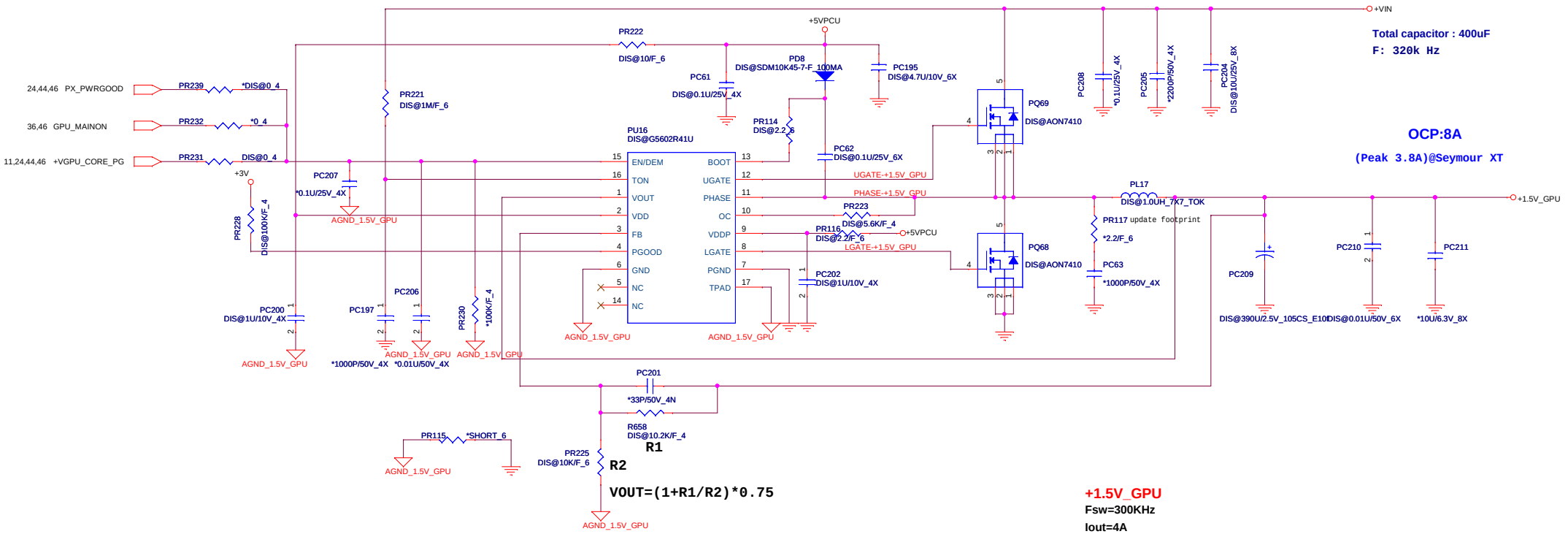

Quanta Computer Inc.		
PROJECT : BLF_BLFD		
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(Peak 0.5A, AVG 0.35A)

(Peak 0.1A, AVG 0.07A)

PC119 10U/10V_8X

PC120 0.1U/50V_6X

PR171 2.2/F_6

PC116 10U/10V_8X

+0.75V_DDR_VTT

1.5SUS_HG

1.5SUS_PHASE

1.5SUS_LG

RT8207LGQW

PU9

FOR DDR III

PC113 0.033U/50V_6X

PR169 5.6K/F_4

PR168 5.1/F_6

PC115 1U/10V_4X

PC118 1U/10V_4X

+5VPCU

PR165 *100K_4 +3VPCU D3A

VDRAM_PWRGD 36

PR164 620K/F_4 +VIN

For RT8207A 400KHZ

S5_1.5V PR161 *SHORT_4 SUS_ON 36

S3_1.5V PR162 *0_4 RUN_ON 36,49

PQ47 RMW130N03FUBTB

PQ48 RMW200N03FUBTB

PR53 *2.2/F_6

PC37 *1000P/50V_4X

RDSon=2.3m ohm

PL11 1.5UH_10X10

+1.5V_SUS

PC122 *0.1U/25V_4X

PC36 *2200P/50V_4X

PC121 10U/25V_8X

PC25 *10U/25V_8X

+VIN

PC126 *0.1U/25V_4X

PC133 *10U/10V_8X

PC129 390U/2.5V_105CS_E10f

OCP:16A

(Peak 13.72A, AVG 10.129A)

ESR : 9mΩ

f : 400k Hz

S3_1.5V PR167 0_4 S5_1.5V

PC111 1000P/50V_4X

PR163 10K/F_4 R1

Vout = (R1/R2) X 0.75 + 0.75

PR166 100_4 APU_VDDIO_RUN_FB_H 7

MEM_P1V5	MEM_P1V35	+1.5VSUS
1	DONT CARE	1.50V
0	1	1.35V
0	0	1.25V

PR49 *0_6/S

+3VPCU

R14 9.76K/F_4 R15 300/F_4 R16 2.49K/F_4 R17 2.49K/F_4

R2

PR51 100K/F_4

12 MEM_P1V5

PR52 100K/F_4

PR50 *100K/F_4

PC34 0.1U/10V_4X

PQ8 2N7002K_300MA

12 MEM_P1V35

PR48 100K/F_4

PR46 100K/F_4

PC33 0.1U/10V_4X

PQ9 2N7002K_300MA

D3A 47,49 MAIND R549 *0_4

+1.5V_SUS

+1.5V_RUN

Q46 *ME2306_4A

D3B

+VIN

D3B

+5VPCU

R488 *100K_4

+3V

R482 *47K_4

PQ55 *2N7002K_300MA

C690 *4700P/25V_4X

D3B

PR191 *1M/F_6

PQ56 *2N7002K_300MA

C701 *4700P/25V_4X

+15V

PR57 *DIS@1M/F_6

+VIN

PR71 *DIS@1M/F_6

+1.5V_SUS

PQ49 *DIS@AON7702

(Peak 2.8A ,RMS 2.3A)

(Peak 6.4A ,RMS 4.4A)

PQ10 *DIS@DTC144EUBTL_30MA

PC39 *DIS@2200P/50V_4X

+1.5V_GPU

24,44,45 PX_PWRGOOD PR240 *DIS@0_4

36,45 GPU_MAINON PR61 *0_4

11,24,44,45 +VGPU_CORE_PG PR62 *0_4

PR70 *DIS@100K

PR63 *DIS@1MF_6

PQ11 *DIS@2N7002K_300MA

D3A

Quanta Computer Inc.

PROJECT : BLF_BLFD

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	DDR1.5V(RT8207LGQW)	1C

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f : 400k Hz
ESR : 17mΩ
Total capacitor : 150 uF
(Peak 6.135A , AVG 4.295A)
OCP:10A

f : 500k Hz
ESR : 17mΩ
Total capacitor : 330uF
(Peak 4.353A, AVG 3.047A)
OCP:8A

RDSon=14m ohm

RDSon=14m ohm

S5 plus mode

S0/S5 > High
S5+ > Low

(Peak 4.7A)

(Peak 4.712A)

Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	System 5V/3V (PM6686TR)	1C
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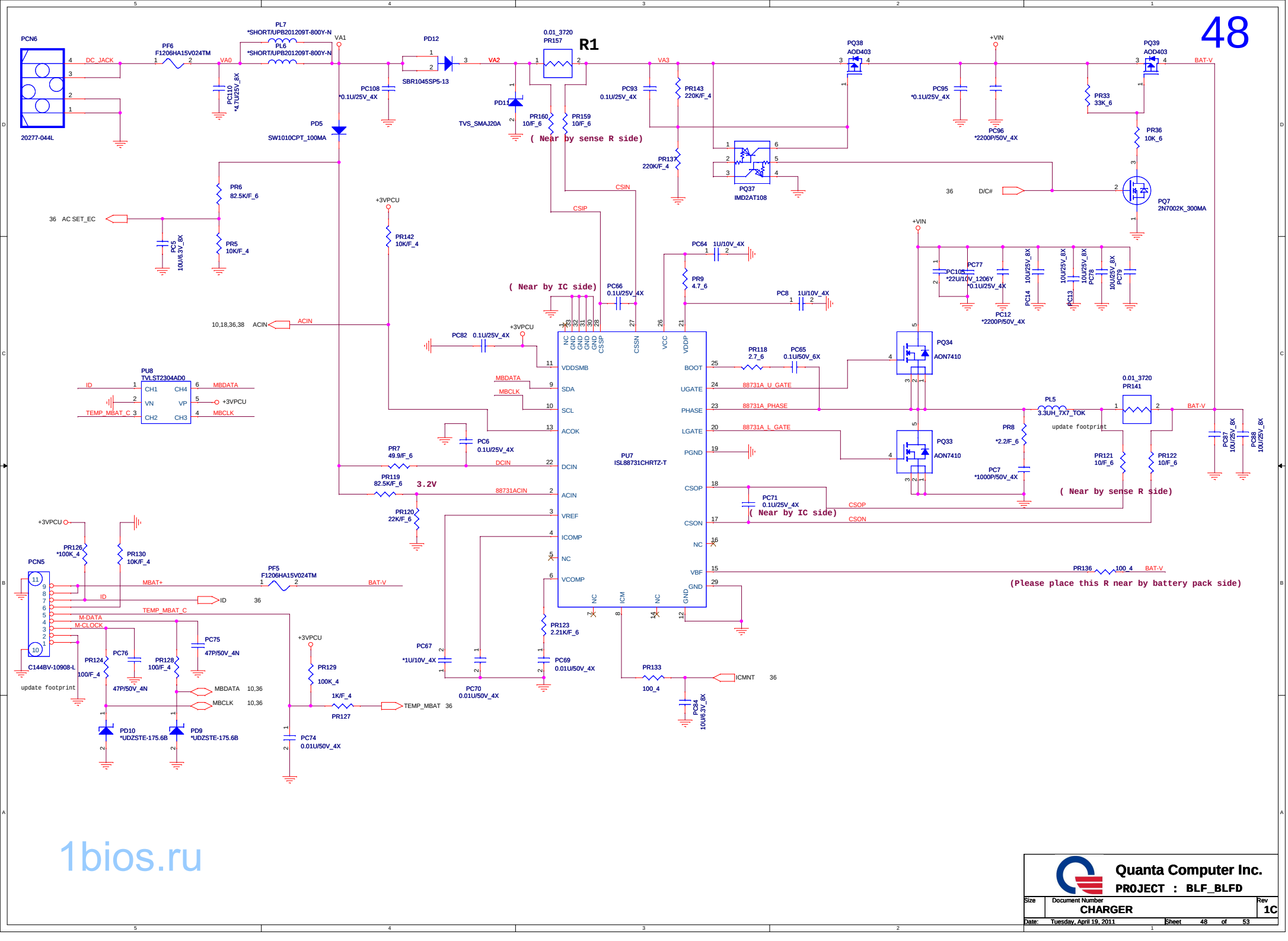
48
PCN6
20277-044L
DC_JACK
PF6
F1206HA15V024TM
PL7
*SHORT/UPB201209T-800Y-N
PL6
*SHORT/UPB201209T-800Y-N
VA1
VA0
PC110
*4.7U/25V_8X
PD12
SBR1045SP5-13
VA2
PD11
TVS_SMAJ20A
0.01_3720
PR157
R1
PR160
10/F_6
PR159
10/F_6
(Near by sense R side)
PC108
*0.1U/25V_4X
PD5
SW1010CPT_100MA
VA3
PC93
0.1U/25V_4X
PR143
220K/F_4
PR137
220K/F_4
PQ38
AOD403
PQ37
IMD2AT108
+VIN
PC95
*0.1U/25V_4X
PC96
*2200P/50V_4X
PQ39
AOD403
BAT-V
PR33
33K_6
PR36
10K_6
PQ7
2N7002K_300MA
36 D/C#
PR6
82.5K/F_6
36 AC SET_EC
PC5
10U/6.3V_8X
PR5
10K/F_4
+3VPCU
PR142
10K/F_4
CSIN
CSIP
PC64 1U/10V_4X
PR9
4.7_6
PC8 1U/10V_4X
(Near by IC side)
PC66
0.1U/25V_4X
10,18,36,38 ACIN
ACIN
PC82 0.1U/25V_4X
+3VPCU
PC105
*22U/10V_1206Y
*0.1U/25V_4X
PC77
PC12
*2200P/50V_4X
PC14
10U/25V_8X
PC13
10U/25V_8X
PC78
10U/25V_8X
PC79
10U/25V_8X
PU8
TVLST2304AD0
ID
TEMP_MBAT_C
MBDATA
+3VPCU
MBCLK
PU7
ISL88731CHRTZ-T
NC
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
PR118
2.7_6
PC65
0.1U/50V_6X
PQ34
AON7410
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PQ33
AON7410
PL5
3.3UH_7X7_TOK
update footprint
0.01_3720
PR141
PR8
*2.2/F_6
PC7
*1000P/50V_4X
PR121
10/F_6
PR122
10/F_6
(Near by sense R side)
PC37
10U/25V_8X
PC38
10U/25V_8X
PC6
0.1U/25V_4X
PR7
49.9/F_6
DCIN
PR119
82.5K/F_6
3.2V
88731ACIN
PR120
22K/F_6
PC71
0.1U/25V_4X
(Near by IC side)
CSOP
CSON
PR136
100_4
BAT-V
(Please place this R near by battery pack side)
+3VPCU
PR126
*100K_4
PR130
10K/F_4
PCN5
C144BV-10908-L
MBAT+
PF5
F1206HA15V024TM
BAT-V
ID
36
TEMP_MBAT_C
M-DATA
M-CLOCK
PC75
47P/50V_4N
PR124
100/F_4
PC76
47P/50V_4N
PR128
100/F_4
update footprint
MBDATA 10,36
MBCLK 10,36
PD10
*UDZSTE-175.6B
PD9
*UDZSTE-175.6B
+3VPCU
PR129
100K_4
1K/F_4
PR127
TEMP_MBAT 36
PC74
0.01U/50V_4X
PC67
*1U/10V_4X
PC70
0.01U/50V_4X
PR123
2.21K/F_6
PC69
0.01U/50V_4X
PR133
100_4
ICMNT 36
PC84
10U/6.3V_8X
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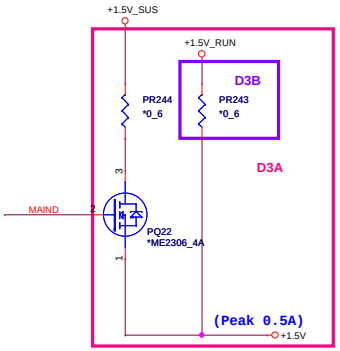
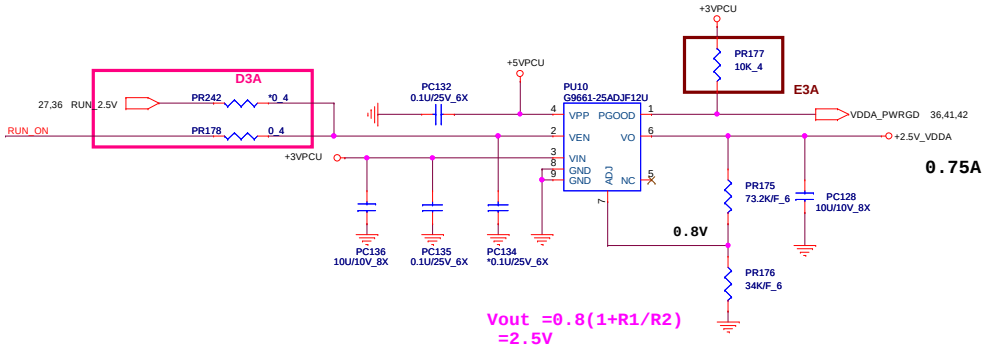
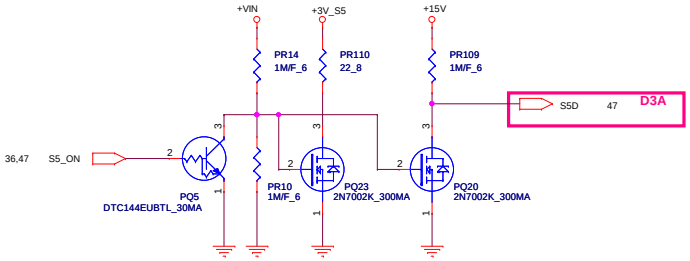
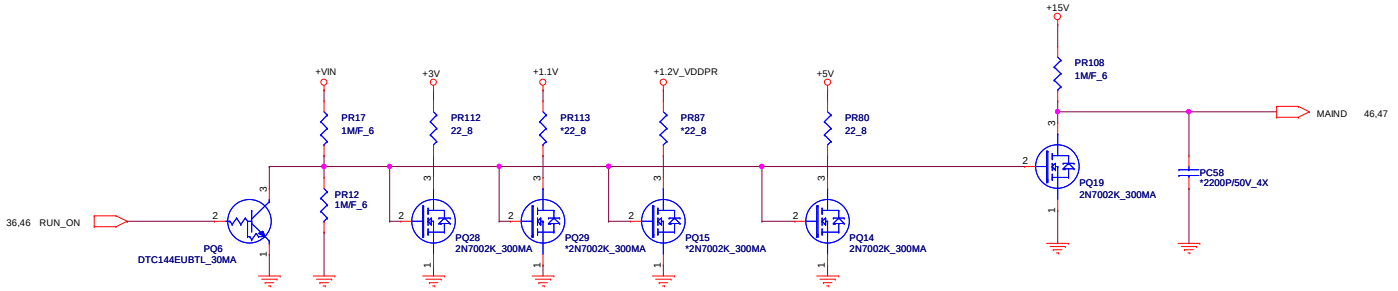


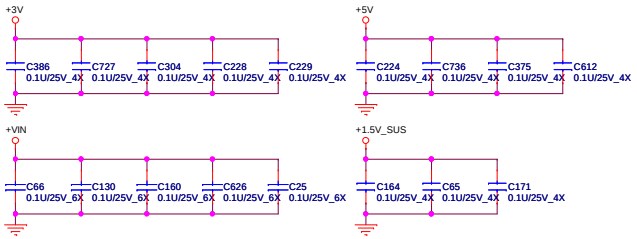


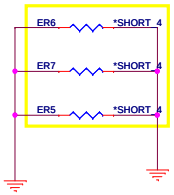


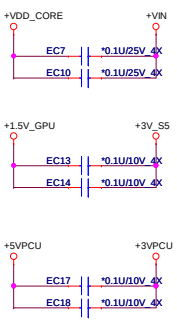


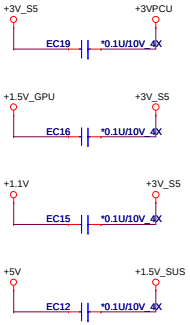
EMI

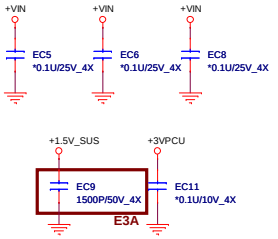
For EMI











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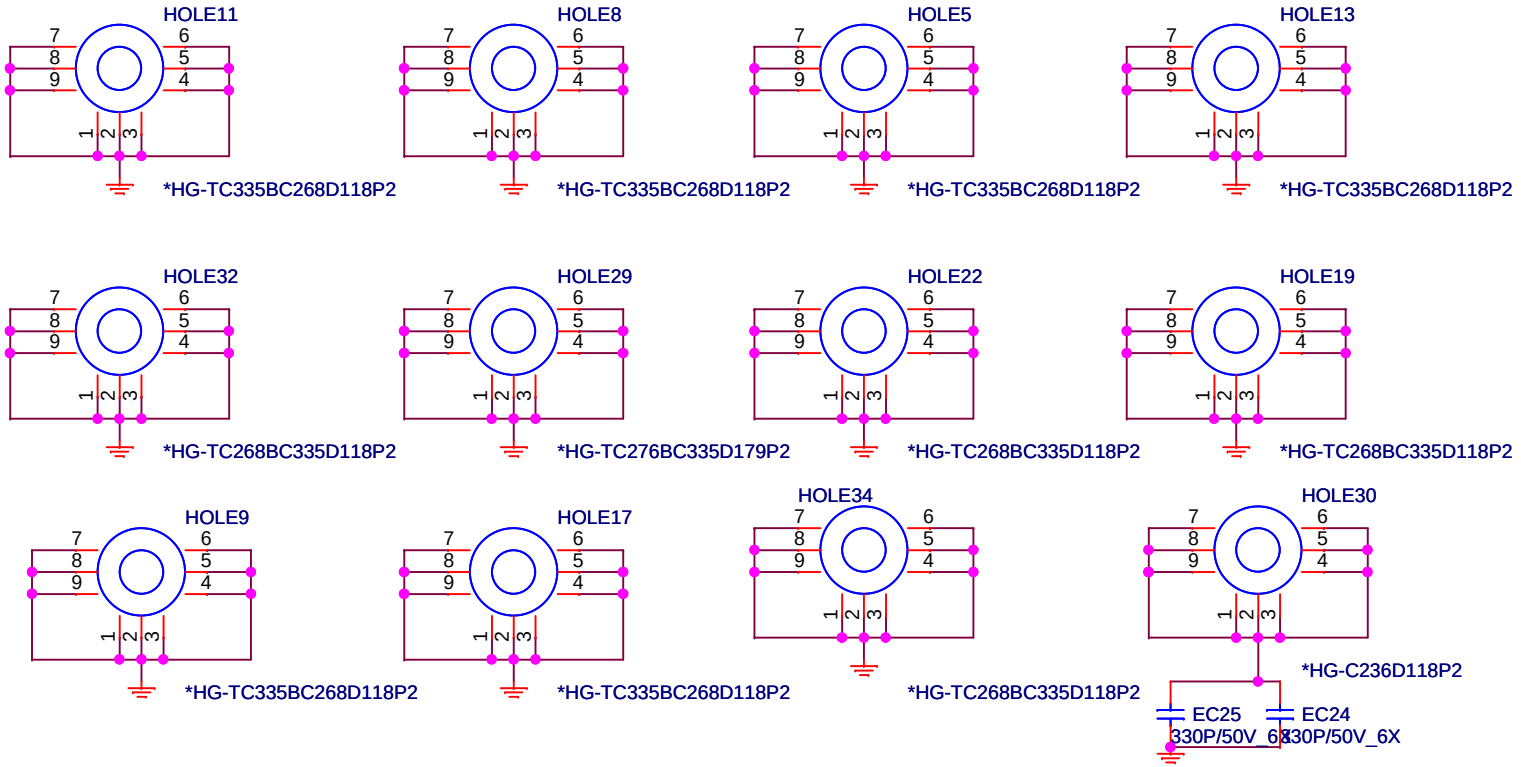

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