Tango/Ballet BLOCK DIAGRAM

01

PCB STACK UP
6L UMA CO-LAY DIS

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

CPU Penryn
478P (uPGA)/35W
PAGE 3,4

CPU THERMAL SENSOR
PAGE 4

FSB 667/800/1066

14.318MHz
CLOCK GEN
ALPRS355B MLF64PIN
PAGE 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

Level Shift
PAGE 18

27MHz

NORTH BRIDGE
Cantiga
PAGE 5~9

DDRII-SODIMM1
PAGE 10
DDRII 667/800 MHz

DDRII-SODIMM2
PAGE 10
DDRII 667/800 MHz

PCI-Express 16X

nVIDIA
NB10M-GE2-S
64 Bit
533p
PAGE 12~16

NBSRCCLK, NBSRCCLK#

HDMI CON
(Option)
PAGE 18

CRT
PAGE18

Dual Link
LCD CONN
PAGE 17

DMI LINK

32.768KHz

SOUTH BRIDGE
ICH-9M
PAGE 19~22

SATA - HDD
PAGE 26
SATA0 150MB

SATA - CD-ROM
PAGE 26
SATA1 150MB

E-SATA
PAGE 26
SATA5 150MB

USB2.0

0,8,9
USB2.0 Ports X3
PAGE 26

5
BlueTooth
(Option)
PAGE 26

3
Webcam
(Option)
PAGE 17

6
Card Reader
RTS5159
(Option) PAGE 23

PCI-E

X1
Mini PCI-E Card
(Wireless LAN)
PAGE 30

X1
LAN
Realtek
PCIE-LAN
RTL8103EL
(10/100 LAN)
PAGE 27

25MHz
RJ45
PAGE 27

Azalia

Analog
IDT92HP75B2
PAGE 24

AUDIO Amplifier
TPA6017
PAGE 25

Jack to Speaker
PAGE 25

Audio Jacks
(Phone/ MIC)
PAGE 24

microphone
PAGE 24

32.768KHz
LPC

ENE KBC
KB3926 C0/D2
PAGE31

Keyboard PAGE 29
Touch Pad PAGE 29

MDC CONN
(Option)
PAGE 28

SPI for HDCP
PAGE 20

GMT G9931P1U
FAN
PAGE 26

SPI
PAGE 29

SYSTEM CHARGER(ISL6251AHAZ-T)
PAGE 31

SYSTEM POWER ISL6237IRZ-T
PAGE 32

DDR II SMDDR_VTERM
1.8V/1.8VSUS(TPS51116REGR)
PAGE 36

VCCP +1.5V AND GMCH
1.05V(RT8204)
PAGE 33

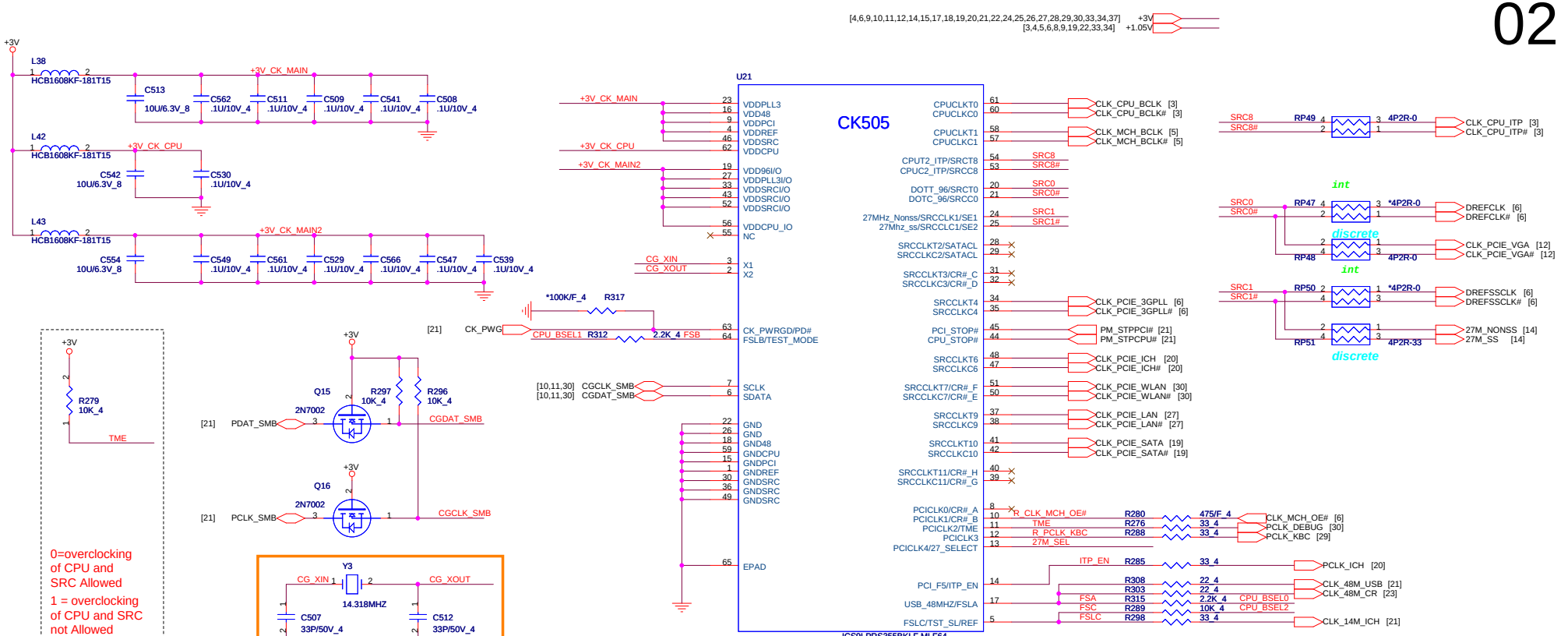
CPU CORE ISL6266A
PAGE 34

NB5

PROJECT : OP6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	A

Date: Tuesday, January 20, 2009 | Sheet 1 of 37



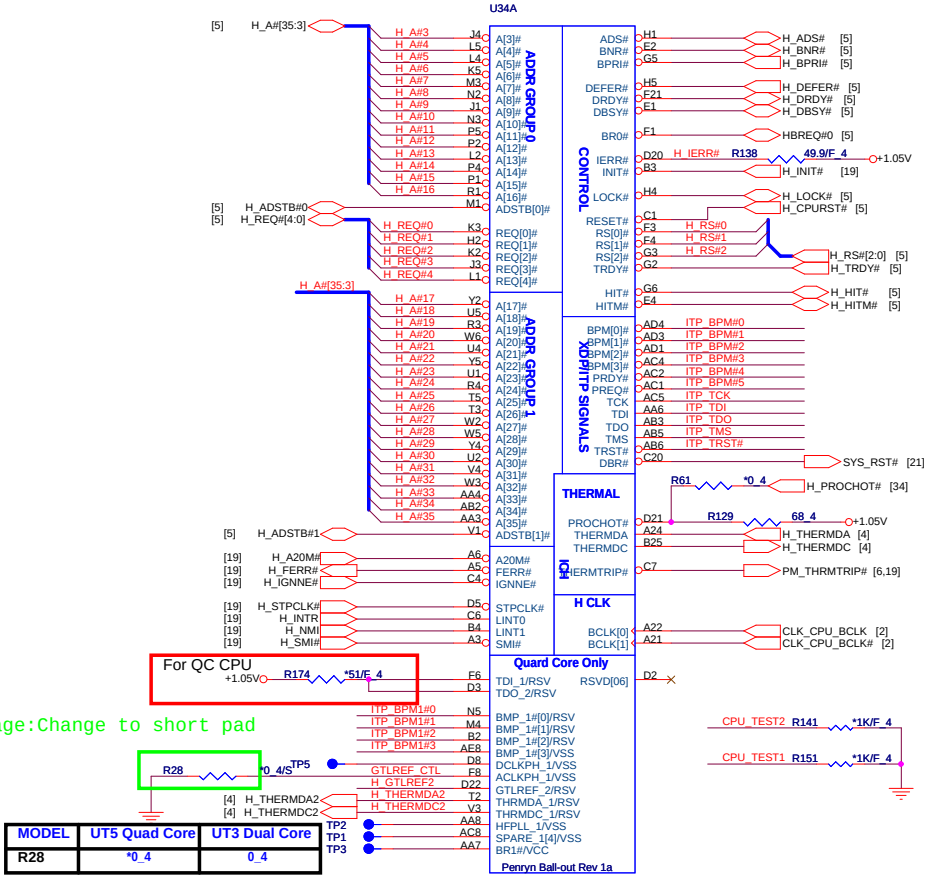
27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

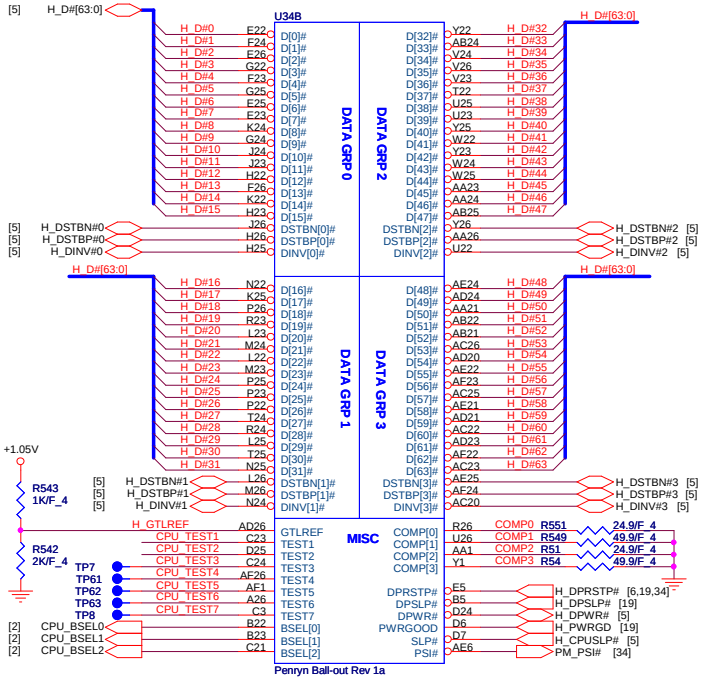
NB5

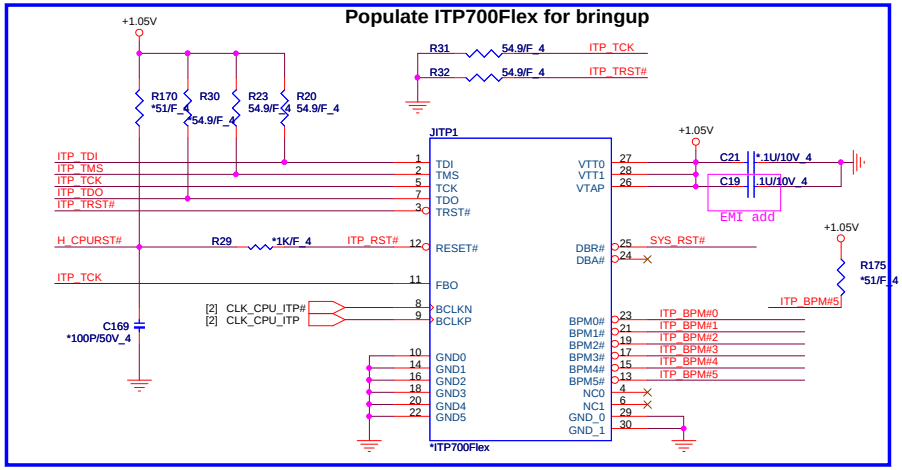
PROJECT : OP6/7
Quanta Computer Inc.

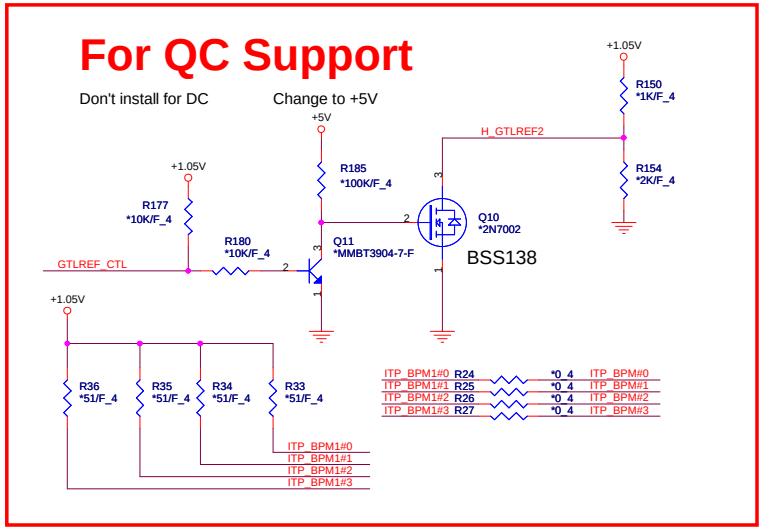
Size	Document Number	Rev
Custom	Clock Generator	SI
Date: Tuesday, January 20, 2009	Sheet 2 of 37	



MODEL	UT5 Quad Core	UT3 Dual Core
R28	*0_4	0_4





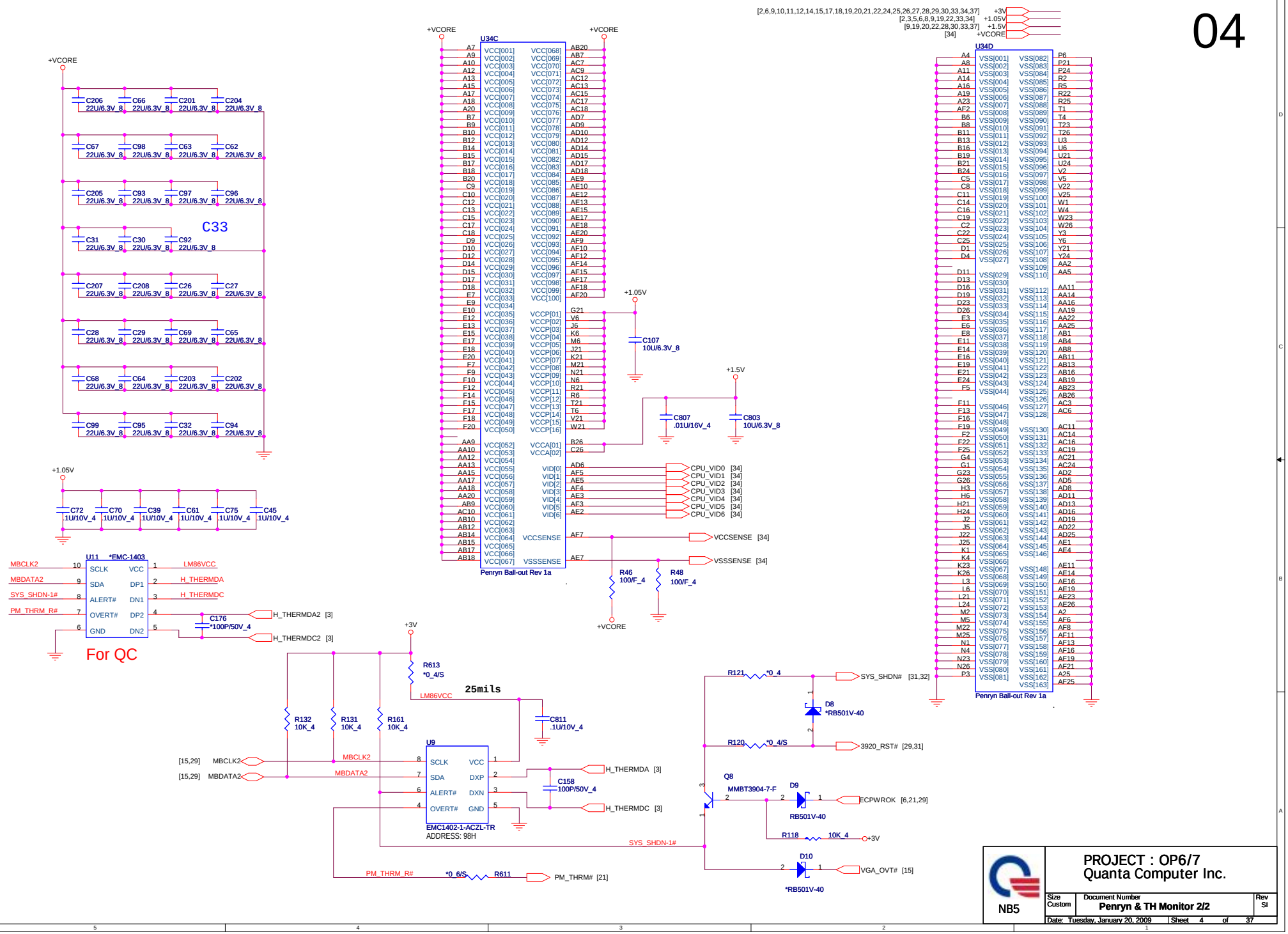


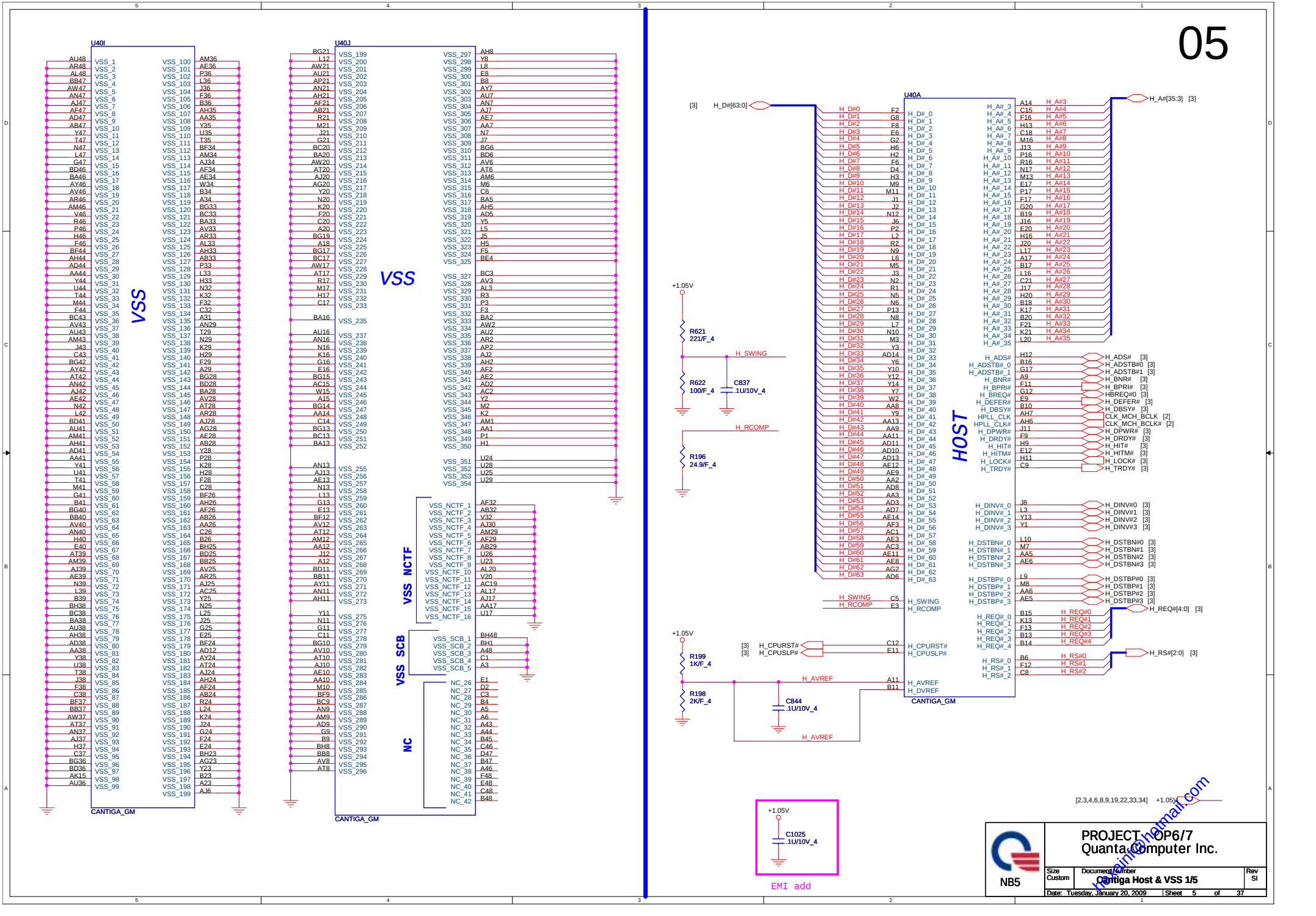
NB5

PROJECT : OP6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn 1/2	SI

Date: Tuesday, January 20, 2009 | Sheet 3 of 37


04
+VCORE
C206 22U/6.3V_8
C66 22U/6.3V_8
C201 22U/6.3V_8
C204 22U/6.3V_8
C67 22U/6.3V_8
C98 22U/6.3V_8
C63 22U/6.3V_8
C62 22U/6.3V_8
C205 22U/6.3V_8
C93 22U/6.3V_8
C97 22U/6.3V_8
C96 22U/6.3V_8
C33
C31 22U/6.3V_8
C30 22U/6.3V_8
C92 22U/6.3V_8
C207 22U/6.3V_8
C208 22U/6.3V_8
C26 22U/6.3V_8
C27 22U/6.3V_8
C28 22U/6.3V_8
C29 22U/6.3V_8
C69 22U/6.3V_8
C65 22U/6.3V_8
C68 22U/6.3V_8
C64 22U/6.3V_8
C203 22U/6.3V_8
C202 22U/6.3V_8
C99 22U/6.3V_8
C95 22U/6.3V_8
C32 22U/6.3V_8
C94 22U/6.3V_8
+1.05V
C72 1U/10V_4
C70 1U/10V_4
C39 1U/10V_4
C61 1U/10V_4
C75 1U/10V_4
C45 1U/10V_4
U11 *EMC-1403
MBCLK2
MBDATA2
SYS_SHDN-1#
PM_THRM_R#
SCLK
SDA
ALERT#
OVERT#
GND
VCC
DP1
DN1
DP2
DN2
LM86VCC
H_THERMDA
H_THERMDC
C176 *100P/50V_4
H_THERMDA2 [3]
H_THERMDC2 [3]
For QC
U34C
Penryn Ball-out Rev 1a
C107 10U/6.3V_8
C807 .01U/16V_4
C803 10U/6.3V_8
+1.5V
CPU_VID0 [34]
CPU_VID1 [34]
CPU_VID2 [34]
CPU_VID3 [34]
CPU_VID4 [34]
CPU_VID5 [34]
CPU_VID6 [34]
VCCSENSE [34]
VSSSENSE [34]
R46 100/F_4
R48 100/F_4
[2,6,9,10,11,12,14,15,17,18,19,20,21,22,24,25,26,27,28,29,30,33,34,37] +3V
[2,3,5,6,8,9,19,22,33,34] +1.05V
[9,19,20,22,28,30,33,37] +1.5V
[34] +VCORE
U34D
Penryn Ball-out Rev 1a
+3V
R613 *0_4/S
25mils
LM86VCC
C811 .1U/10V_4
R132 10K_4
R131 10K_4
R161 10K_4
U9
EMC1402-1-ACZL-TR
ADDRESS: 98H
[15,29] MBCLK2
[15,29] MBDATA2
C158 100P/50V_4
H_THERMDA [3]
H_THERMDC [3]
SYS_SHDN-1#
PM_THRM_R#
*0_6/S
R611
PM_THRM# [21]
R121 *0_4
SYS_SHDN# [31,32]
D8 *RB501V-40
R120 *0_4/S
3920_RST# [29,31]
Q8 MMBT3904-7-F
D9 RB501V-40
ECPWROK [6,21,29]
R118 10K_4
D10 *RB501V-40
VGA_OVT# [15]
NB5
PROJECT : OP6/7
Quanta Computer Inc.
Size Custom
Document Number
Penryn & TH Monitor 2/2
Rev SI
Date: Tuesday, January 20, 2009
Sheet 4 of 37


05
U40I
VSS
CANTIGA_GM
U40J
VSS
VSS NCTF
VSS SCB
NC
CANTIGA_GM
U40A
HOST
CANTIGA_GM
H_D#[63:0]
H_A#[35:3]
+1.05V
R621
221/F_4
R622
100/F_4
C837
.1U/10V_4
H_SWING
H_RCOMP
R196
24.9/F_4
R199
1K/F_4
R198
2K/F_4
C844
.1U/10V_4
H_AVREF
H_CPURST#
H_CPUSLP#
H_REQ#[4:0]
H_RS#[2:0]
H_ADS#
H_ADSTB#0
H_ADSTB#1
H_BNR#
H_BPRI#
H_BREQ#0
H_DEFER#
H_DBSY#
CLK_MCH_BCLK
CLK_MCH_BCLK#
H_DPWR#
H_DRDY#
H_HIT#
H_HITM#
H_LOCK#
H_TRDY#
H_DINV#0
H_DINV#1
H_DINV#2
H_DINV#3
H_DSTBN#0
H_DSTBN#1
H_DSTBN#2
H_DSTBN#3
H_DSTBP#0
H_DSTBP#1
H_DSTBP#2
H_DSTBP#3
[2,3,4,6,8,9,19,22,33,34]
+1.05V
C1025
.1U/10V_4
EMI add
PROJECT : OP6/7
Quanta Computer Inc.
NB5
Size
Custom
Document Number
Cantiga Host & VSS 1/5
Rev
SI
Date: Tuesday, January 20, 2009
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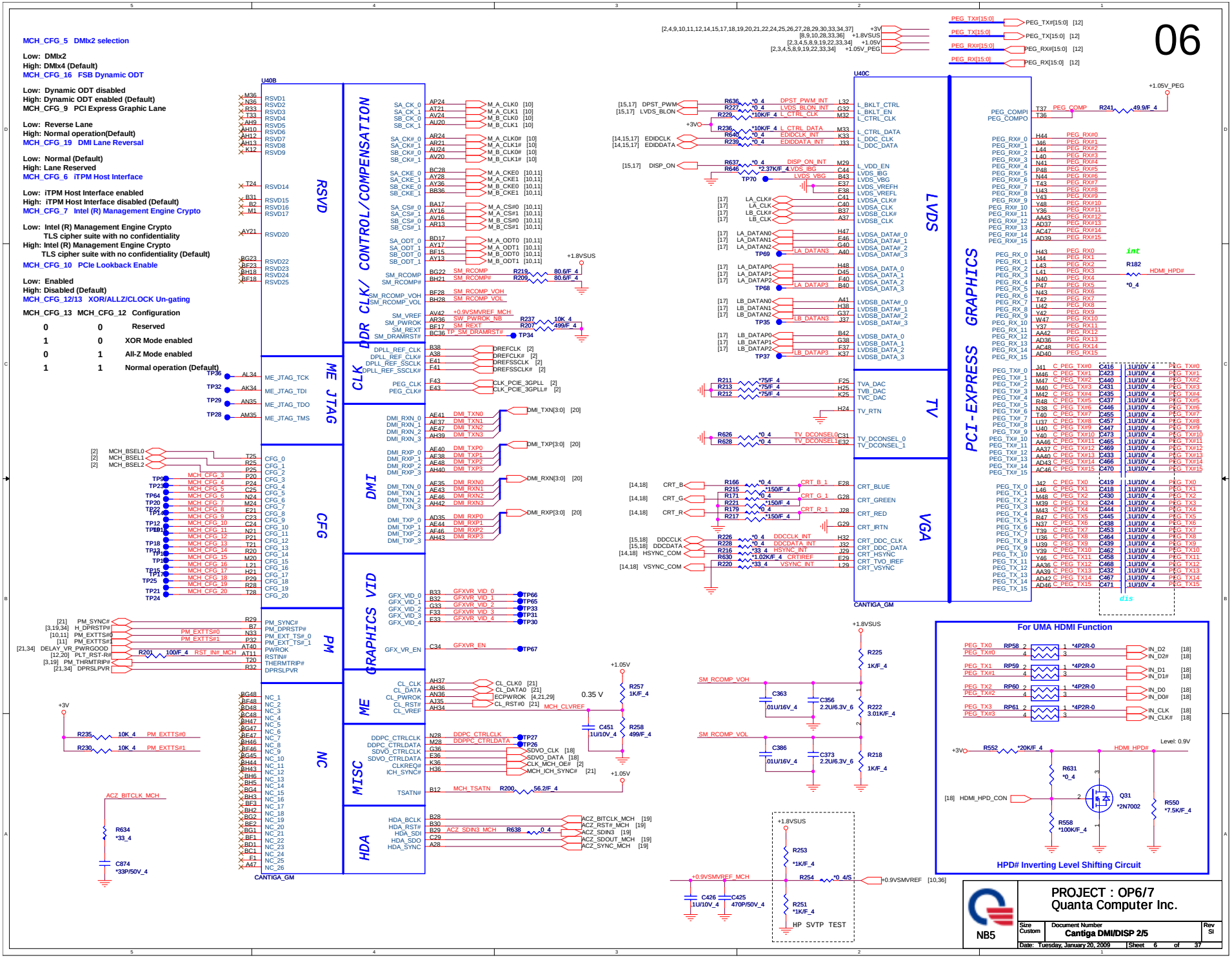
MCH_CFG_5 DMIx2 selection
Low: DMIx2
High: DMIx4 (Default)
MCH_CFG_16 FSB Dynamic ODT
Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)
MCH_CFG_9 PCI Express Graphic Lane
Low: Reverse Lane
High: Normal operation(Default)
MCH_CFG_19 DMI Lane Reversal
Low: Normal (Default)
High: Lane Reserved
MCH_CFG_6 iTPM Host Interface
Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)
MCH_CFG_7 Intel (R) Management Engine Crypto
Low: Intel (R) Management Engine Crypto TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto TLS cipher suite with no confidentiality (Default)
MCH_CFG_10 PCIe Lookback Enable
Low: Enabled
High: Disabled (Default)
MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating
MCH_CFG_13 MCH_CFG_12 Configuration
0 0 Reserved
1 0 XOR Mode enabled
0 1 All-Z Mode enabled
1 1 Normal operation (Default)
U40B
RSVD
CLK / DDR CLK / CONTROL / COMPENSATION
ME JTAG
DMI
CFG
GRAPHICS VID
PM
ME
MISC
HDA
NC
CANTIGA_GM
U40C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CANTIGA_GM
For UMA HDMI Function
HPD# Inverting Level Shifting Circuit
06
PROJECT : OP6/7
Quanta Computer Inc.
NB5
Cantiga DMI/DISP 2/5
Date: Tuesday, January 20, 2009
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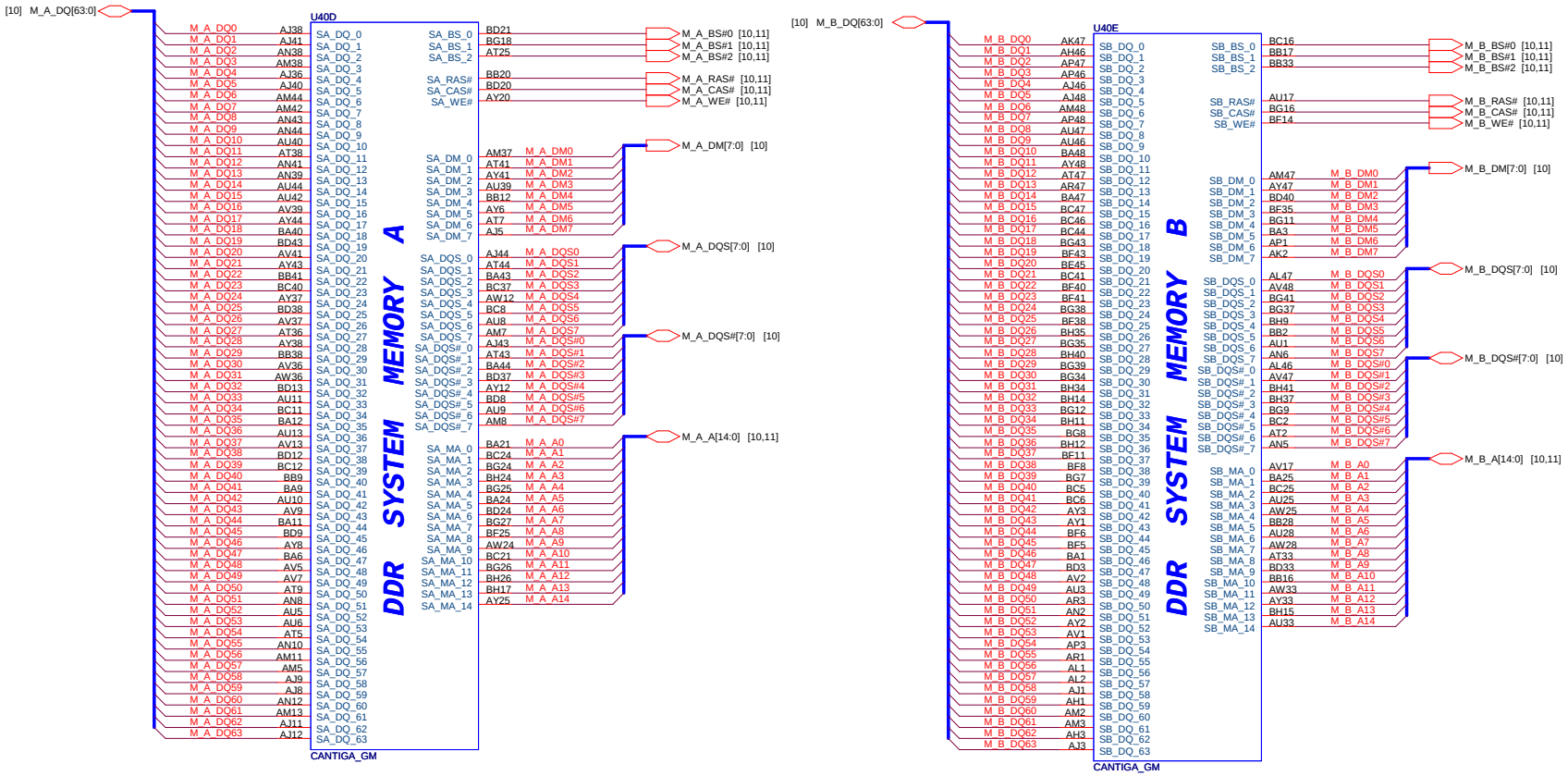
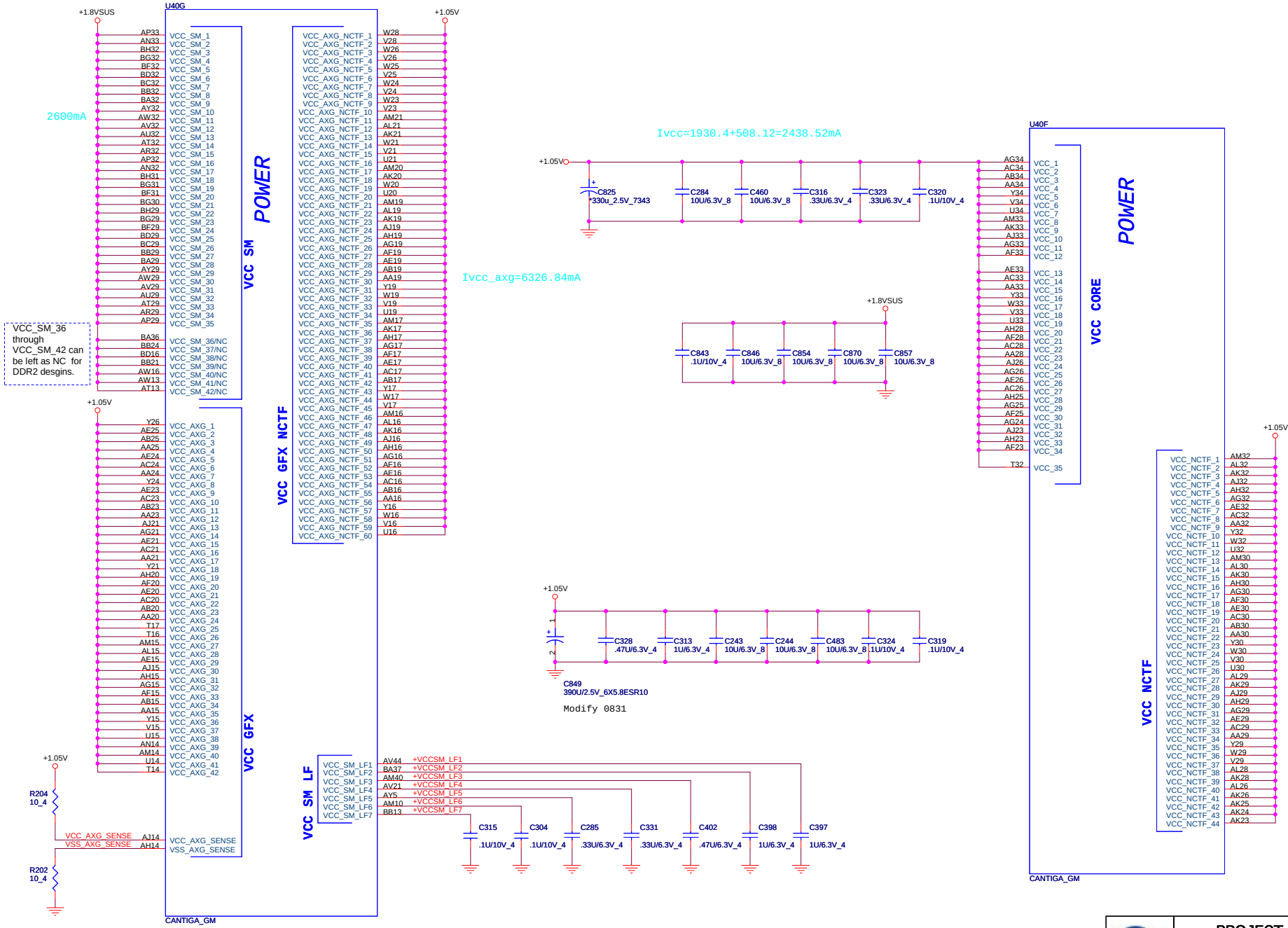


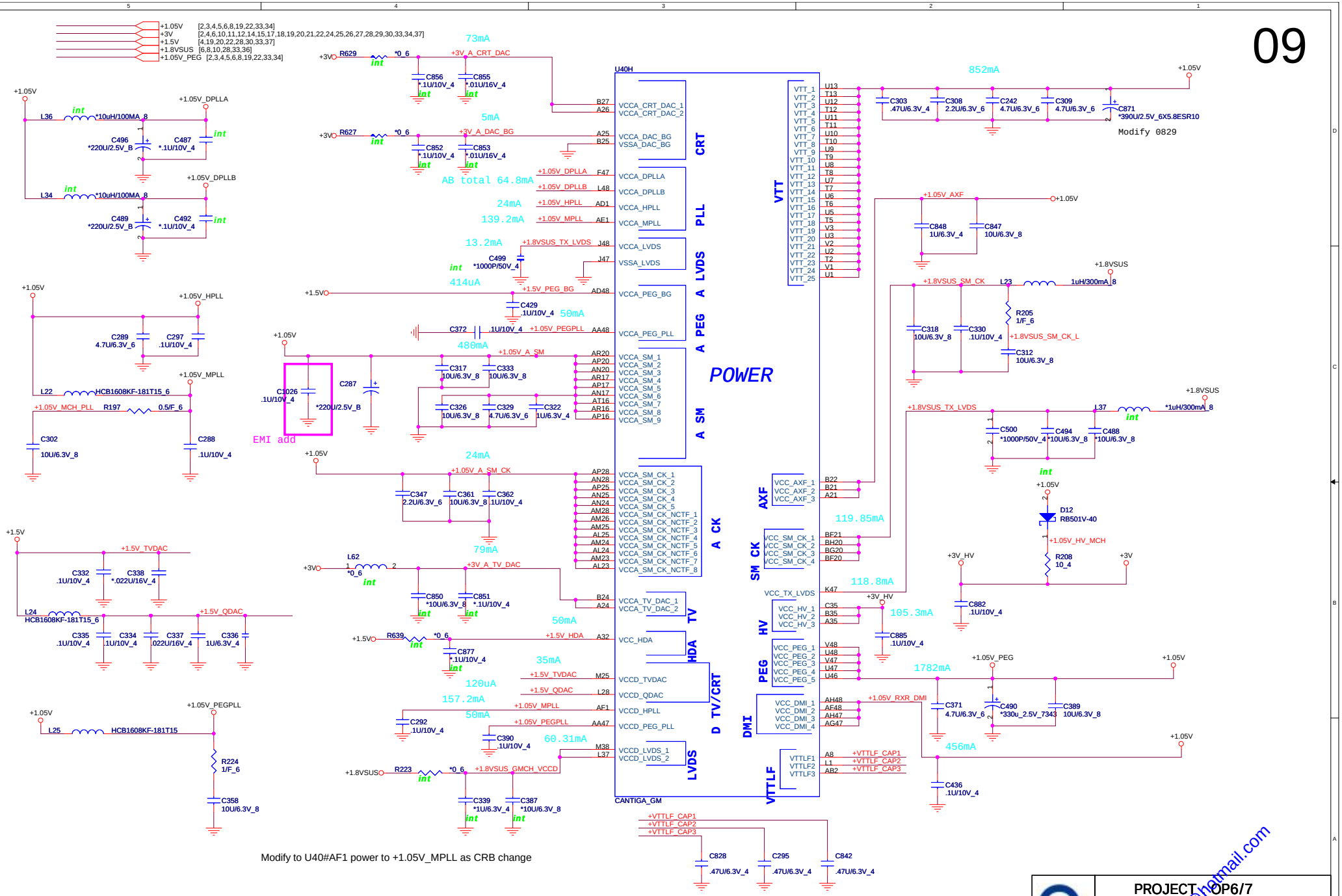
NB5

PROJECT : OP6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga DDR2 3/5	SI
Date: Tuesday, January 20, 2009	Sheet 7 of 37	



NB5	PROJECT : OP6/7 Quanta Computer Inc.	
Size: Custom	Document Number: Cantiga Vcc 4/5	Rev: SI
Date: Tuesday, January 20, 2009	Sheet 8 of 37	


09
+1.05V [2,3,4,5,6,8,19,22,33,34]
+3V [2,4,6,10,11,12,14,15,17,18,19,20,21,22,24,25,26,27,28,29,30,33,34,37]
+1.5V [4,19,20,22,28,30,33,37]
+1.8VSUS [6,8,10,28,33,36]
+1.05V_PEG [2,3,4,5,6,8,19,22,33,34]
U40H
CANTIGA_GM
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
73mA
5mA
AB total 64.8mA
24mA
139.2mA
13.2mA
414uA
50mA
480mA
24mA
79mA
50mA
35mA
120uA
157.2mA
50mA
60.31mA
852mA
119.85mA
118.8mA
105.3mA
1782mA
456mA
Modify 0829
EMI add
Modify to U40#AF1 power to +1.05V_MPLL as CRB change
PROJECT : OP6/7
Quanta Computer Inc.
NB5
Cantiga Power 5/5
Size Custom
Rev SI
Date: Tuesday, January 20, 2009
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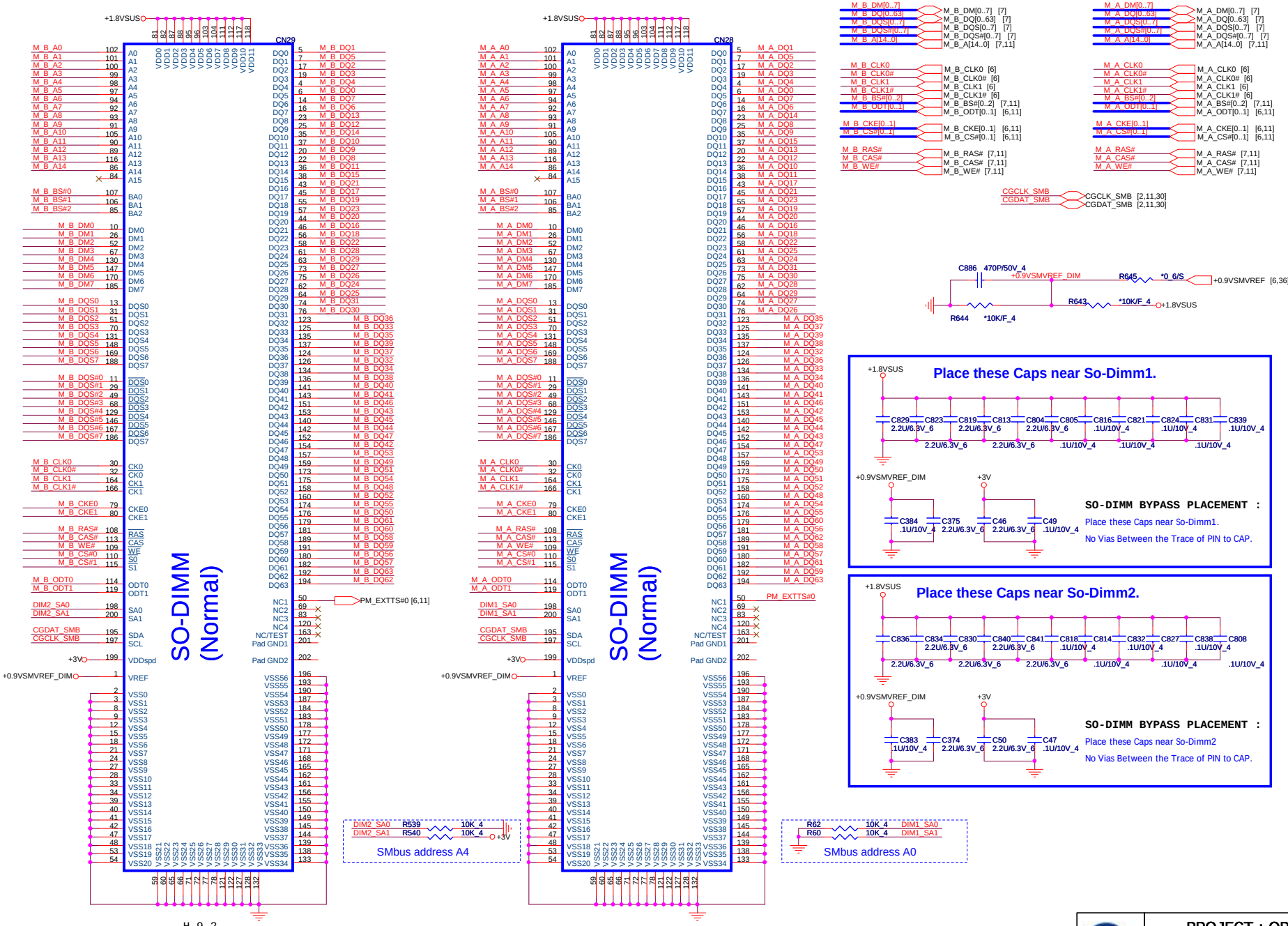
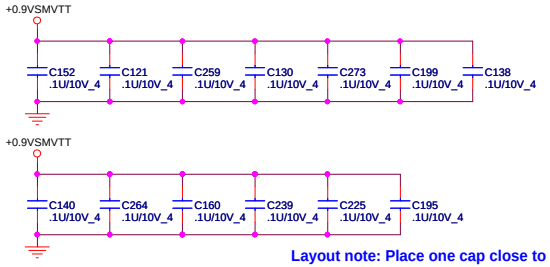
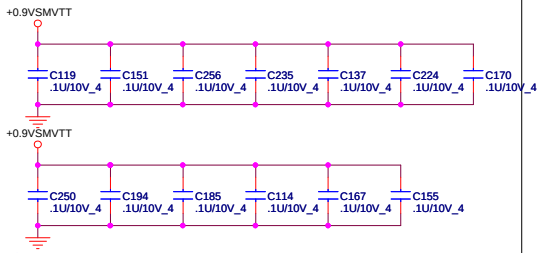

CN29
SO-DIMM (Normal)
+1.8VSUS
+3V
+0.9VSMVREF_DIM
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_A14
M_B_BS#0
M_B_BS#1
M_B_BS#2
M_B_DM0
M_B_DM1
M_B_DM2
M_B_DM3
M_B_DM4
M_B_DM5
M_B_DM6
M_B_DM7
M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7
M_B_DQS0#
M_B_DQS1#
M_B_DQS2#
M_B_DQS3#
M_B_DQS4#
M_B_DQS5#
M_B_DQS6#
M_B_DQS7#
M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_CKE0
M_B_CKE1
M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_CS#0
M_B_CS#1
M_B_ODT0
M_B_ODT1
DIM2_SA0
DIM2_SA1
CGDAT_SMB
CGCLK_SMB
M_B_DQ1
M_B_DQ5
M_B_DQ2
M_B_DQ3
M_B_DQ4
M_B_DQ0
M_B_DQ7
M_B_DQ6
M_B_DQ13
M_B_DQ12
M_B_DQ14
M_B_DQ10
M_B_DQ9
M_B_DQ8
M_B_DQ11
M_B_DQ15
M_B_DQ21
M_B_DQ17
M_B_DQ19
M_B_DQ23
M_B_DQ20
M_B_DQ16
M_B_DQ18
M_B_DQ22
M_B_DQ28
M_B_DQ29
M_B_DQ27
M_B_DQ26
M_B_DQ24
M_B_DQ25
M_B_DQ31
M_B_DQ30
M_B_DQ36
M_B_DQ33
M_B_DQ35
M_B_DQ38
M_B_DQ37
M_B_DQ32
M_B_DQ34
M_B_DQ40
M_B_DQ41
M_B_DQ46
M_B_DQ43
M_B_DQ45
M_B_DQ44
M_B_DQ47
M_B_DQ42
M_B_DQ53
M_B_DQ49
M_B_DQ51
M_B_DQ48
M_B_DQ52
M_B_DQ55
M_B_DQ50
M_B_DQ61
M_B_DQ60
M_B_DQ58
M_B_DQ59
M_B_DQ56
M_B_DQ57
M_B_DQ63
M_B_DQ62
PM_EXTTS#0 [6,11]
DIM2_SA0 R539 10K_4
DIM2_SA1 R540 10K_4 +3V
SMbus address A4
H 9.2
CN28
SO-DIMM (Normal)
M_A_A0
M_A_A1
M_A_A2
M_A_A3
M_A_A4
M_A_A5
M_A_A6
M_A_A7
M_A_A8
M_A_A9
M_A_A10
M_A_A11
M_A_A12
M_A_A13
M_A_A14
M_A_BS#0
M_A_BS#1
M_A_BS#2
M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7
M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7
M_A_DQS0#
M_A_DQS1#
M_A_DQS2#
M_A_DQS3#
M_A_DQS4#
M_A_DQS5#
M_A_DQS6#
M_A_DQS7#
M_A_CLK0
M_A_CLK0#
M_A_CLK1
M_A_CLK1#
M_A_CKE0
M_A_CKE1
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_CS#0
M_A_CS#1
M_A_ODT0
M_A_ODT1
DIM1_SA0
DIM1_SA1
CGDAT_SMB
CGCLK_SMB
M_A_DQ1
M_A_DQ5
M_A_DQ2
M_A_DQ3
M_A_DQ4
M_A_DQ0
M_A_DQ7
M_A_DQ6
M_A_DQ14
M_A_DQ8
M_A_DQ9
M_A_DQ15
M_A_DQ13
M_A_DQ12
M_A_DQ10
M_A_DQ11
M_A_DQ17
M_A_DQ21
M_A_DQ23
M_A_DQ19
M_A_DQ20
M_A_DQ16
M_A_DQ18
M_A_DQ22
M_A_DQ25
M_A_DQ24
M_A_DQ31
M_A_DQ30
M_A_DQ28
M_A_DQ29
M_A_DQ27
M_A_DQ26
M_A_DQ35
M_A_DQ37
M_A_DQ39
M_A_DQ38
M_A_DQ32
M_A_DQ36
M_A_DQ33
M_A_DQ34
M_A_DQ40
M_A_DQ41
M_A_DQ46
M_A_DQ42
M_A_DQ45
M_A_DQ44
M_A_DQ43
M_A_DQ47
M_A_DQ53
M_A_DQ49
M_A_DQ50
M_A_DQ51
M_A_DQ52
M_A_DQ48
M_A_DQ54
M_A_DQ55
M_A_DQ60
M_A_DQ56
M_A_DQ62
M_A_DQ58
M_A_DQ57
M_A_DQ61
M_A_DQ59
M_A_DQ63
PM_EXTTS#0
R62 10K_4 DIM1_SA0
R60 10K_4 DIM1_SA1
SMbus address A0
H 5.2
M_B_DM[0..7] M_B_DM[0..7] [7]
M_B_DQ[0..63] M_B_DQ[0..63] [7]
M_B_DQS[0..7] M_B_DQS[0..7] [7]
M_B_DQS#[0..7] M_B_DQS#[0..7] [7]
M_B_A[14..0] M_B_A[14..0] [7,11]
M_B_CLK0 M_B_CLK0 [6]
M_B_CLK0# M_B_CLK0# [6]
M_B_CLK1 M_B_CLK1 [6]
M_B_CLK1# M_B_CLK1# [6]
M_B_BS#[0..2] M_B_BS#[0..2] [7,11]
M_B_ODT[0..1] M_B_ODT[0..1] [6,11]
M_B_CKE[0..1] M_B_CKE[0..1] [6,11]
M_B_CS#[0..1] M_B_CS#[0..1] [6,11]
M_B_RAS# M_B_RAS# [7,11]
M_B_CAS# M_B_CAS# [7,11]
M_B_WE# M_B_WE# [7,11]
M_A_DM[0..7] M_A_DM[0..7] [7]
M_A_DQ[0..63] M_A_DQ[0..63] [7]
M_A_DQS[0..7] M_A_DQS[0..7] [7]
M_A_DQS#[0..7] M_A_DQS#[0..7] [7]
M_A_A[14..0] M_A_A[14..0] [7,11]
M_A_CLK0 M_A_CLK0 [6]
M_A_CLK0# M_A_CLK0# [6]
M_A_CLK1 M_A_CLK1 [6]
M_A_CLK1# M_A_CLK1# [6]
M_A_BS#[0..2] M_A_BS#[0..2] [7,11]
M_A_ODT[0..1] M_A_ODT[0..1] [6,11]
M_A_CKE[0..1] M_A_CKE[0..1] [6,11]
M_A_CS#[0..1] M_A_CS#[0..1] [6,11]
M_A_RAS# M_A_RAS# [7,11]
M_A_CAS# M_A_CAS# [7,11]
M_A_WE# M_A_WE# [7,11]
CGCLK_SMB CGCLK_SMB [2,11,30]
CGDAT_SMB CGDAT_SMB [2,11,30]
C886 470P/50V_4
+0.9VSMVREF_DIM
R645 *0_6/S +0.9VSMVREF [6,36]
R643 *10K/F_4 +1.8VSUS
R644 *10K/F_4
Place these Caps near So-Dimm1.
+1.8VSUS
C829 2.2U/6.3V_6
C823 2.2U/6.3V_6
C819 2.2U/6.3V_6
C813 2.2U/6.3V_6
C804 2.2U/6.3V_6
C805 .1U/10V_4
C816 .1U/10V_4
C821 .1U/10V_4
C824 .1U/10V_4
C831 .1U/10V_4
C839 .1U/10V_4
+0.9VSMVREF_DIM
+3V
C384 .1U/10V_4
C375 2.2U/6.3V_6
C46 2.2U/6.3V_6
C49 .1U/10V_4
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.
Place these Caps near So-Dimm2.
+1.8VSUS
C836 2.2U/6.3V_6
C834 2.2U/6.3V_6
C830 2.2U/6.3V_6
C840 2.2U/6.3V_6
C841 .1U/10V_4
C818 .1U/10V_4
C814 .1U/10V_4
C832 .1U/10V_4
C827 .1U/10V_4
C838 .1U/10V_4
C808 .1U/10V_4
+0.9VSMVREF_DIM
+3V
C383 .1U/10V_4
C374 2.2U/6.3V_6
C50 2.2U/6.3V_6
C47 .1U/10V_4
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm2
No Vias Between the Trace of PIN to CAP.
[6,8,9,28,33,36] +1.8VSUS
[2,4,6,9,11,12,14,15,17,18,19,20,21,22,24,25,26,27,28,29,30,33,34,37] +3V
NB5
PROJECT : OP6/7
Quanta Computer Inc.
Size Custom
Document Number DDR2 DIMM
Rev SI
Date: Tuesday, January 20, 2009
Sheet 10 of 37

DDRII DUAL CHANNEL A,B.

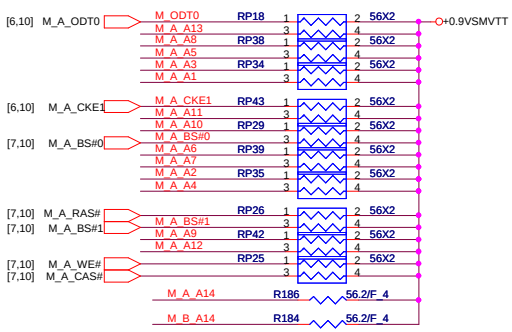
DDRII A CHANNEL

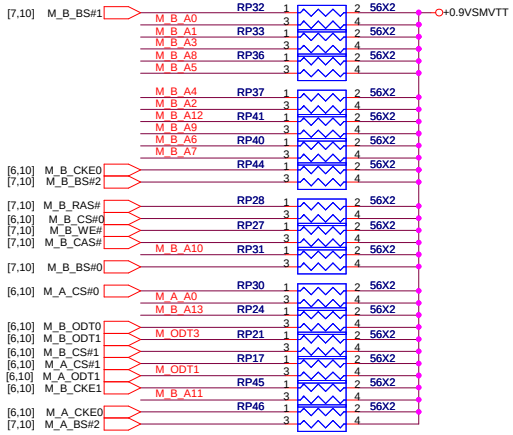


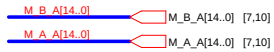
DDRII B CHANNEL

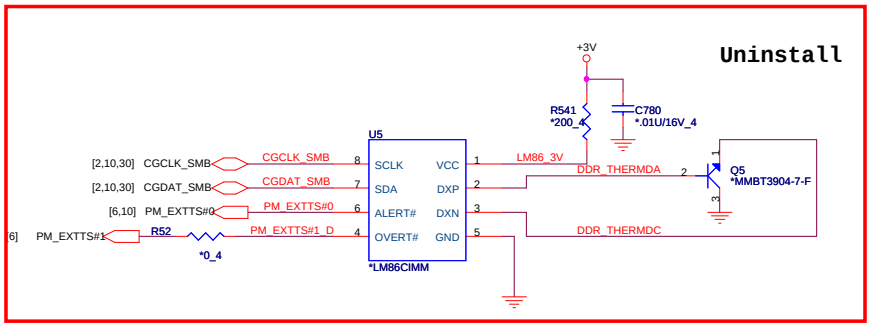


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





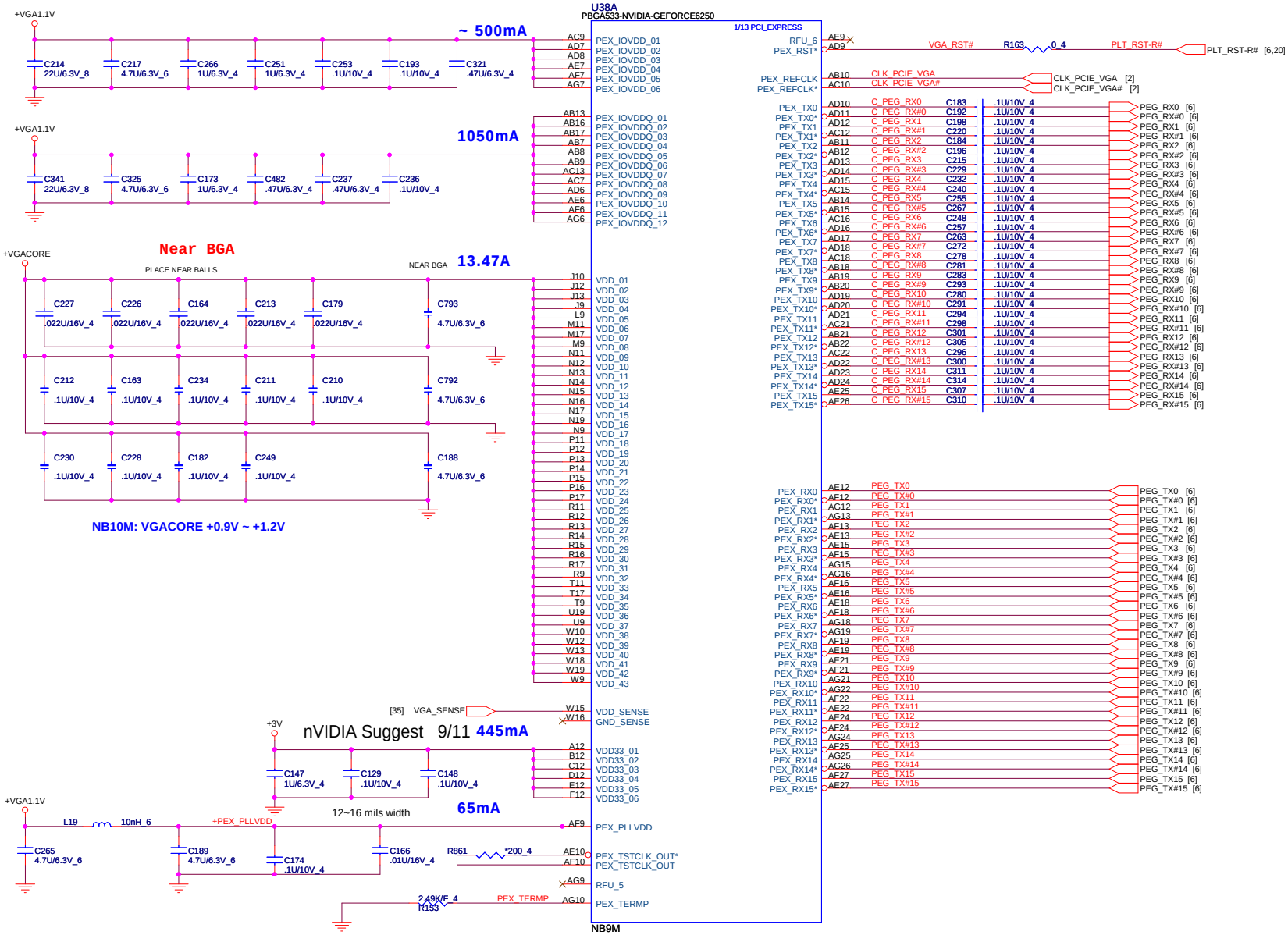


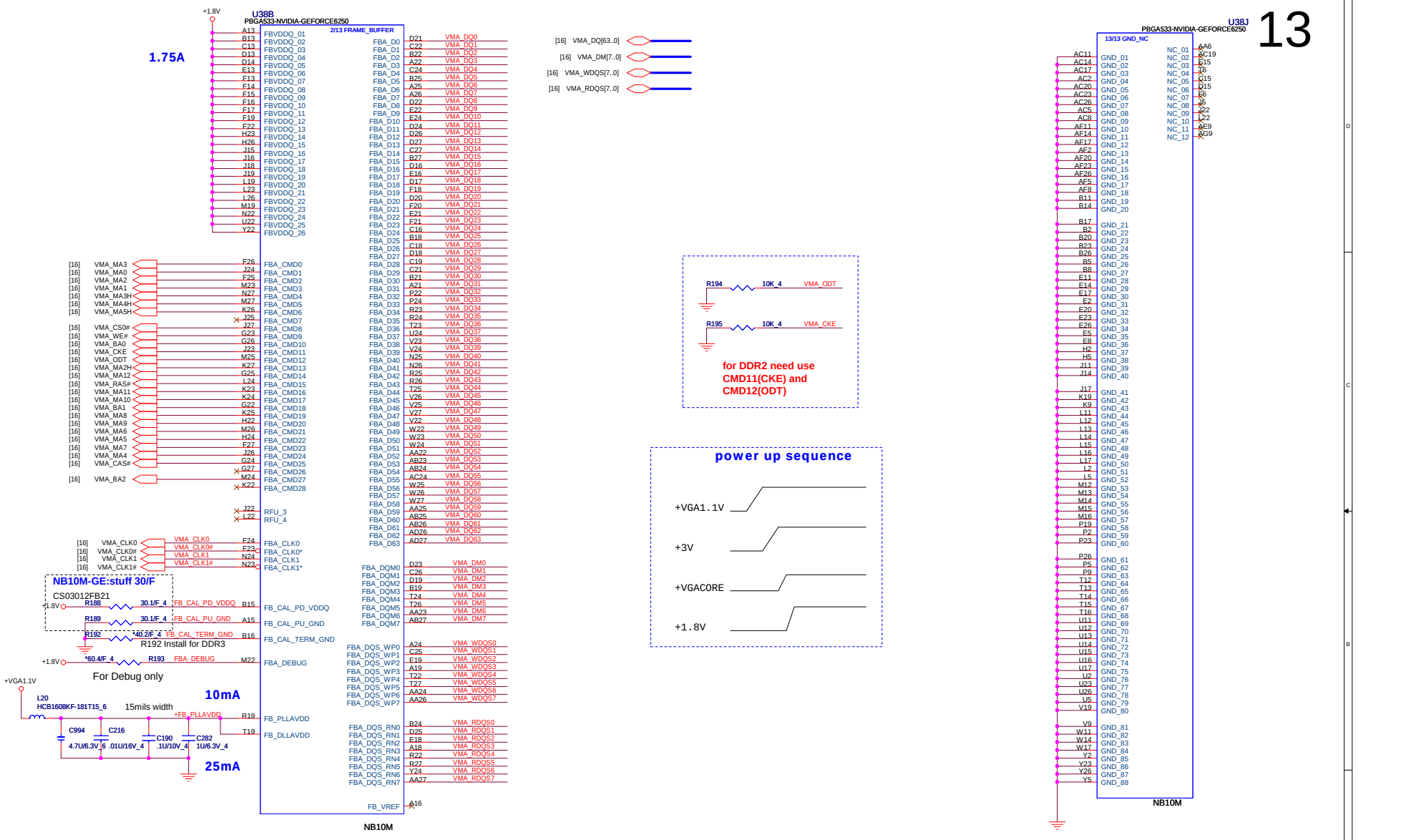


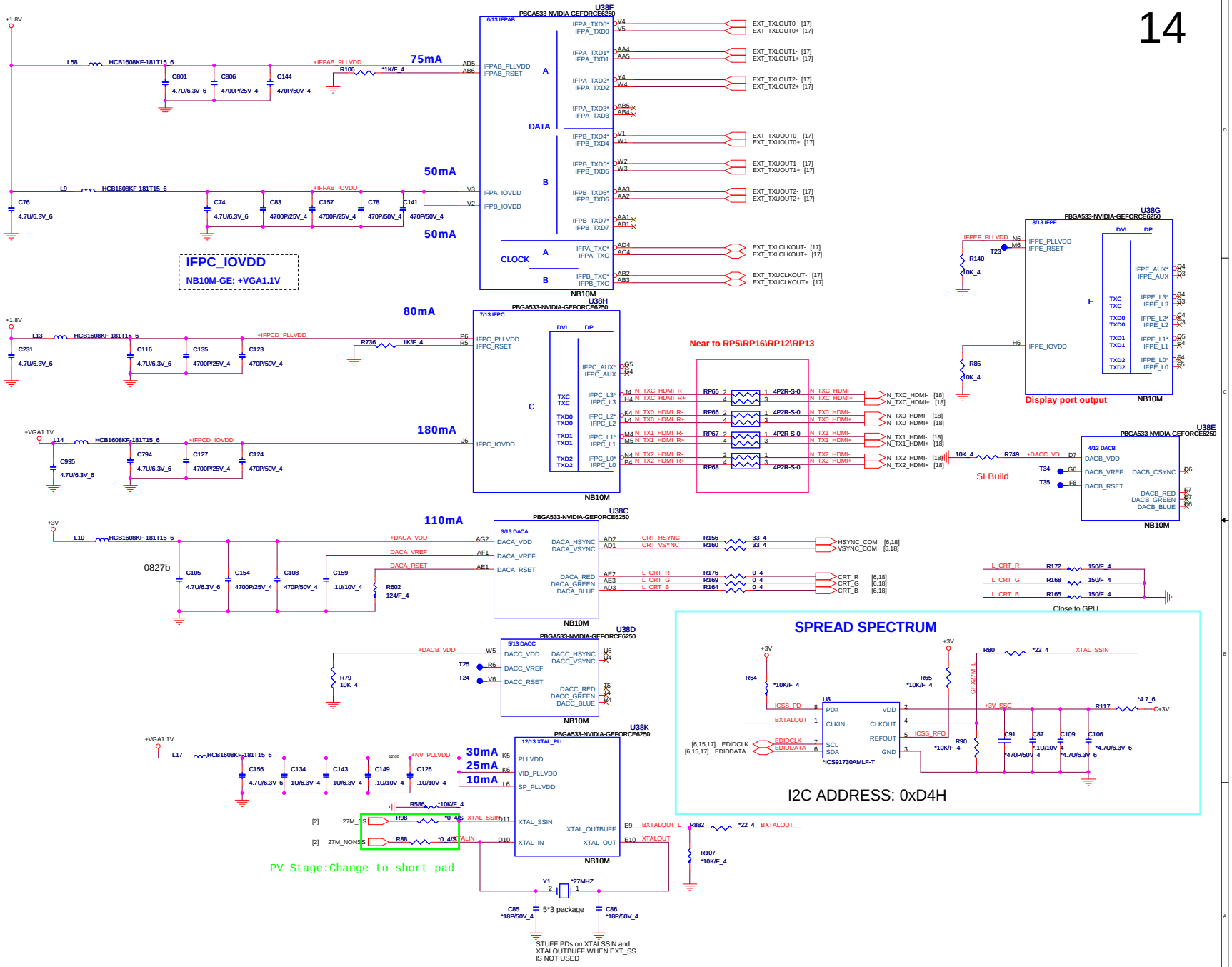
+0.9VSMVTT [36]

+3V [2,4,6,9,10,12,14,15,17,18,19,20,21,22,24,25,26,27,28,29,30,33,34,37]

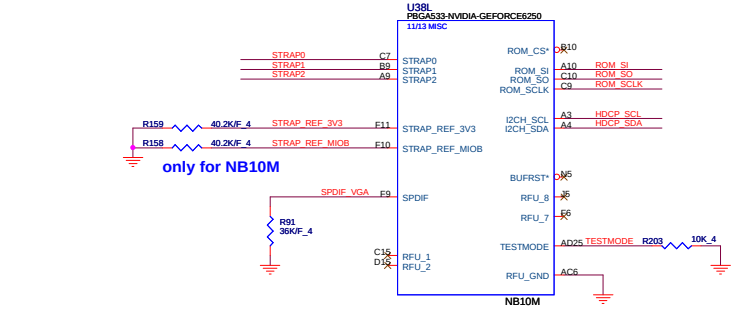
NB5	PROJECT : OP6/7 Quanta Computer Inc.	
Size: Custom	Document Number: DDR2 termination	Rev: SI
Date: Tuesday, January 20, 2009	Sheet 11 of 37	


U38A
PBGA533-NVIDIA-GEFORCE6250
1/13 PCI_EXPRESS
~ 500mA
1050mA
Near BGA
13.47A
NEAR BGA
PLACE NEAR BALLS
NB10M: VGACORE +0.9V ~ +1.2V
nVIDIA Suggest 9/11 445mA
65mA
12~16 mils width
NB9M



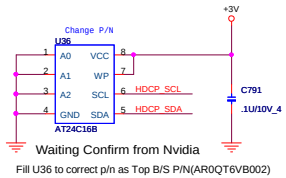


PROJECT : OP6/7 Quanta Computer Inc.			
NB5	Size: Custom	Document Number: NV10M (DISPLAY) 3/5	Rev: DB
	Date: Tuesday, January 20, 2009	Sheet 14 of 37	



DB:Remove GPU thermal sensor footprint

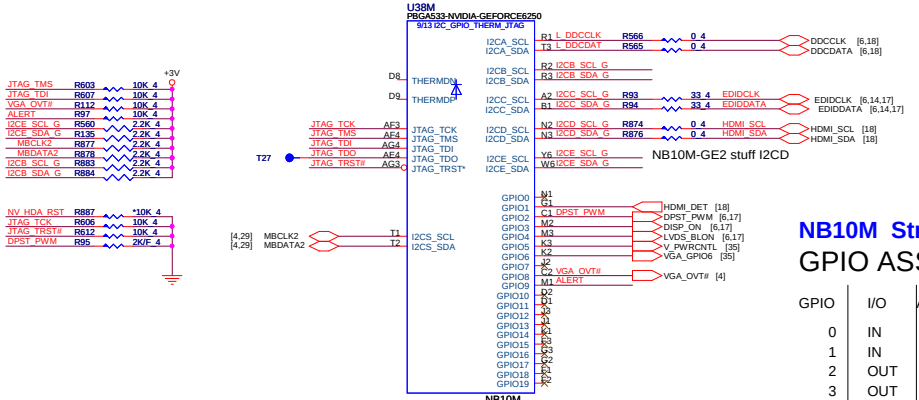
HDCP ROM

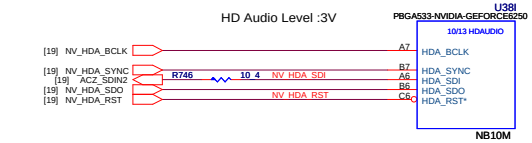


Waiting Confirm from Nvidia

Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM





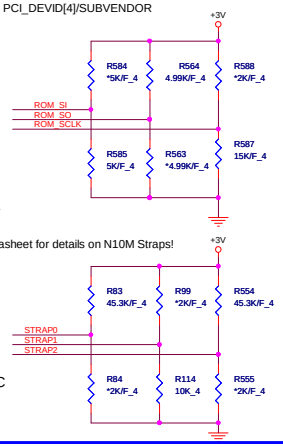
NB10M Strraps

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

SEE Datasheet for details on N10M Straps!

PCI_DEVID[4]/SUBVENDOR



RAM ID: ROM_SI R585

64M*16 HYN 0000 PD 5K
SAM 0001 PD 10K
QIM 0010 PD 15K

	Logical	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE2]	TVMODE[1]	TVMODE[0]	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

PCI_DEVID: STRAP2 R554

NB10M-GE2 0x6EF 8 1111 PU 45K

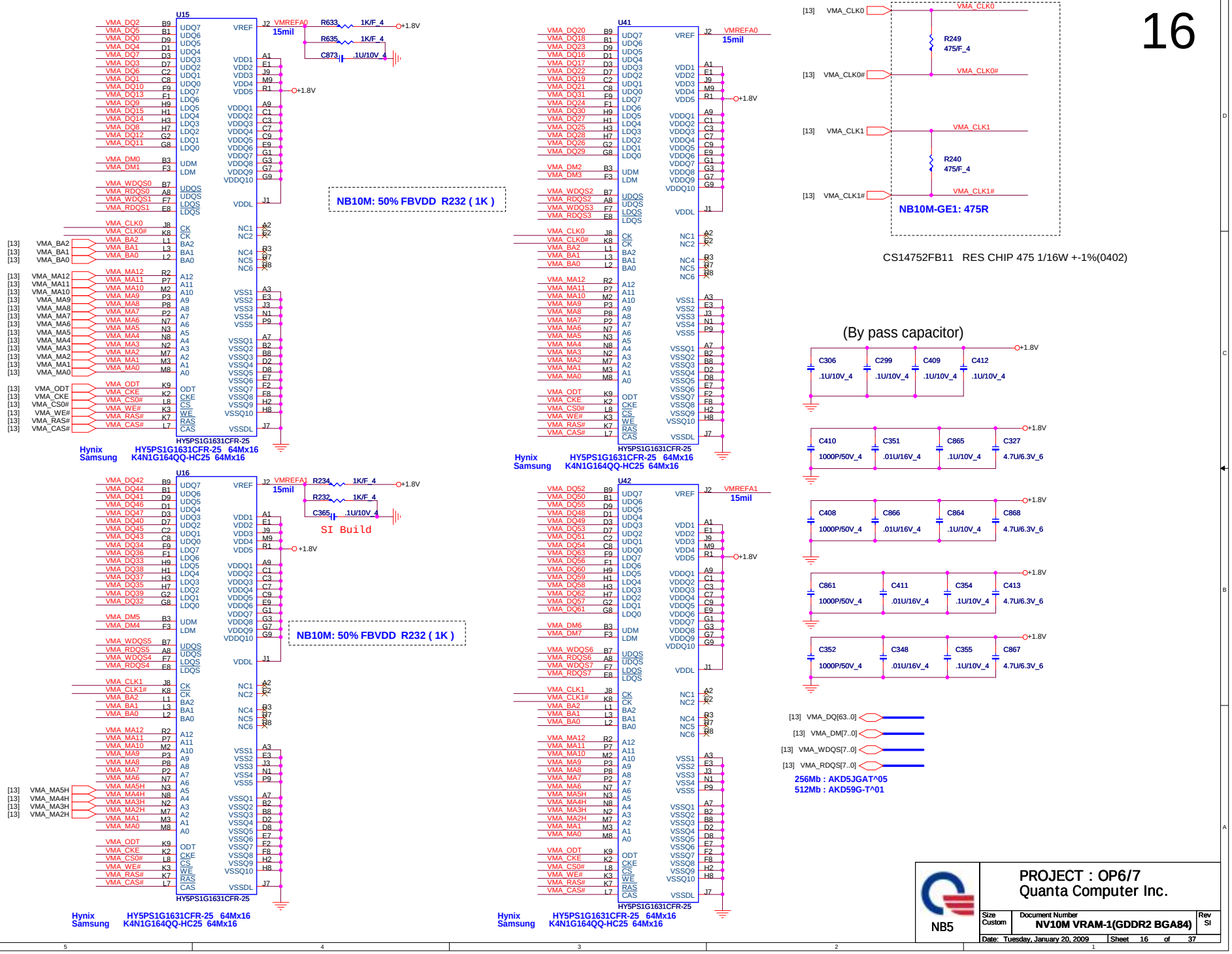
Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

NB10M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor	
0000	DDR2 64Mx16x4, 64bit, 512MB	Hynix	H5PS1G63EFR-20L
0001	DDR2 64Mx16x4, 64bit, 512MB	Samsung	K4N1G164QQ-HC20
0010	DDR2 64Mx16x4, 64bit, 512MB	Qimonda	HYB18T1G161C2F-20

NB5	PROJECT : OP6V2 Quanta Computer Inc.		
	Size: C	Document Number: NV10M (GPIO & STRRAPS) 4/5	Rev: DB
	Date: Tuesday, January 20, 2009	Sheet 15 of 37	



PROJECT : OP6/7
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	NV10M VRAM-1(GDDR2 BGA84)	SI

Date: Tuesday, January 20, 2009 Sheet 16 of 37

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB FOR UMA VGA

[6]	LA_CLK	RP9	*0_4P2R	TXLCLKOUT+	
[6]	LA_CLK#			TXLCLKOUT-	
[6]	LA_DATAN0	RP1	*0_4P2R	TXLOUT0-	
[6]	LA_DATAP0			TXLOUT0+	
[6]	LA_DATAP1	RP4	*0_4P2R	TXLOUT1+	
[6]	LA_DATAN1			TXLOUT1-	
[6]	LA_DATAP2	RP7	*0_4P2R	TXLOUT2+	
[6]	LA_DATAN2			TXLOUT2-	
[6]	LB_CLK#	RP20	*0_4P2R	TXUCLKOUT-	
[6]	LB_CLK			TXUCLKOUT+	
[6]	LB_DATAP0	RP11	*0_4P2R	TXUOUT0+	
[6]	LB_DATAN0			TXUOUT0-	
[6]	LB_DATAP1	RP15	*0_4P2R	TXUOUT1+	
[6]	LB_DATAN1			TXUOUT1-	
[6]	LB_DATAN2	RP23	*0_4P2R	TXUOUT2-	
[6]	LB_DATAP2			TXUOUT2+	

OPTION SIGNAL FROM Nvidia to VGA

[14]	EXT_TXLCLKOUT+	RP8	0_4P2R	TXLCLKOUT+	
[14]	EXT_TXLCLKOUT-			TXLCLKOUT-	
[14]	EXT_TXLOUT0+	RP2	0_4P2R	TXLOUT0+	
[14]	EXT_TXLOUT0-			TXLOUT0-	
[14]	EXT_TXLOUT1+	RP3	0_4P2R	TXLOUT1+	
[14]	EXT_TXLOUT1-			TXLOUT1-	
[14]	EXT_TXLOUT2+	RP6	0_4P2R	TXLOUT2+	
[14]	EXT_TXLOUT2-			TXLOUT2-	
[14]	EXT_TXUCLKOUT+	RP19	0_4P2R	TXUCLKOUT+	
[14]	EXT_TXUCLKOUT-			TXUCLKOUT-	
[14]	EXT_TXUOUT0+	RP10	0_4P2R	TXUOUT0+	
[14]	EXT_TXUOUT0-			TXUOUT0-	
[14]	EXT_TXUOUT1-	RP14	0_4P2R	TXUOUT1-	
[14]	EXT_TXUOUT1+			TXUOUT1+	
[14]	EXT_TXUOUT2-	RP22	0_4P2R	TXUOUT2-	
[14]	EXT_TXUOUT2+			TXUOUT2+	

+3V
R520 2.2K_4 EDIDCLK
R522 2.2K_4 EDIDDATA

[2,4,6,9,10,11,12,14,15,18,19,20,21,22,24,25,26,27,28,29,30,33,34,37] +3V
[3,18,22,24,25,26,28,29,37] +5V
[31,32,33,34,35,36,37] +VIN
[19,23,24,26,28,29,31,32,37] +3VPCU
[32,37] +12VALW

+VIN_BLIGHT
+VIN L53 FBM2125 HM330-T +VIN_BLIGHT
C753 .1U/50V_6
C751 .01U/50V_6
C750 .1U/50V_6
C6 *10U/25V_12

+3VLCD_CON
+3V
C9 1000P/50V_4
[6,14,15] EDIDCLK
[6,14,15] EDIDDATA

+5V
U10
VIN VOUT
SHDN
GND SET
AT5231H-3.9KER
C153 1U/6.3V_4
R119 *0_6
R139 *215K/F_4
R142 *100K/F_4
+3V +3.9V_CAM
C115 4.7U/6.3V_6
[20]
[20]

SI-2 modified for fix camera power fail

TXLOUT0- TXLOUT0+
TXLOUT1- TXLOUT1+
TXLOUT2- TXLOUT2+
TXLCLKOUT- TXLCLKOUT+
TXUOUT0- TXUOUT0+
TXUOUT1- TXUOUT1+
TXUOUT2- TXUOUT2+
TXUCLKOUT- TXUCLKOUT+
VADJ1
BLON_CON

CN1
GS12401-1011-40P-R-NH

L16 *WCM2012-90
USBP3+
USBP3-
+3.9V_CAM
C122 .01U/16V_4
C117 *4.7U/6.3V_6

EMI

+VIN
C761 C762 C763 C764 C765 C789 C790
.1U/50V_6

[6,15] DPST_PWM DPST_PWM R526 *0_4
[29] PWM_VADJ PWM_VADJ R524 *0_4/S VADJ1
C754 *4.7U/6.3V_6
C756 .1U/10V_4

+12VALW
R10 330K_6
Q1 AO3404
C12 .1U/10V_4
+3V

+5VSUS
R527 100K/F_4
Q25 DTC144EUA
Q26 2N7002
[6,15] DISP_ON
C759 .022U/16V_4
LCDONG
LCDON#
Q27 2N7002
+3VLCD
L52 PBY201209T-4A/08
R516 22_8
LCDDISCHG
+3VLCD_CON
C757 .01U/16V_4
C746 .1U/10V_4
C748 10U/6.3V_8

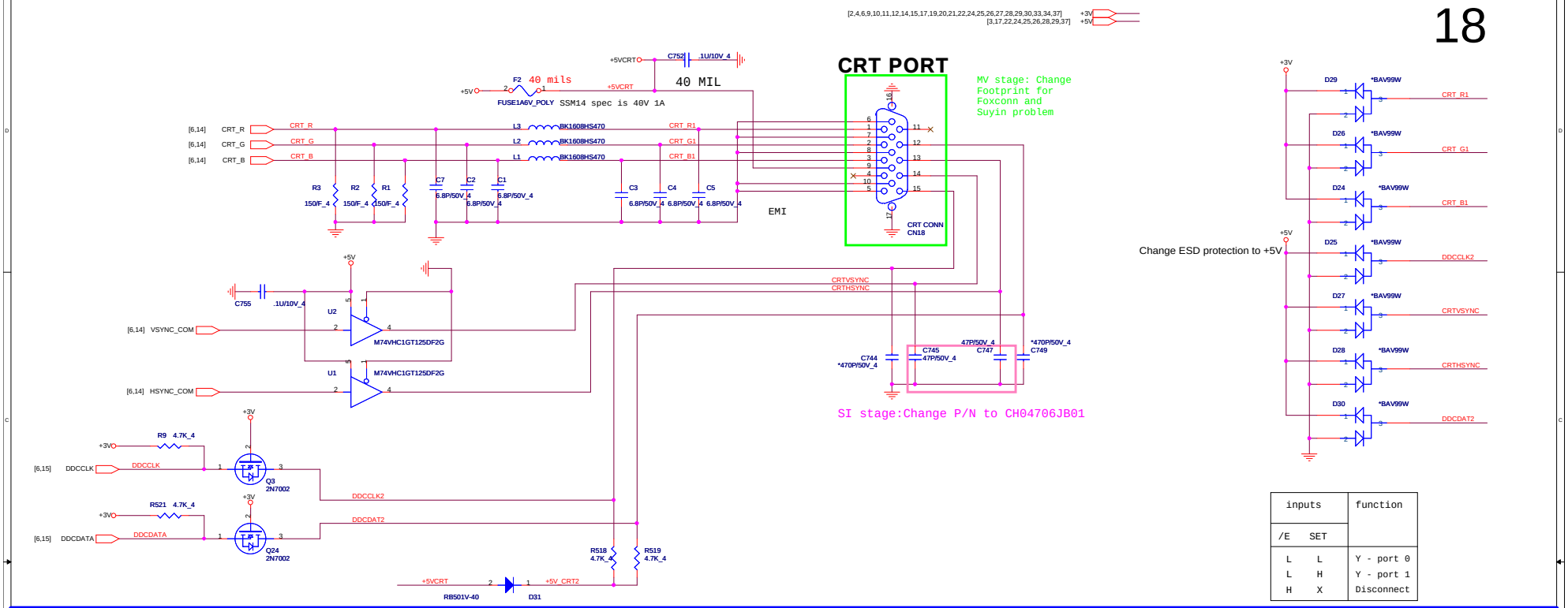
EMI add
+3V +3V +3V
C1027 .1U/10V_4
C1028 .1U/10V_4
C1029 .1U/10V_4

D1 RB501V-40
PN_BLON
BLON_CON
R4 100K/F_4
C8 22P/50V_4

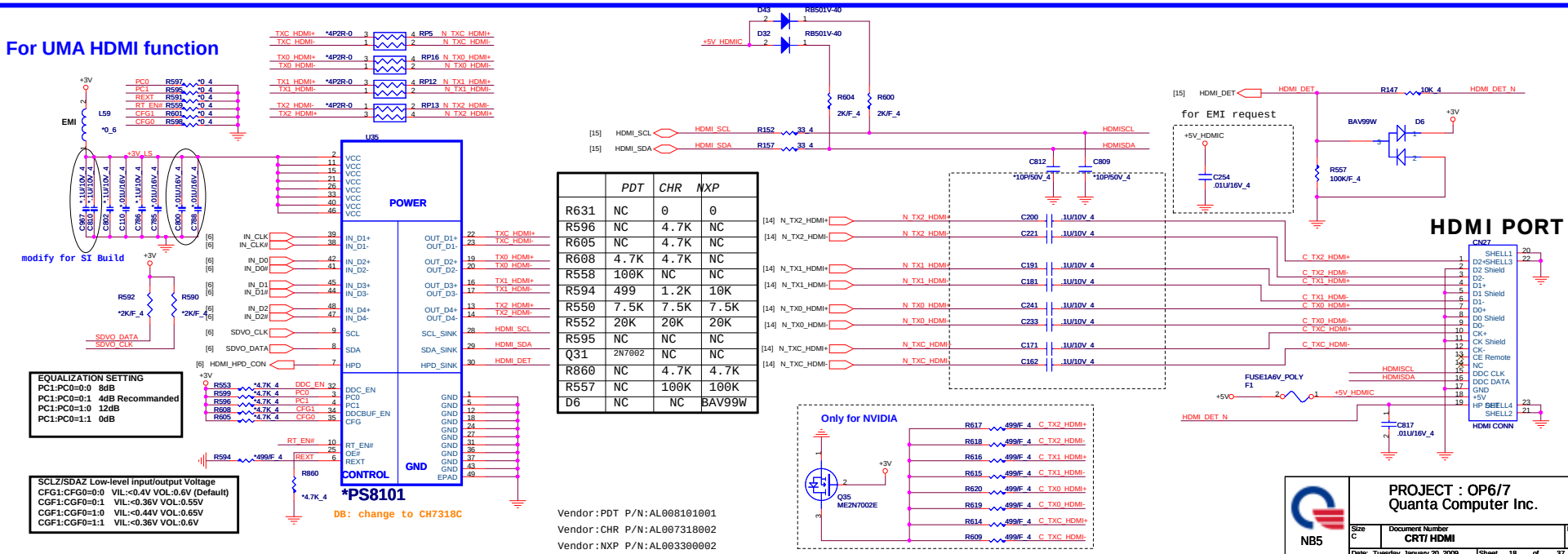
+3VPCU
R8 33K_6
Close to EC
[6,15] LVDS_BLON
R6 1K/F_4
D2 RB501V-40
LID_EC# [28,29]
Q2 DTC144EUA
[21] LCD_BK

DISP_ON R525 100K/F_4
LVDS_BLON R7 100K/F_4

NB5	PROJECT : OP6/7 Quanta Computer Inc.	
	Size: B Document Number: LCD CONN/Lid function	Rev: SI
	Date: Tuesday, January 20, 2009 | Sheet 17 of 37	



For UMA HDMI function



	PDT	CHR	NXP
R631	NC	0	0
R596	NC	4.7K	NC
R605	NC	4.7K	NC
R608	4.7K	4.7K	NC
R558	100K	NC	NC
R594	499	1.2K	10K
R550	7.5K	7.5K	7.5K
R552	20K	20K	20K
R595	NC	NC	NC
Q31	2N7002	NC	NC
R860	NC	4.7K	4.7K
R557	NC	100K	100K
D6	NC	NC	BAV99W

Vendor:PDT P/N:AL008101001
Vendor:CHR P/N:AL007318002
Vendor:NXP P/N:AL003300002

NB5	PROJECT : OP6/7 Quanta Computer Inc.		
	Size C	Document Number CRT/ HDMI	Rev SI
	Date: Tuesday, January 20, 2009	Sheet 18 of 37	

DB: change from 18P to 15P(TXC suggestion)

[17,23,24,26,28,29,31,32,37] +3VPCU
[22] +3VRTC
[2,4,6,9,10,11,12,14,15,17,18,20,21,22,24,25,26,27,28,29,30,33,34,37] +3V
[4,9,20,22,28,30,33,37] +1.5V
[2,3,4,5,6,8,9,22,33,34] +1.05V
[20,21,22,37] +3VS5

20MIL

modify for SI Build
For CR2032(Large)

update footprint (0830)

MV change R331,R327,R330,R326 to 49.9 ohm

Delete Pin AG7 for Lan_DISABLE#

Notice: GPIO33 is also a strap pin. Don't pull it to high.

HP Request

SATA HDD1

SATA ODD

E-SATA CONNECT

For HD Audio

For MDC

For UMA

Close to U45

For Discrete

U45A

ICH9M REV 1.0

SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS

Select	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

TPM physical presence	
ICH_GPIO57	Low: Default

PROJECT : OP6/7
Quanta Computer Inc.

NB5

Size: Custom | Document Number: ICH9-M Host 1/4 | Rev: SI

Date: Tuesday, January 20, 2009 | Sheet 19 of 37

MINI CARD PCI-E(WLAN)

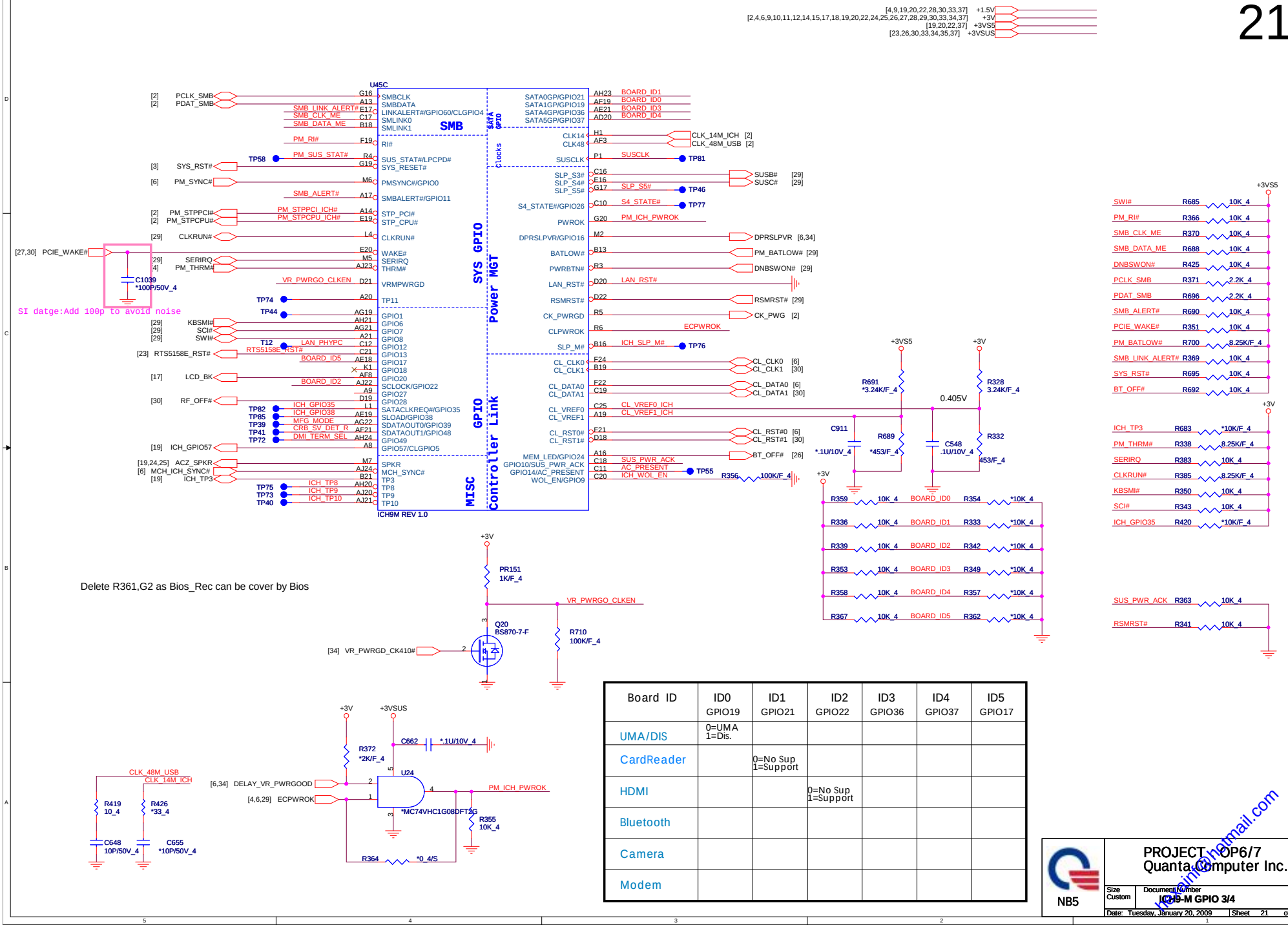
PCIE-LAN

E-SATA and USB Connector
USB Connector
FINGERPRINT
Carama USB
Docking
BLUETOOTH
Cardread
NEW CARD
USB Connector
USB Connector
Robson Min-Card
TV Min-Card

remove HDCP ROM

512K byte SPI ROM
For HDCP only

EMI 0828



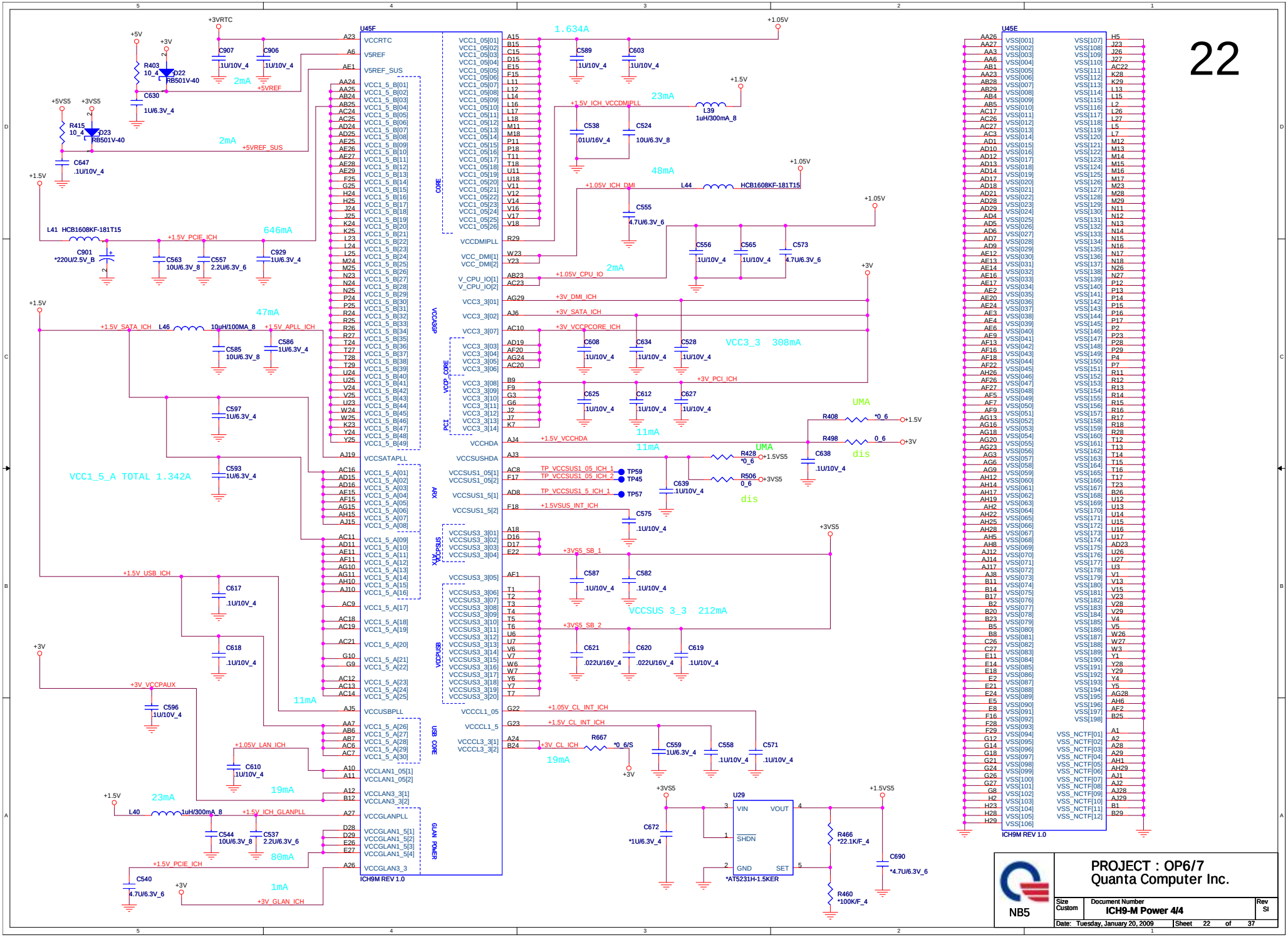
Board ID	ID0 GPIO19	ID1 GPIO21	ID2 GPIO22	ID3 GPIO36	ID4 GPIO37	ID5 GPIO17
UMA/DIS	0=UMA 1=Dis.					
CardReader		0=No Sup 1=Support				
HDMI			0=No Sup 1=Support			
Bluetooth						
Camera						
Modem						

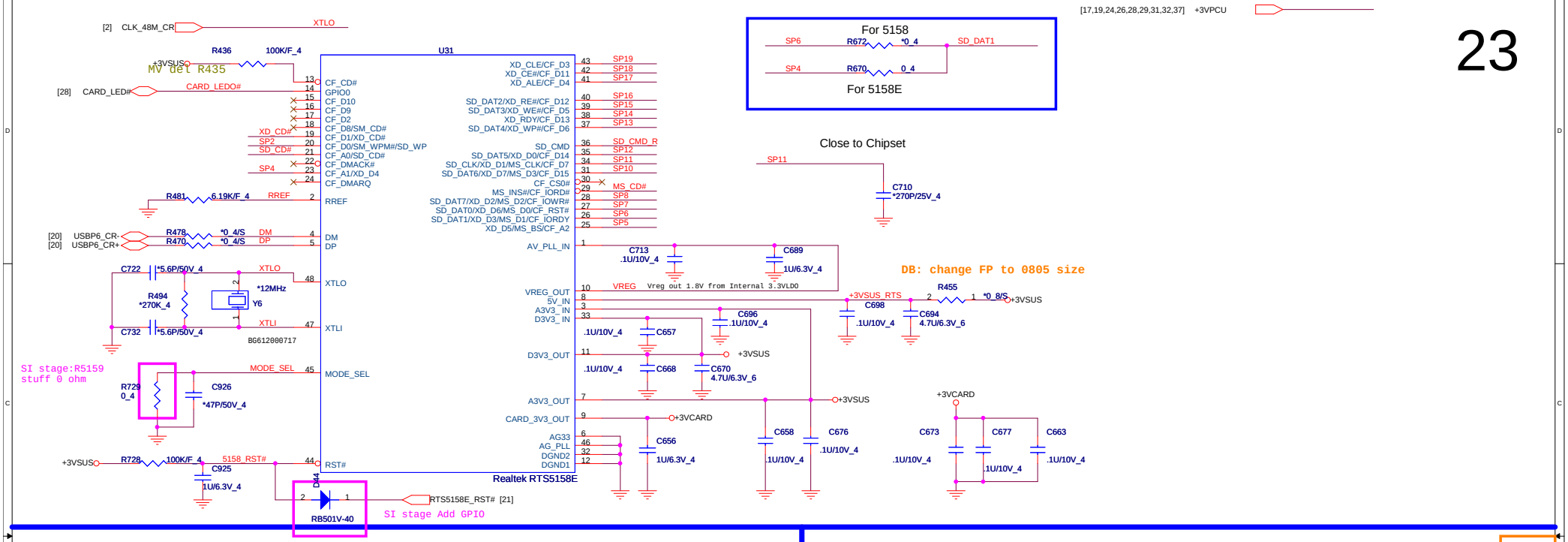
NB5

PROJECT : OP6/7
Quanta Computer Inc.

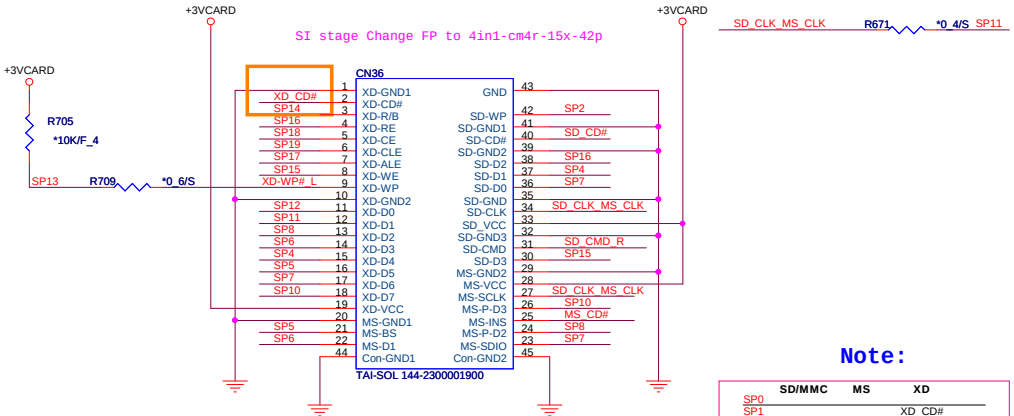
Size	Document Number	Rev
Custom	ICH9-M GPIO 3/4	SI

Date: Tuesday, January 20, 2009 | Sheet 21 of 37

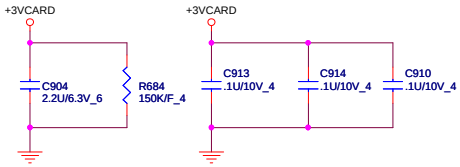

U45F
U45E
VCC1_5_A TOTAL 1.342A
VCCUSUS 3_3 212mA
VCC3_3 308mA
1.634A
23mA
48mA
2mA
646mA
47mA
11mA
19mA
80mA
1mA
UMA
dis
ICH9M REV 1.0
PROJECT : OP6/7
Quanta Computer Inc.
NB5
ICH9-M Power 4/4
Tuesday, January 20, 2009
22



4 IN1 CARD READER XD,/SD,MS/MSP

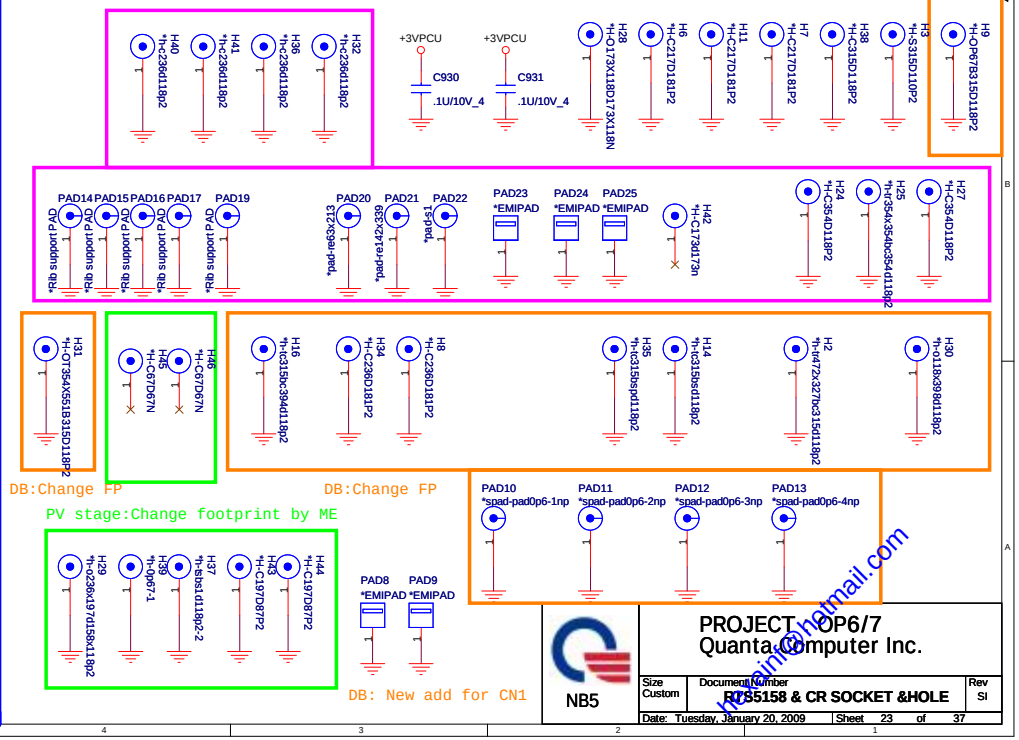


CLOSE CONN



Note:

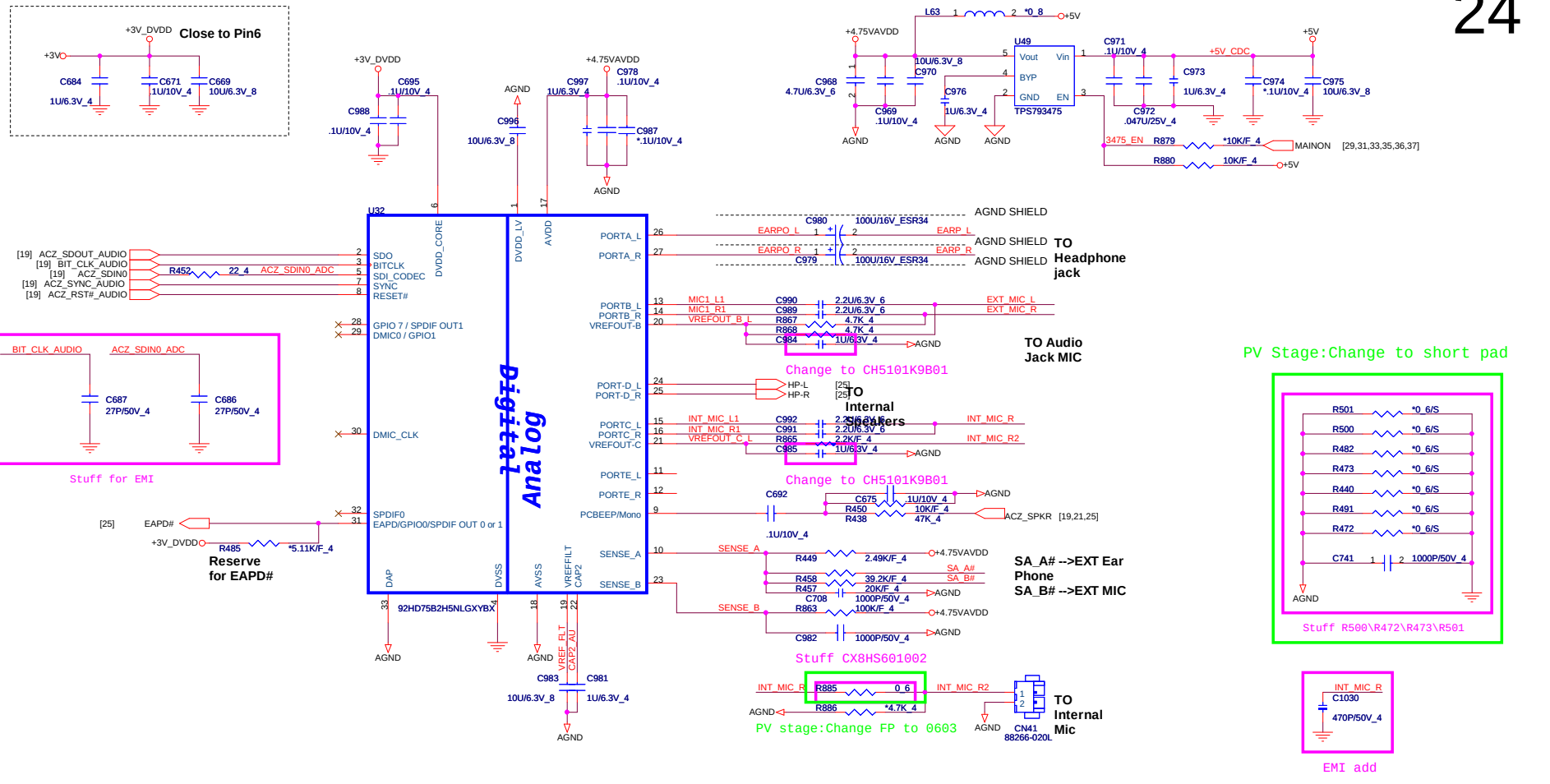
	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

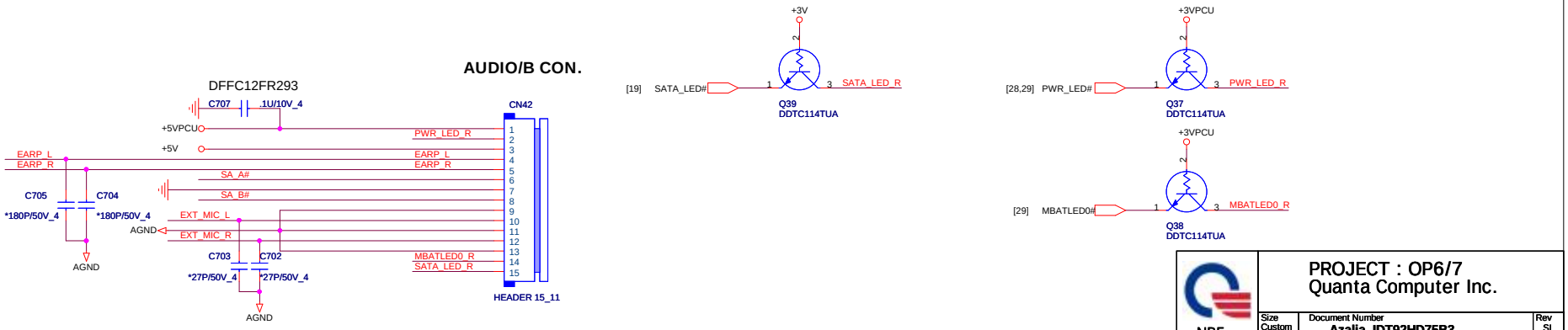


NB5

PROJECT : OP6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5158 & CR SOCKET &HOLE	SI
Date: Tuesday, January 20, 2009	Sheet 23 of 37	





NB5

PROJECT : OP6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia IDT92HD75B3	SI

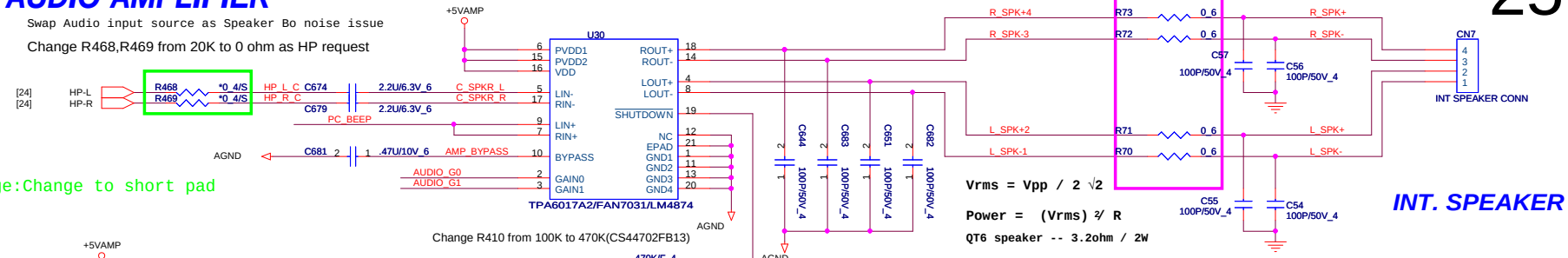
Date: Tuesday, January 20, 2009 | Sheet 24 of 37

AUDIO AMPLIFIER

Swap Audio input source as Speaker Bo noise issue

Change R468,R469 from 20K to 0 ohm as HP request

Change P/N to CX8HS601002 for EMI



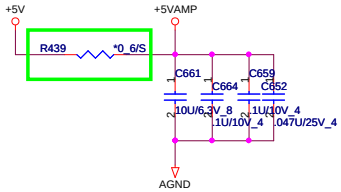
PV Stage:Change to short pad

Vrms = Vpp / 2 √2

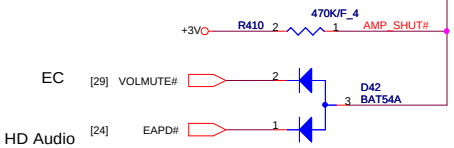
Power = (Vrms) ² / R

QT6 speaker -- 3.2ohm / 2W

INT. SPEAKER



Change R410 from 100K to 470K(CS44702FB13)



AL001431K04

AL6017A2K12

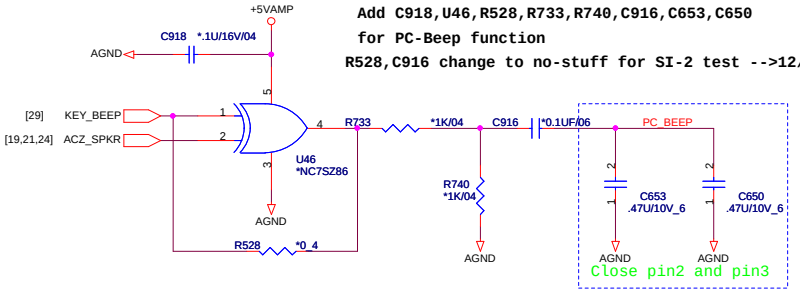
APA2031 ,AL002031K00

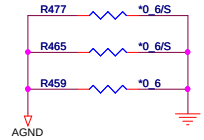
6017A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

Add C918,U46,R528,R733,R740,C916,C653,C650 for PC-Beep function

R528,C916 change to no-stuff for SI-2 test -->12/6



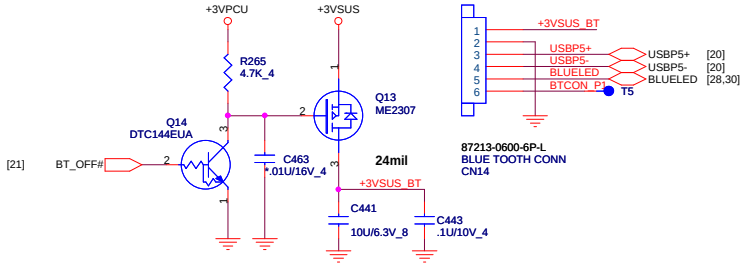


NB5

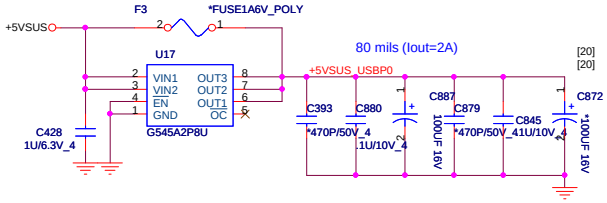
PROJECT : OP6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6047A4/Accelerometer	SI
Date: Tuesday, January 20, 2009	Sheet 25 of 37	

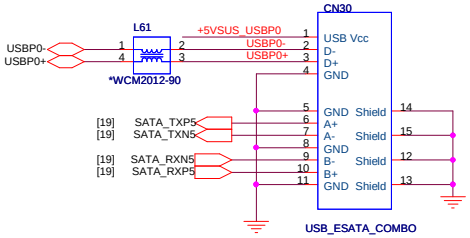
BLUETOOTH



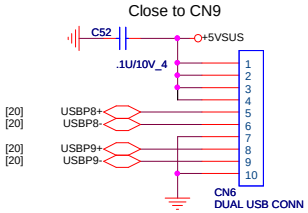
LEFT SIDE USBX1 and E-SATA/USB COMBO



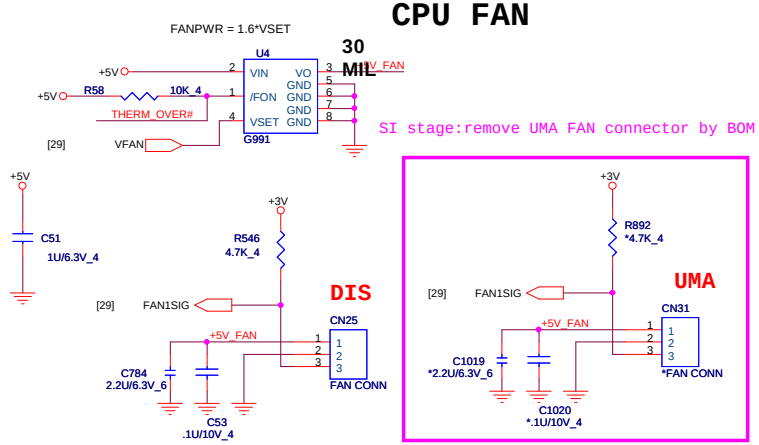
USB & ESATA



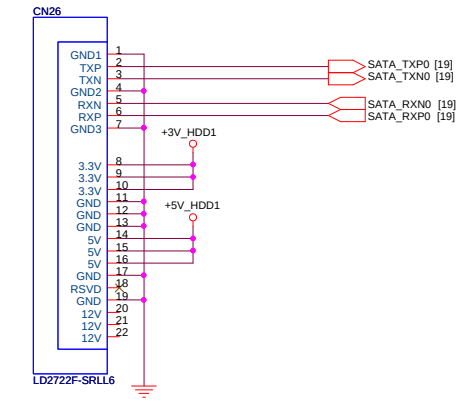
RIGHT SIDE USBX2

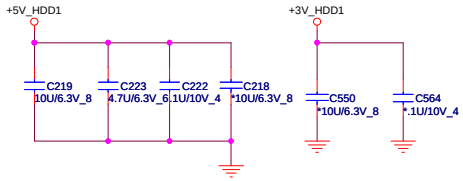


CPU FAN

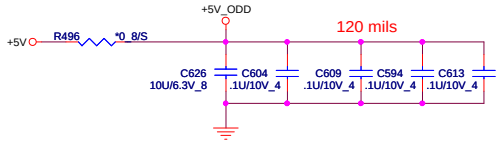


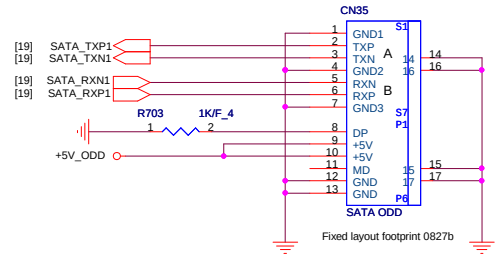
SATA_1 CONNECTOR





SATA CD-ROM





CN35 part number

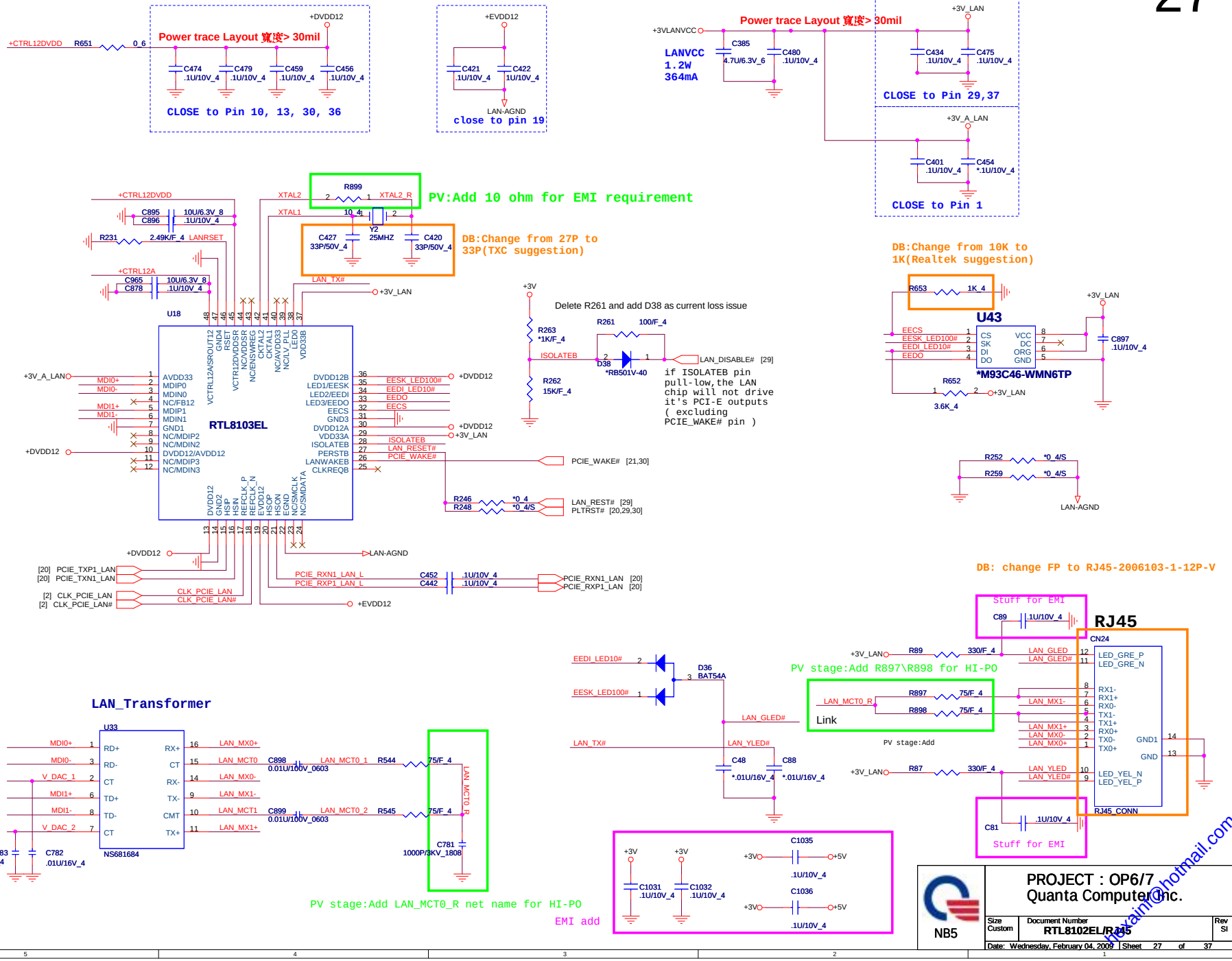
UT3	DFHD13MR006
	DFHD13MR008
	DFHD13MR009
UT5	DFHS13FR030
	DFHS13FR040

NB5

PROJECT : OP6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/ESATA/USB/ODD/HDD	SI

Date: Tuesday, January 20, 2009 Sheet 26 of 37


Power trace Layout 寬度> 30mil
CLOSE to Pin 10, 13, 30, 36
close to pin 19
LANVCC
1.2W
364mA
Power trace Layout 寬度> 30mil
CLOSE to Pin 29,37
CLOSE to Pin 1
PV:Add 10 ohm for EMI requirement
DB:Change from 27P to 33P(TXC suggestion)
DB:Change from 10K to 1K(Realtek suggestion)
Delete R261 and add D38 as current loss issue
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)
RTL8103EL
U43
*M93C46-WMN6TP
DB: change FP to RJ45-2006103-1-12P-V
RJ45
LAN_Transformer
NS681684
PV stage:Add R897\R898 for HI-PO
PV stage:Add LAN_MCT0_R net name for HI-PO
EMI add
Stuff for EMI
Link
PROJECT : OP6/7
Quanta Computer Inc.
RTL8102EL/RT45
NB5
Date: Wednesday, February 04, 2009
Sheet 27 of 37

POWER BOTTON CONNECT

1. +3VPCU(LIDSWITCH PWR)
2. LIDSWITCH
3. GND
4. RF_SW#
5. +5VPCU (PWRLED PWR)
6. NUMLED#
7. POWERON#
8. PWR_LED#
9. WLSLED_ON#
10. WLSLED_OFF#

DB:Add C1023\C1024 for EMI

DB:Add Q49 to control wireless LED

Close LED3

Close LED7

Close LED2

Close LED1

Close LED8

Blue

Amber

PV Stage:modify LED control by EC

KEYBOARD PULL-UP

Footprint: "gb1rf260-1253-7f-26p-l

R430 Change to 100k ohm ,pull low

MDC

DB: change FP to H-C217D147P2

DB: change FP to MDC-1-179373-2-12P-RUV

SI modified

FOR 16"

FOR 17.3"

Del R167

PROJECT : OP6/7	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: KB/LED/POWER CONN/MDC; Rev: SI
Date: Tuesday, January 20, 2009	Sheet 28 of 37

TOUCH PAD CONNECTOR

25 mils

Fixed Library 8/28

CN13 TOUCH PAD CONN

Add for EMI

close conn

TOUCH PAD L/R FOR 17" only

CN43 BL123-04R-TAND

PV stage:Pin4 connect to GND for EMI requirement

TOUCH PAD ON/OFF FOR 16"

SW2 TMG-533-S-V-TR

TOUCH PAD L/R FOR 16"

SW3 SW6 TMG-533-S-V-TR

TOUCH PAD ON/OFF FOR 17.3"

SW4 PA TMG-533-S-V-TR

U20 KB3926 C0

user for B1

For KB3926 B, C version

SI modified

DB:Change from 18P to 27P(TXC suggestion)

Hi ==> 120W

Low ==> 65W/90W

ID	R851	R852
OP7	10K	N/A
OP6	N/A	10K

2M byte SPI BIOS

SPI ROM

Add Pin 117,103 for DSM,Pin 116 for Bluetooth,Pin 23 for Key Beep to Amplifier

Add T37,T38,T39 for EC
Delete T10 and tie pin 117 from Lan for DSM

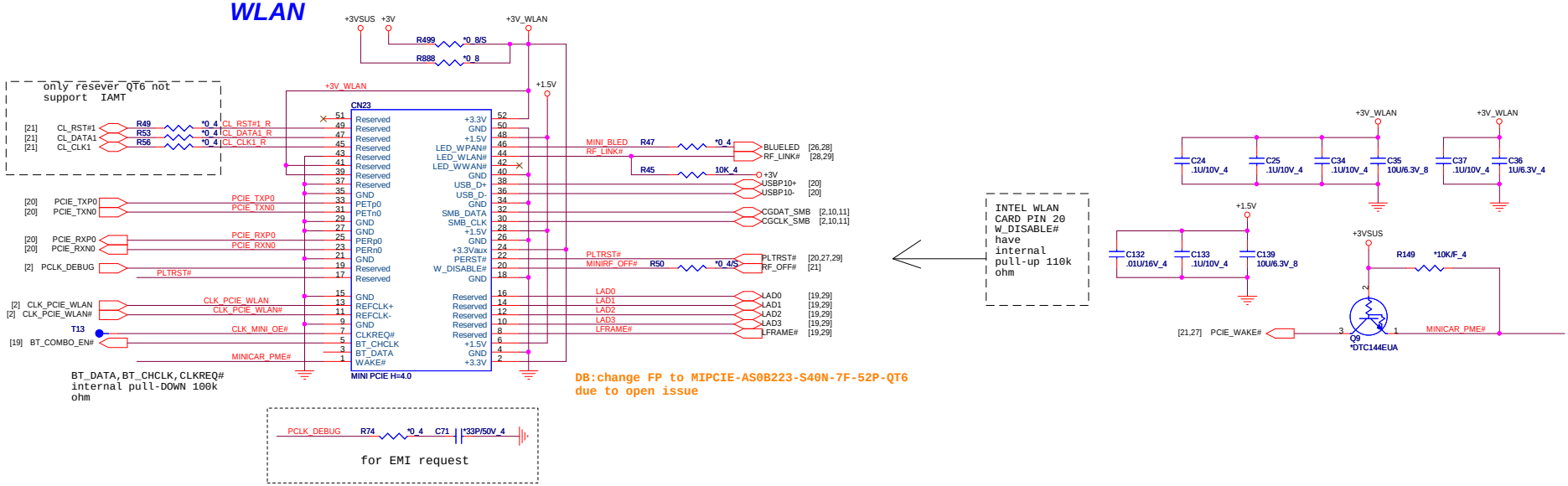
EMI Change value

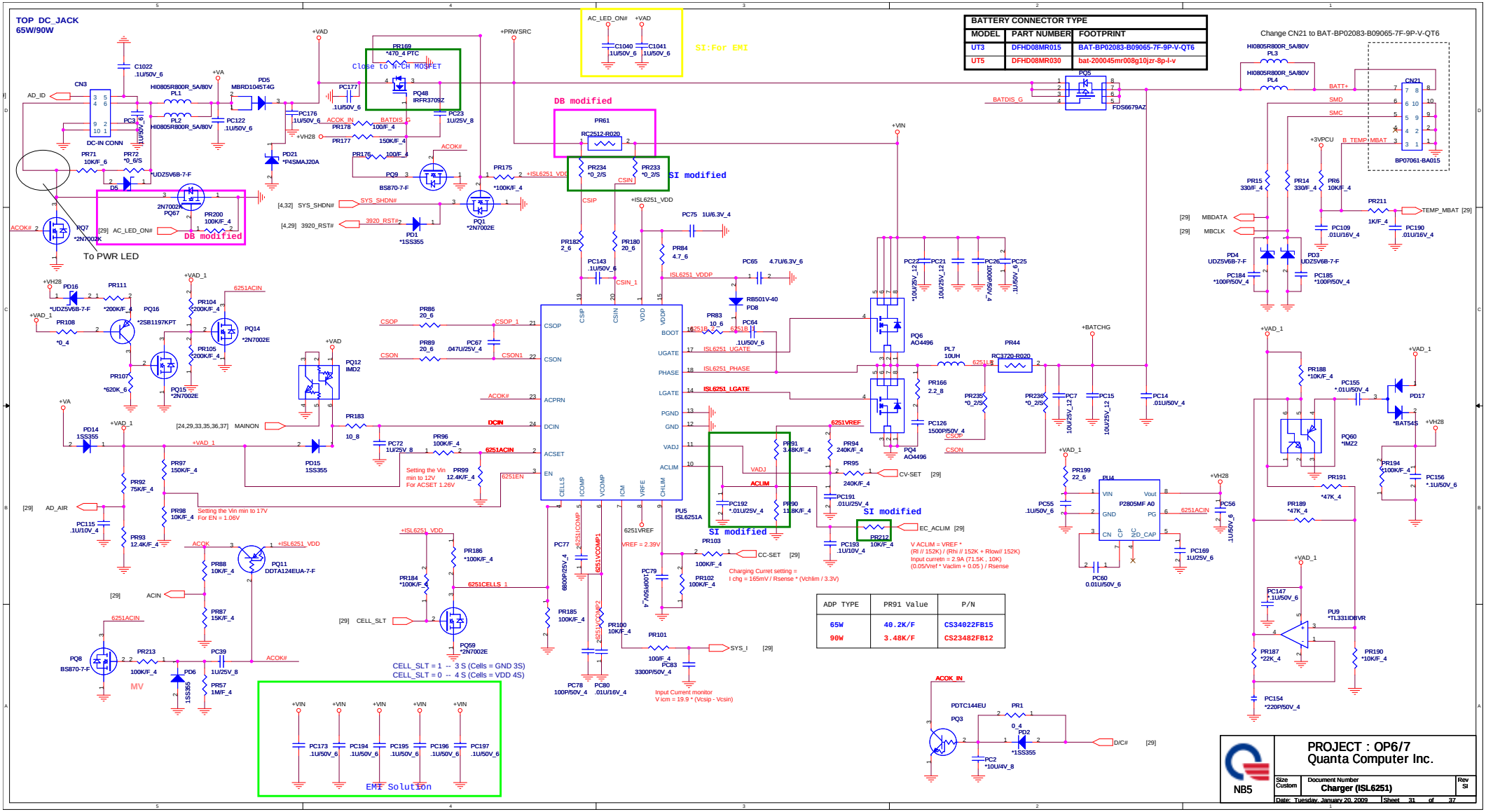
EMI Change value

PROJECT	OP6/7
Quanta Computer Inc.	
Size	Custom
Document Number	KB3926/ROM/TP
Rev	SI
Date	Tuesday, January 20, 2009
Sheet	29 of 37

NB5

Mini PCI-E Card 1
WLAN





DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 9A

SI modified

SI modified

Rds(on) 20m ohm

Rds(on) 20m ohm

PU2 TPS51427A

9	BYP	REFIN2	32
10	OUT1	ILIM2	31
11	FB1	OUT2	30
12	ILIM1	SKIP	29
13	PGOOD1	PGOOD2	28
14	ON1	ON2	27
15	DH1	DH2	26
16	LX1	LX2	25
37	PAD		
36	PAD		
39	PAD		
40	PAD		
38	PAD		
35	PAD		
34	PAD		
33	PAD		
17	BST1		
18	DL1		
19	VDD		
20	N.C		
21	AGND		
22	PGND		
23	DL2		
24	BST2		
42	PAD		
41	PAD		

8	DOREFIN	REFIN	1
7	LDO	ILIM	2
6	IN	OUT	3
5	N.C	SKIP	4
4	ONLDO	PGOOD	5
3	VCC	ON	6
2	TON	DH	7
1	REF	LX	8

PR21 1K/F_4
PR19 150K/F_4
PR22 *0_6/S
PR214 *0_4
PD48 UDZ5V6B-7-F
PR26 *47_6
PC29 10U/25V_12
PC31 1000P/50V_4
PC30 .1U/50V_6
PC9 4.7U/25V_8
PC130 0.1U/10V_4
PR25 *0_4
PC13 .1U/50V_6
PC12 .1U/10V_4
PC11 1U/6.3V_4
PR20 *0_4/S
PR23 *0_4/S
PR27 309K/F_4
PR39 309K/F_4
PL8 2.5uH/7.5A
PQ55 AO4496
PQ47 AO4468
PC49 .1U/50V_6
PR69 4.7_6
PR47 4.7_6
PC34 .1U/50V_6
PC62 .01U/50V_6
PC63 .01U/50V_6
PC70 0.1U/25V_8
PD12
PD13
BAV99
BAV99
PR73 *SHORT-1A
PC52 1U/6.3V_4
PR45 100K/F_4
PC71 2.2U/50V_8
PC134 330U/6.3V_6X5.8
PC135 .1U/10V_4
PR31 *0_4
PR35 *0_4/S
PR165 2.2_8
PC124 1500P/50V_4
PC186 330P/50V_4
PC4 .1U/50V_6
PC125 1000P/50V_4
PC6 10U/25V_12
PQ49 AO4496
PQ50 AO4468
PL9 2.5uH_7.5A
PR168 2.2_8
PC129 1500P/50V_4
PR29 *0_4/S
PR33 *0_4
PC138 .1U/10V_4
PC144 330U/6.3V_6X5.8
PR36 *0_4/S
PC180 *.1U/10V_4
PC181 *.1U/10V_4

+VIN
+5VALW
+5V_VCC1
+5VPCU
+5V_ALWP
+3VPCU
+3.3V_ALWP
5V_DH
5V_LX
5V_DL
3V_LX
3V_DH
3V_DL
PGOOD1
PGOOD2
+12VALW
+15VALW
[4,31] SYS_SHDN#
HWPG [29,33,35,36]
EMI reserved

NB5

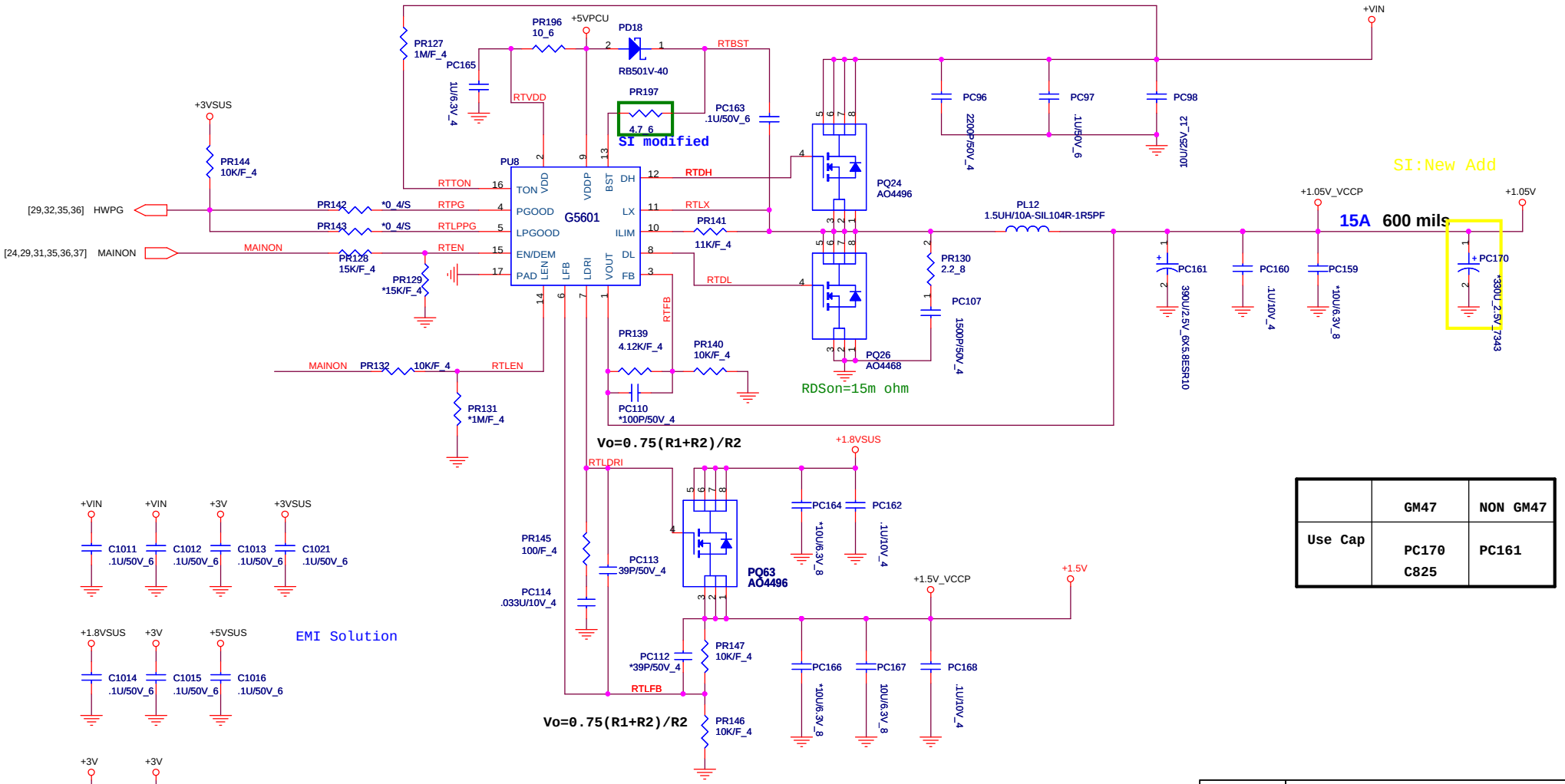
PROJECT : OP6/7
Quanta Computer Inc.

Size	Document Number	Rev
B	+5V/+3V (ISL6237)	SI

Date: Tuesday, January 20, 2009 | Sheet 32 of 37

VCCP1.05V & +1.5V

+1.05Volt +/- 5%
Countinue current:7.5A
Peak current:10A
OCP minimum 15A



EMI Solution

+VIN: C1011 .1U/50V_6, C1012 .1U/50V_6
+3V: C1013 .1U/50V_6
+3VSUS: C1021 .1U/50V_6
+1.8VSUS: C1014 .1U/50V_6
+3V: C1015 .1U/50V_6
+5VSUS: C1016 .1U/50V_6
+3V: C1017 .1U/50V_6, C1018 .1U/50V_6

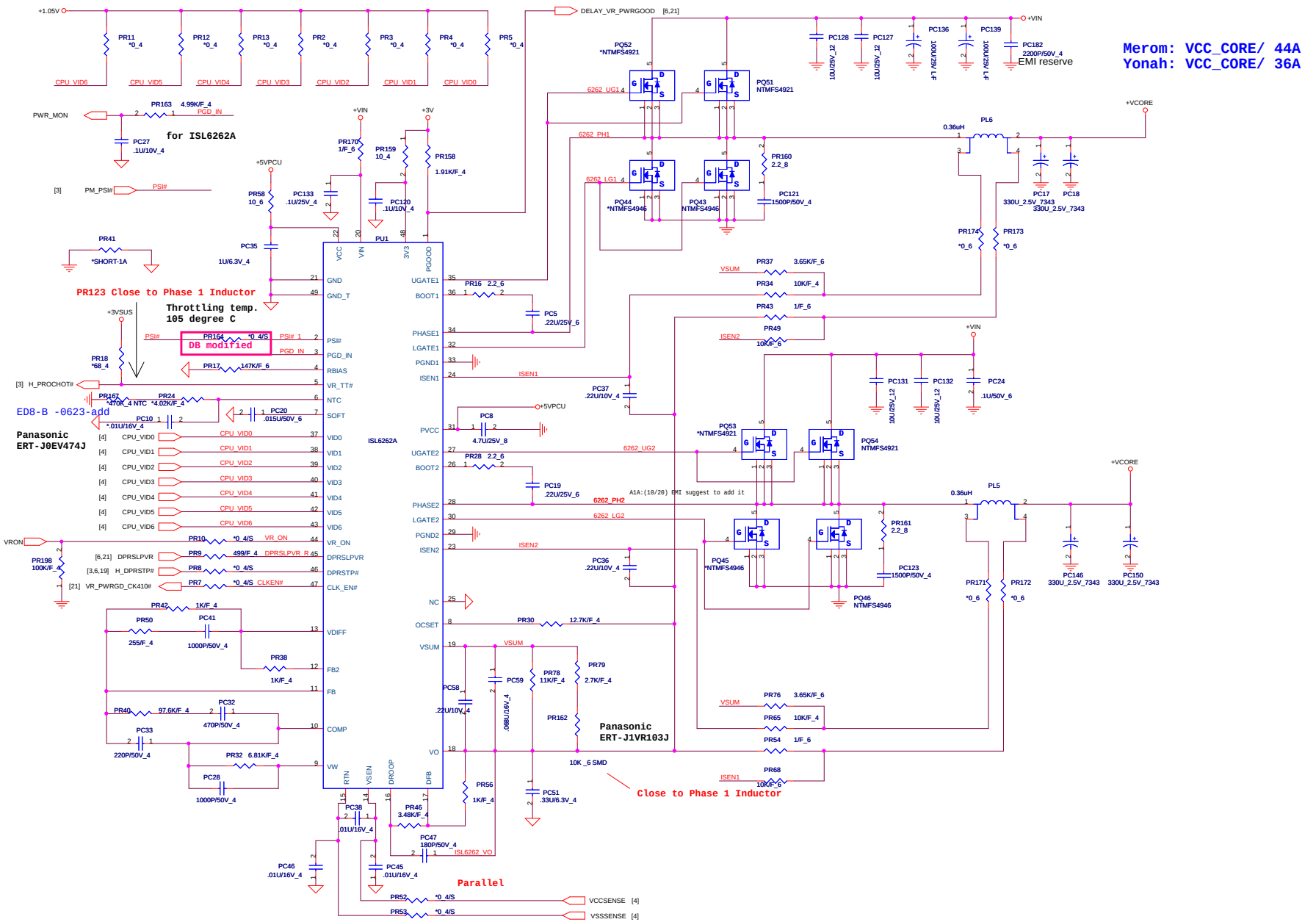
	GM47	NON GM47
Use Cap	PC170 C825	PC161

NB5

PROJECT : OP6/7
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.05V/+1.5V (RT8204)	SI

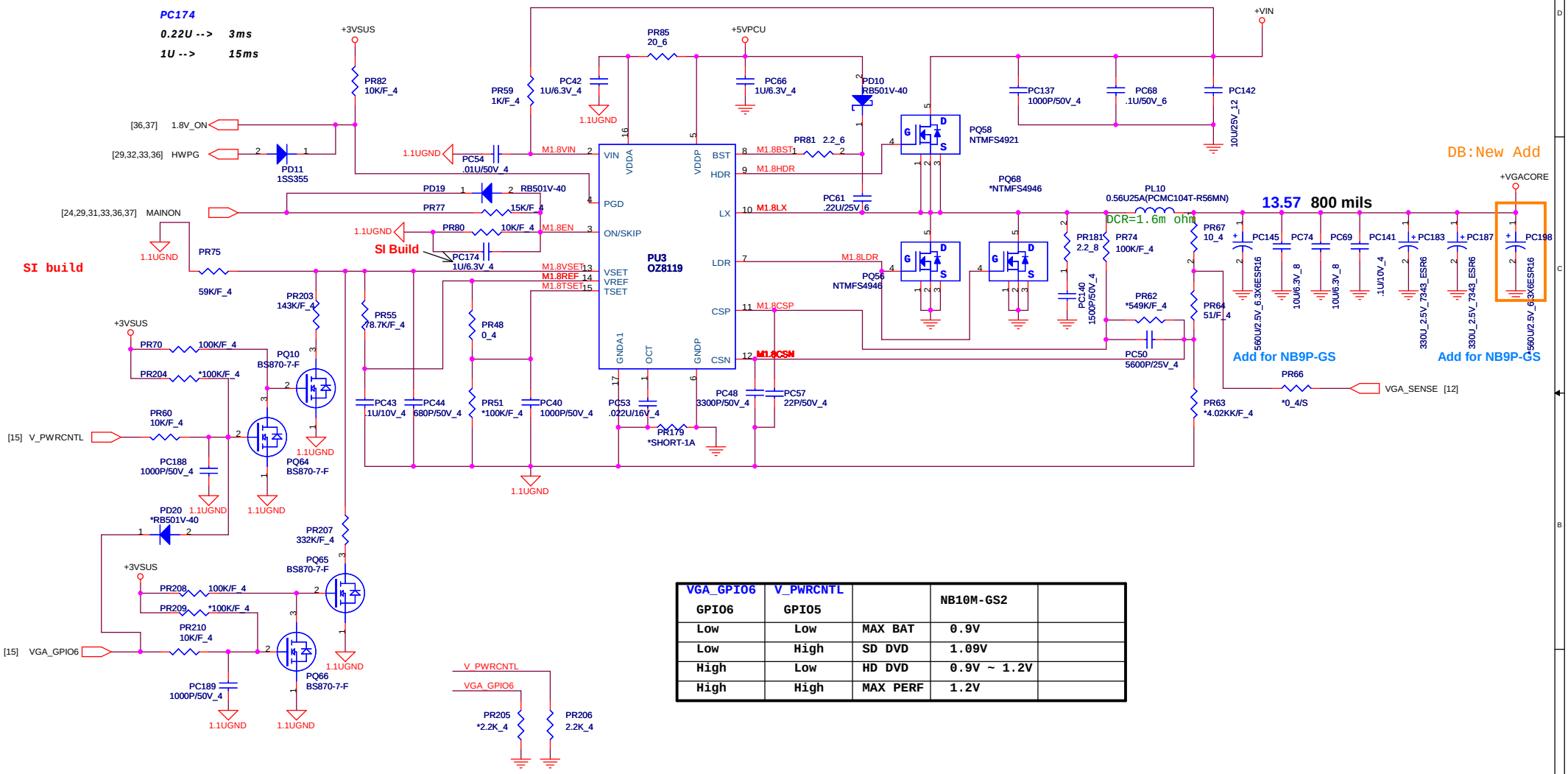
Date: Tuesday, January 20, 2009 | Sheet 33 of 37



PROJECT : OP6/7	
Quanta Computer Inc.	
NB5	Size: Custom
Document Number: CPU Core (ISL6262A)	Rev: SI
Date: Tuesday, January 20, 2009	Sheet 34 of 37

VGA Core & VCC1.1

+1.1Volt +/- 5%
Countinue current:17.54A
Peak current:22.8A
OCP minimum 23A



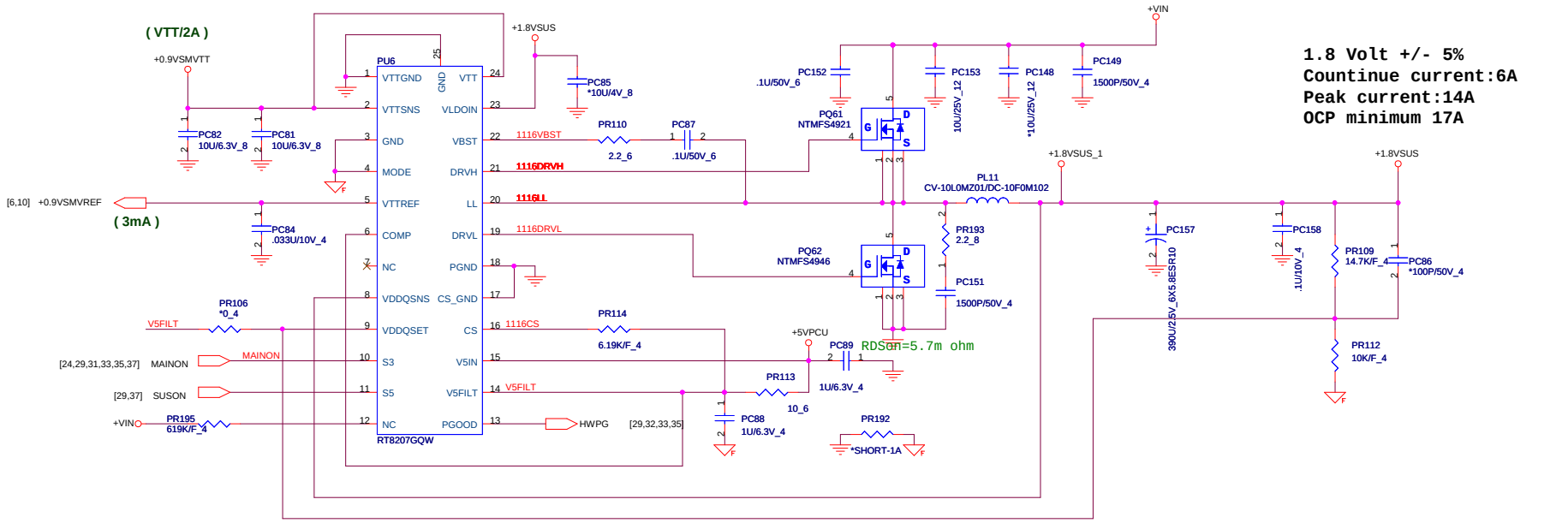
VGA_GPIO6	V_PWRCNTL		NB10M-GS2	
GPIO6	GPIO5			
Low	Low	MAX BAT	0.9V	
Low	High	SD DVD	1.09V	
High	Low	HD DVD	0.9V ~ 1.2V	
High	High	MAX PERF	1.2V	

PROJECT : QP6/7
Quanta Computer Inc.

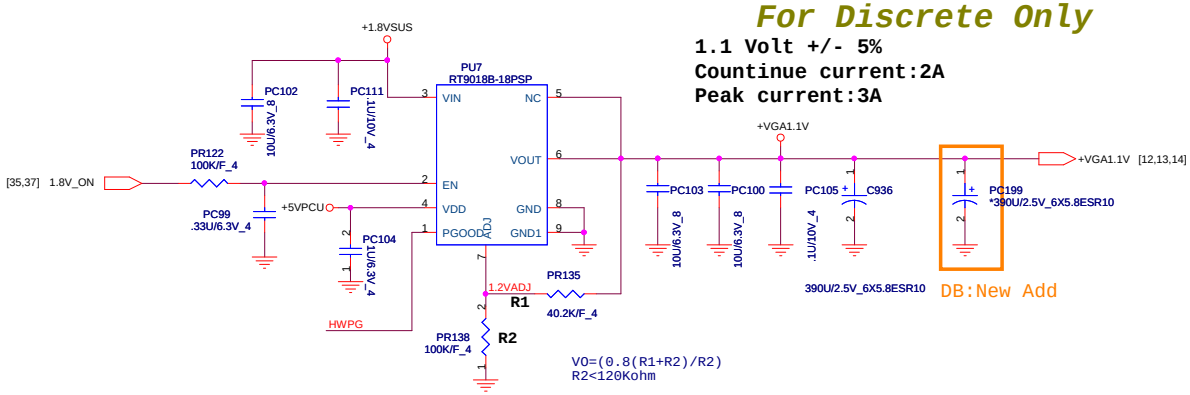
Size	Document Number	Rev
Custom	VGA Core OZ8119	SI

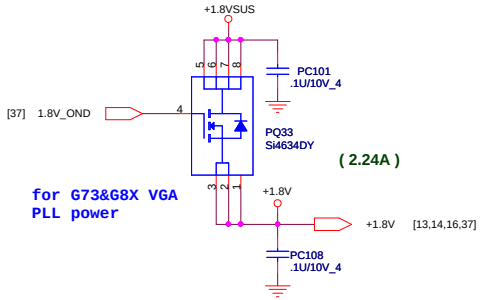
Date: Tuesday, January 20, 2009 Sheet 35 of 37

NB5



Change PR122 tied to 1.8V_ON as power sequence reuqest





NB5

PROJECT : OP6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.8V/DDR_VTER/+1.8v/+1.1V	SI

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