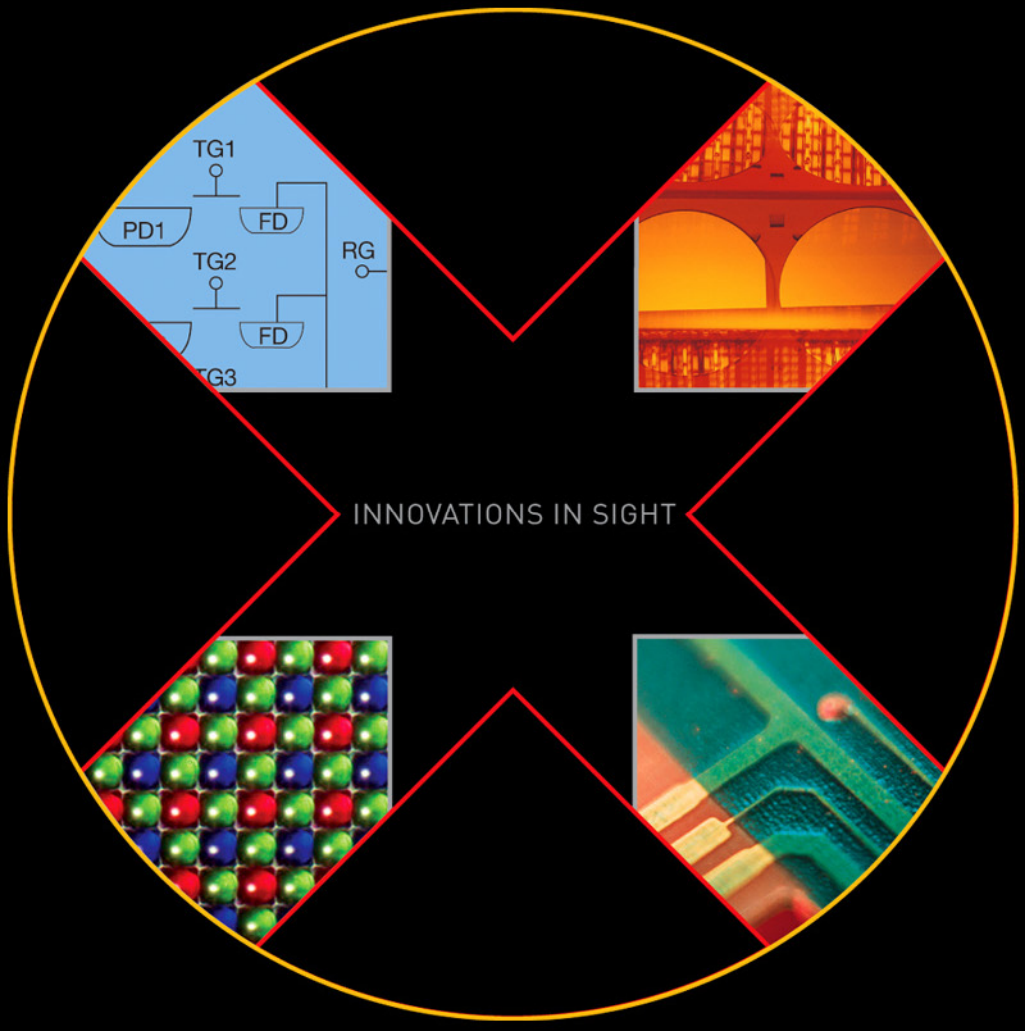
DEVICE PERFORMANCE SPECIFICATION

Revision 2.0 MTD/PS-0856

October 17, 2005



KODAK KAF-39000 IMAGE SENSOR

7216 (H) X 5412 (V) FULL-FRAME CCD COLOR IMAGE SENSOR

Kodak

Image Sensor Solutions

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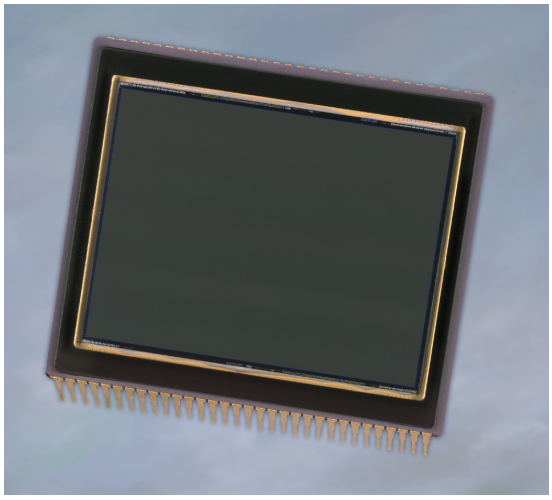
SUMMARY SPECIFICATION

KODAK KAF-39000 IMAGE SENSOR

7216 (H) X 5412 (V) FULL FRAME CCD COLOR IMAGE SENSOR

DESCRIPTION

The KAF-39000 is a dual output, high performance color array CCD (charge coupled device) image sensor with 7216(H) x 5412(V) photoactive pixels designed for a wide range of color image sensing applications including digital imaging. Each pixel contains anti-blooming protection by means of a lateral overflow drain thereby preventing image corruption during high light level conditions. Each of the 6.8µm square pixels are selectively covered with red, green or blue pigmented filters for color separation. Total chip size is 50.7 mm x 39.0 mm and is housed in a 64 pin, 2.347" x 2.000" (59.61 x 50.80 mm) DIL ceramic package with 0.070" (1.78 mm) pin spacing.



FEATURES

- Ultra-high resolution
- Broad dynamic range
- Low noise architecture
- Large active imaging area

APPLICATIONS

- Professional Digital Still Cameras and Camera Backs

Parameter	Typical Value
Architecture	Full Frame CCD; with Square Pixels
Total Number of Pixels	7326 (H) x 5494 (V) = 40.2 M
Number of Effective Pixels	7256 (H) x 5452 (V) = 39.5M
Number of Active Pixels	7216(H) x 5412 (V) = 39.0M
Pixel Size	6.8 µm (H) x 6.8 µm (V)
Imager Size	61.3 mm (diagonal)
Chip Size	50.7mm (H) x 39.0mm (V)
Aspect Ratio	4:3
Saturation Signal	60 K e^-
Charge to Voltage Conversion	26 µV/e^-
Quantum Efficiency (RGB)	20%, 23%, 18%
Read Noise (f=24 MHz)	16 e^-
Dark Signal (T=40°C)	4 mV
Dark Current Doubling Temperature	6.3° C
Linear Dynamic Range (f=24 MHz, T=40 C)	71.4 dB
Charge Transfer Efficiency (HCTE/VCTE)	0.999995 0.999999
Blooming Protection (4ms exposure time)	1000X saturation exposure
Maximum Data Rate	24 MHz
Readout Mode	Dual output only

Parameters above are specified at T = 20° C unless otherwise noted.

DEVICE DESCRIPTION

ARCHITECTURE

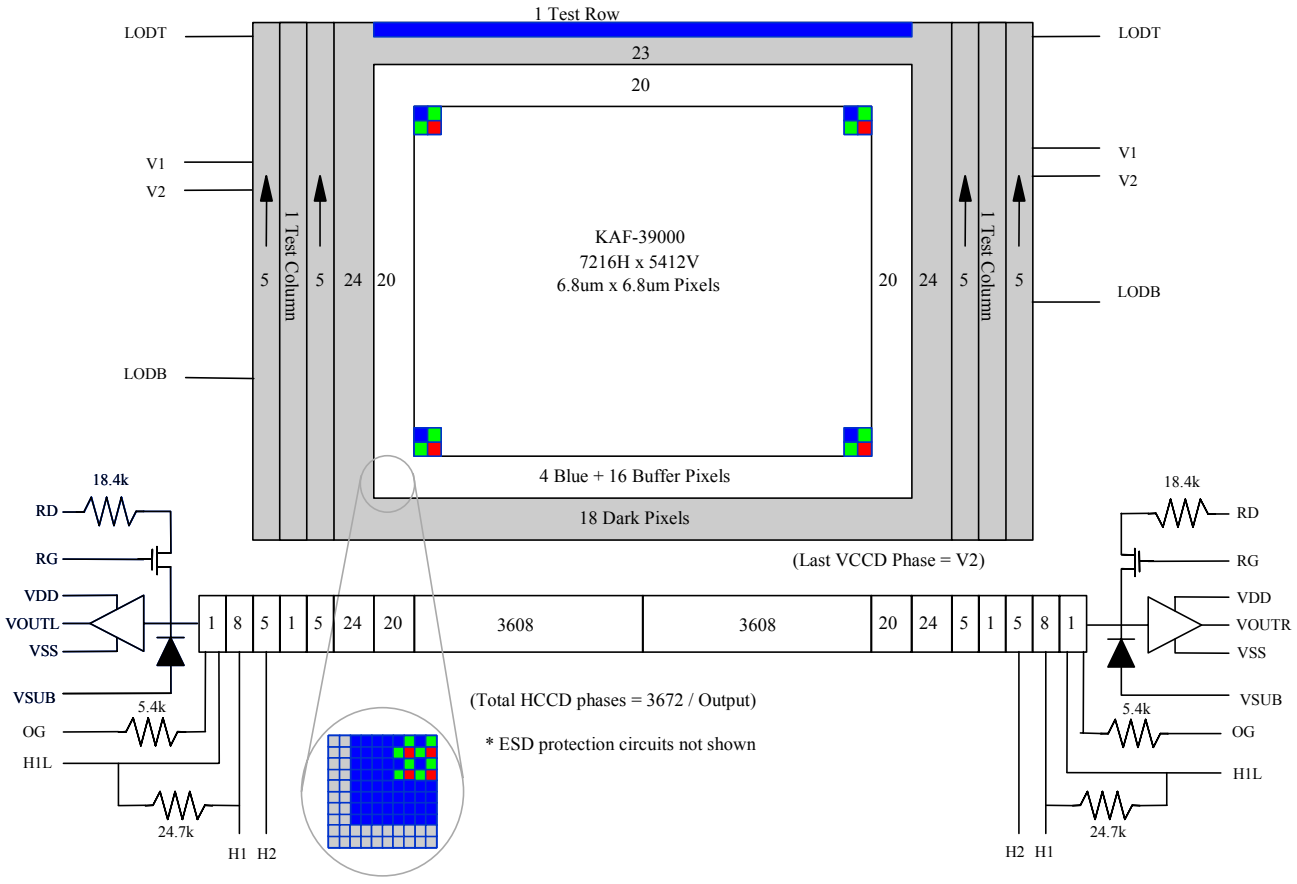


Figure 1 - Block Diagram

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 24 leading dark pixels on every line. There are also 18 full dark lines at the start and 23 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a *dark reference*.

Dummy Pixels

Within each horizontal shift register there are 20 leading pixels. These are designated as *dummy pixels* and should not be used to determine a dark reference level.

Active Buffer Pixels

20 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but they are not tested for defects and non-uniformities. Of these 20 pixels, the outermost 4 pixels are covered with blue

pigment while the remaining are arranged in a Bayer pattern (R, GR, GB, B)

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

CHARGE TRANSPORT

The integrated charge from each pixel is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCDs to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the output amplifier. On each falling edge of H1L a new charge packet sensed by the output amplifier.

HORIZONTAL REGISTER

Output Structure

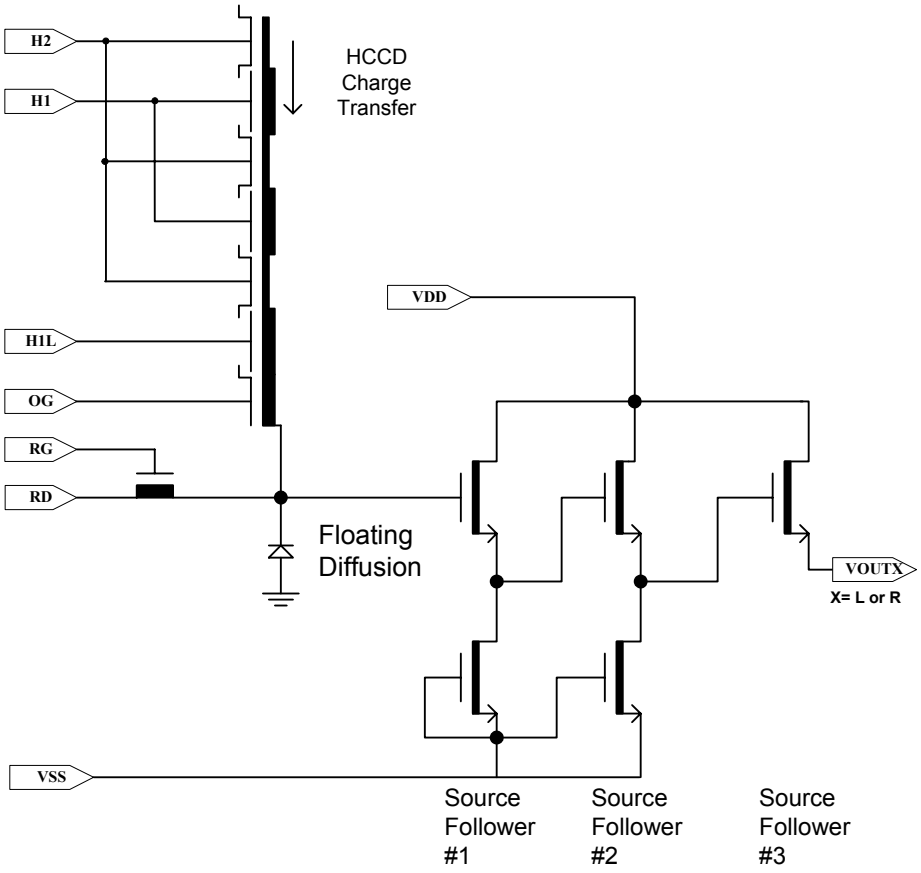


Figure 2 - Output Architecture (Left or Right)

The output consists of a floating diffusion capacitance connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip current source must be added to the VOUT pin of the device. See Figure 3.

Output Load

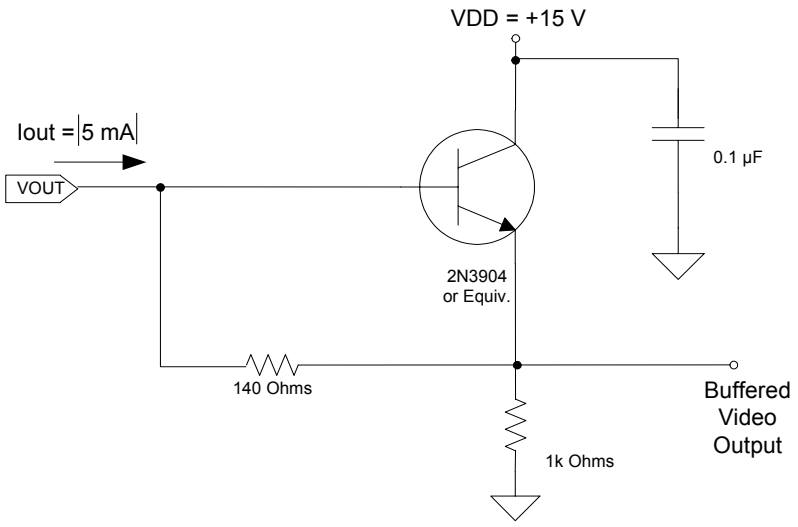
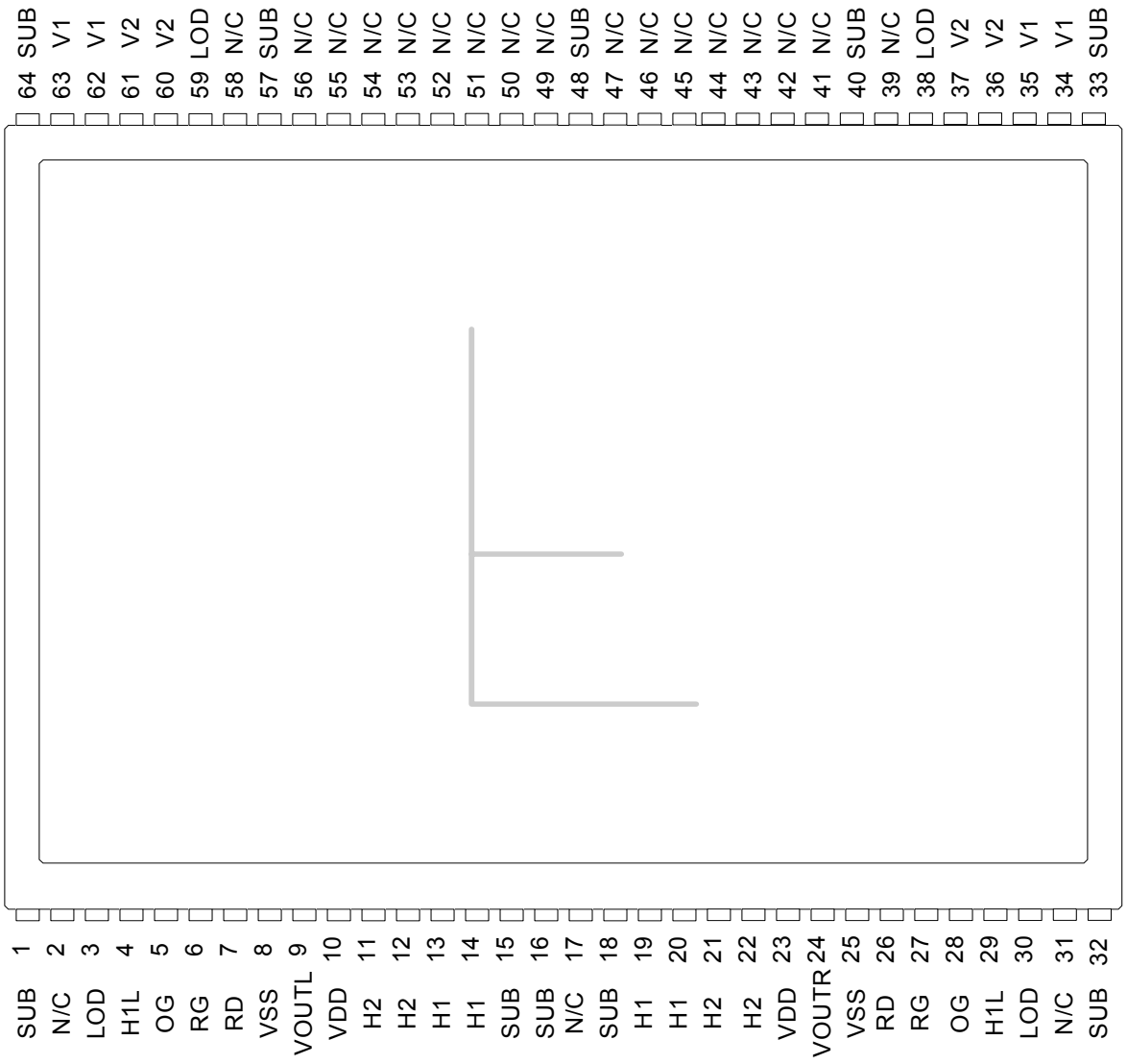


Figure 3 - Recommended Output Structure Load Diagram.
Note: Component values may be revised based on operating conditions and other design considerations.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation



Note: Pins with the same name are to be tied together on the circuit board and have the same timing.

Pin	Name	Description
1	SUB	Substrate
2	N/C	No Connection
3	LOD	Lateral Overflow Drain
4	H1L	Horizontal Phase 1, Last Gate
5	OG	Output Gate
6	RG	Reset Gate
7	RD	Reset Drain
8	VSS	Output Amplifier Return
9	VOUTL	Video Output: Left
10	VDD	Output Amplifier Supply
11	H2	Horizontal Phase 2
12	H2	Horizontal Phase 2
13	H1	Horizontal Phase 1
14	H1	Horizontal Phase 1
15	SUB	Substrate
16	SUB	Substrate
17	N/C	No Connection
18	SUB	Substrate
19	H1	Horizontal Phase 1
20	H1	Horizontal Phase 1
21	H2	Horizontal Phase 2
22	H2	Horizontal Phase 2
23	VDD	Output Amplifier Supply
24	VOUTR	Video Output:Right
25	VSS	Output Amplifier Return
26	RD	Reset Drain
27	RG	Reset Gate
28	OG	Output Gate
29	H1L	Horizontal Phase 1, Last Gate
30	LOD	Lateral Overflow Drain
31	N/C	No Connection
32	SUB	Substrate

Pin	Name	Description
64	SUB	Substrate
63	V1	Vertical Phase 1
62	V1	Vertical Phase 1
61	V2	Vertical Phase 2
60	V2	Vertical Phase 2
59	LOD	Lateral Overflow Drain
58	N/C	No Connection
57	SUB	Substrate
56	N/C	No Connection
55	N/C	No Connection
54	N/C	No Connection
53	N/C	No Connection
52	N/C	No Connection
51	N/C	No Connection
50	N/C	No Connection
49	N/C	No Connection
48	SUB	Substrate
47	N/C	No Connection
46	N/C	No Connection
45	N/C	No Connection
44	N/C	No Connection
43	N/C	No Connection
42	N/C	No Connection
41	N/C	No Connection
40	SUB	Substrate
39	N/C	No Connection
38	LOD	Lateral Overflow Drain
37	V2	Vertical Phase 2
36	V2	Vertical Phase 2
35	V1	Vertical Phase 1
34	V1	Vertical Phase 1
33	SUB	Substrate

Note: The leads are on a 0.070" spacing

PERFORMANCE

IMAGE PERFORMANCE OPERATIONAL CONDITIONS

Description	Condition - Unless otherwise noted	Notes
Frame time ($t_{readout}$ + t_{int})	1327 ms	Includes overclock pixels
Integration time (tint)	250 ms	
Horizontal clock frequency	24 MHz	
Temperature	> 20°C	Room temperature
Mode	integrate – readout cycle	
Operation	Nominal operating voltages and timing with min. vertical pulse width t_{vw} = 17 µs	

IMAGE PERFORMANCE SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Sample Plan
Saturation Signal	Vsat Ne^-_{sat} Q/V	1300 54k	1560 60k 26		mV e^- µV/e^-	1	die design design
Quantum Efficiency red green blue	Rr Rg Rb		20 23 18		%QE %QE %QE	3	design design design
High Level Photoresponse Non-Linearity	PRNL		5	10	%	2	die
Photo Response Non-Uniformity	PRNU red PRNU g, b		10	20	%p-p	3	die
Readout Dark Current	Vdark,read		4	10	mV	5	die
Integration Dark Signal	Vdark,int		6.5	20	mV/s	4	die
Dark Signal Non-Uniformity	DSNU		2	8	mV p-p	6	die
Dark Signal Doubling Temperature	ΔT		6.3		°C		design
Read Noise	NR		16	40	e^- rms		die
Total Noise	N		21		e^- rms	7	design
Linear Dynamic Range	DR		70.5		dB	8	design
Red-Green Hue Shift Blue-Green Hue Shift	RGHueUnif BGHueUnif		6	12	%	9	die
Horizontal Charge Transfer Efficiency	HCTE		0.999995			10	die
Vertical Charge Transfer Efficiency	VCTE		0.999999				die
Blooming Protection	X_ab	250	1000		x Esat	11	design
DC Offset, output amplifier	Vodc	7.5	8.5	9.5	V	12	die
Output Amplifier Bandwidth	f_{-3dB}	80	114	122	MHz	13	design
Output Impedance, Amplifier	ROUT	130	140	200	Ohms		die
Reset Feedthrough	V_{rft}		1		V	14	design

Notes:

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst-case deviation (from 10 mV to Vsat min), relative to a linear fit applied between 0 and 65% of $Vsat_{min}$.
3. Difference between the maximum and minimum average signal levels of 146 x 146 blocks within the sensor on a per color basis as a % of average signal level.
4. T=60°C. Average non-illuminated signal with respect to over-clocked vertical register signal.
5. T=60°C, 24MHz pixel rate, readout time=900 ms
6. T=60°C. Absolute difference between the maximum and minimum average signal levels of 146 x 146 blocks within the sensor.
7. rms deviation of a multi-sampled pixel measured in the dark including amplifier and dark current shot noise.
8. $20\log(Vsat/V_N)$ - see Note 6 and note 1. V_N = Nread * nominal charge to voltage
9. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest (146 x 146 blocks) within the sensor. The specification refers to the largest value of the response difference imaged in Daylight 5500 K.
10. Measured per transfer at Vsat min. Typically, no degradation in CTE is observed up to 24 MHz.
11. X_ab is the number of times above the Vsat illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X_ab is measured at 4ms.
12. Video level offset with respect to ground
13. Last stage only. Assumes 10 pF off-chip load.
14. Amplitude of feed-through pulse in VOUT due to RG coupling.

TYPICAL PERFORMANCE CURVES

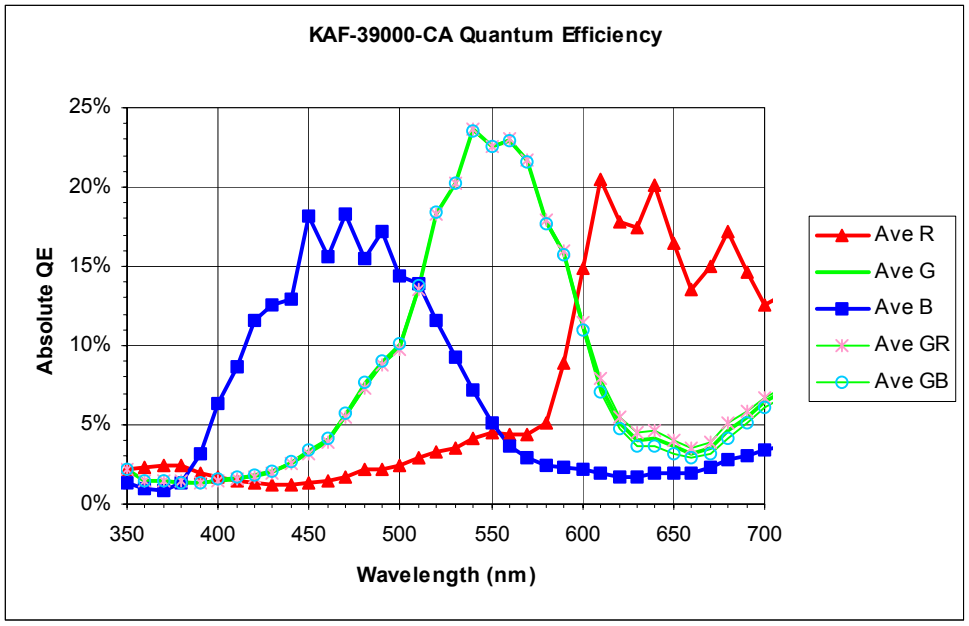


Figure 4 - Typical Quantum Efficiency

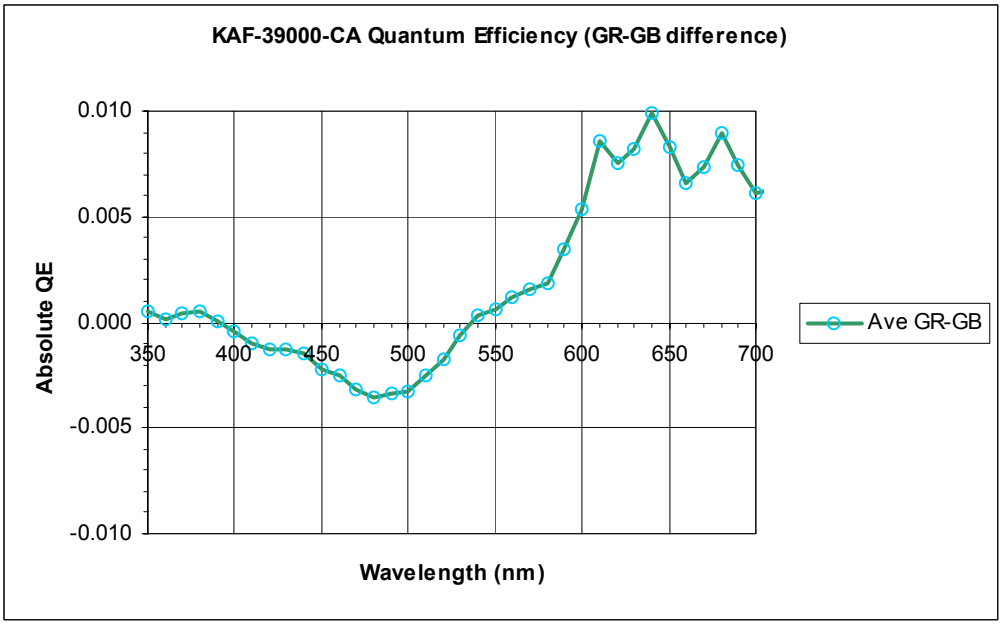


Figure 5 - Typical GR - GB QE Difference

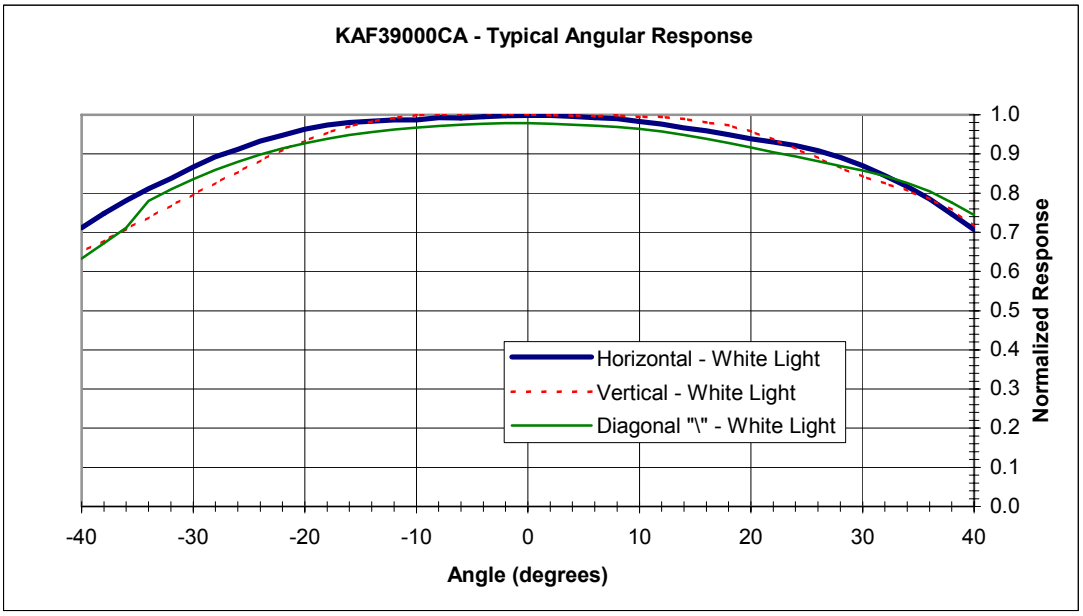


Figure 6 - Typical Normalized Angle QE

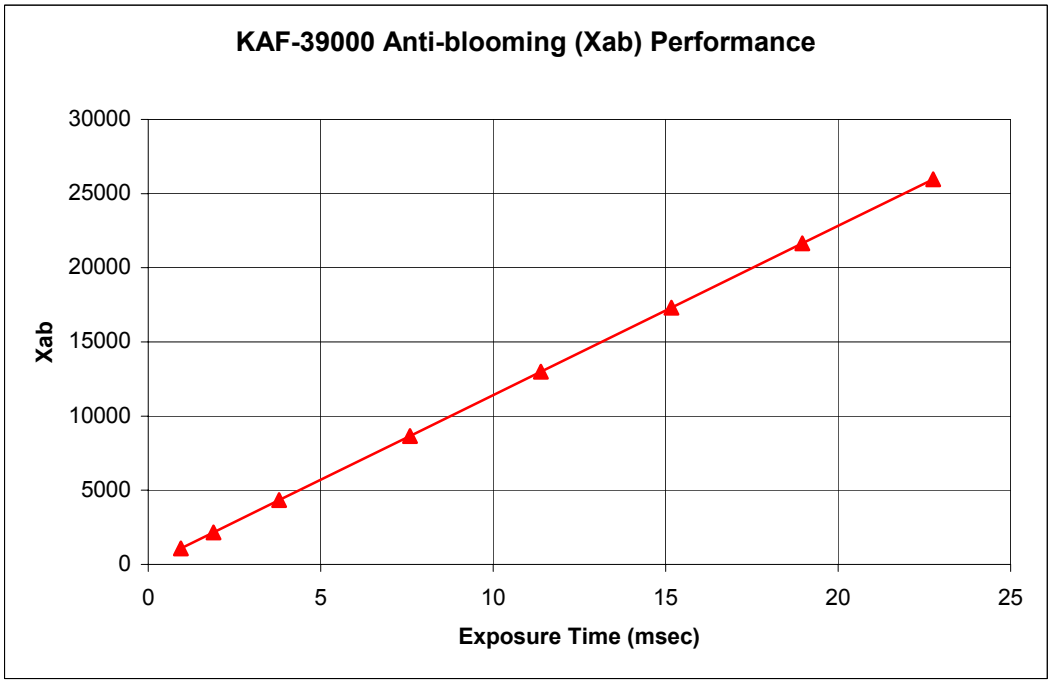


Figure 7 - Typical Anti-blooming Performance

DEFECT DEFINITIONS

Defect Operational Conditions

All defect tests performed at T ~30 °C, t_{int} = 250 ms and $t_{readout}$ = 1077 ms

Defect Specifications

Classification	Points	Clusters	Columns	Includes dead columns
Standard Quality (SQ)	<4,000	<50	<20	yes

Point Defects

A pixel that deviates by more than 9 mV above neighboring pixels under non-illuminated conditions

-- OR --

A pixel that deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions

Cluster Defect

A grouping of not more than 10 adjacent point defects

Cluster defects are separated by no less than 4 good pixels in any direction

Column Defect

A grouping of more than 10 point defects along a single column

-- OR --

A column that deviates by more than 0.9 mV above or below neighboring columns under non-illuminated conditions

-- OR --

A column that deviates by more than 1.5% above or below neighboring columns under illuminated conditions

Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

Dead Columns

A column that deviates by more than 50% below neighboring columns under illuminated conditions

Saturated Columns

A column that deviates by more than 100 mV above neighboring columns under non-illuminated conditions. No saturated columns are allowed

OPERATION

ABSOLUTE MAXIMUM RATINGS

Description[9]	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	-0.5	+17.5	V	1,2
Gate Pin Voltages	V_{gate1}	-13.5	+13.5	V	1,3
Overlapping Gate Voltages	V_{1-2}	-13.5	+13.5	V	4
Non-overlapping Gate Voltages	V_{g-g}	-13.5	+13.5	V	5
Output Bias Current	I_{out}		-30	mA	6
LODT Diode Voltage	V_{LODT}	-0.5	+13.0	V	7
Operating Temperature	T_{OP}	0	60	°C	9

Notes:

1. Referenced to pin VSUB
2. Includes pins: VRD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H1L, H2, RG, VOG.
4. Voltage difference between overlapping gates. Includes: V1 to V2; H1, H1L to H2; H1L to VOG; V1 to H2.
5. Voltage difference between non-overlapping gates. Includes: V1 to H1, H1L; V2, VOG to H2.
6. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
7. V1, H1, V2, H2, H1L, VOG, and VRD are tied to 0 V.
8. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.
9. Noise performance will degrade at higher temperatures.

POWER-UP SEQUENCE

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (VSUB).
2. Supply the appropriate biases and clocks to the remaining pins.

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	V_{RD}	11.3	11.5	11.7	V	I_{RD} = 0.01	
Output Amplifier Return	VV_{SS}	0.5	0.7	1.0	V	I_{SS} = 3.0	
Output Amplifier Supply	VV_{DD}	14.5	15.0	15.5	V	I_{OUT} + I_{SS}	
Substrate	V_{SUB}		0		V	0.01	
Output Gate	V_{OG}	-3.2	-3.0	-2.8	V	0.01	
Lateral Drain	V_{LOD}	9.8	10.0	10.2	V	0.01	
Video Output Current	I_{OUT}		-5	-10	mA		1

Notes:

1. An output load sink must be applied to VOUT to activate output amplifier – see Figure 3.

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance	Notes
V1 Low Level	V1L	Low	-9.2	-9.0	-8.8	V	360 nF	1
V1 High Level	V1H	High	2.3	2.5	2.7	V		1
V2 Low Level	V2L	Low	-9.2	-9.0	-8.8	V	440 nF	1
V2 High Level	V2H	High	2.3	2.5	2.7	V		1
H1 Low Level	H1L	Low	-4.7	-4.5	-4.3	V	550 pF	1
H1 High Level	H1H	High	2.5	2.7	2.9	V		1
H1L Low Level	$H1L_{low,}$	Low	-6.7	-6.5	-6.3	V	13 pF	1
H1L High Level	$H1L_{high}$	High	2.5	2.7	2.9	V		1
H2 Low Level	H2L	Low	-5.2	-5.0	-4.8	V	370 pF	1
H2 High Level	H2H	High	2.0	2.2	2.4	V		1
RG Low Level	V_{RGL}	Low	0.3	0.5	0.7	V	13 pF	1
RG High Level	V_{RGH}	High	7.8	8.0	8.2	V		1

Notes:

1. All pins draw less than 10 µA DC current. Capacitance values relative to SUB (substrate).

Timing Requirements

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H			24	MHz	1, 2
V1, V2 Clock Frequency	f_V			30	kHz	1, 2
H1, H2 Rise, Fall Times	t_{H1r} , t_{H1f}	5		10	%	3, 7
V1, V2 Rise, Fall Times	t_{V1r} , t_{V1f}	5		10	%	3
V1 - V2 Cross-over	V_{VCR}	-1	0	1	V	
H1 - H2 Cross-over	V_{HCR}	-2.8	-1.4	0	V	
Off Time	t_{off}	0	153		µs	
H1, H2 Setup Time	t_{HS}	1	5		µs	
RG Clock Pulse Width	t_{RGw}	5			ns	4
RG Rise, Fall Times	t_{RGr} , t_{RGf}	5		10	%	3
V1, V2 Clock Pulse Width	t_{Vw}	17	19		µs	2, 6,9

Timing Characteristics

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Pixel Period (1 Count)	t_e	42	42		ns	2
H1L – VOUT Delay	t_{HV}		5		ns	
RG - VOUT Delay	t_{RV}		5		ns	
Readout Time	$t_{readout}$	1033	1077		ms	6, 8
Integration Time	t_{int}		-			5, 6
Line Time	t_{line}	188	181		µs	6
Fast Flush Time	t_{flush}	210	260		ms	

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration time is user specified.
6. Longer times will degrade noise performance.
7. The maximum specification or 10ns whichever is greater based on the frequency of the horizontal clocks.
8. $t_{readout} = t_{line} * 5494$ lines.
9. Measured where Vclock is at 0 volts

Frame Timing

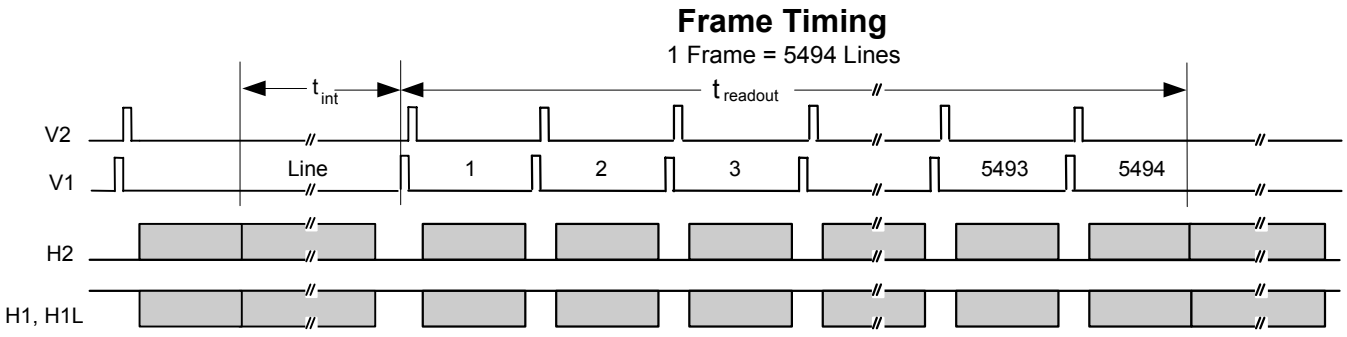


Figure 8 - Frame Timing

Frame Timing Detail

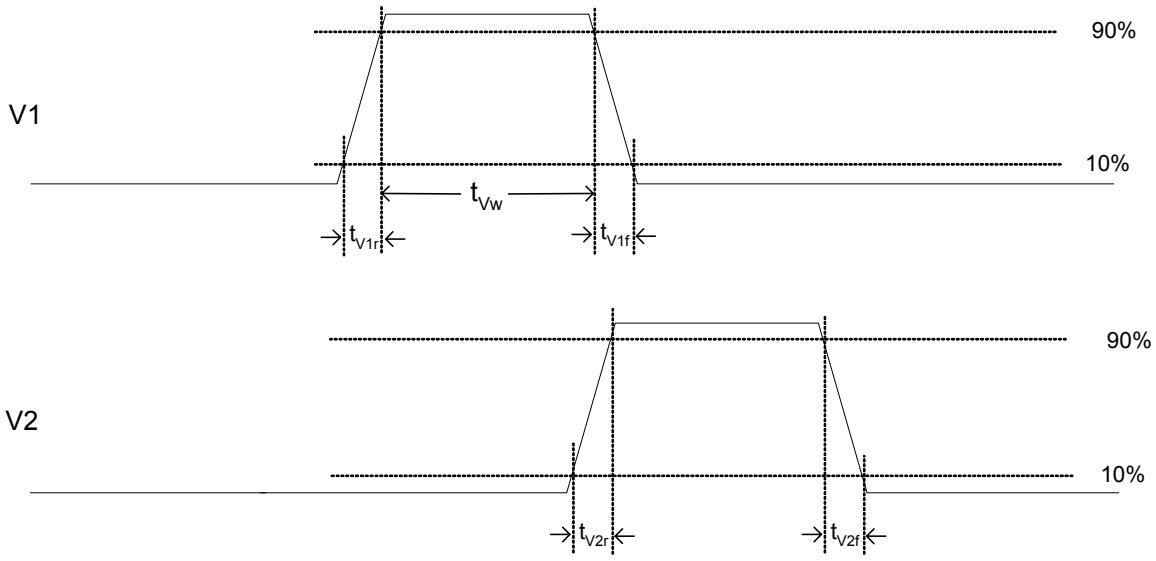


Figure 9 - Frame Timing Detail

Line Timing

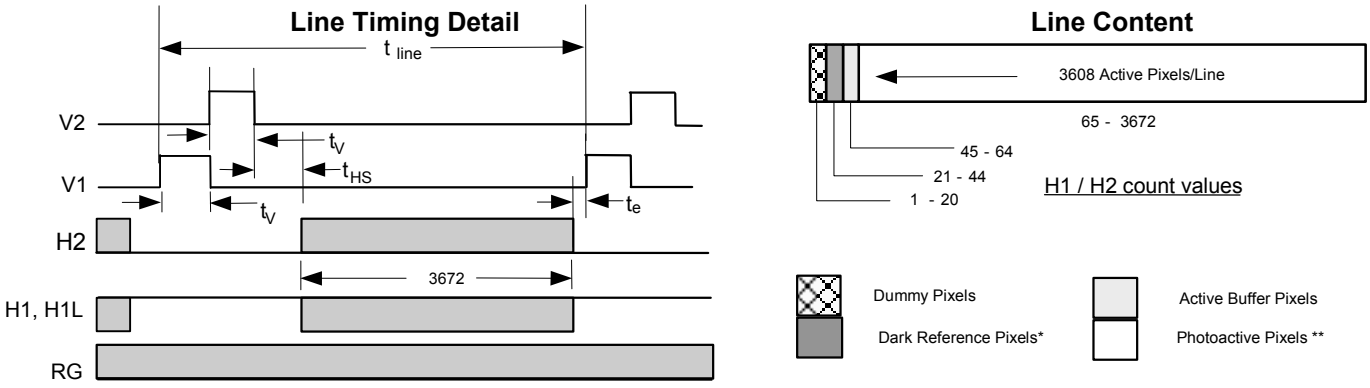


Figure 10 - Line Timing

Pixel Timing Detail

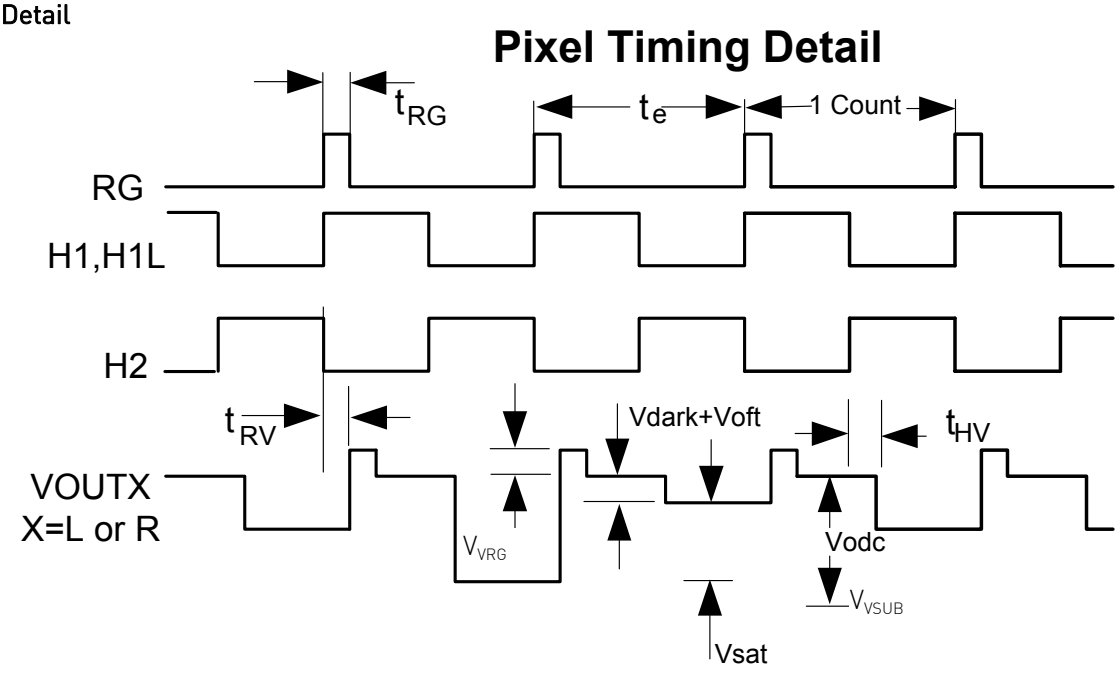


Figure 11 – Pixel Timing

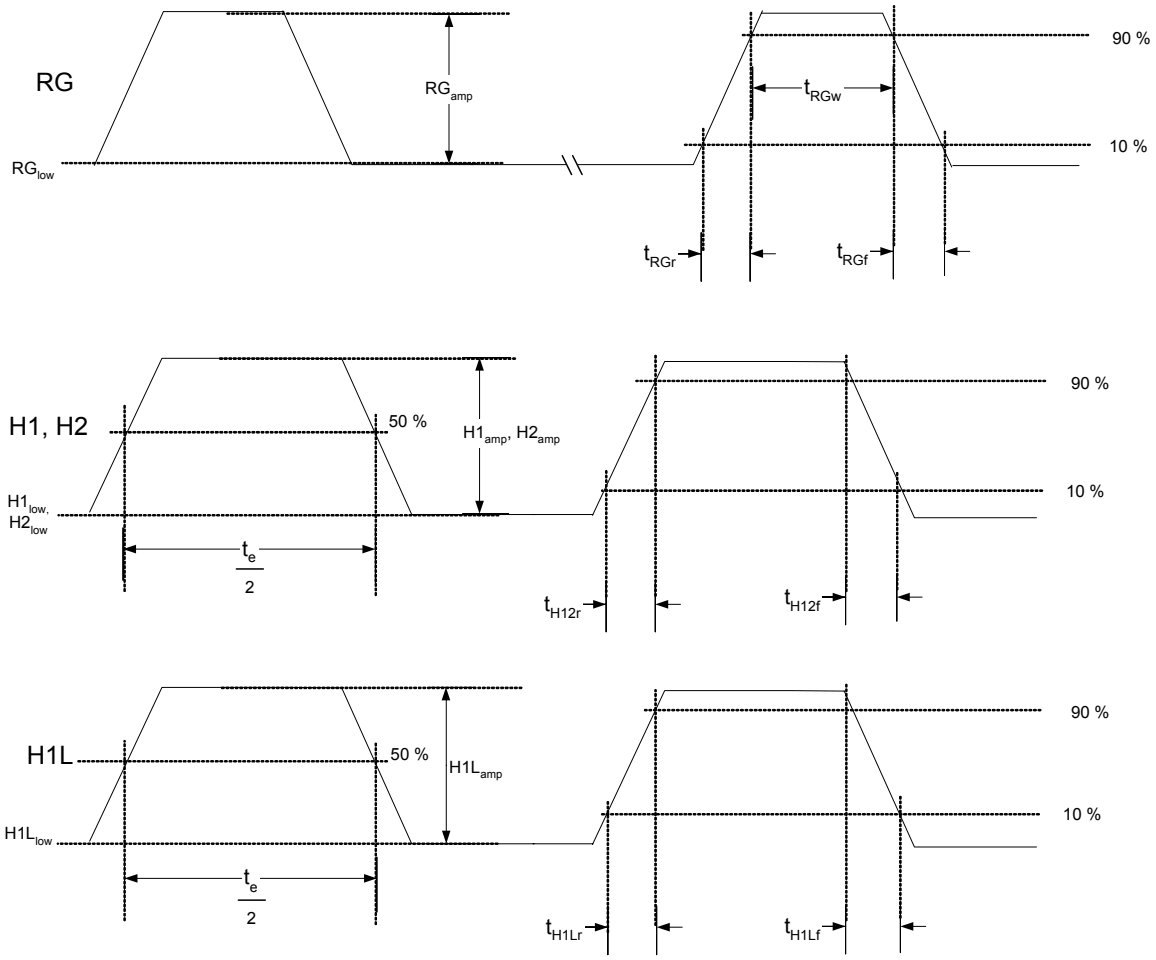


Figure 12 - Pixel Timing Detail

Timing Edge Alignment

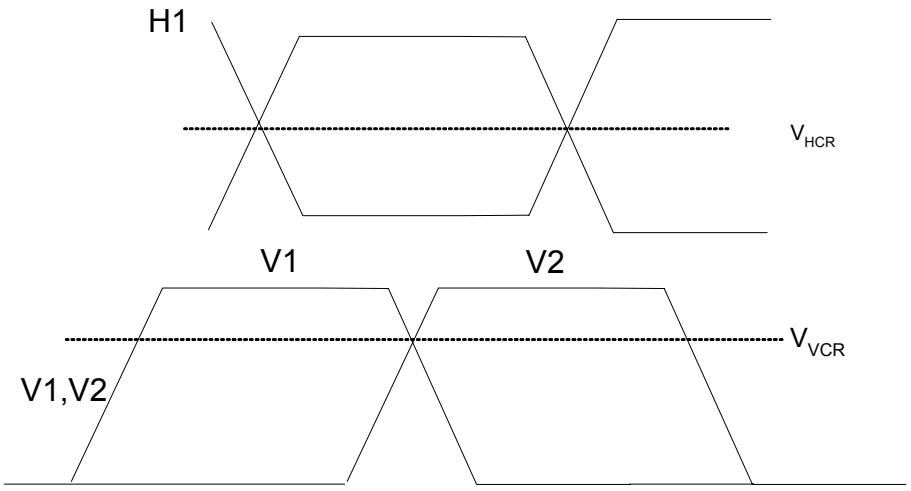


Figure 13 - Timing Edge Alignment

MODE OF OPERATION

POWER-UP FLUSH CYCLE

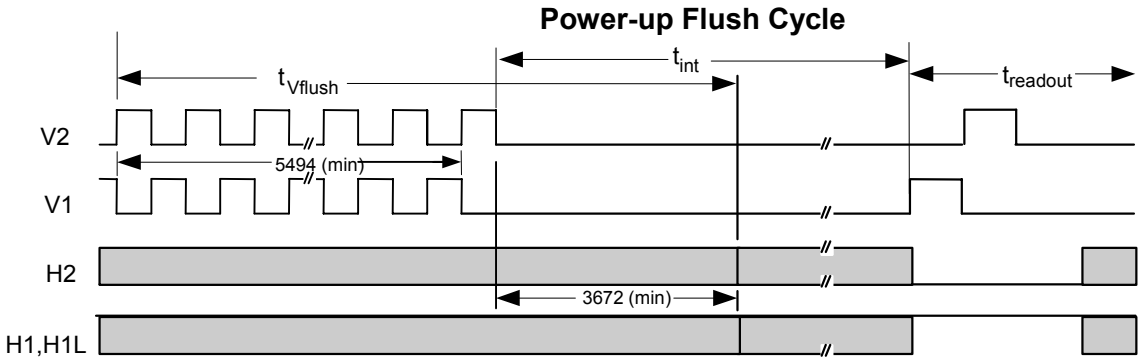


Figure 14 – Power-up Flush Cycle

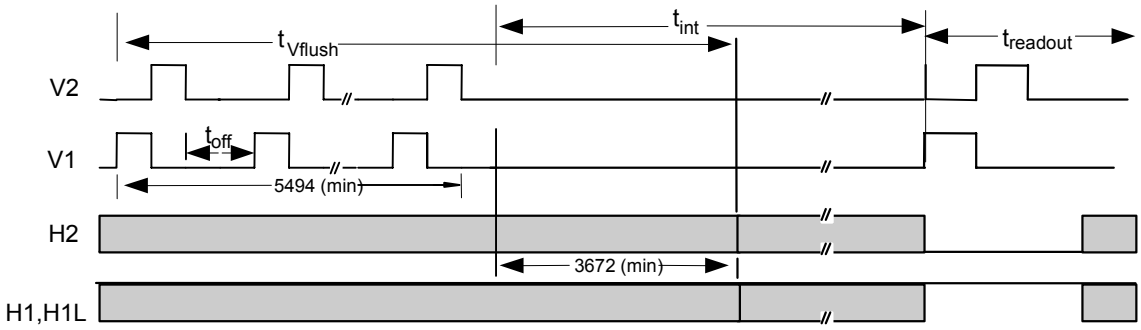


Figure 15 – Modified (Slow) Flush Cycle

STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	70	°C	1

Note:

1. Long-term storage toward the maximum temperature will accelerate color filter degradation

ESD

This device contains limited protection against Electrostatic Discharge (ESD) and is rated as a Class 0 device, JESD22 Human Body, and Class A, JESD22 Machine Mode

Devices should be handled in accordance with strict handling precautions. See ISS Application Note MTD/PS-0224, "Electrostatic Discharge Control".

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.

Caution: Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-0237, "Cover Glass Cleaning Procedure for Image Sensors"

SOLDERING RECOMMENDATIONS

Partial Heating Method: 280 °C maximum pin temperature; 10 seconds maximum duration per pin.

MECHANICAL DRAWINGS

PACKAGE

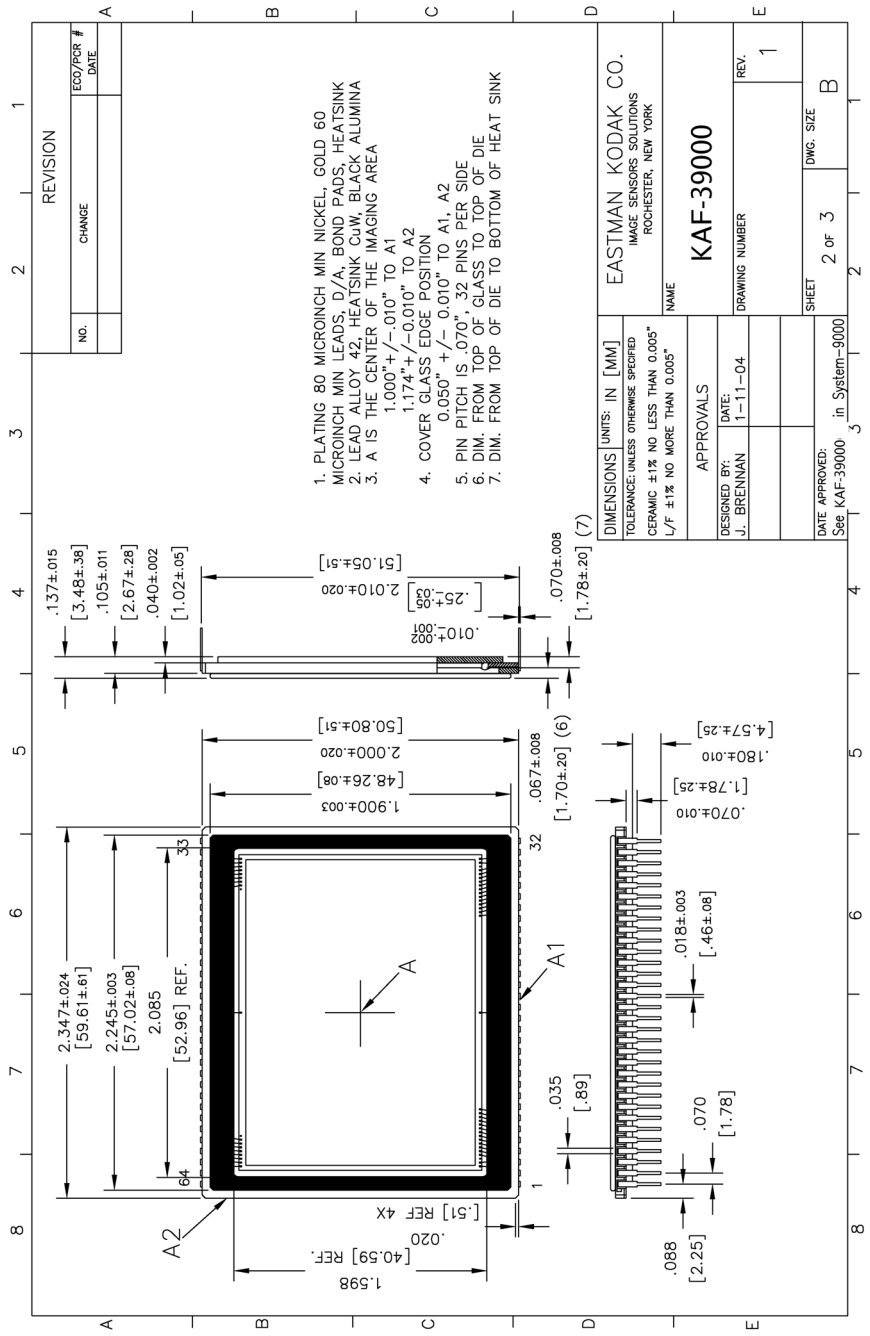
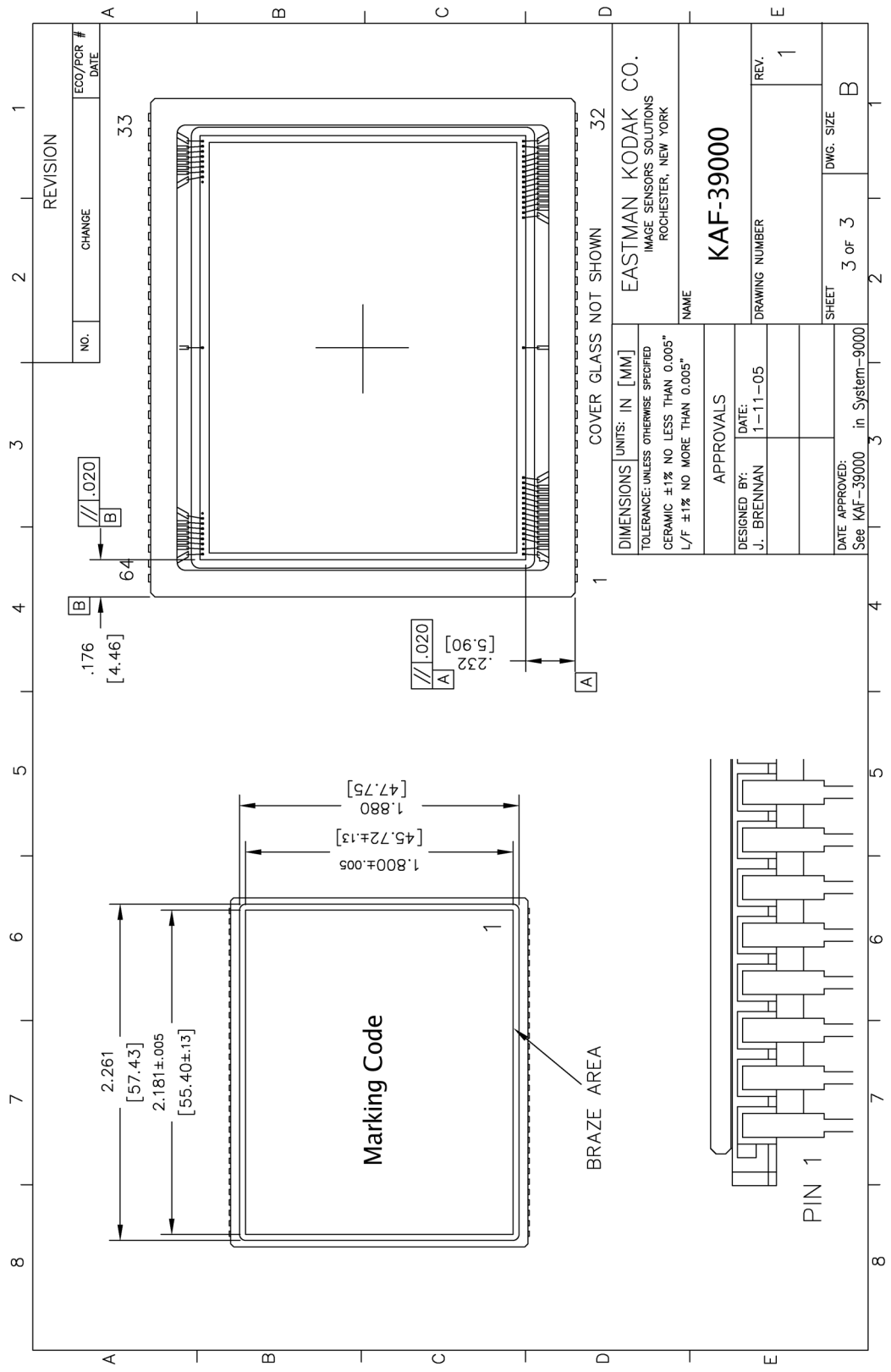


Figure 16 – Completed Assembly Drawing


REVISION
NO.
CHANGE
ECO/PCR #
DATE
33
32
1
64
COVER GLASS NOT SHOWN
.020 B
.176 [4.46]
.020 A
.232 [5.90]
1.880 [47.75]
1.800±.005 [45.72±.13]
2.261 [57.43]
2.181±.005 [55.40±.13]
Marking Code
BRAZE AREA
PIN 1
EASTMAN KODAK CO.
IMAGE SENSORS SOLUTIONS
ROCHESTER, NEW YORK
NAME
KAF-39000
DRAWING NUMBER
REV. 1
SHEET 3 OF 3
DWG. SIZE B
DIMENSIONS UNITS: IN [MM]
TOLERANCE: UNLESS OTHERWISE SPECIFIED
CERAMIC ±1% NO LESS THAN 0.005"
L/F ±1% NO MORE THAN 0.005"
APPROVALS
DESIGNED BY: J. BRENNAN
DATE: 1-11-05
DATE APPROVED: See KAF-39000 in System-9000

Configuration	Marking Code
Color, sealed double ant-reflection coated cover glass	KAF-39000-CA SN

COVER GLASS SPECIFICATION

1. Scratch and dig: 10 micron max
2. Substrate material Schott D-263
3. Multilayer anti-reflective coating

Wavelength	Reflectance
420-450	≤ 2%
450-630	≤ 1%
630-680	≤ 2%

QUALITY ASSURANCE AND RELIABILITY

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

Liability of the Customer: Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224 for handling recommendations.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

ORDERING INFORMATION

AVAILABLE PART CONFIGURATIONS

Type	Description	Glass Configuration
KAF-39000	Color	Double Anti-Reflective, sealed

Please contact Image Sensor Solutions for available part numbers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial Release.
2.0	New specification format. Corrected pin out diagram and package information. Update Performance Table, T_{vw}, Frame Time, dark signal components identified. Updated fast flush time. Added anti blooming performance plot. Added min/max values for performance parameters. Changed name from KAF-39000CE to KAF-39000.

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