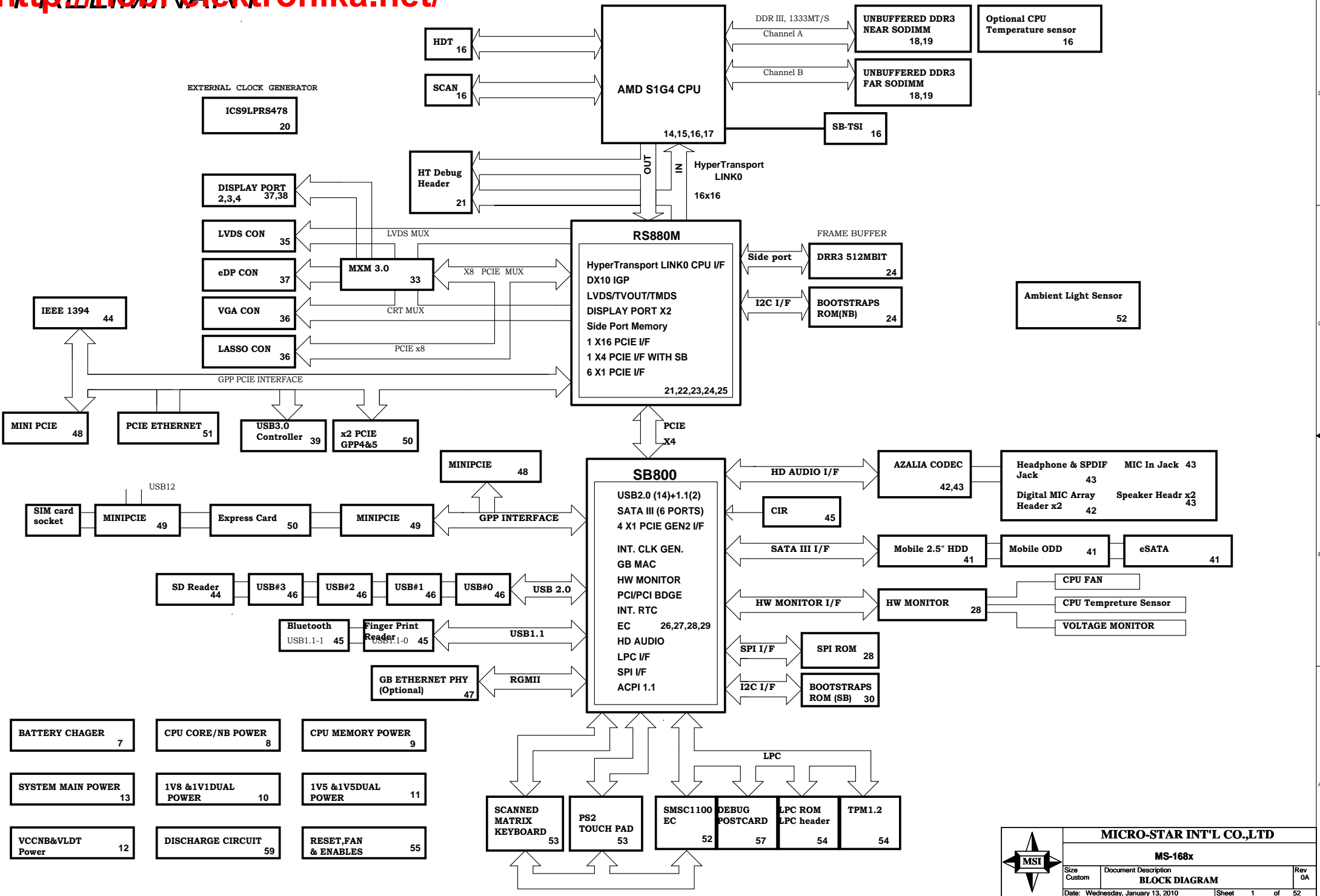


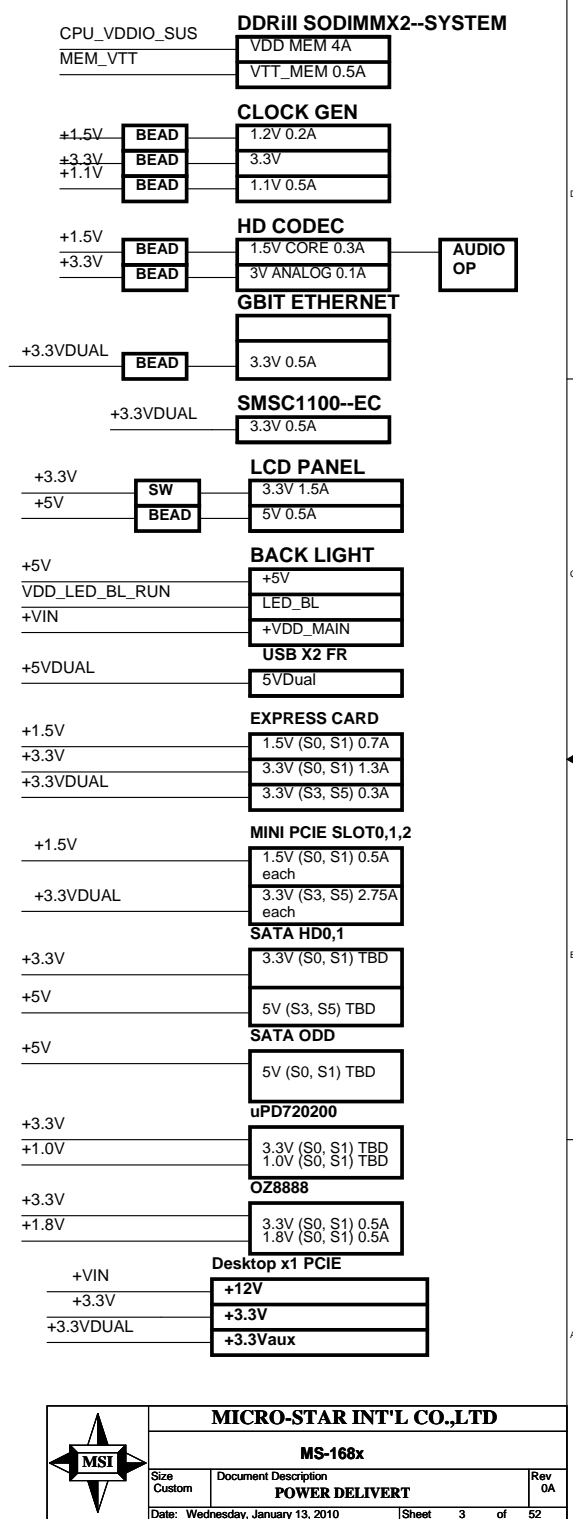
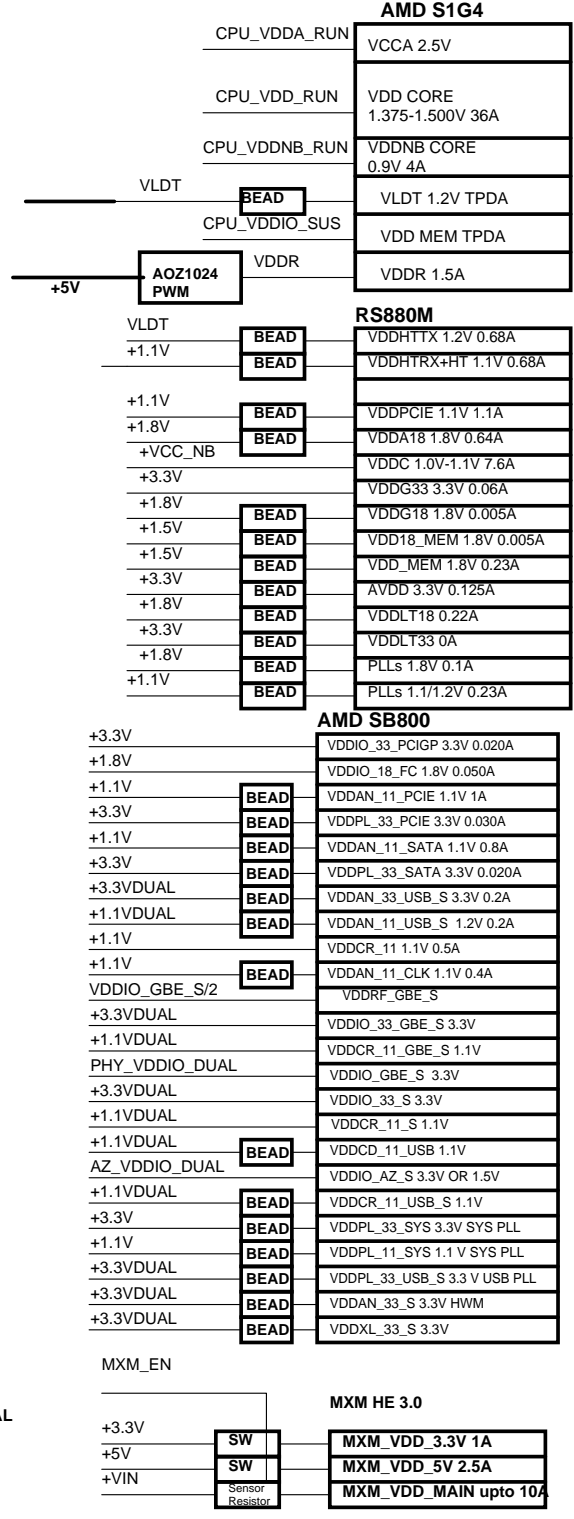
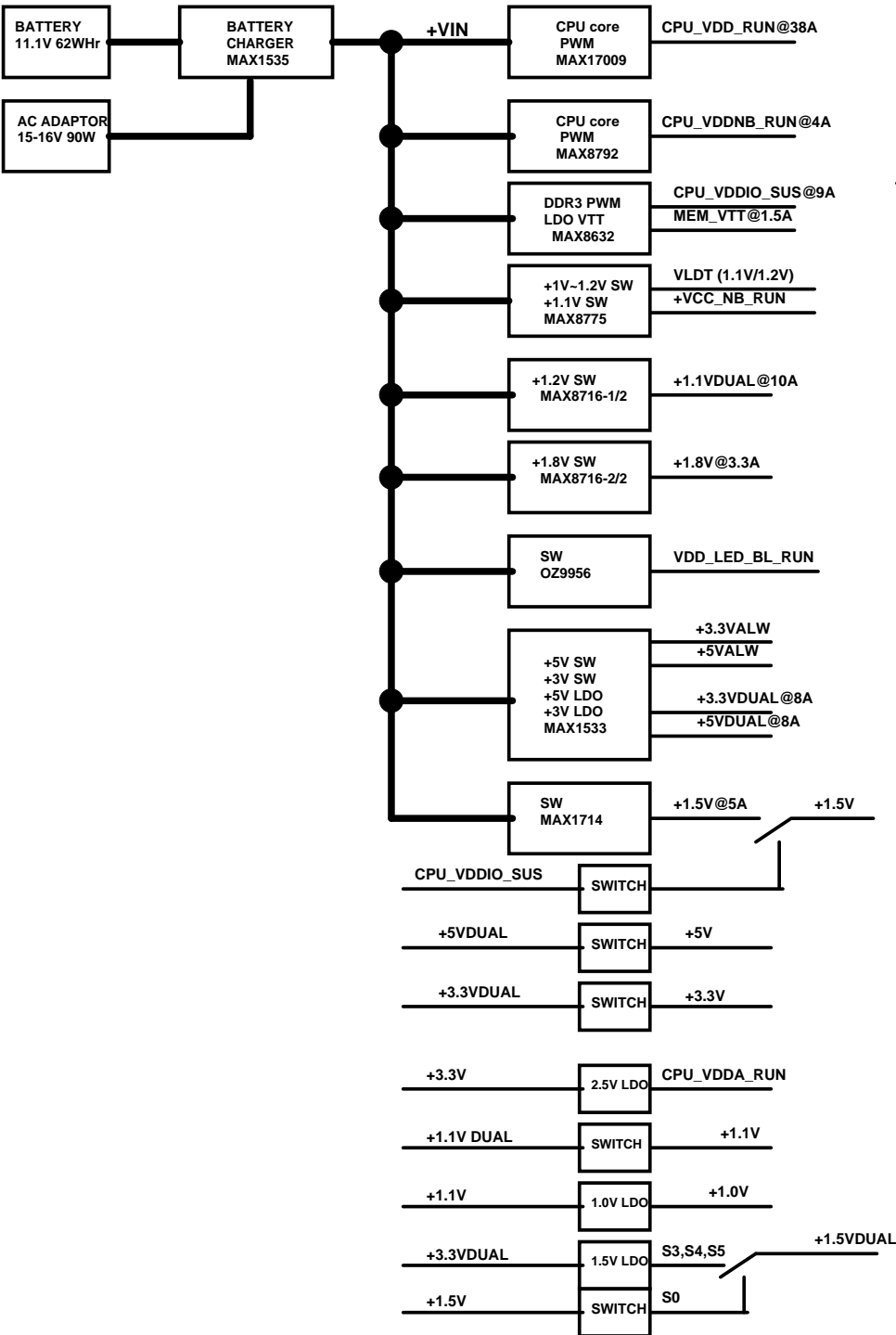
MSI S1G4 SCHEMATIC DESIGN



- BATTERY CHAGER 7
- CPU CORE/NB POWER 8
- CPU MEMORY POWER 9
- SYSTEM MAIN POWER 13
- 1V8 & 1V1 DUAL POWER 10
- 1V5 & 1V5 DUAL POWER 11
- VCCNB&VLDT Power 12
- DISCHARGE CIRCUIT 59
- RESET,FAN & ENABLES 55

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P02 : TABLE OF CONTENTS	P33 : MXM 3.0 EDGE
P03 : POWER DELIVERY CHART	P34 : LVDS / CRT SWITCH
P04 : POWER SEQUENCE CHART	P35 : LVDS CON / BACKLIGHT
P05 : CLOCK DISTRIBUTION	P36 : CRT / LASSO CONN
P06 : MISC TABLES	P37 : EDP / DPD
P07 : BATTERY CHARGER	P38 : DPB / DPC
P08 : CPU CORE PWR	P39 : USB3.0 (1)
P09 : CPU MEM PWR	P40 : USB3.0 (2)
P10 : 1V1DUAL / 1V1 /18V /3V3 /5V	P41 : SATA CONN / DEBUG
P11 : 1V5 / 1V5DUAL	P42 : HD AUDIO CODEC
P12 : NBCORE / VLDT	P43 : HD AUDIO CONN
P13 : SYSTEM POWER	P44 : 1394 / SD READER
P14 : S1G4 HT I/F	P45 : FP / BT / CIR
P15 : S1G4 DDRIII MEMORY I/F	P46 : USB2.0 PORTS
P16 : S1G4 CTRL / DEBUG	P47 : LAN PHY (B50610)
P17 : S1G4 PWR / GND	P48 : MINI PCIE SLOT 0, 3
P18 : DDR3 SODIMMS A/B CHANNLE	P49 : MINI PCIE SLOT 1, 2
P19 : DDR3 SODIMMS DECOUPLING	P50 : X4 GPP / PCIE EXPRESS CARD
P20 : EXTERNAL CLOCK GEN	P51 : LOM (57760)
P21 : RS880M HT I/F	P52 : KBC - SMSC1100L
P22 : RS880M PCIE I/F	P53 : KBCBIOS / KBD /MOUSE
P23 : RS880M SYSTEM	P54 : CONFIG ROM / LPC ROM / TPM
P24 : RS880M SPMEM/STRAPS	P55 : RESET / FAN / LED / PWRGD
P25 : RS880M POWER	P56 : ACPI CONN
P26 : SB8X0 PCIE/PCI/CPU/LPC/CLK	P57 : DEBUG - POST LEDS
P27 : SB8X0 GPIO/USB/AZ/RGMII	P58 : DUAL RAIL ENABLE
P28 : SB8X0 SATA/IDE/HWM/SPI	P59 : DISCHARGE CIRCUIT
P29 : SB8X0 POWER / DECOUPLING	P60 : SB800 A11 PU RES
P30 : SB8X0 STRAPS	P61 : CHANGE HISTROY
P31 : PCIE SWITCH	P62 : POWER ON SEQUENCE CHART



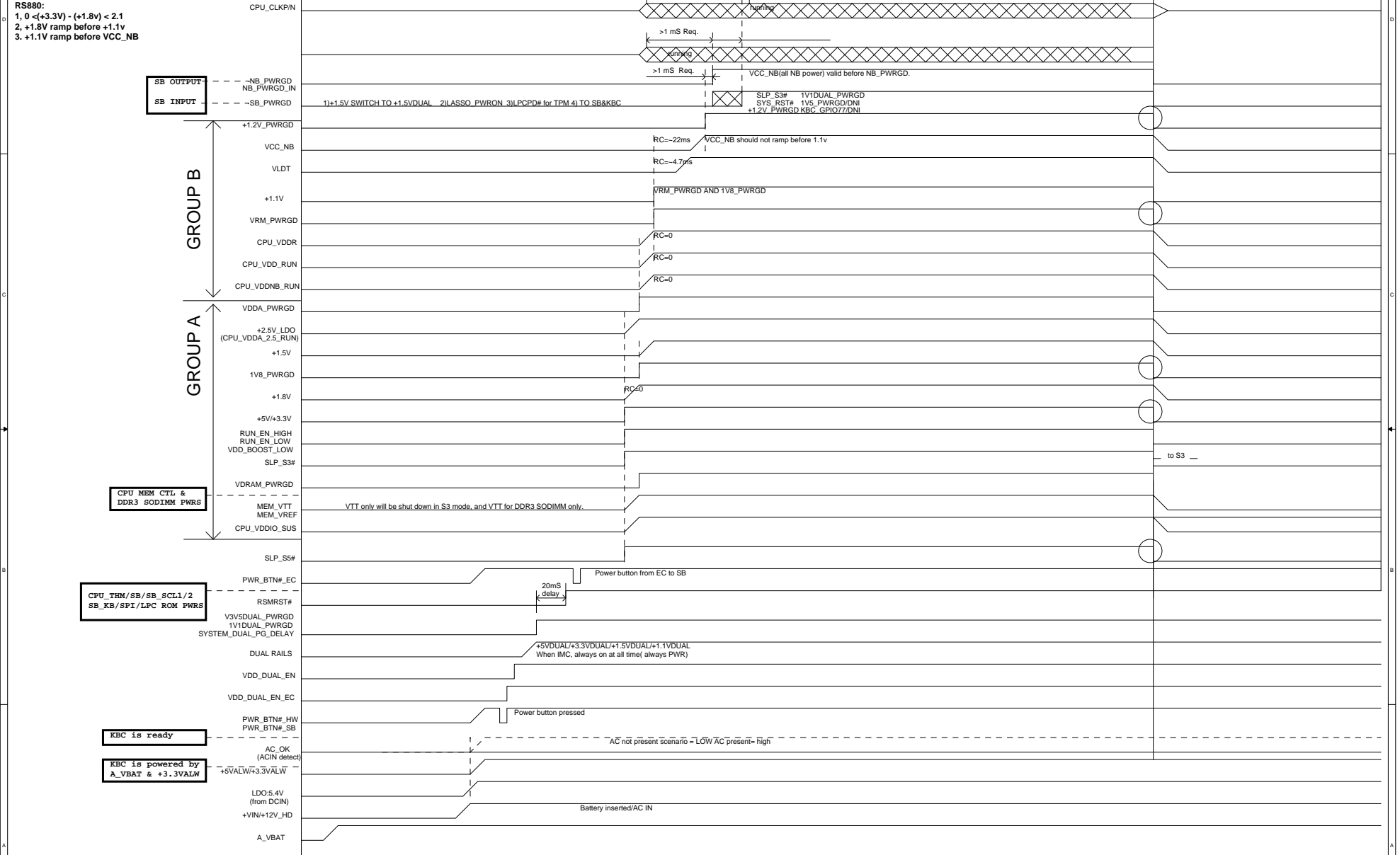
MICRO-STAR INT'L CO.,LTD

MS-168x

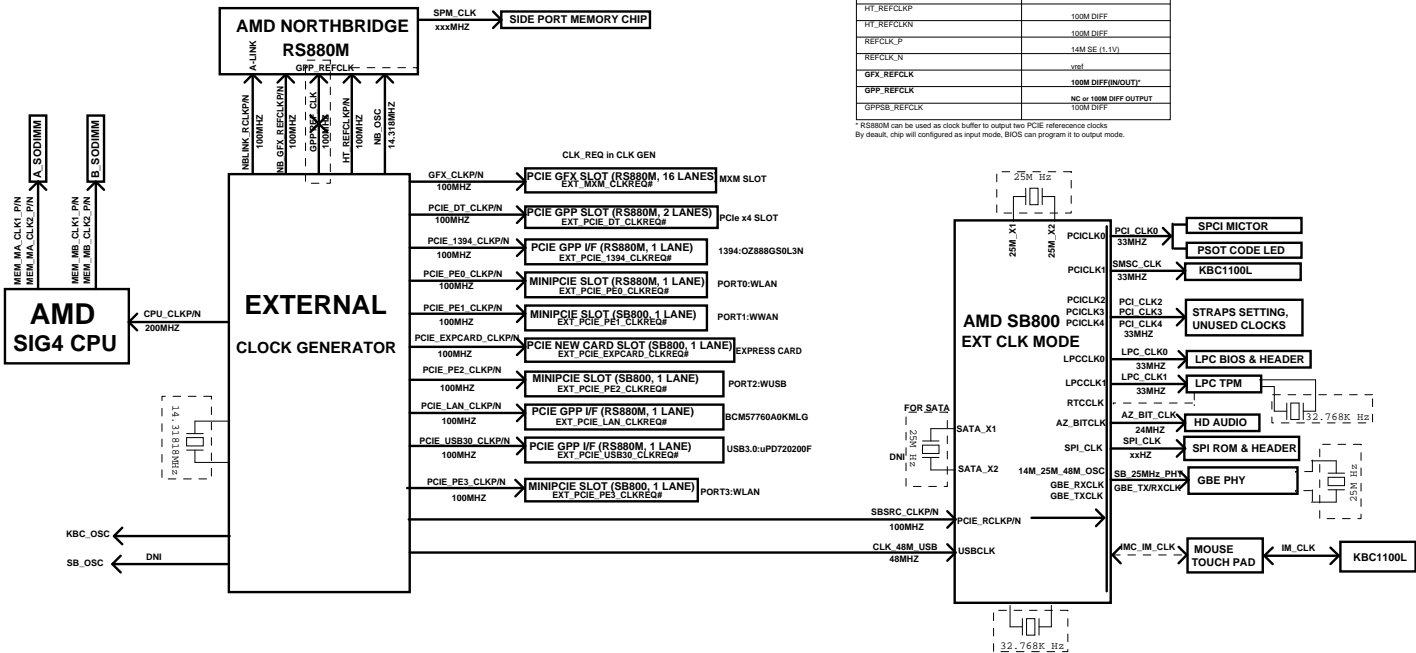
Size Custom Document Description **POWER DELIVERT** Rev 0A

Date: Wednesday, January 13, 2010 | Sheet 3 of 52

- RS80:**
- +3.3VDUAL ramp before +1.1VDUAL
 - +3.3V ramp before +1.8v
 - +1.8v ramp before +1.1v
 - +3.3v ramp before +1.1v
 - +3.3VALW_R ramping down time > 300us
 - 50uS <= All power rails except +3.3VALW_R <= 40mS
 - 100uS <= +3.3VALW_R <= 40mS
- RS880:**
- 0 < (+3.3V) - (+1.8v) < 2.1
 - +1.8v ramp before +1.1v
 - +1.1v ramp before VCC_NB



EXTERNAL CLOCK MODE

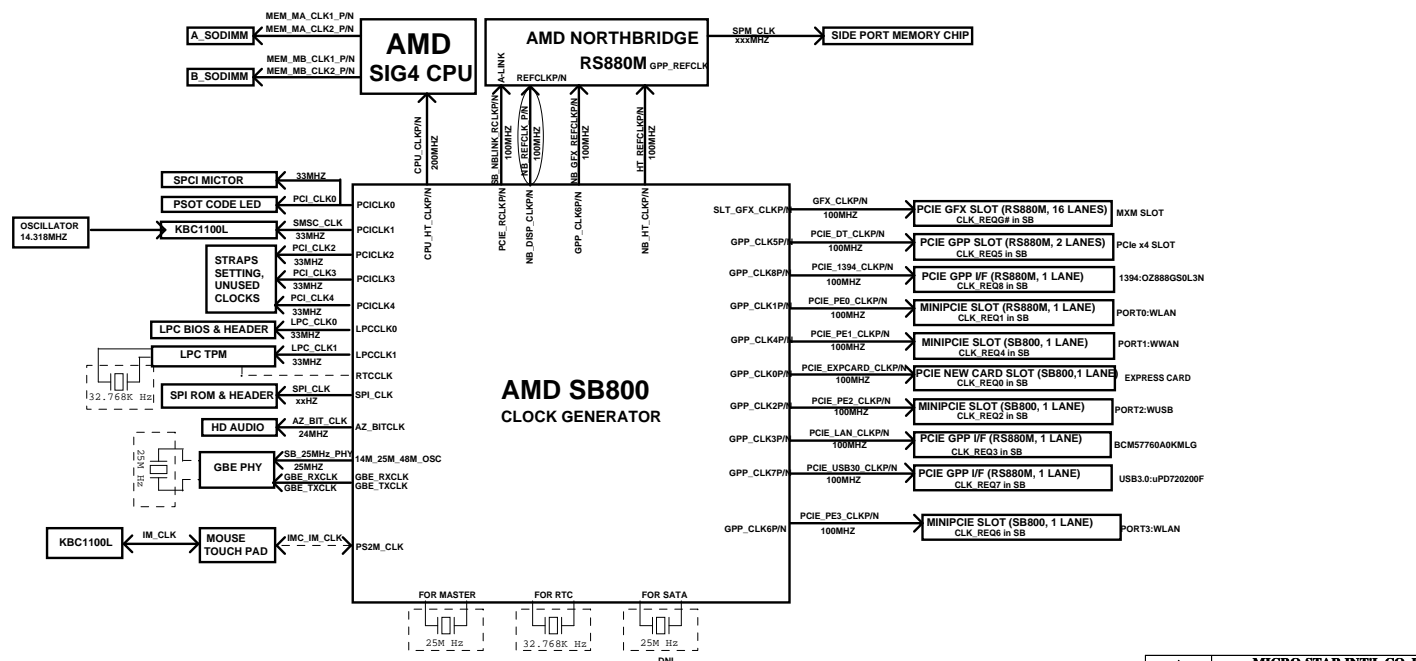


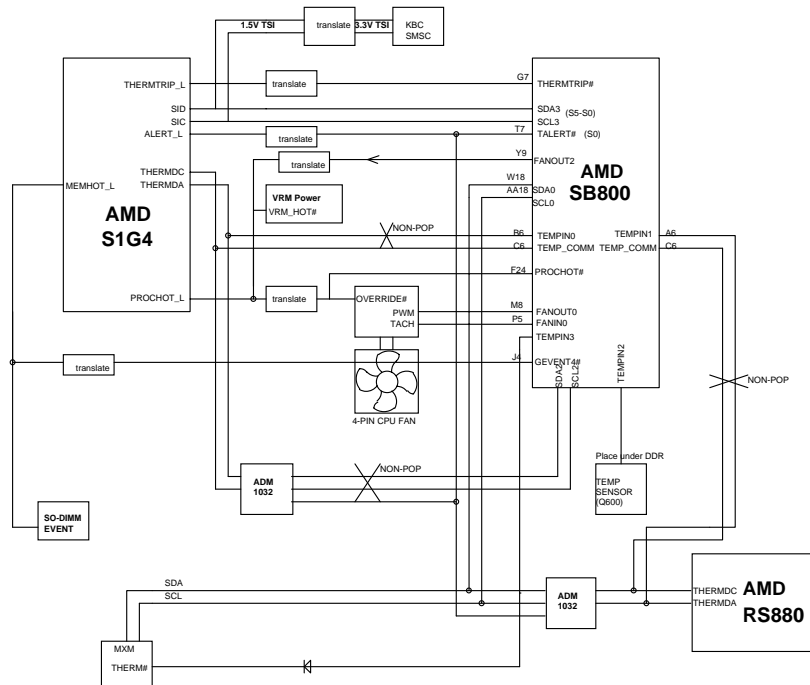
NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DREF
HT_REFCLKN	100M DREF
REFCLK_P	14M SE (1.1V)
REFCLK_N	14M SE (1.1V)
GFX_REFCLK	100M DREF/IN/OUT
GPP_REFCLK	100M DREF/IN/OUT
GPPSB_REFCLK	100M DREF

RS880M can be used as clock buffer to output two PCIE reference clocks
 By default, chip will configured as input mode, BIOS can program it to output mode.

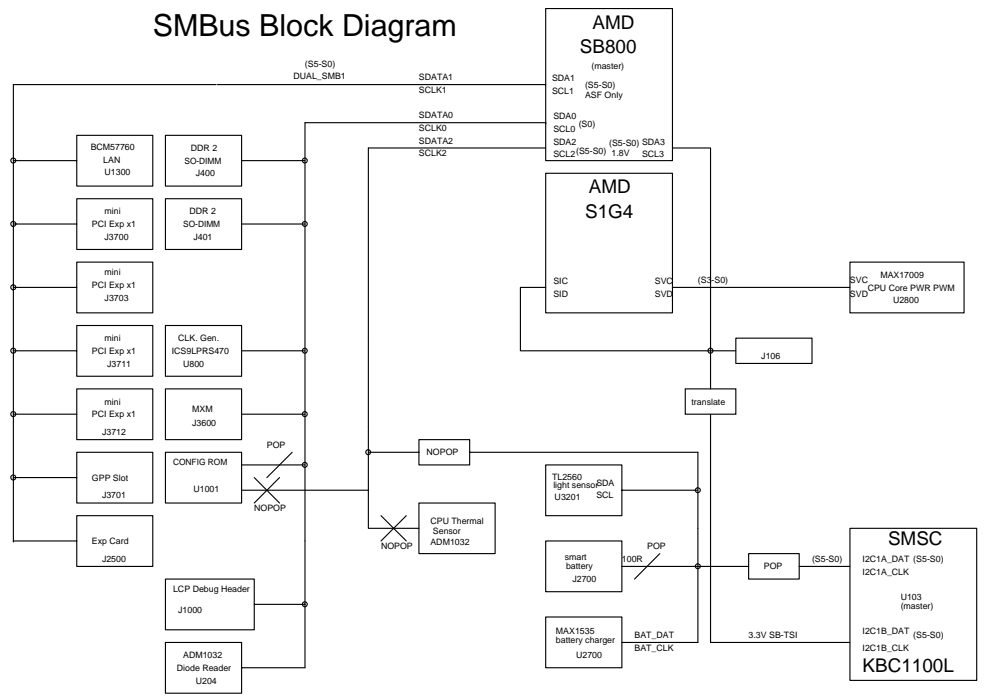
INTERNAL CLOCK MODE





Thermal disaster prevention is implemented by PROCHOT_L and THERMTRIP_L with hardware non-system dependant functions. Fan speed control will only be implemented by SB TSI software based implementation

SMBus Block Diagram



Power State / Voltage Rail Activity Summary

Global System State	Sleep State	Processor Power State	Description	RTC	ALW	DUAL	SUS	RUN
G0	S0	C0	Running	ON	ON	ON	ON	ON
G0	S0	C0	Running	P-state transitions under OS control	ON	ON	ON	ON
G0	S0	C1	Halt		ON	ON	ON	ON
G0	S0	C2	Stop grant, caches snooperable		ON	ON	ON	ON
G0	S0	C3	TBD		ON	ON	ON	ON
G0	S0	C4	TBD		ON	ON	ON	ON
G1	S1	OFF	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF	Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF	Suspend to disk	ON	ON	ON	OFF	OFF
G2	S5	OFF	Soft-off	ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	Battery IN	ON	ON	ON	OFF	OFF
G3	OFF	OFF	Mechanical off	ON	OFF	OFF	OFF	OFF

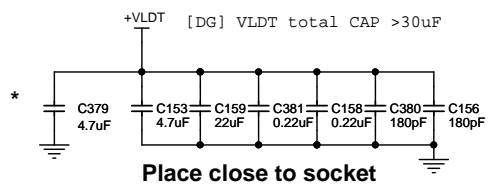
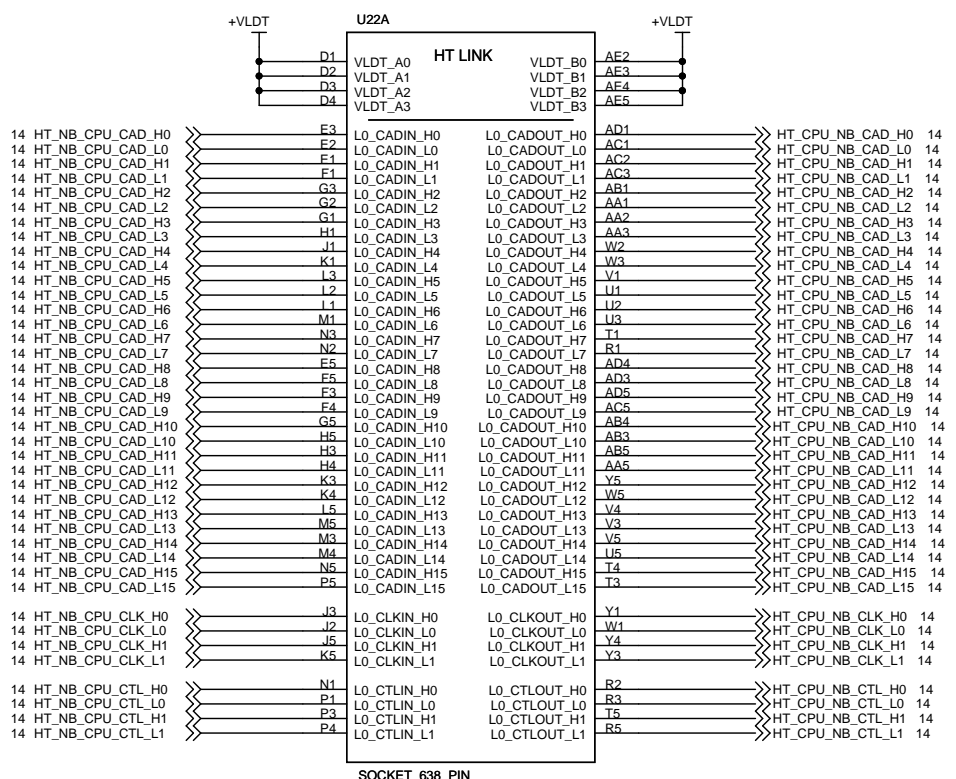
Group Name Description

INT: Stuff when use internal clock generator
 EXT: Stuff when use external clock generator
 DNI: DO NOT INSTALL
 KBC: Stuff when use external KBC
 IMC: Stuff when use internal EC
 A11: Resistors marked with "A11" is only for SB800A11 ONLY.

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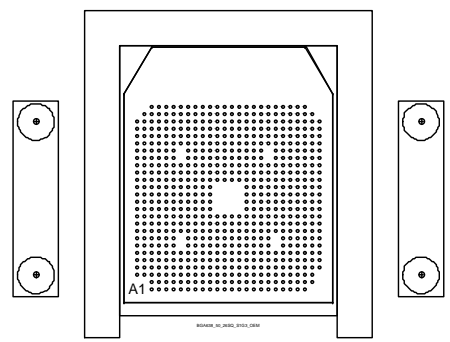
MS-168x

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SMBUS BLOCK		
Date: Wednesday, January 13, 2010	Sheet 6	of 52



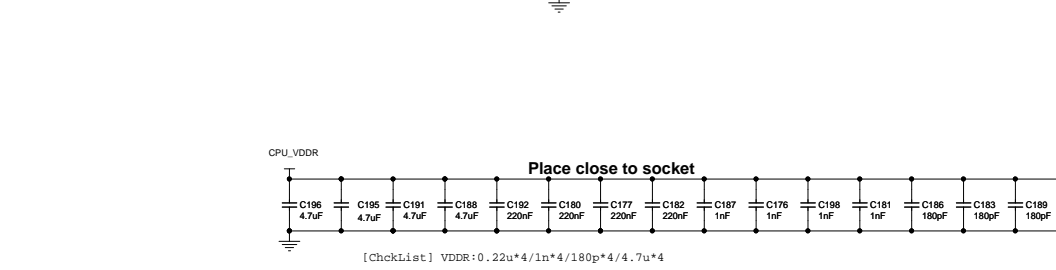
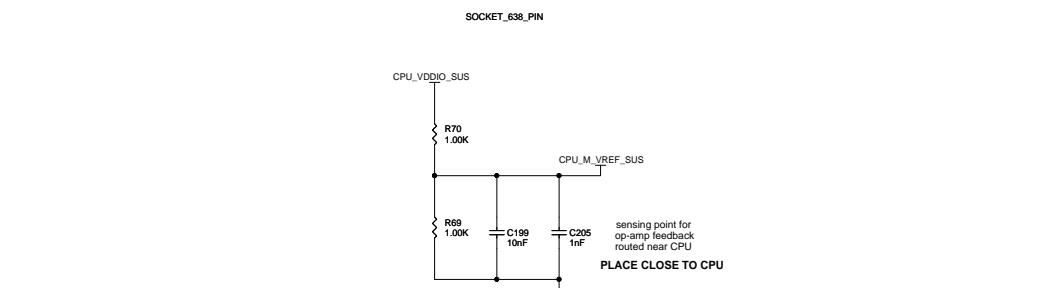
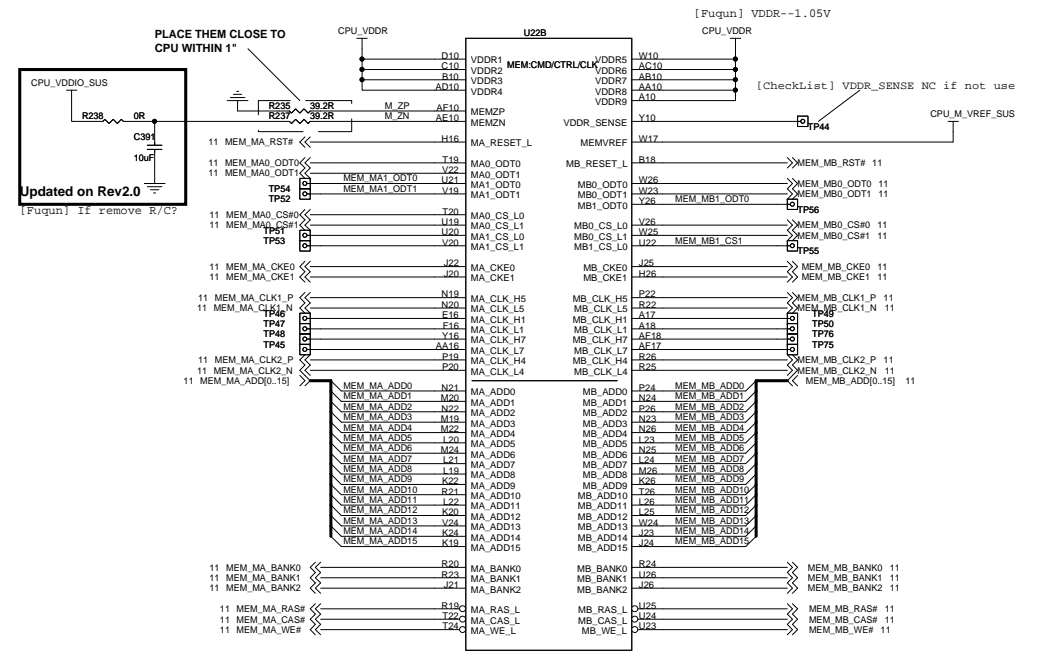
*** If VLDT is connected only on one side, one 4.7uF cap should be added to the island side**

[ChckList] Can change 22u*1/4.7u*2 to 10u*3

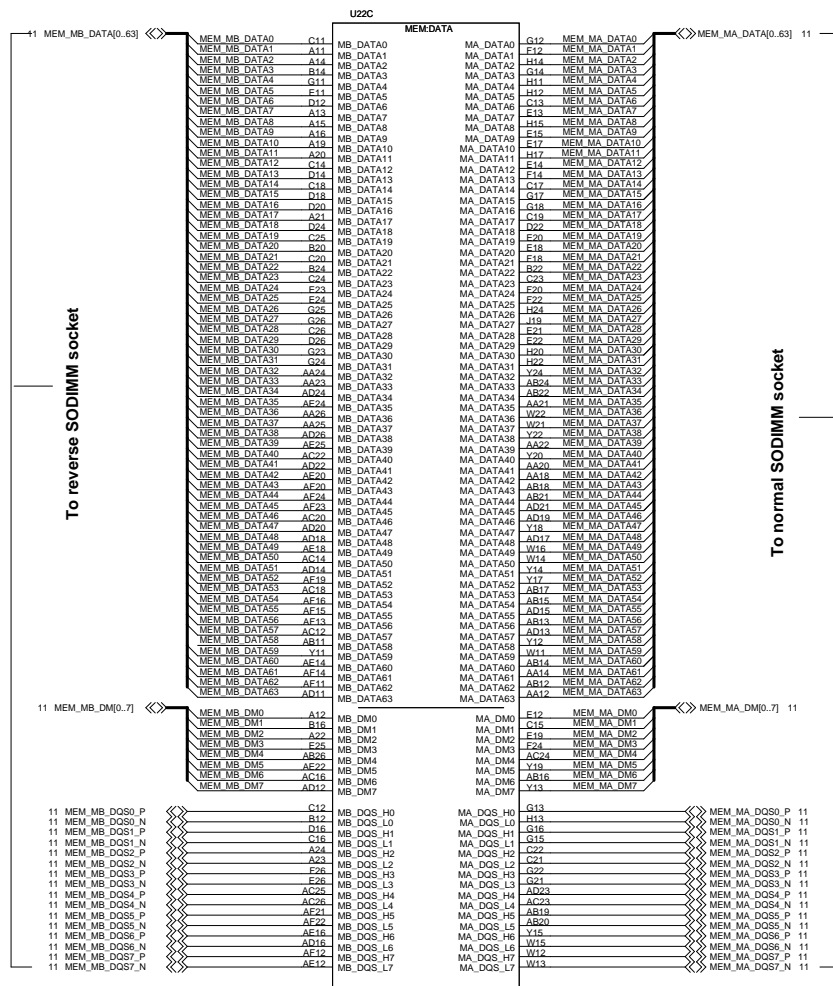


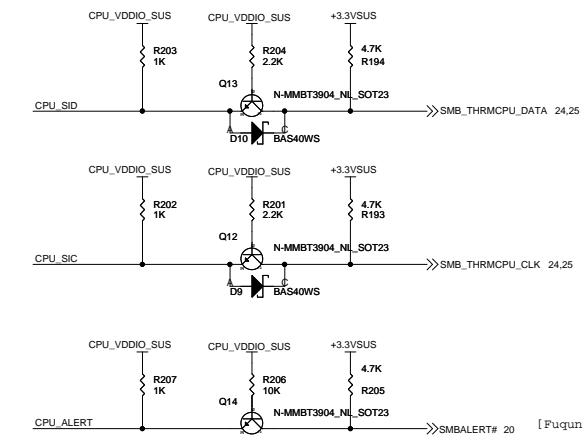
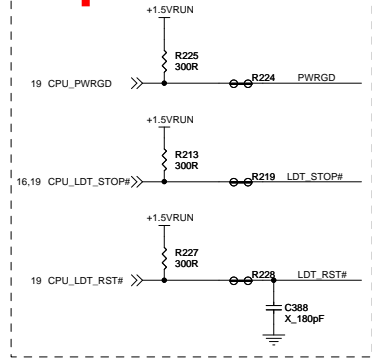
[CheckList] If the I/O device does not support the CTLIN1 pair, pull up 51ohm

MSI			MICRO-STAR INT'L CO.,LTD	
MS-168x				
Size B	Document Description SIG4 HT I/F			Rev 0A
Date: Friday, February 05, 2010	Sheet 7 of 52			



Processor Memory Interface

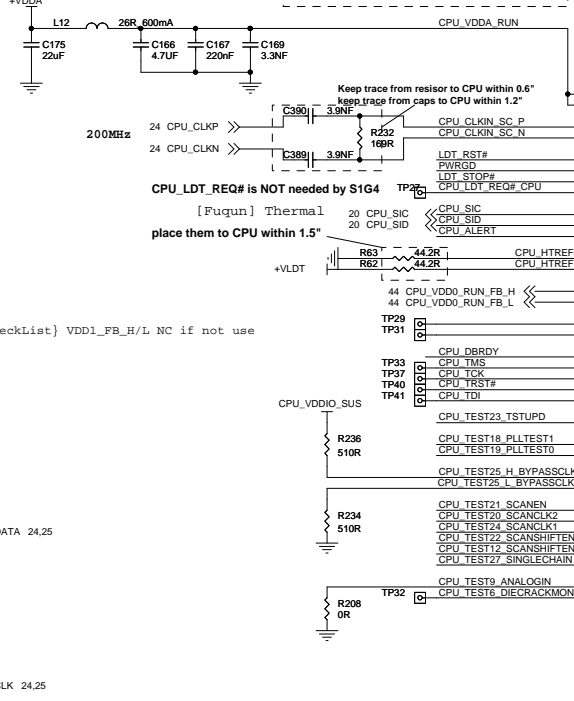




THERMDA/THERMDC is not used;
CPU thermal control is based on TSI by default.

[CheckList] VDD1_FB_H/L NC if not use

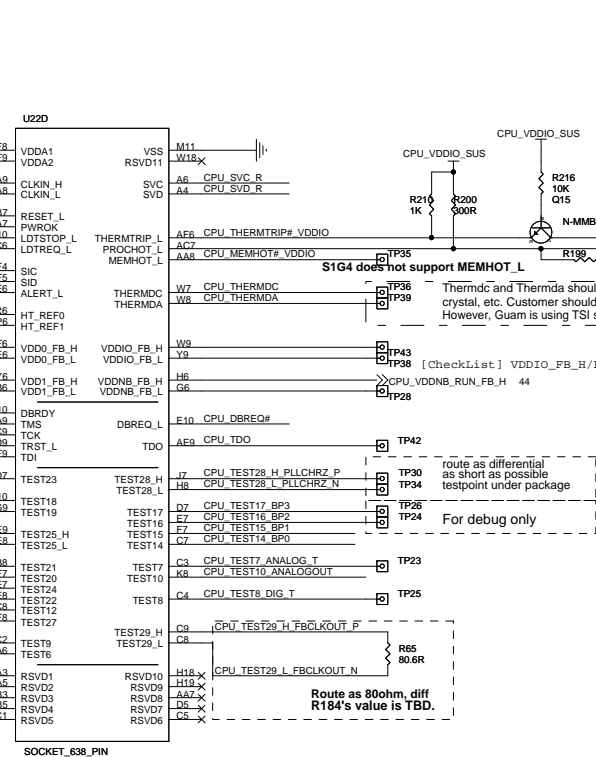
LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.



[Fuqun] Thermal place them to CPU within 1.5"

[Fuqun] Thermal

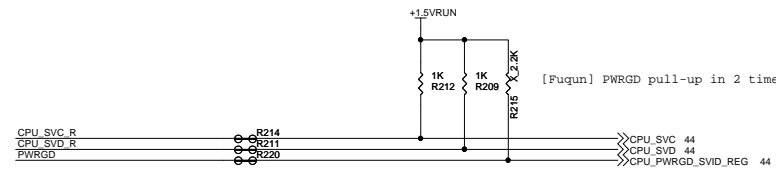
- [Fuqun] RSV/D/TEST6/7/8/10/28--NC
- [Fuqun] TEST14/15/16/17--Test Point
- [Fuqun] TEST23/25--Test Point
- [Fuqun] TEST12/18-24--Pull down 1Kohn to VSS
- [Fuqun] TEST27 pull-up 1Kohm to VDDIO
- [Fuqun] TEST25_H pull-up 510ohm to VDDIO
- [Fuqun] TEST25_L pull-down 510ohm to VSS
- [Fuqun] TEST9 is tied to VSS
- [Fuqun] There is a (+1%) differential termination between TEST29_L and TEST29_H
- [Fuqun] CPU_DBRDY not need pull down in checklist



Route as 80ohm, diff. R184's value is TBD.

[Fuqun] TEST23--R358 NC in ref schematic?

[Fuqun] PWRGD pull-up in 2 times (R187 and R163)?



SVC	SVD	BOOT VOLTAGE(VDD)	
		(CPU/VRM_PREG# = VDD(SND))	(CPU/VRM_PREG# = OPEN)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

VID OVERRIDE TABLE (VDD)

MICRO-STAR INT'L CO.,LTD

MS-168x

Size Custom Document Description **SIG4 CTRL and DEBEG** Rev 0A

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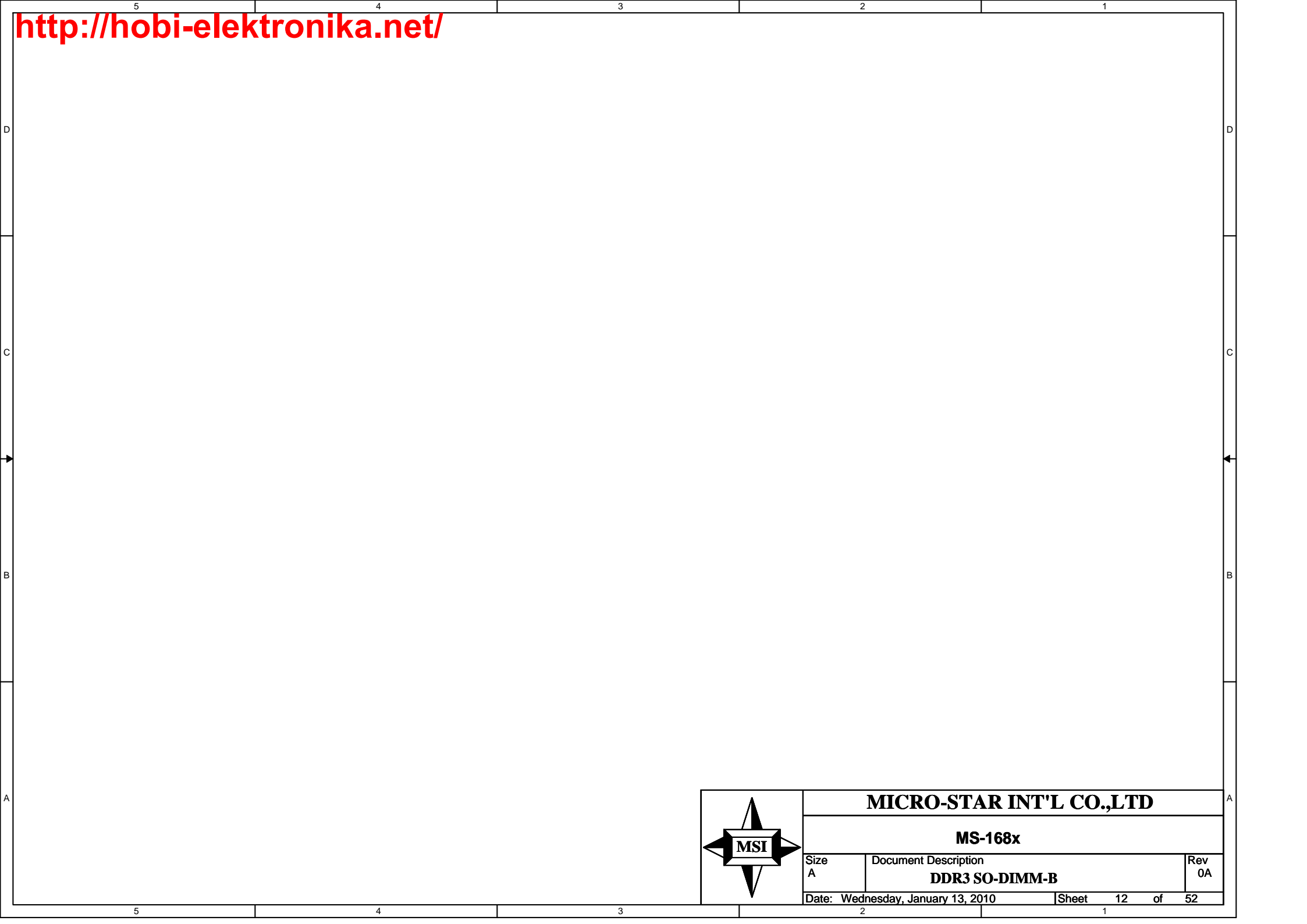
[DateSheet] Internal Termination:Systems that do not require use of these pins can rely on the internal termination to pull the signals to the proper inactive state. When these pins are used, they must not be driven with open-drain outputs, otherwise additional termination is required

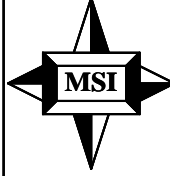
[DateSheet] Internal pull_up 870-1250 ohm: SSA[2:0], TCK, TMS, TRST_L, TDI, DBREQ_L, PLATFORM_TYPE, TEST27

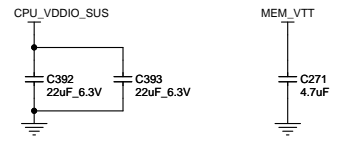
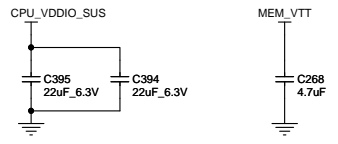
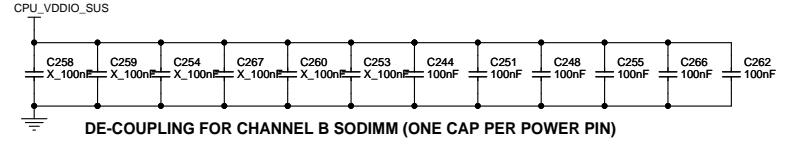
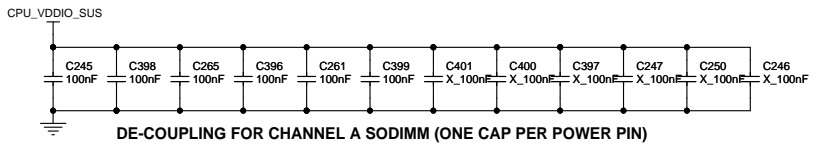
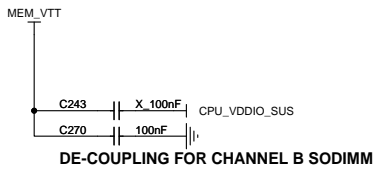
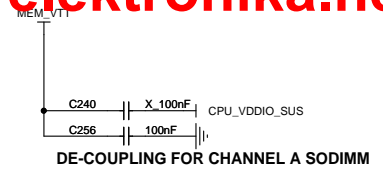
[DateSheet] Internal pull_down 870-1250 ohm: TEST12, TEST[20:24]

Internal pull_up 870-1250 ohm: SSA[2:0], TCK, TMS, TRST_L, TDI, DBREQ_L, PLATFORM_TYPE, TEST27

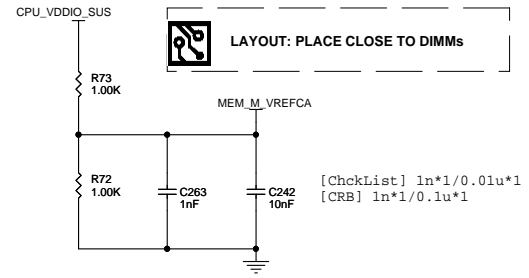
R147, R152 is installed ONLY when SCAN is enabled
R215, R185 internal ONLY
R162 is TBD



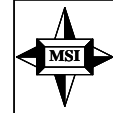
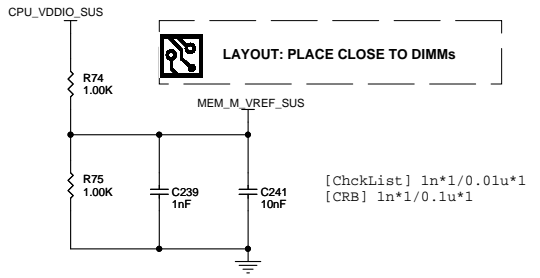
	MICRO-STAR INT'L CO.,LTD		
	MS-168x		
	Size A	Document Description DDR3 SO-DIMM-B	Rev 0A
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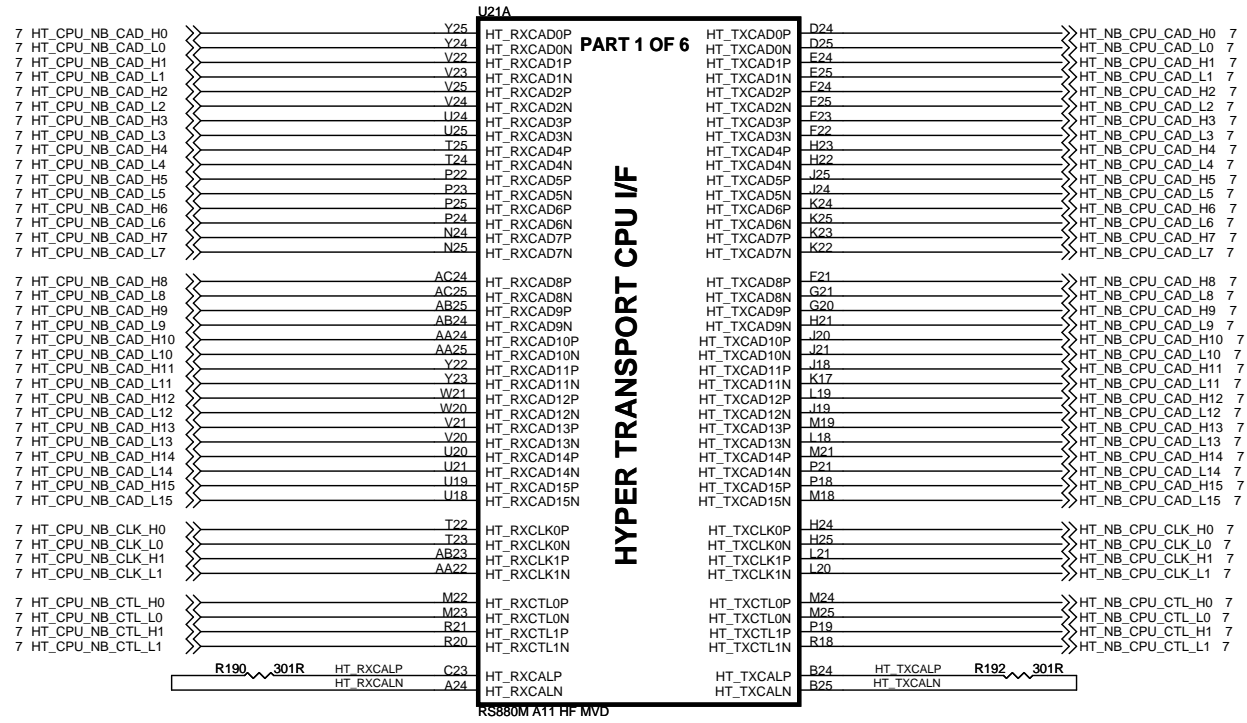
MEM_M_VREFCA



MEM_VREF_SUS



MICRO-STAR INT'L CO.,LTD		
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Size Custom	Document Description DDR3 DECOUPLING	Rev 0A
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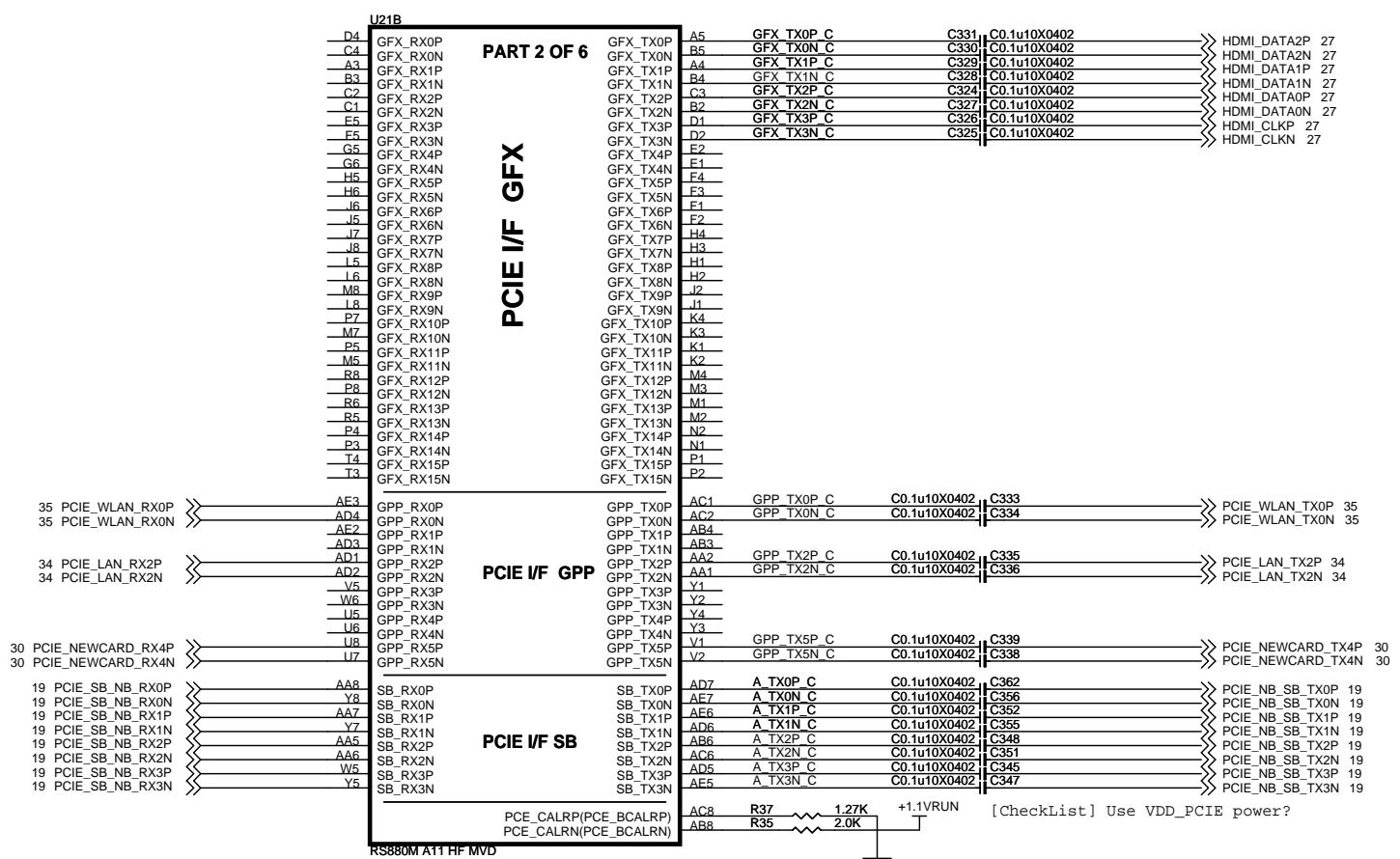
MSI		
MICRO-STAR INT'L CO.,LTD		
MS-168x		
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MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot



MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot



RS880M Display Port Support (muxed on GFX)

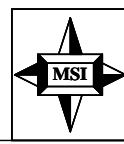
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1



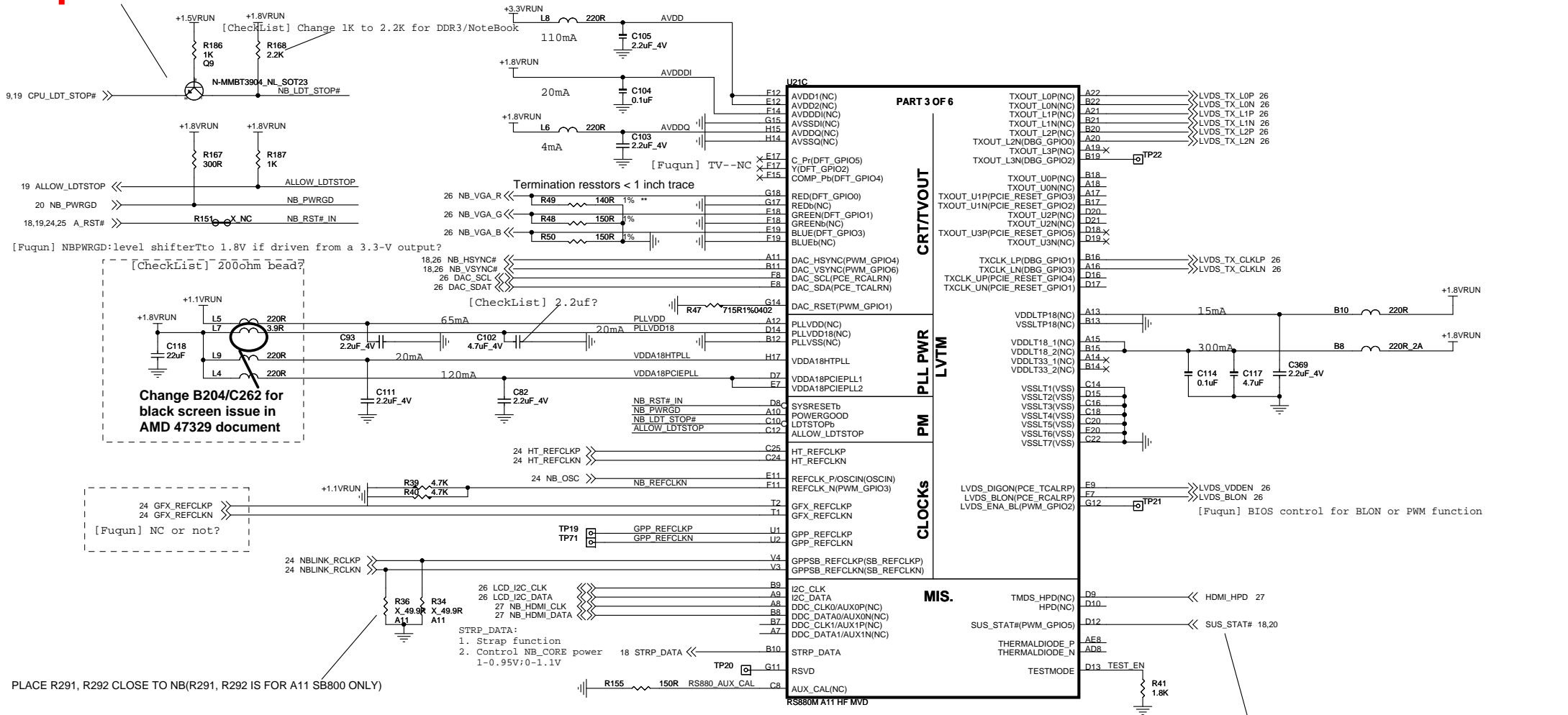
Keep the impedance of PCIE lane to 85ohm +/-15%
Including the A-link



All PCIE lane shou route 8" max for Gen2 connector and max 12" for Gen2 on board devices
Guam has the Lasso lane over 8" due to the large board, should use shorter lasso calbe for Guam.
Customer need to follow the MBDG.



MICRO-STAR INT'L CO.,LTD		
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RS880M DEBUG PIN MAPPING

DEBUG_OUT0	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLON
DEBUG_OUT3	TMDS_HPD
DEBUG_OUT4	AUX1N
DEBUG_OUT5	AUX1P
DEBUG_OUT6	HPD
DEBUG_OUT7	AUX_CAL

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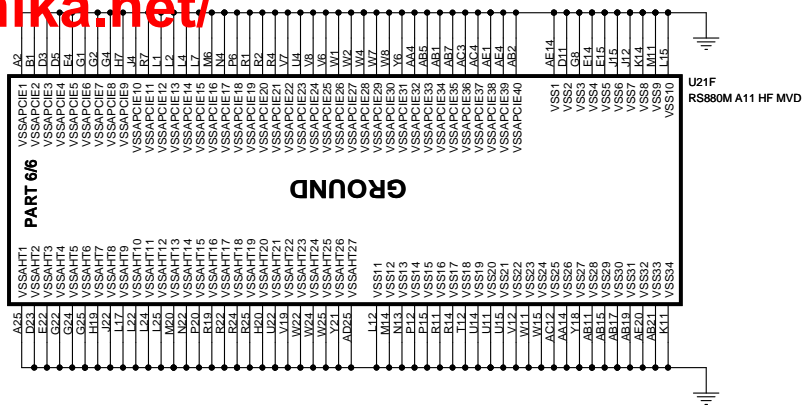
MS-168x

Size: Custom | Document Description: **RS880M-1/F** | Rev: 0A

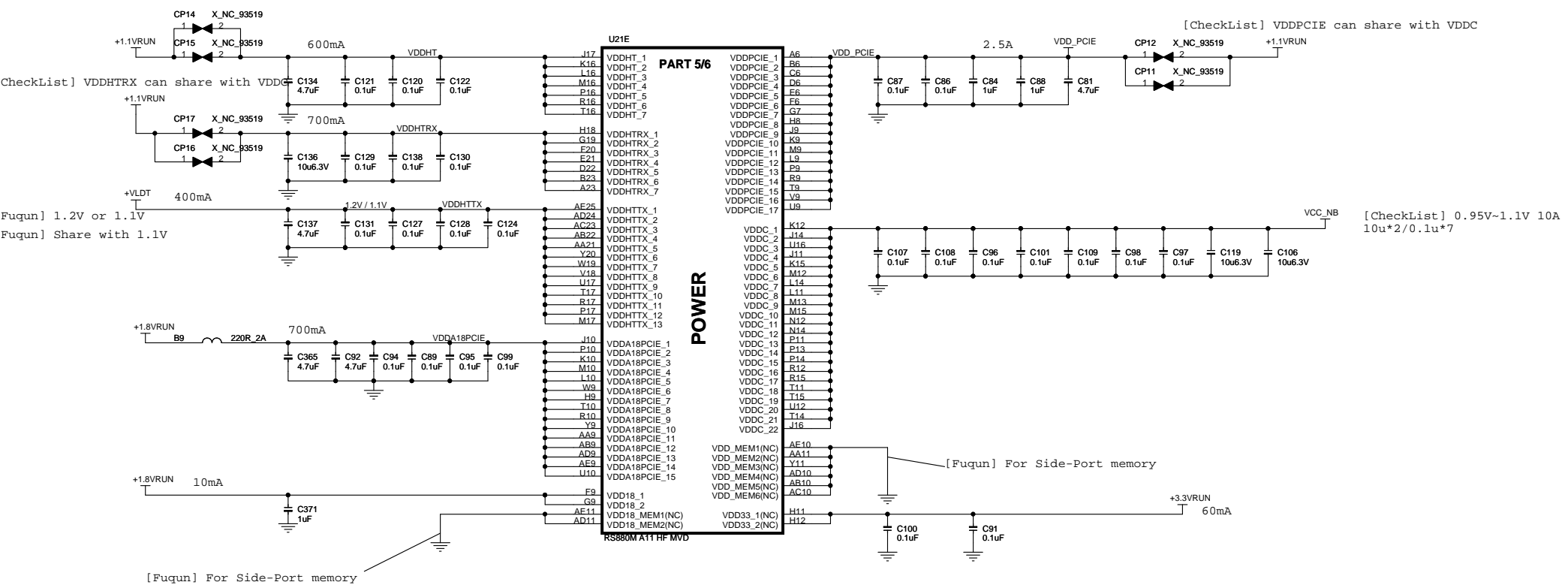
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RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC



[CheckList] VDDHT can share with VDDC



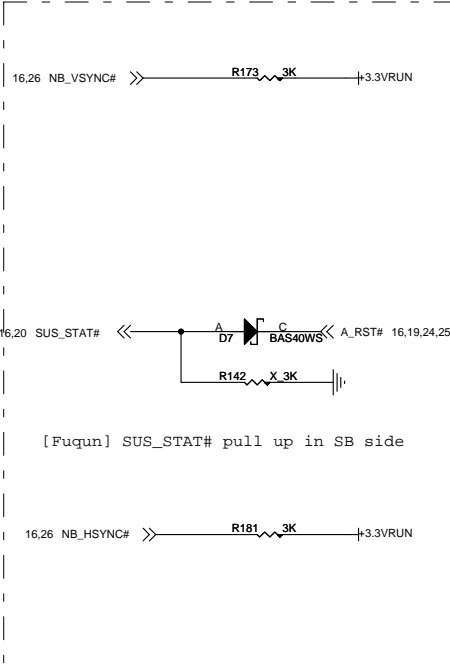
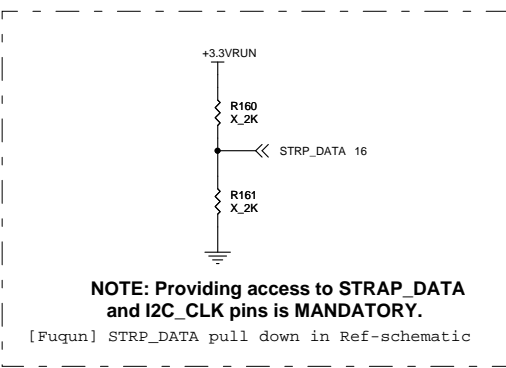
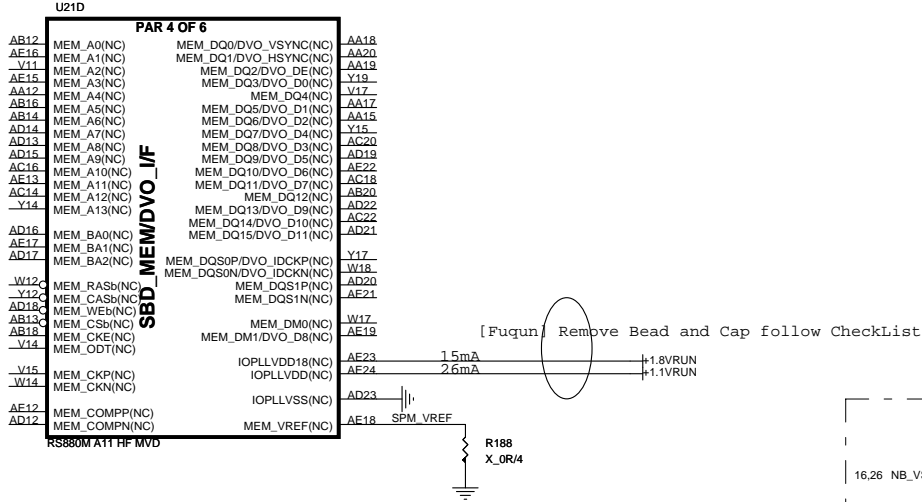


MICRO-STAR INT'L CO.,LTD

MS-168x

Size: Custom | Document Description: **RS880M-POWER** | Rev: 0A

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STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M	
1 = Disable	
0 = Enable	

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

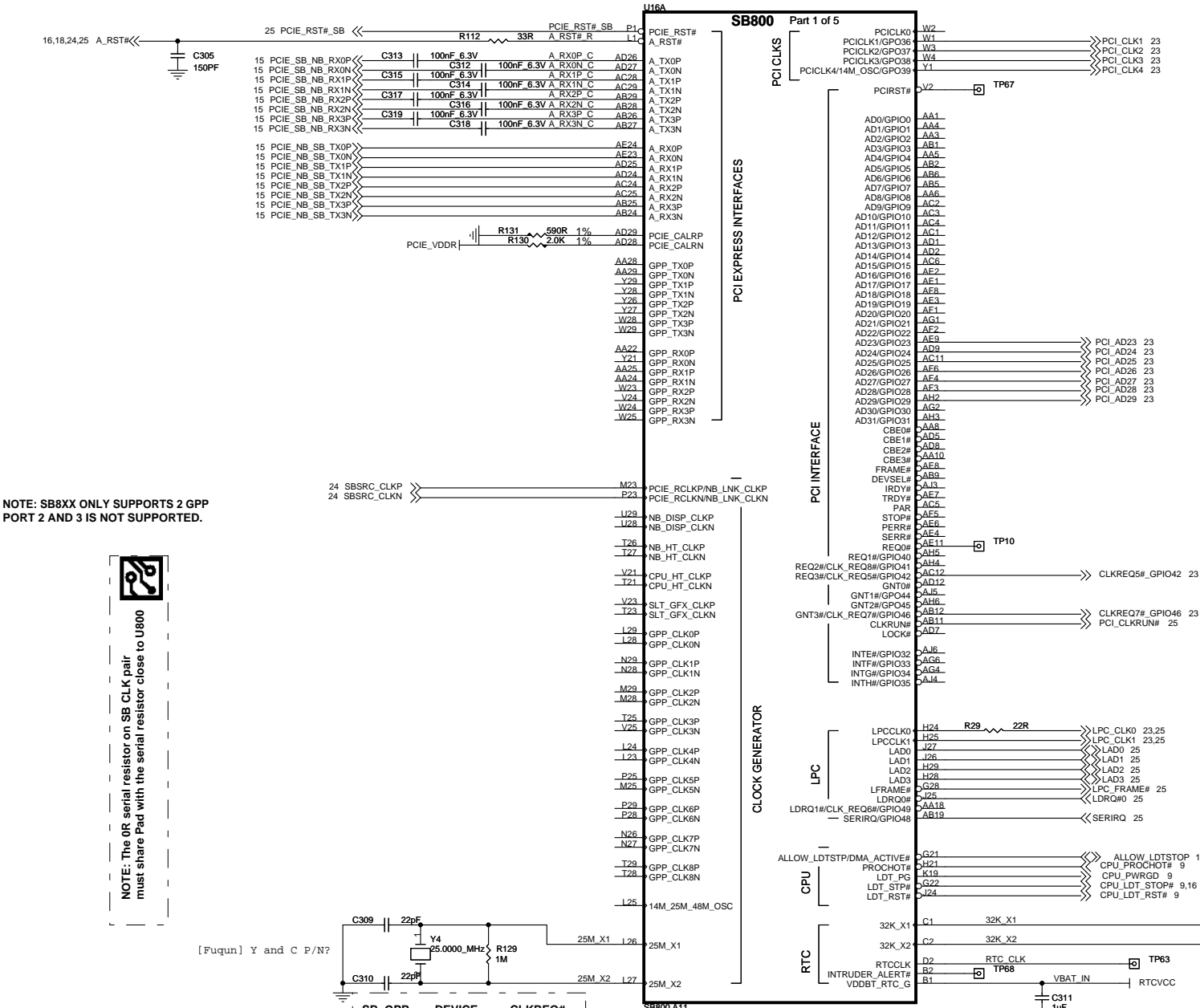
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

COUPLING CAPS CLOSE TO U600



PEX_STD_SW#: Low - Standard(desktop) Swing Level Input(3T) - Low Swing Level Mode (Default)

NOTE: SB8XX ONLY SUPPORTS 2 GPP PORT 2 AND 3 IS NOT SUPPORTED.

NOTE: The 0R serial resistor on SB CLK pair must share Pad with the serial resistor close to U800

[Fuqun] Y and C P/N?

SB_GPP GFX_CLK	DEVICE	CLKREQ#	CLK_REQ#
0	MXM3.0 EXPRESS	0	
1	PE0	1	
2	PE2	2	
3	LAN	3	
4	PE1	4	
5	X4DT	5	
6	PE3	6	
7	USB3.0	7	
8	1394	8	

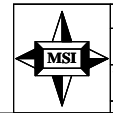
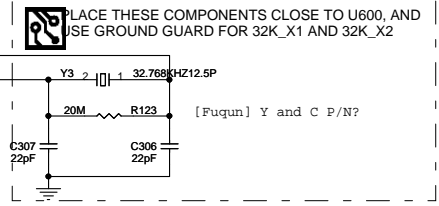
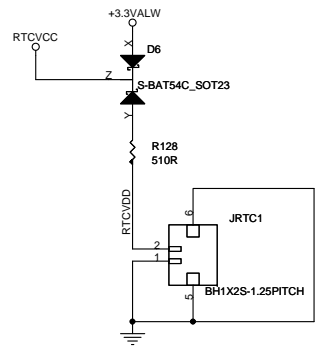
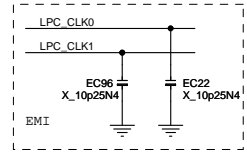
POWER EXPRESS SUPPORT

PE_GPIO0 MXM RESET H: Enable

PE_GPIO1 MXM POWER ENABLE H: Enable

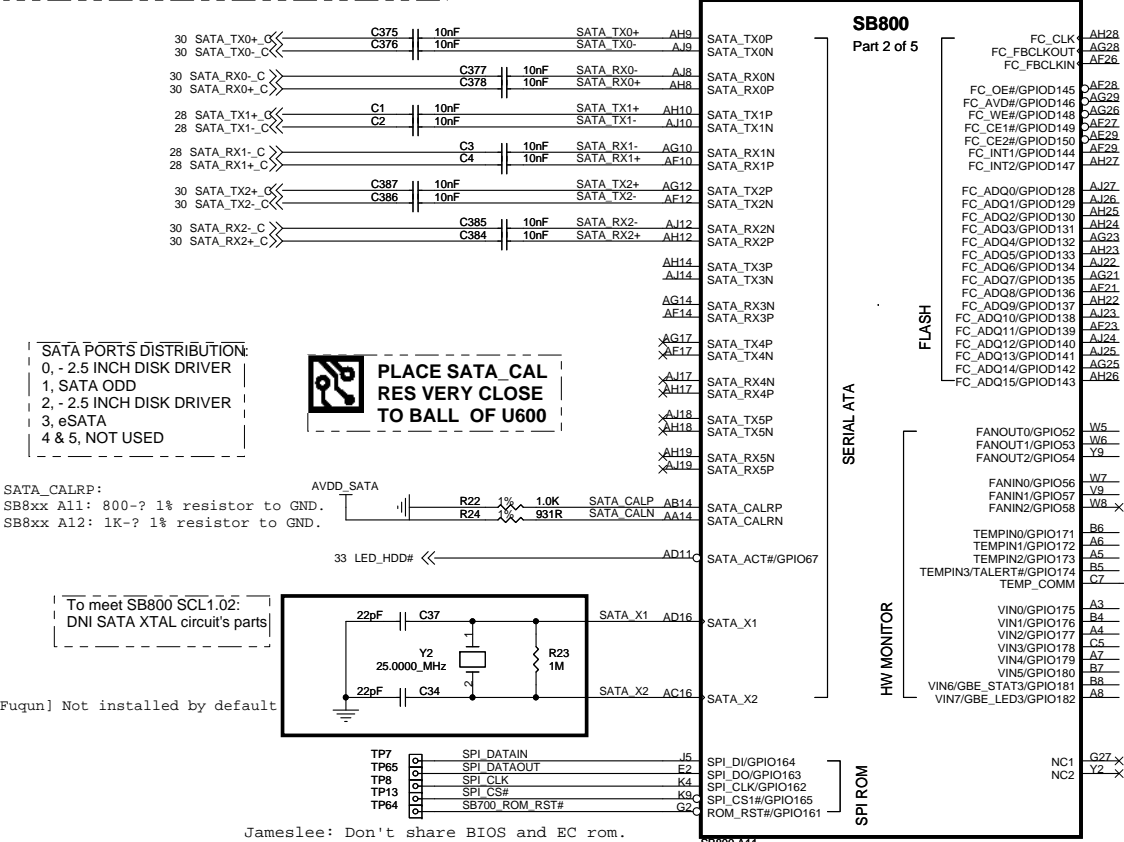
PE_GPIO2 MODE SWITCH(BY NB) H:MXM L:NB

TMDS_HPDD MXM HOT PLUG



MICRO-STAR INT'L CO.,LTD			
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Custom	SB820-PCIE/PCI/CPU/LPC/CLK	0A	
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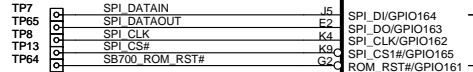
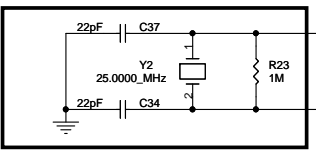
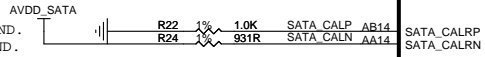
SATA trace should use only 1via on the trace. customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only



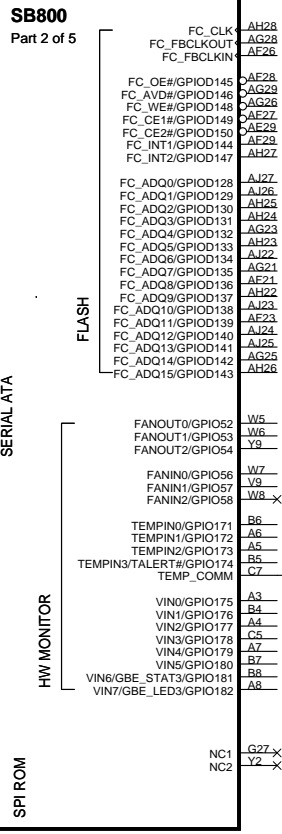
SATA PORTS DISTRIBUTION:
 0, - 2.5 INCH DISK DRIVER
 1, SATA ODD
 2, - 2.5 INCH DISK DRIVER
 3, eSATA
 4 & 5, NOT USED

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

SATA_CALRP:
 SB8xx A11: 800-? 1% resistor to GND.
 SB8xx A12: 1K-? 1% resistor to GND.



Jameslee: Don't share BIOS and EC rom.

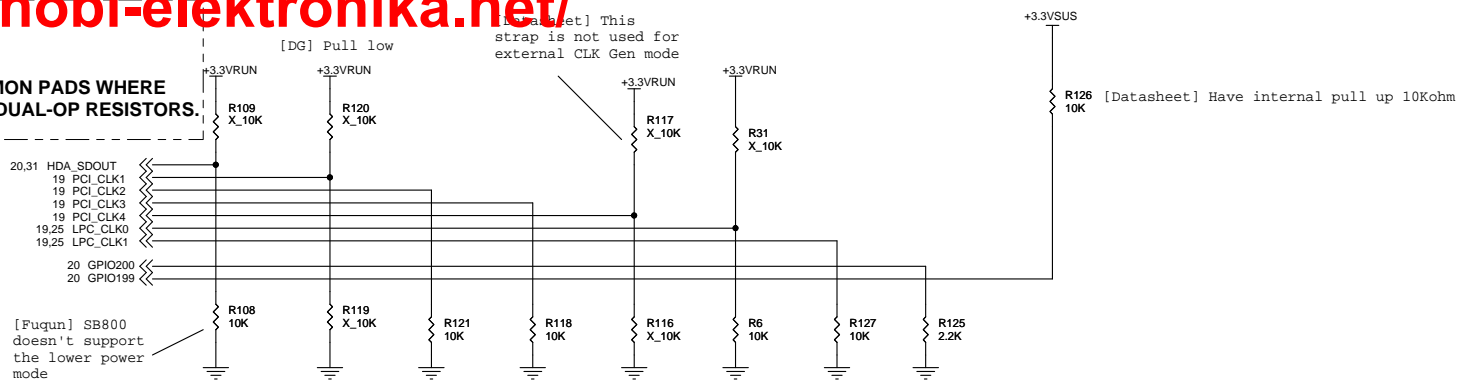


Connect C7 and D8, then go to GND directly.

[Fuqun] HWM need pull-low follow MS-124X?

NOTE: ROUTE TEMP_COMM AS A 10MIL TRACE

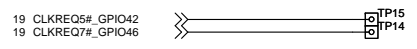
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

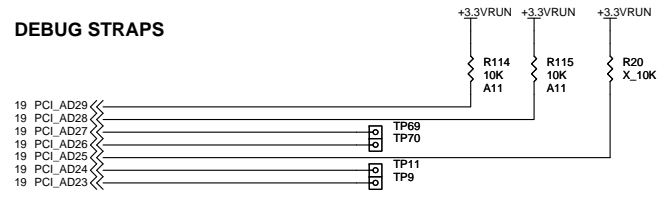
SB PCIE EEPROM STRAPS



PCI_CLK1(SMSC_CLK1)-->SB820M: Only provision for pull-down is required, not installed by default--checklist
 [Fuqun] GPIO199 NC in checklist
 [Fuqun] PCI_CLK4 high or low?

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

DEBUG STRAPS



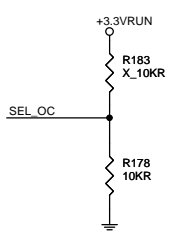
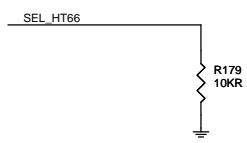
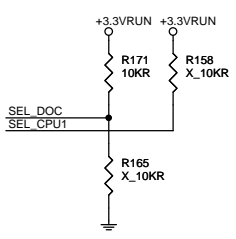
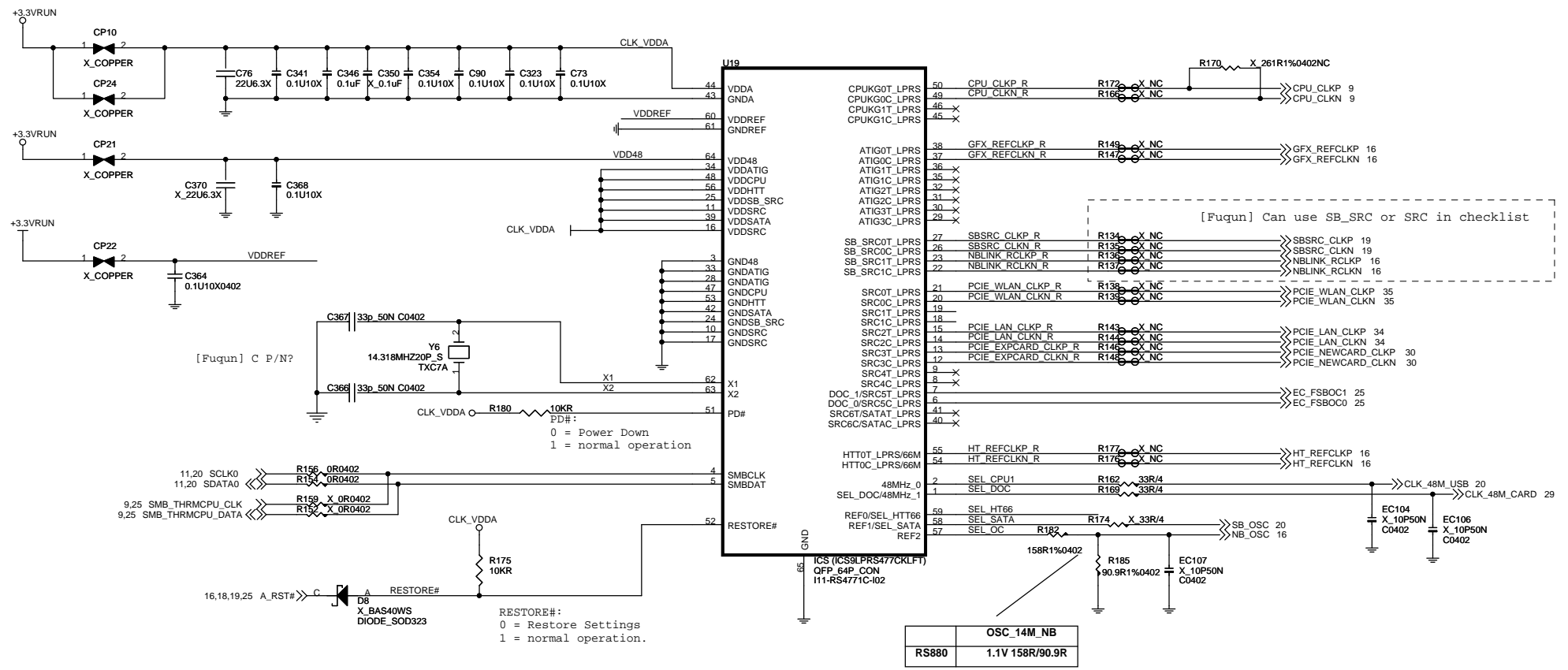
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

PCI23/24/26/27 have internal pull high 15kohm, But PCI25?
 Why PCI28/29 pull high?

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- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U11
- 2- PUT DECOUPLING CAPS CLOSE TO U11 POWER PIN



SEL_DOC/48MHz-1	1	DOC INPUT
	0	SRCLK5
SEL_CPU1/48MHz-2	1	SRCLK7
	0	CPUKG1

* default

SEL_HT66	1	66 MHz 3.3V single ended HTT clock
	0	100 MHz differential HTT clock
SEL_SATA	1	100MHz differential spreading SRC clock
	0	100 MHz spreading differential SATA clock

SEL_OC	1	Higher overclocking ability
	0	limited overclocking ability

* default

	OSC_14M_NB
RS880	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

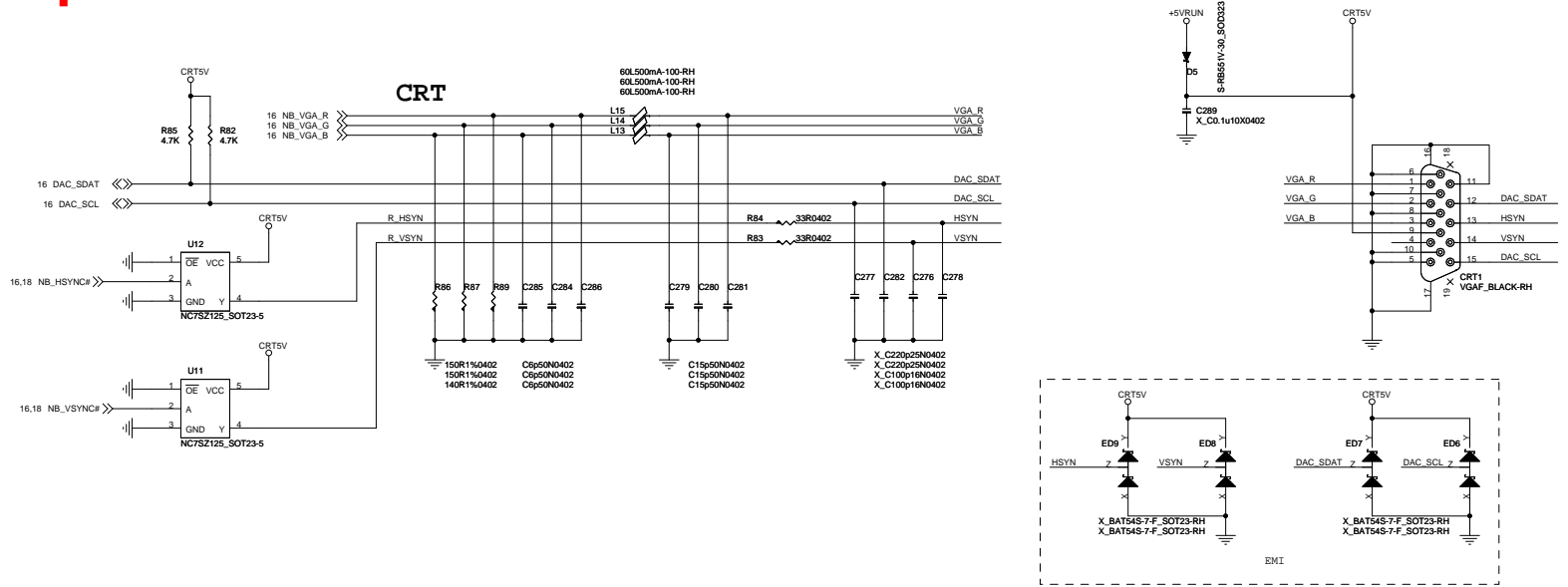
NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

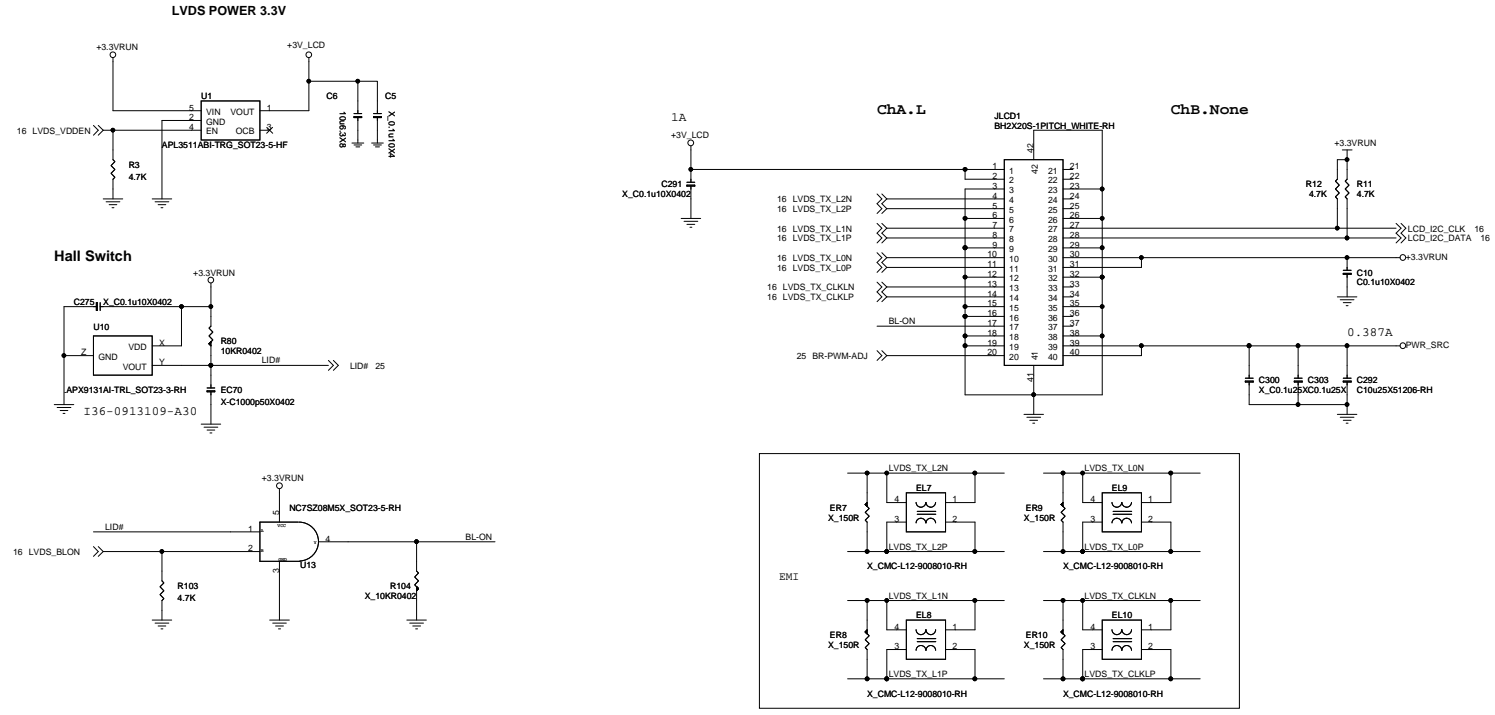
MICRO-STAR INT'L CO.,LTD

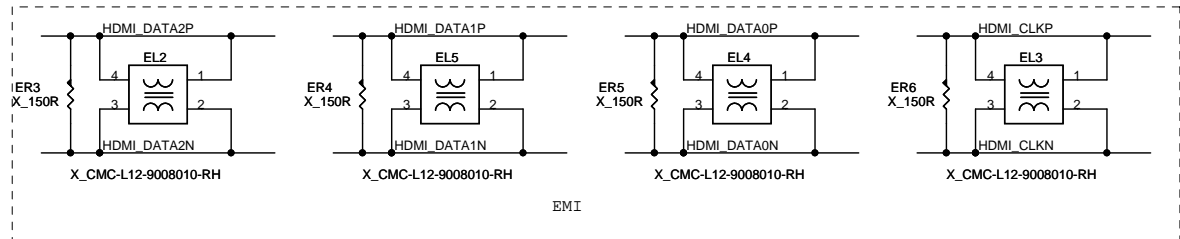
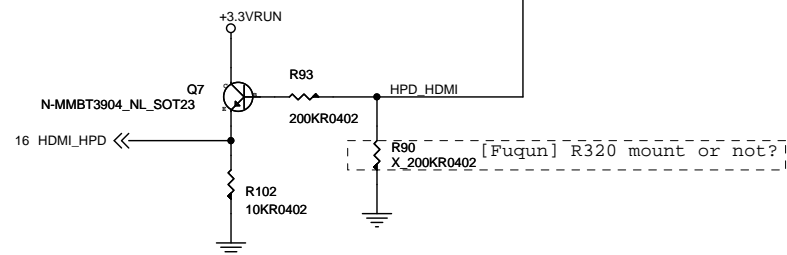
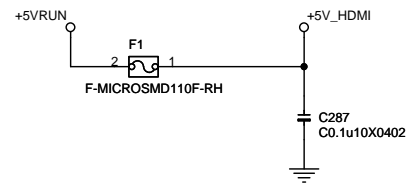
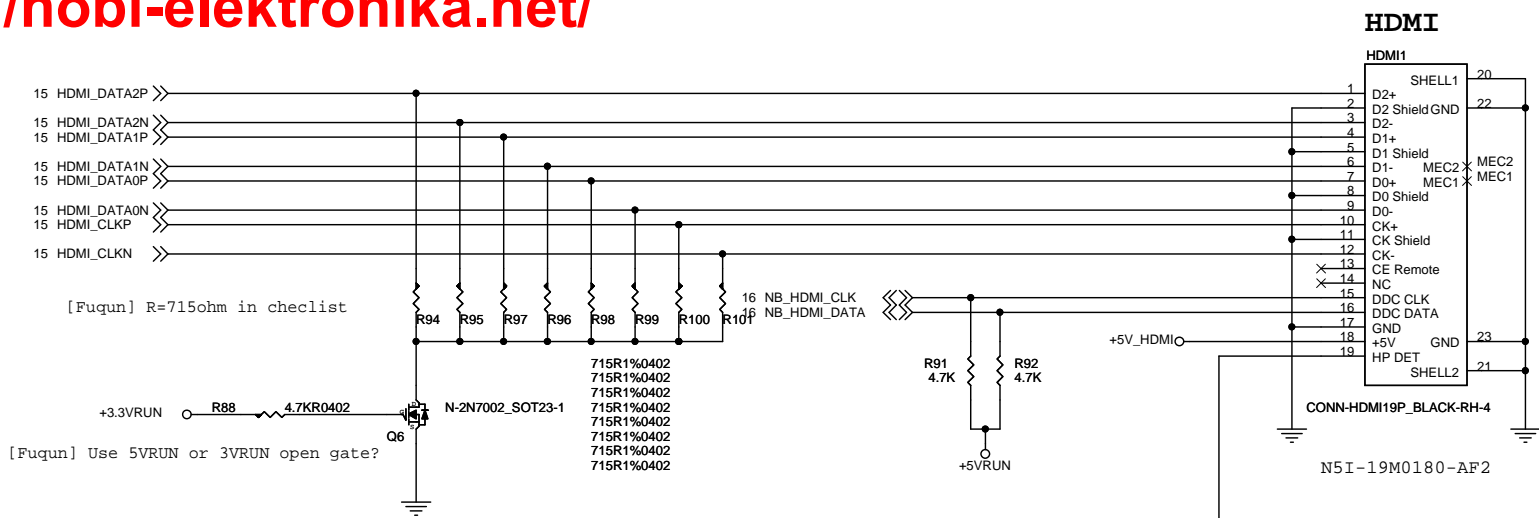
MS-168x


Size Custom	Document Description CLK GEN	Rev 0A
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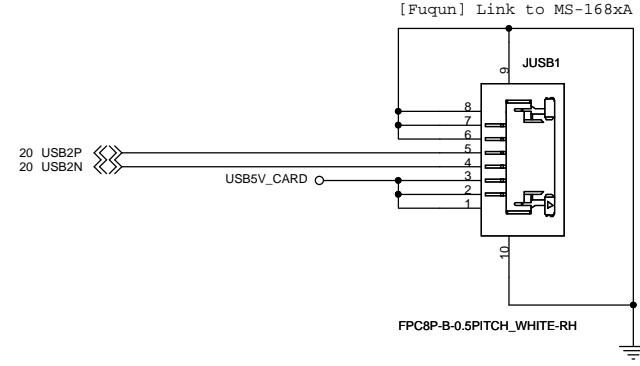
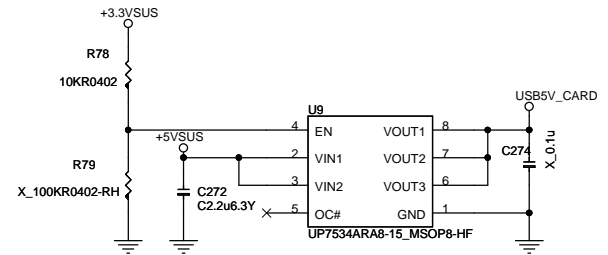
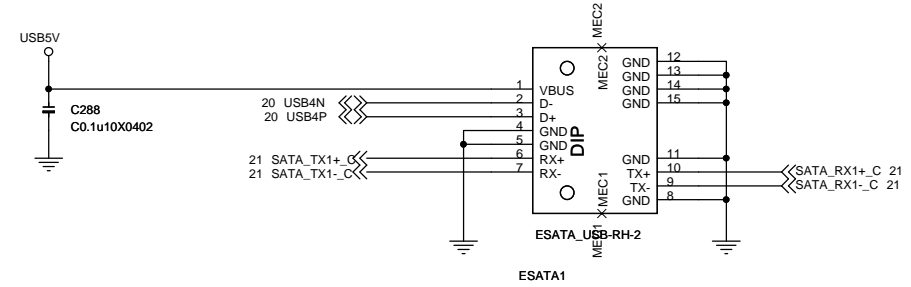
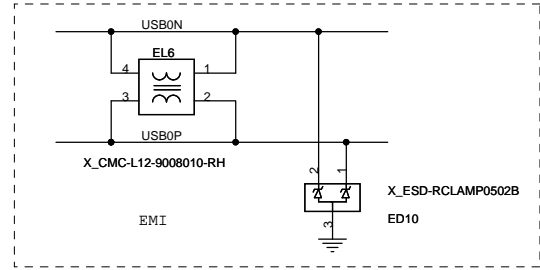
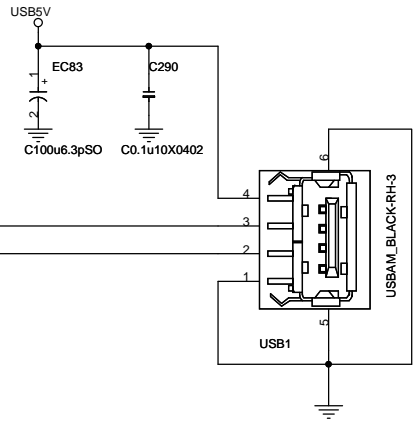
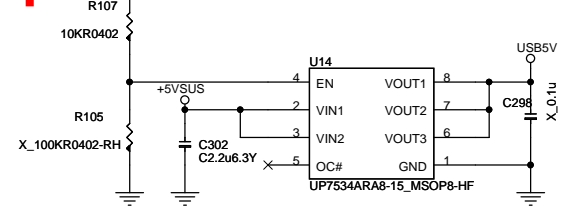


LVDS



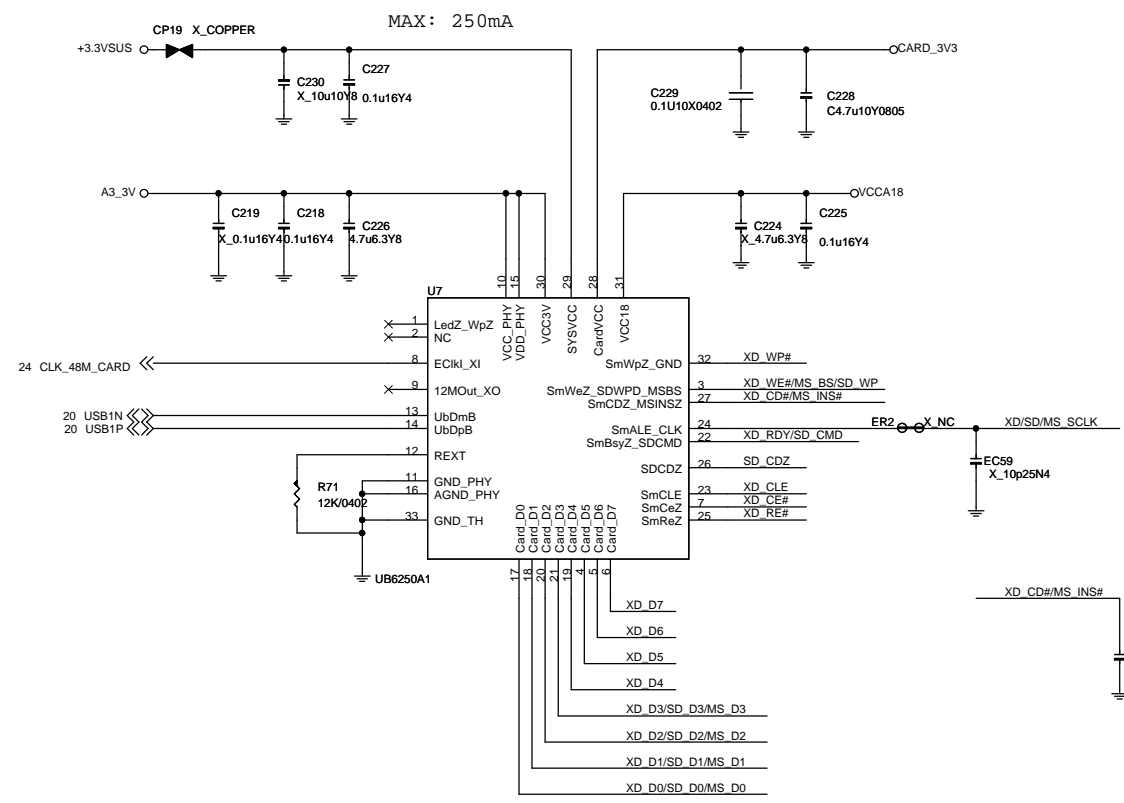


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MS-168x				
Size B	Document Description HDMI			Rev 0A
Date: Saturday, February 20, 2010		Sheet 27 of 52		

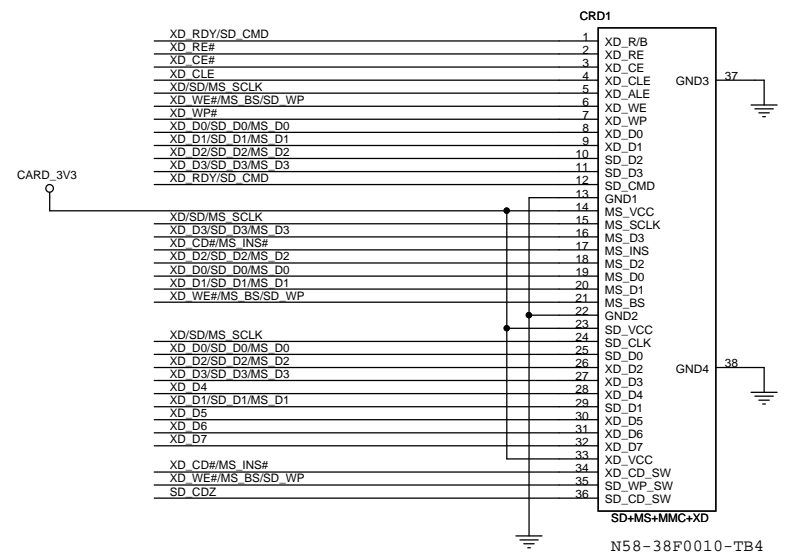


MICRO-STAR INT'L CO.,LTD		
MS-168x		
Size Custom	Document Description USB and ESATA	Rev 0A
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Card Reader Controller



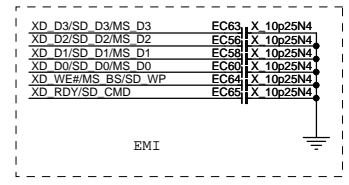
Flash Card Socket



ENE UB6250 USB20 Flash Card Reader Controller

Pins for SD, MMC, MS, and xD memory cards

Name	No	I/O	XD	SD	MMC	MS
xDceZ	7	O	xD card EN			
xDcle	23	O	xD CMD latch EN			
xDAle	24	O	xD ADDR latch EN	SD clock	MMC clock	MS serial clock
xDbsyZ	22	B	xD Ready/busy	SD CMD/response	MMC CMD/response	
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3
xDData4	19	B	xD D4		MMC D4	MS D4
xDData5	4	B	xD D5		MMC D5	MS D5
xDData6	5	B	xD D6		MMC D6	MS D6
xDData7	6	B	xD D7		MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP		MS Busy
xDReZ	25	O	xD R EN			
xDWpZ	32	O	xD WP			
SDcdZ	26	I		SD CD	MMC CD	
xDcZ	27	I	xD CD			MS CD

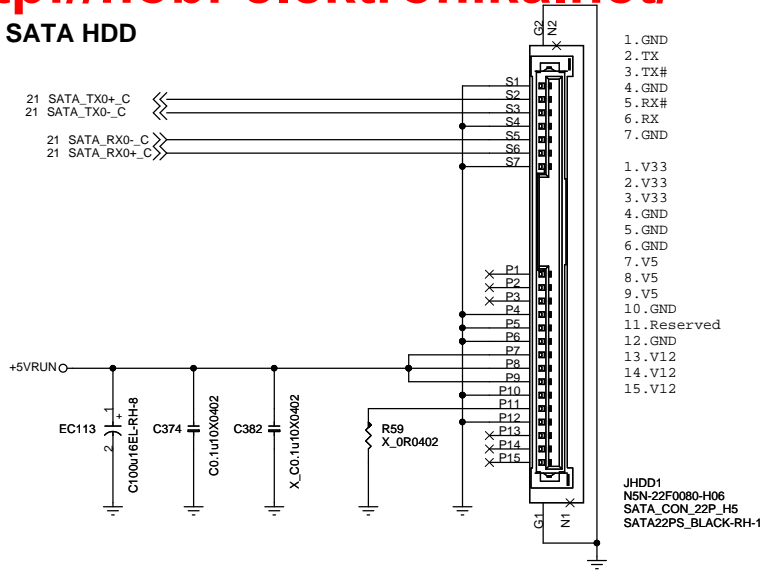


MICRO-STAR INT'L CO.,LTD

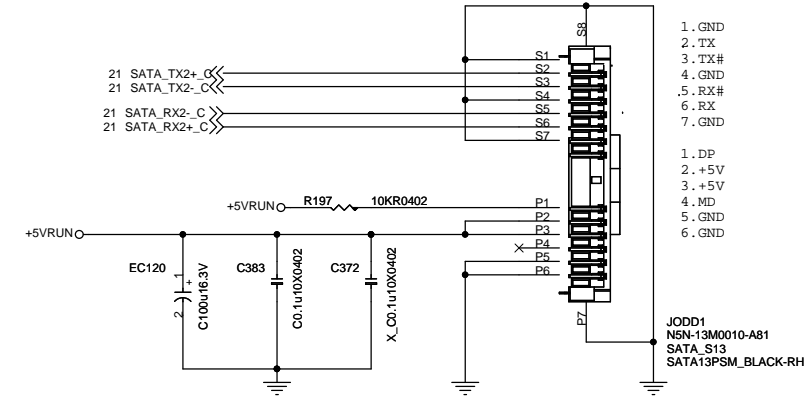
MS-168x

Size Custom	Document Description UB6250	Rev 0A
Date: Friday, February 05, 2010		Sheet 29 of 52

SATA HDD

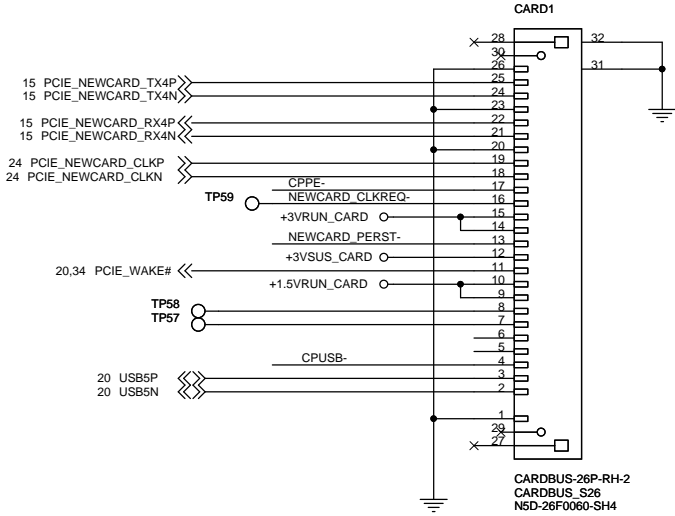
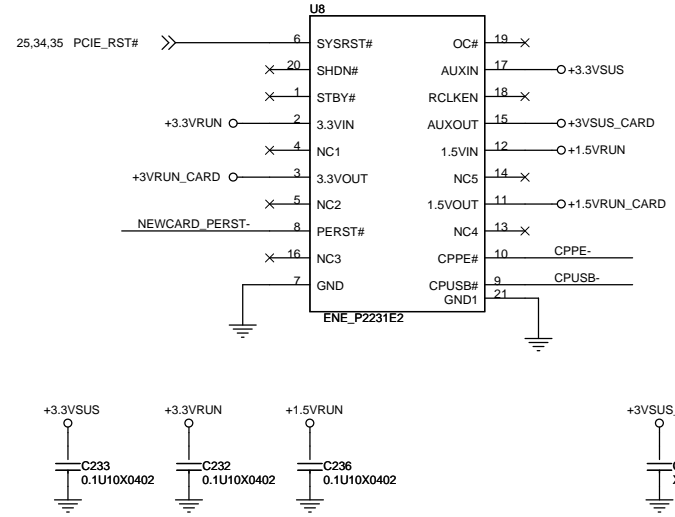


SATA ODD

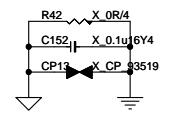
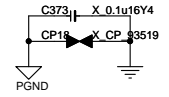
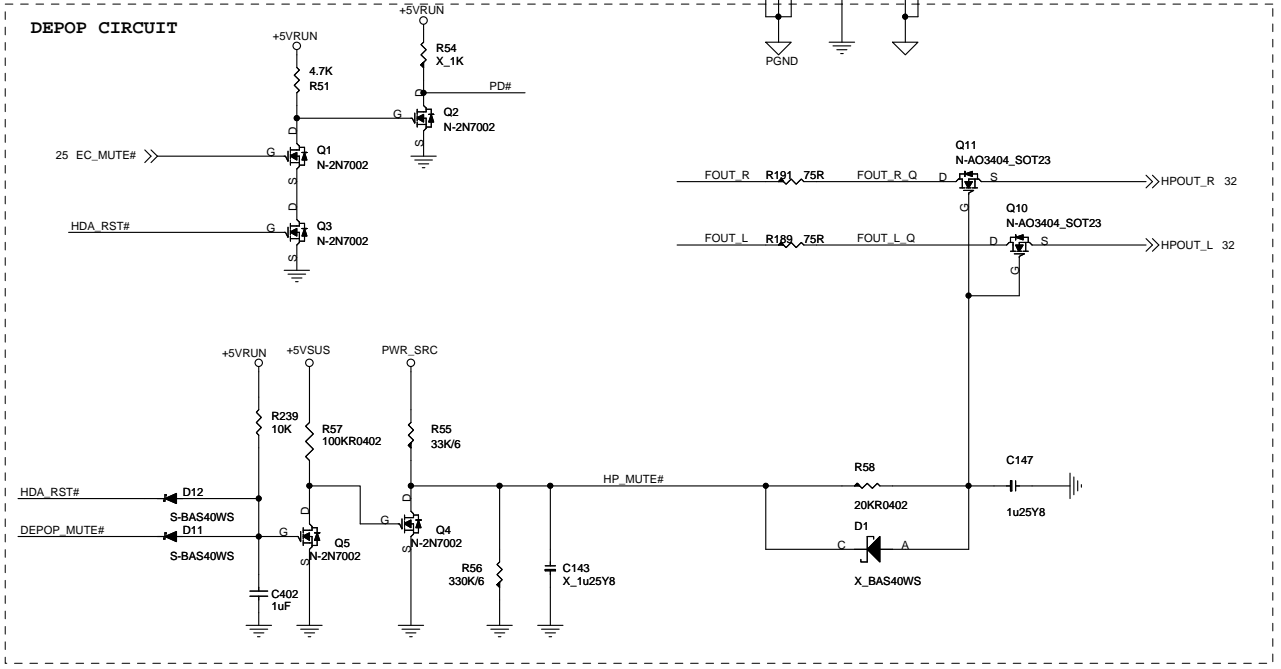
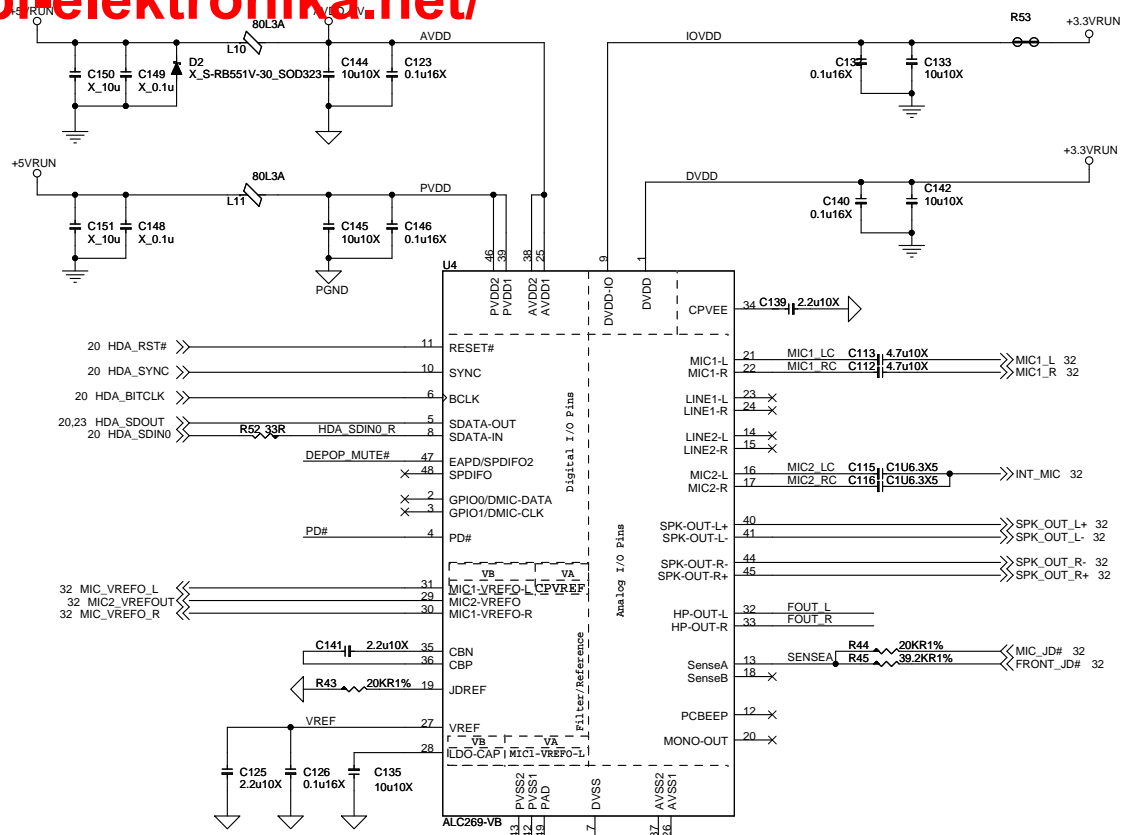


NEW CARD

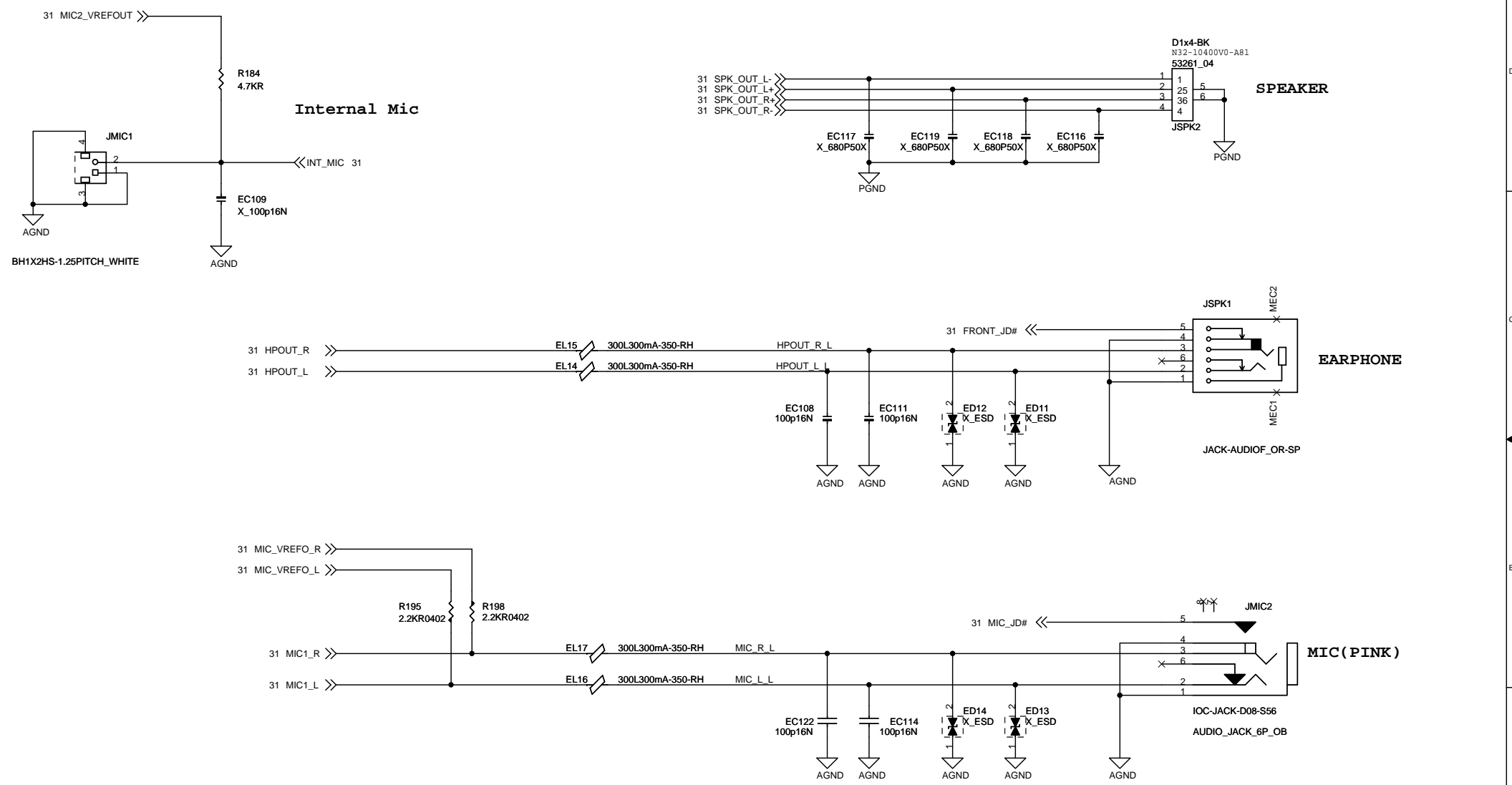
[CheckList] PCIE_RST# and GPIO_RST#-->PCIE device




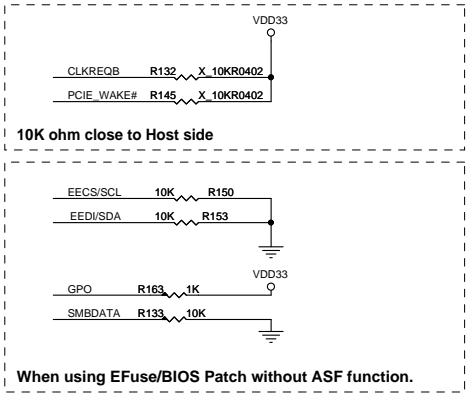
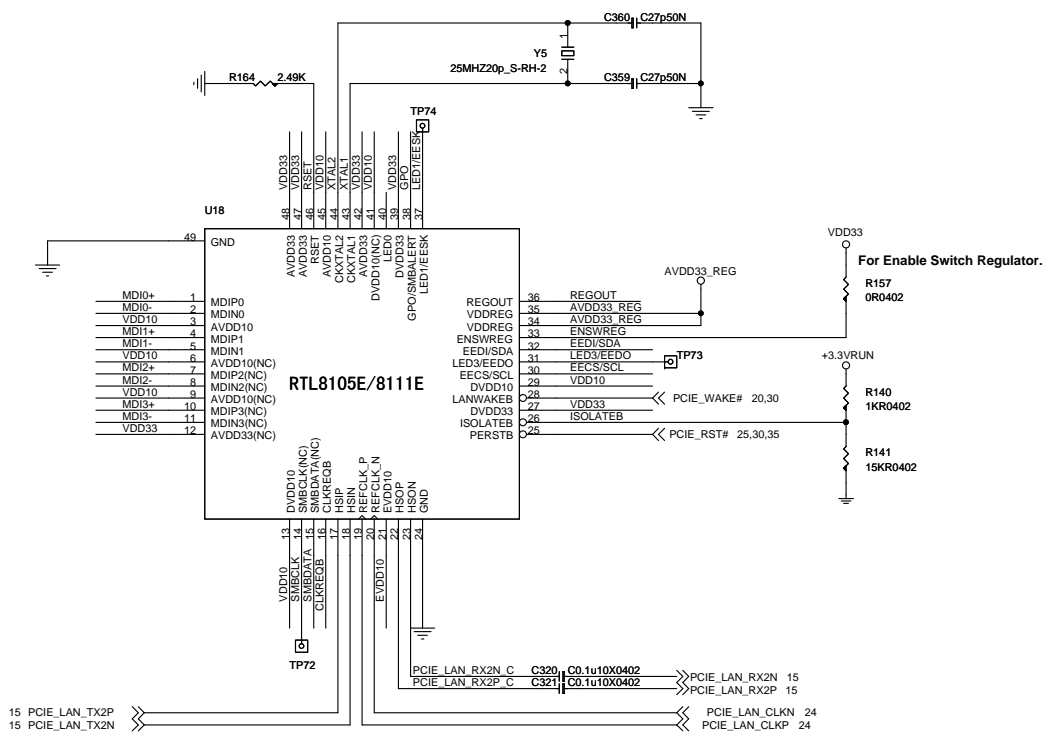
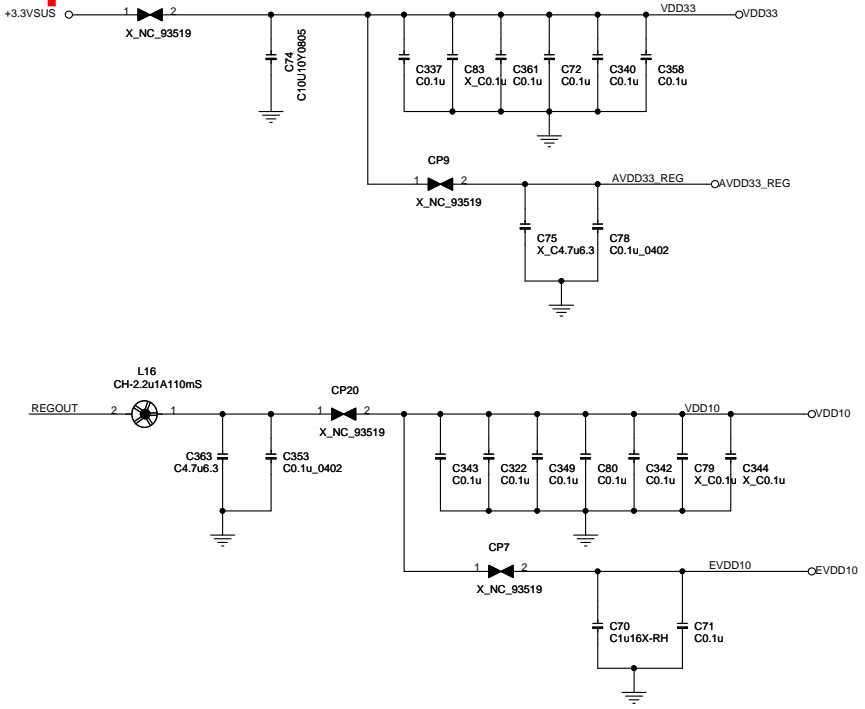
MICRO-STAR INT'L CO.,LTD		
MS-168x		
Size Custom	Document Description HDD/ODD/NEW CARD	Rev 0A
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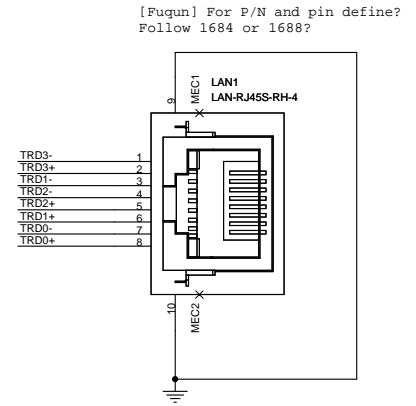
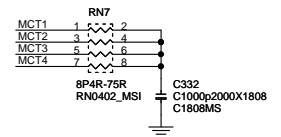
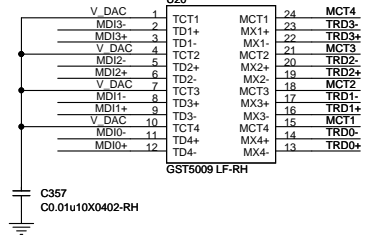
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MS-168x		
Size Custom	Document Description ALC662	Rev 0A
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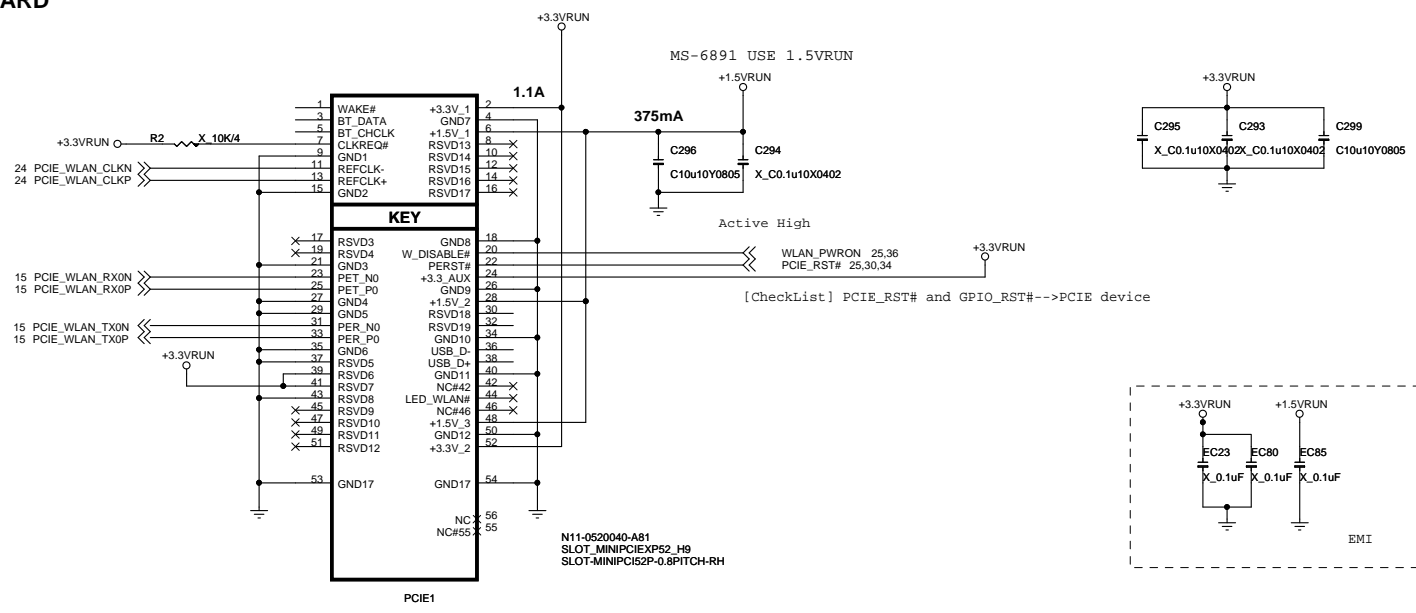
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MS-168x				
Size B	Document Description SPK / HP / MIC			Rev 0A
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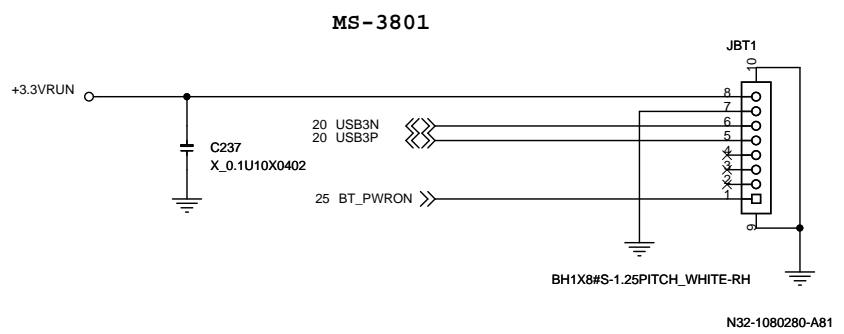
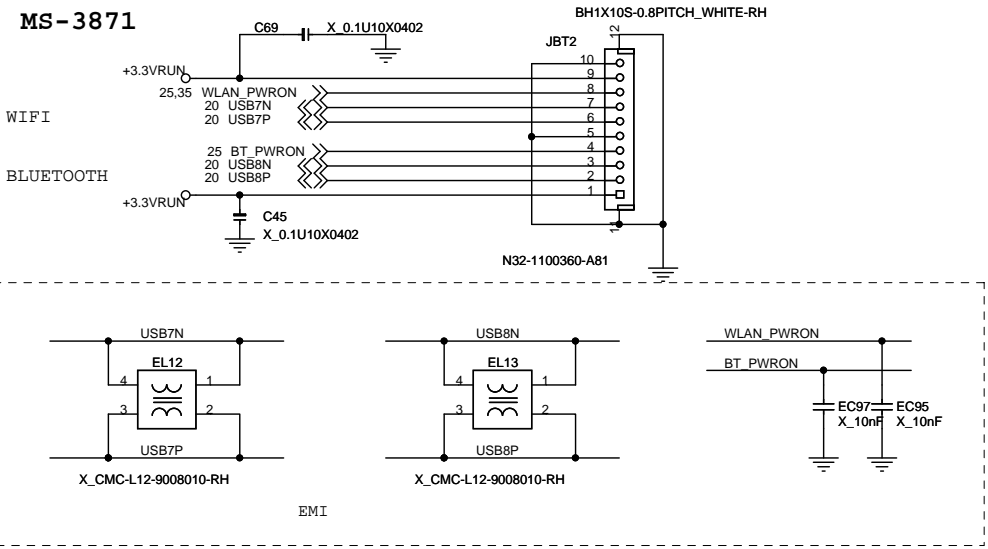
LAN MAGNETICS



[Fuqun] For P/N and pin define? Follow 1684 or 1688?

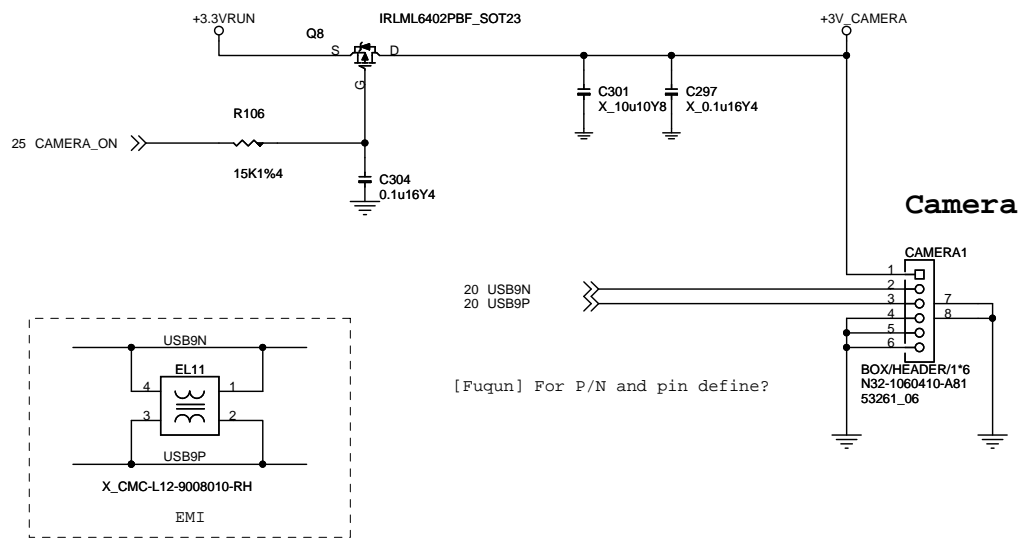


BLUETOOTH

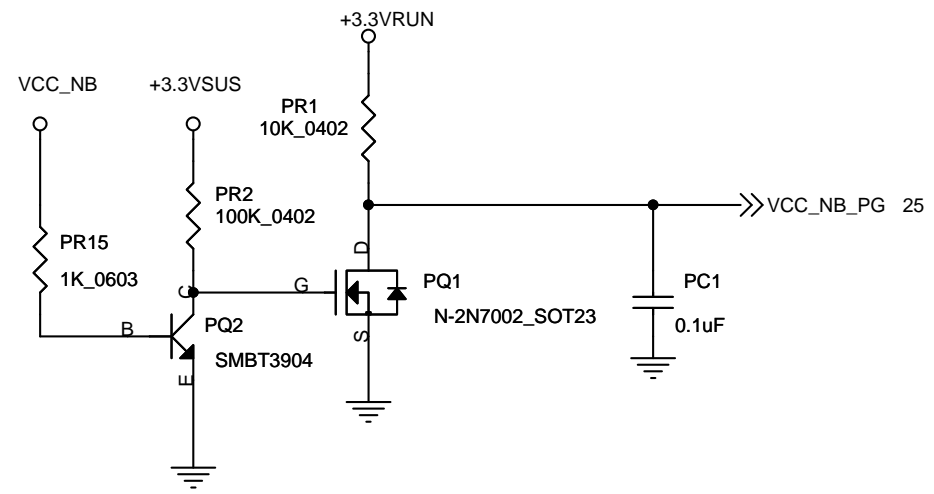


CAMERA

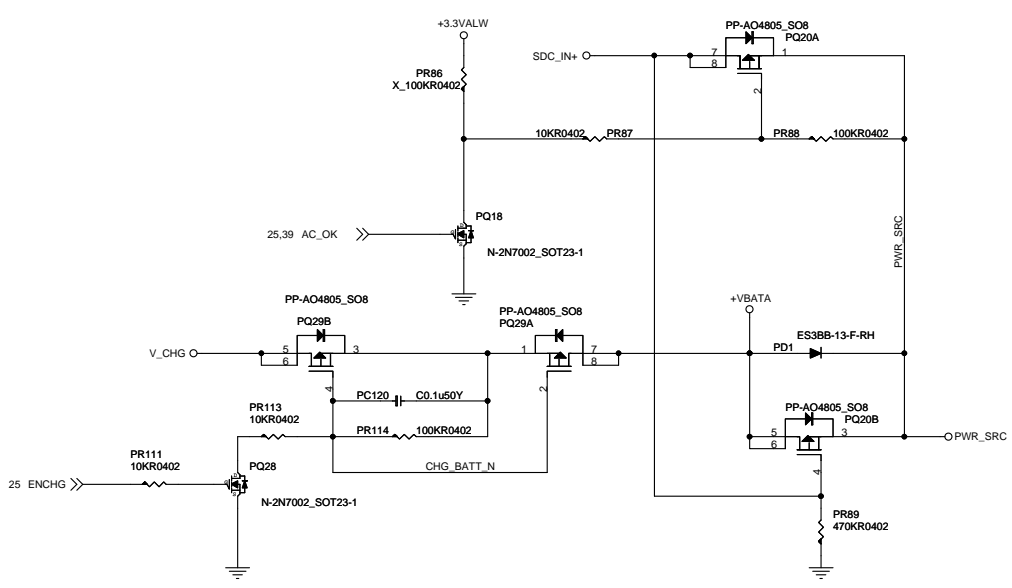
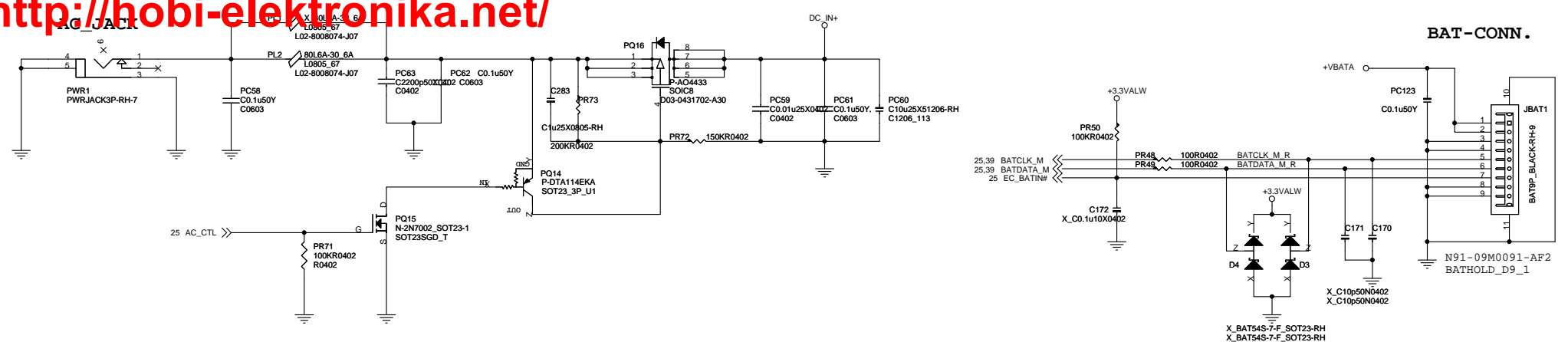
MAX: 130mA



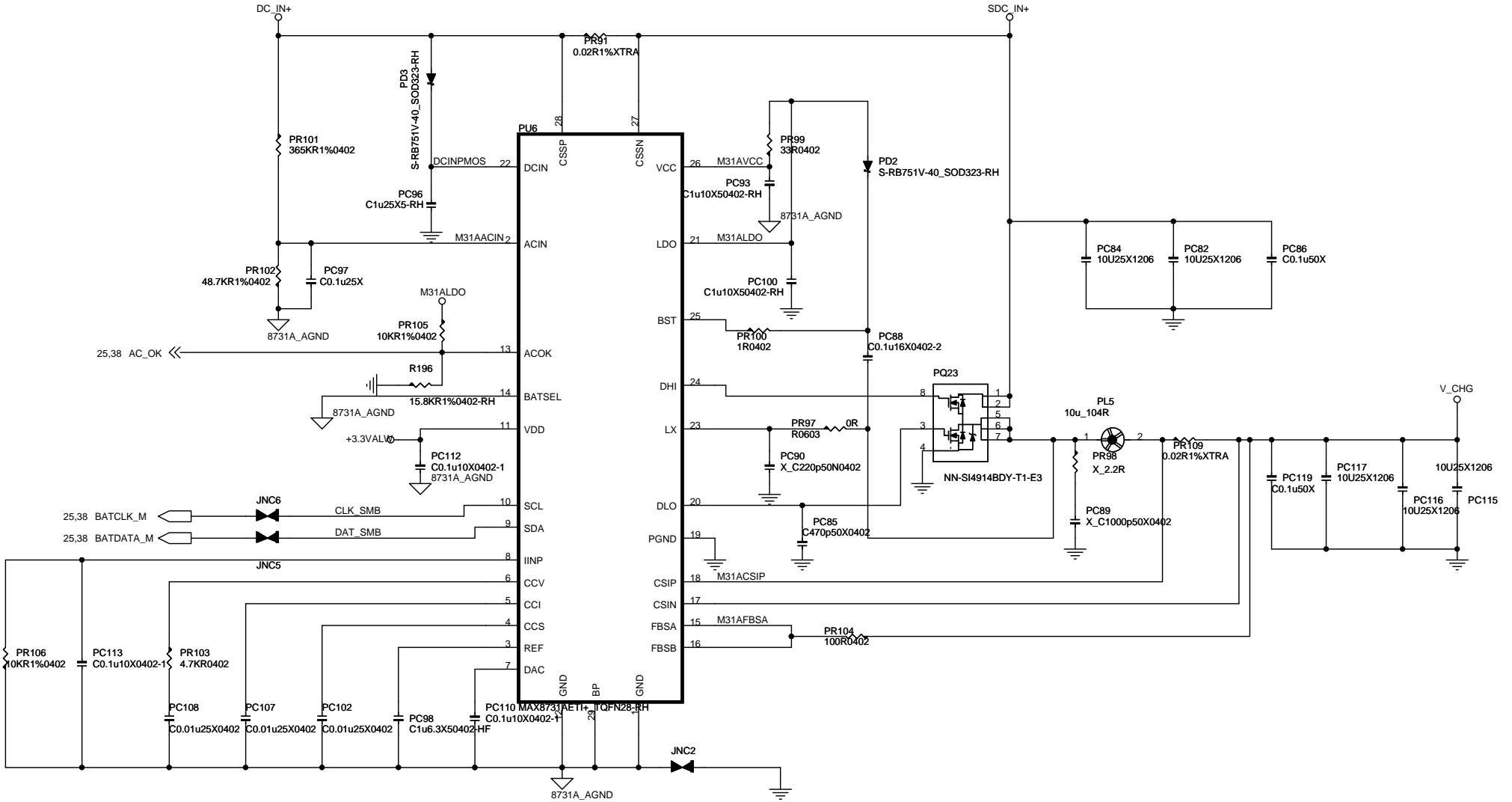
MICRO-STAR INT'L CO.,LTD		
MS-168x		
Size B	Document Description CAMERA/BT	Rev 0A
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MICRO-STAR INT'L CO.,LTD		
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Size A	Document Description POWER LOGIC	Rev 0A
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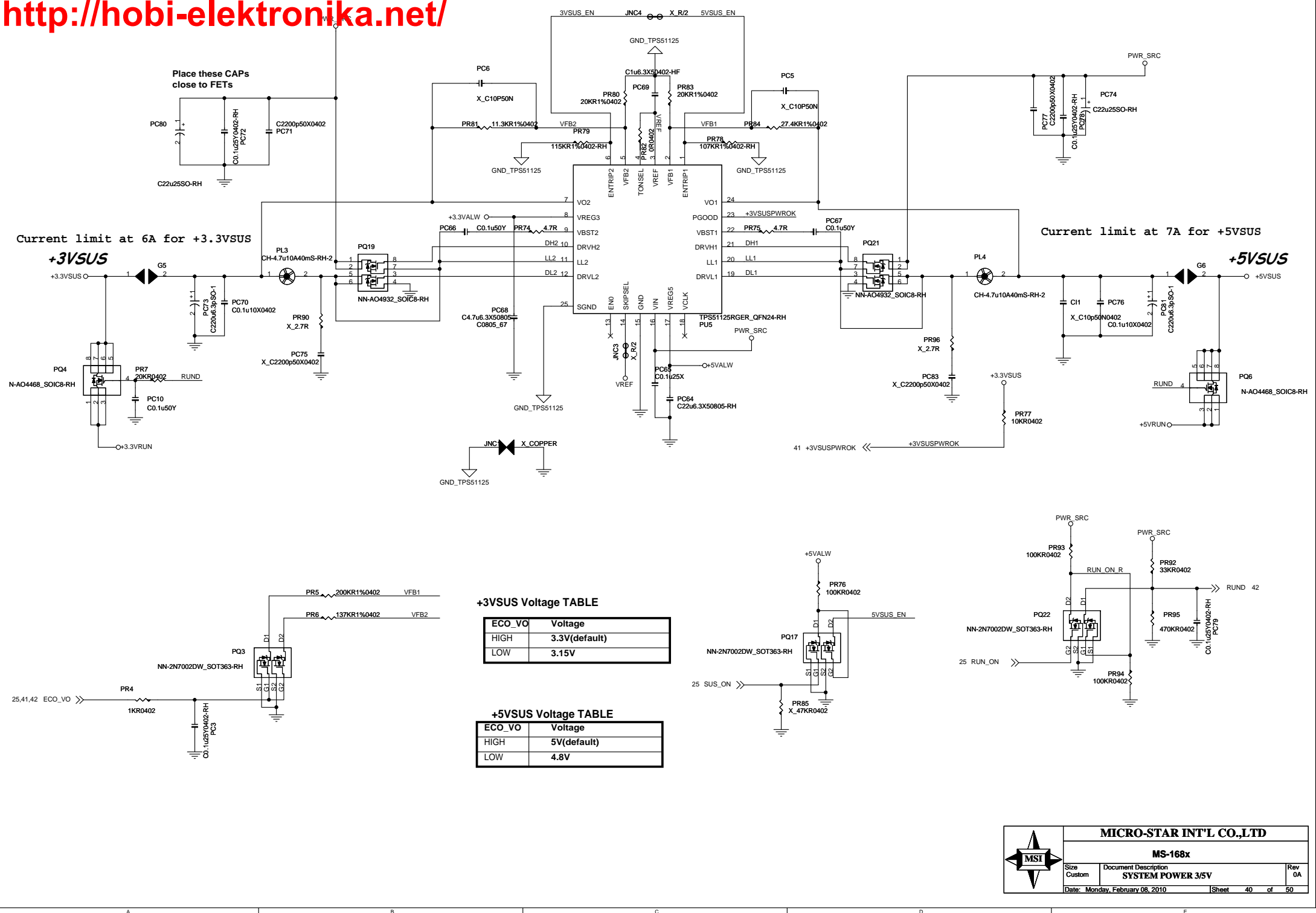


Adapter input voltage set 19 Voltage



IINP :
 1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
 2. $V_{IINP} = IINPUT \times RS1 \times 3mA/V \times PR25$

			MICRO-STAR INT'L CO.,LTD		
			MS-168x		
Size B	Document Description CHARGER				Rev 0A
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Current limit at 6A for +3.3VSUS

Current limit at 7A for +5VSUS

+3VSUS

+5VSUS

+3VSUS Voltage TABLE

ECO_VO	Voltage
HIGH	3.3V(default)
LOW	3.15V

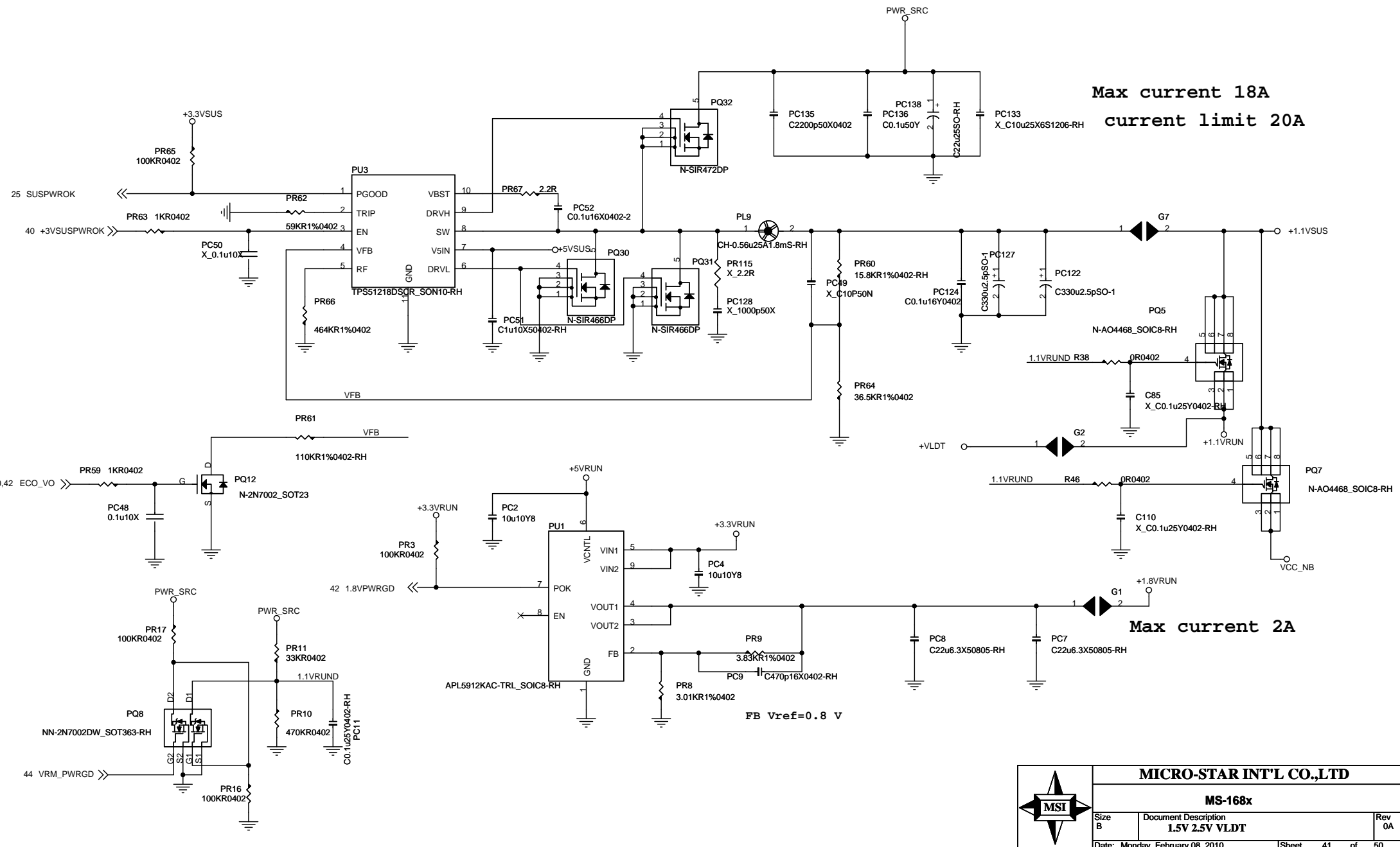
+5VSUS Voltage TABLE

ECO_VO	Voltage
HIGH	5V(default)
LOW	4.8V

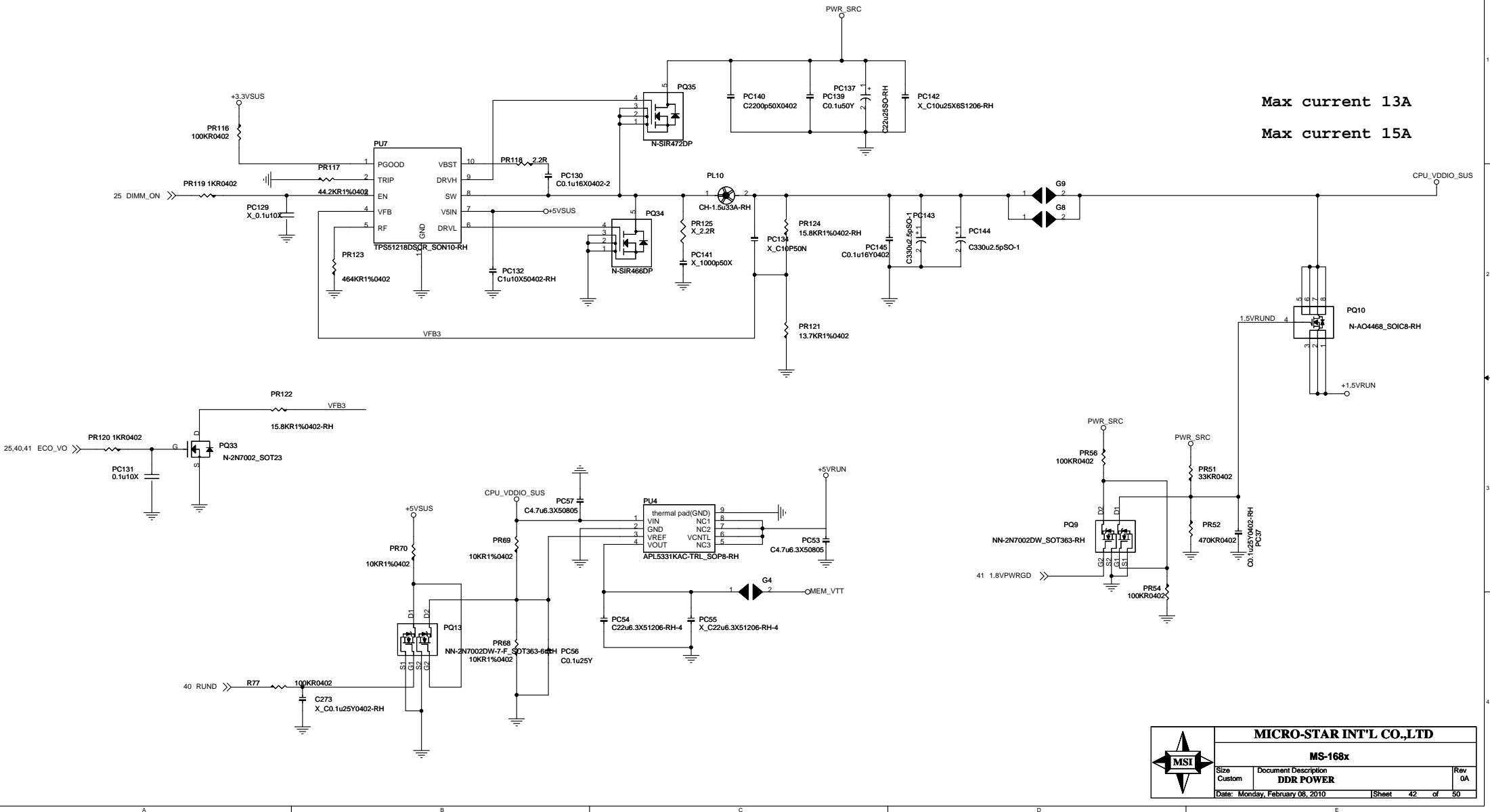
MICRO-STAR INT'L CO.,LTD

MS-168x

Size Custom	Document Description SYSTEM POWER 3/SV	Rev 0A
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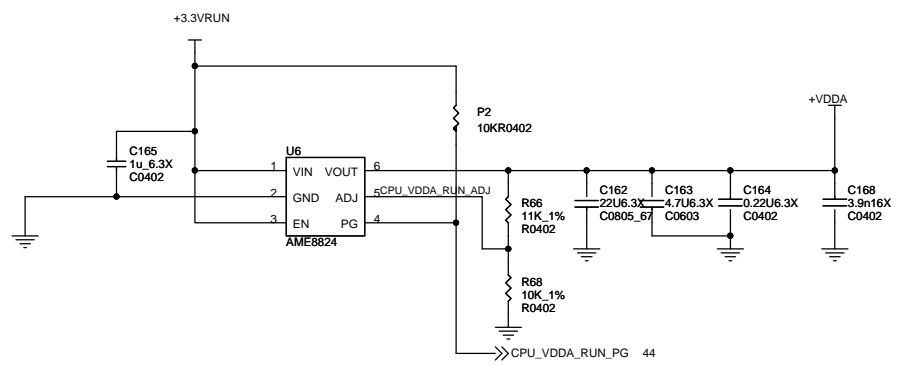
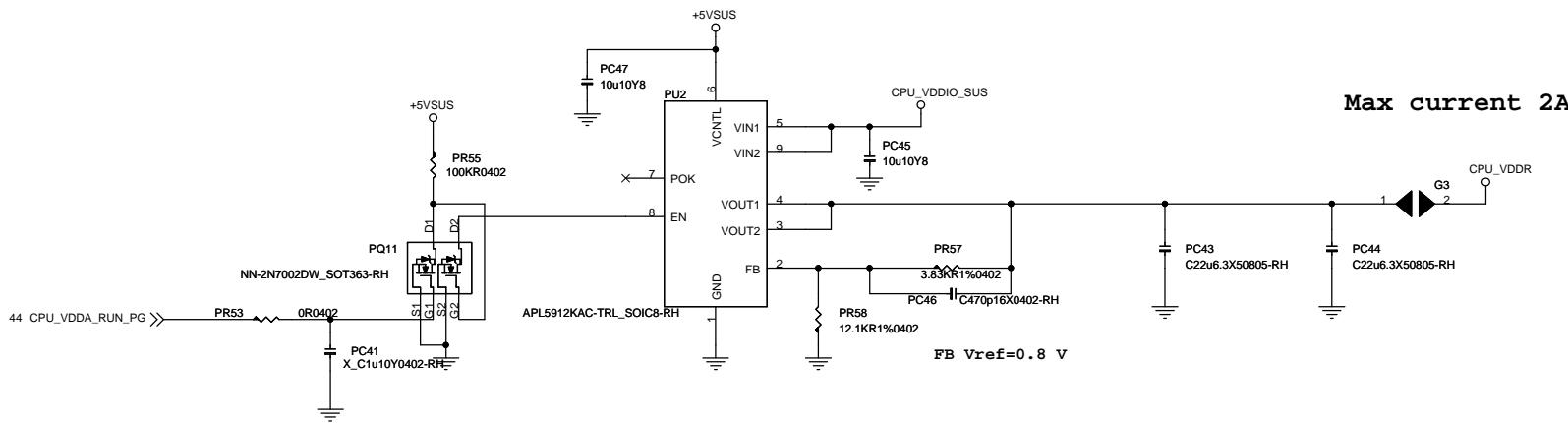



MSI		
MICRO-STAR INT'L CO.,LTD		
MS-168x		
Size B	Document Description	Rev 0A
	1.5V 2.5V VLDT	
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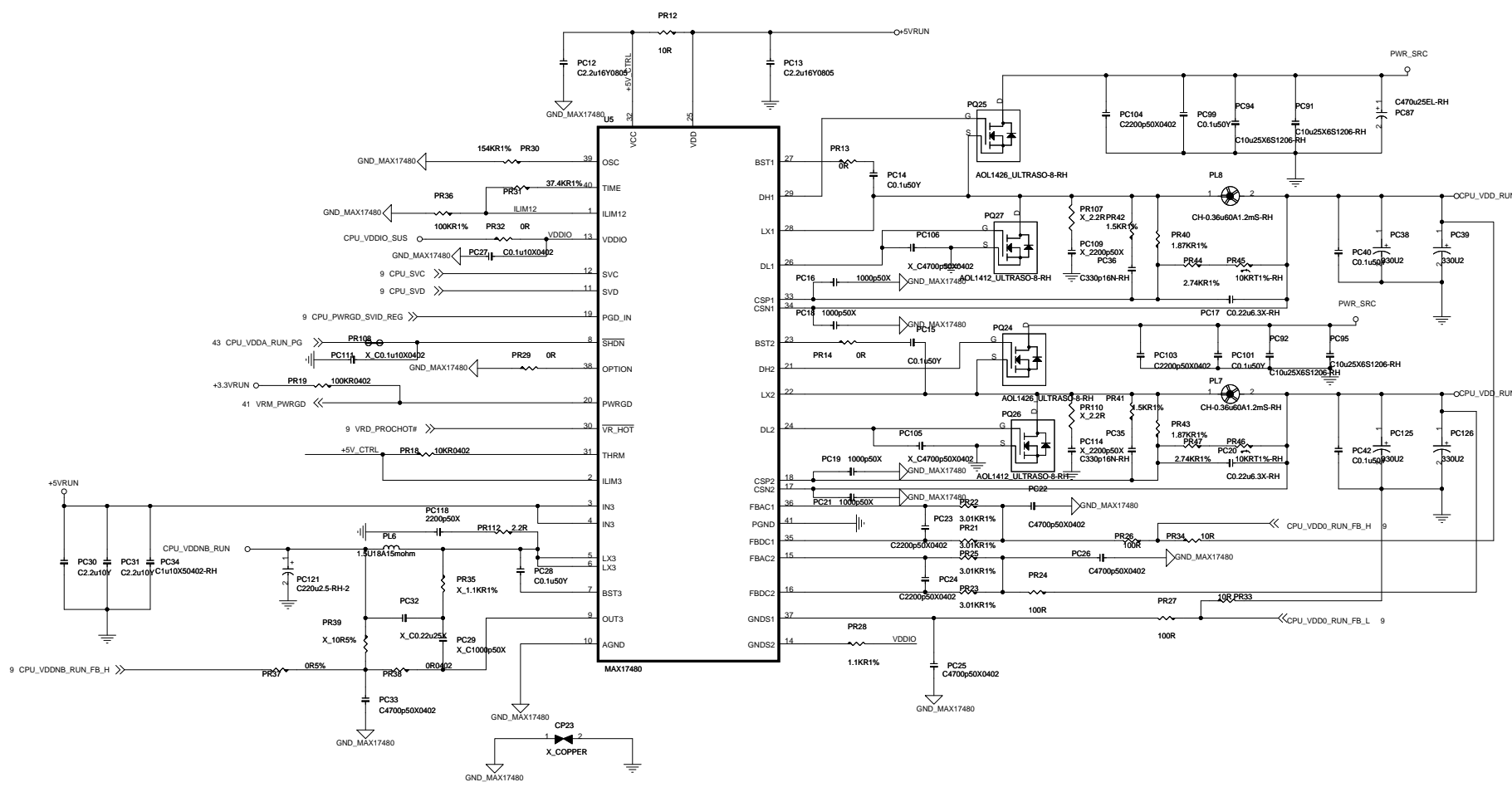


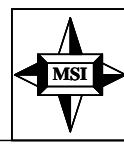
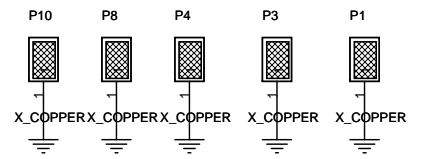
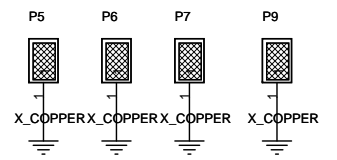
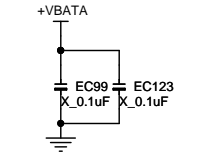
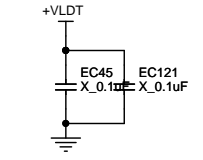
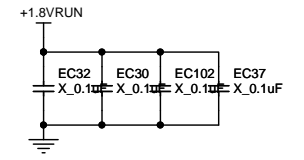
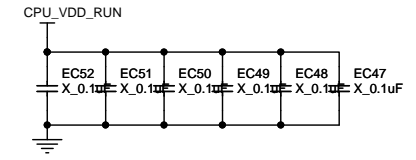
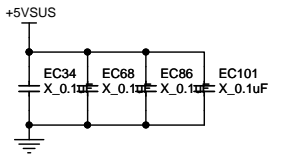
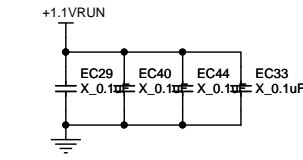
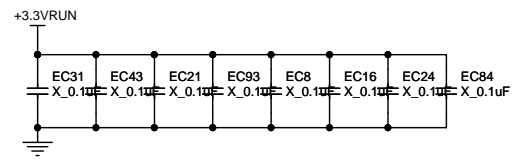
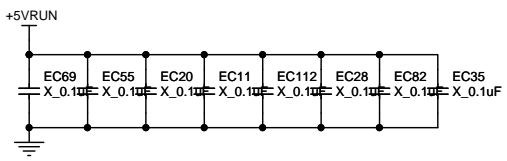
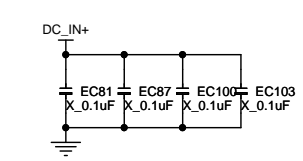
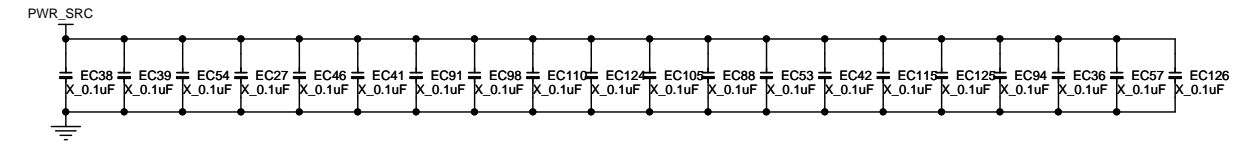
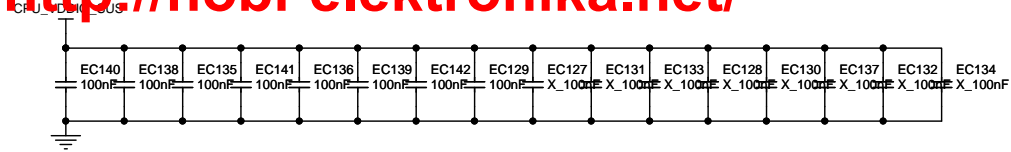
Max current 13A
Max current 15A

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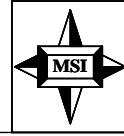
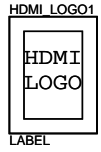
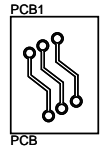
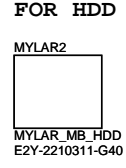
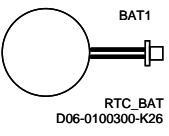
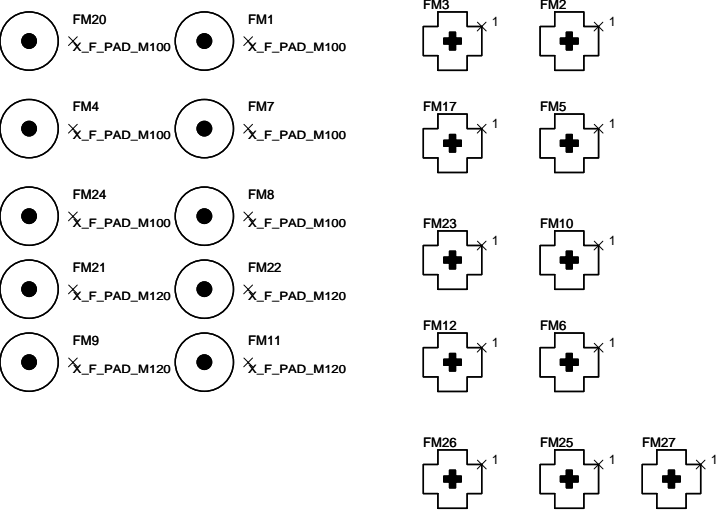
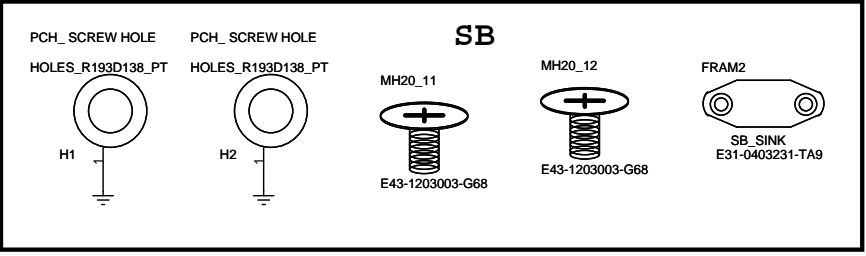
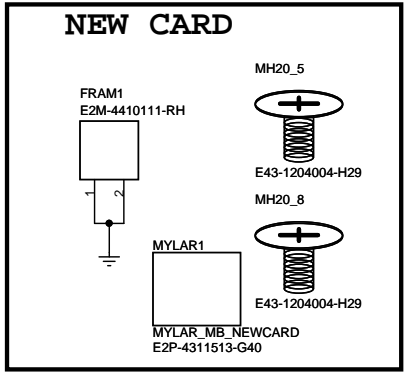
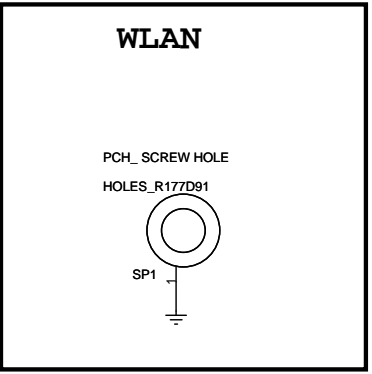
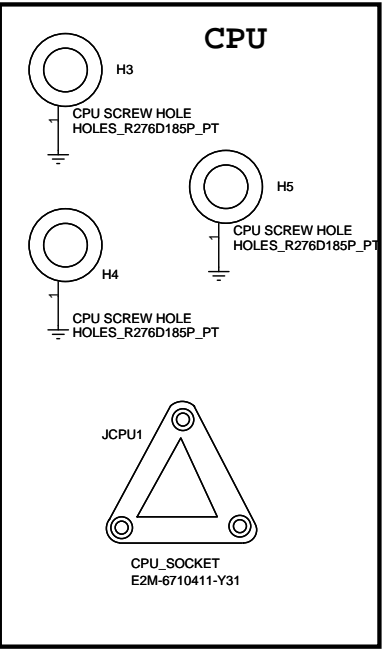
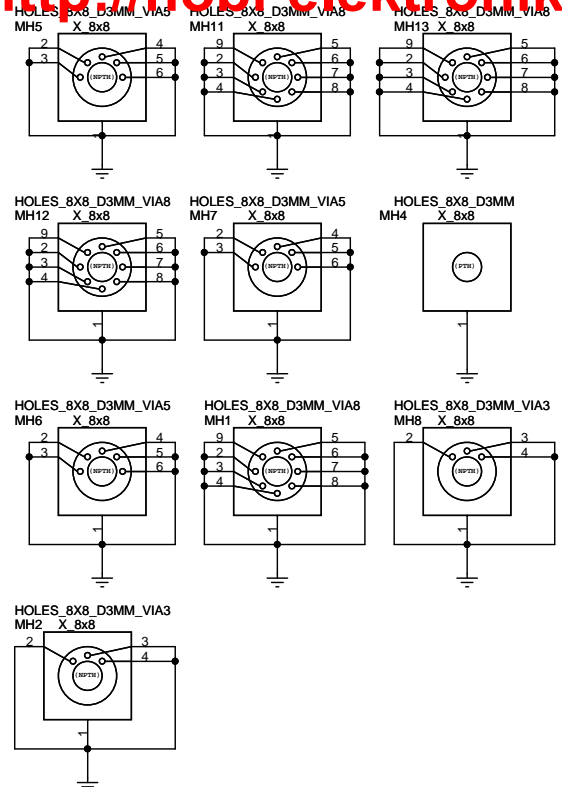


		
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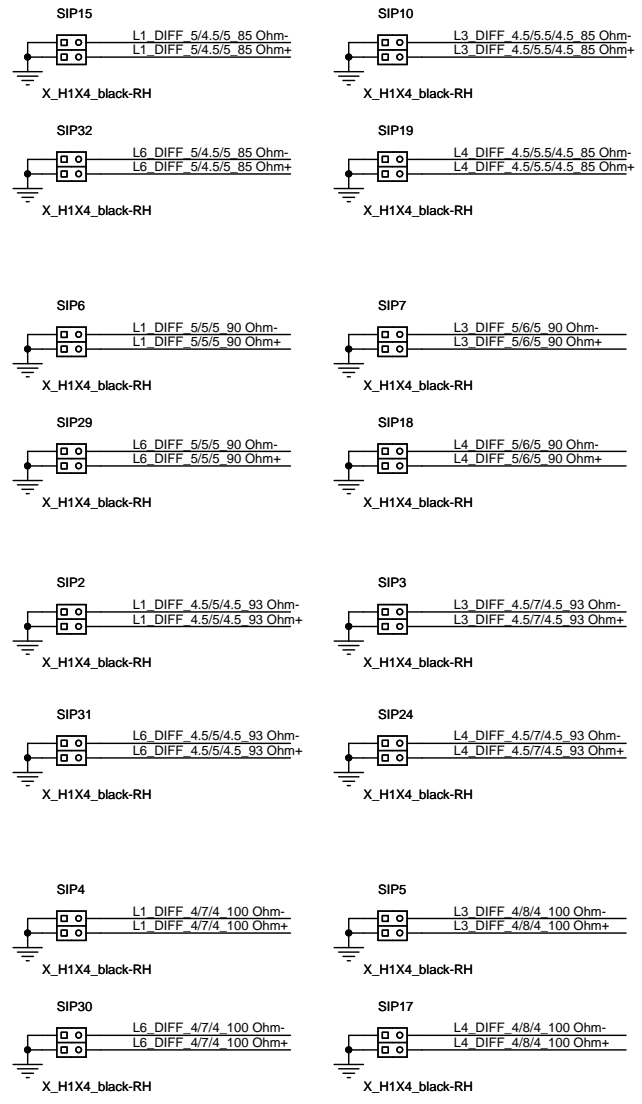
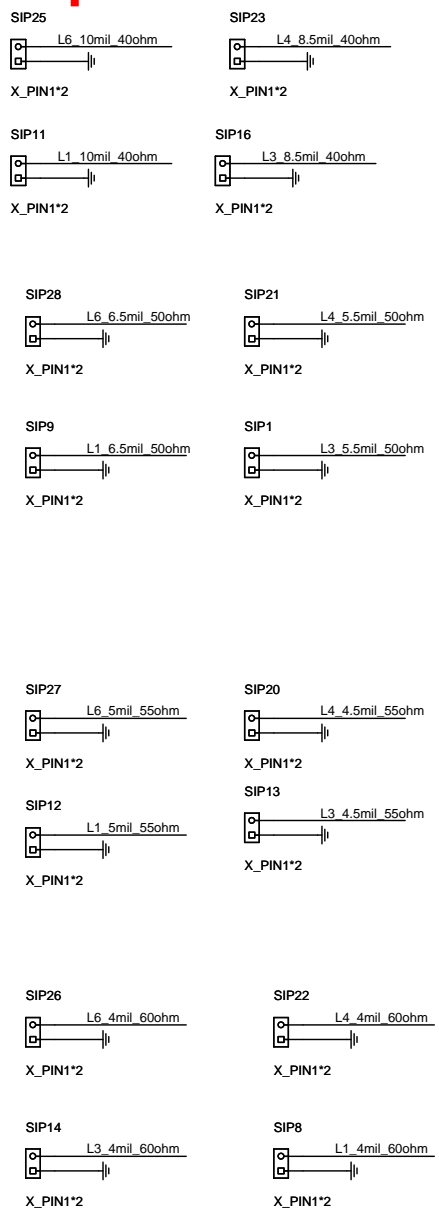



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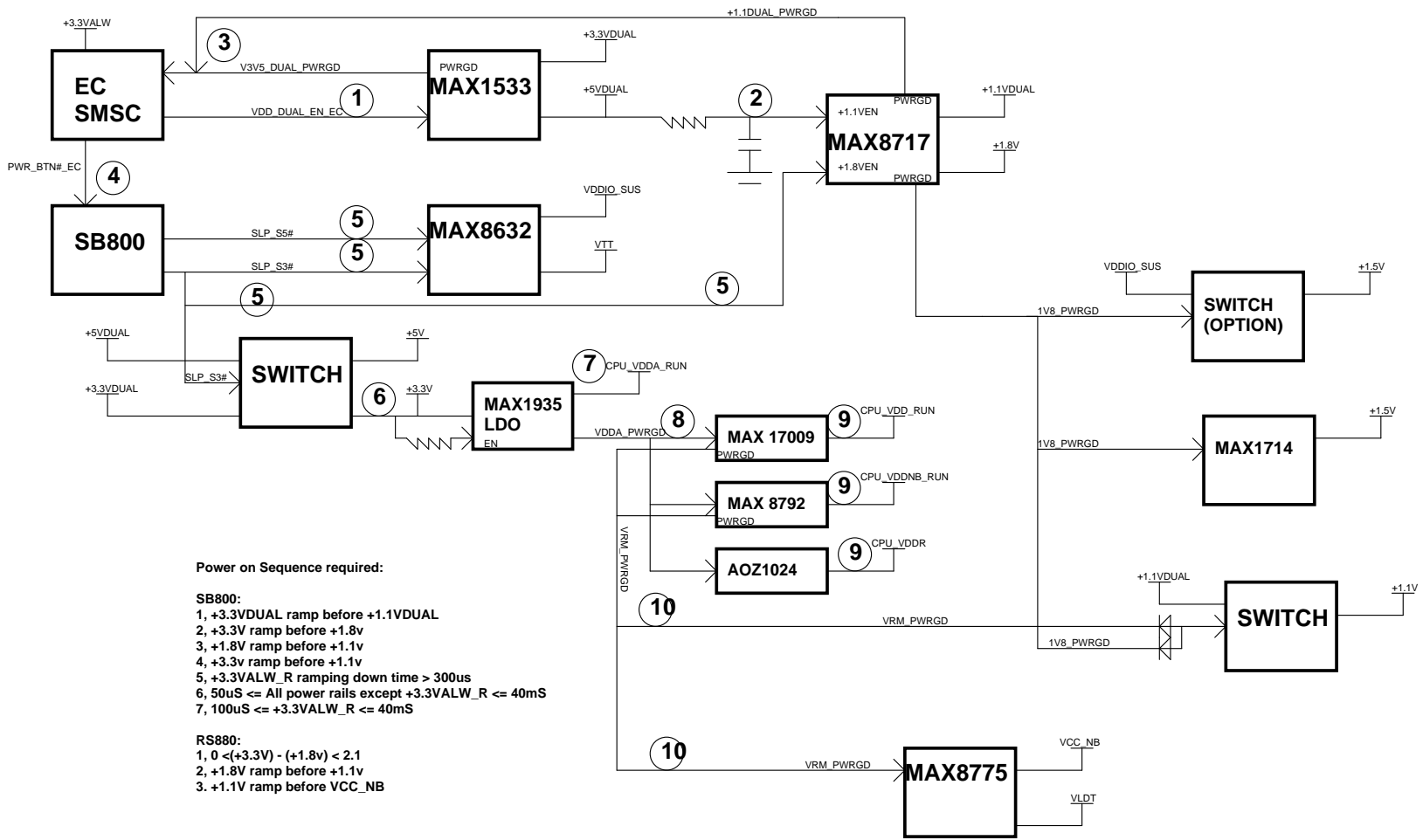


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Differential signal

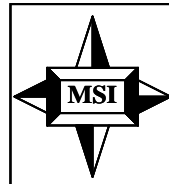
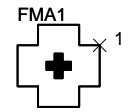
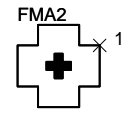
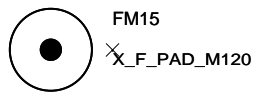
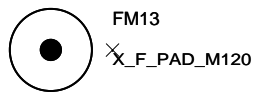
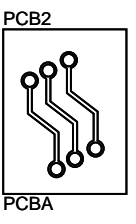
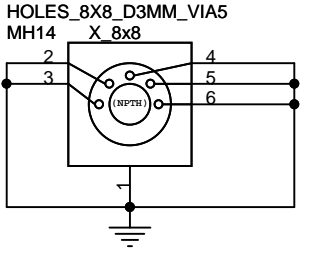
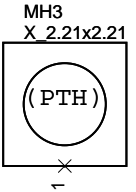
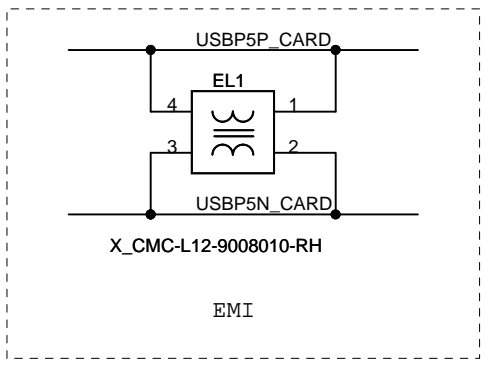
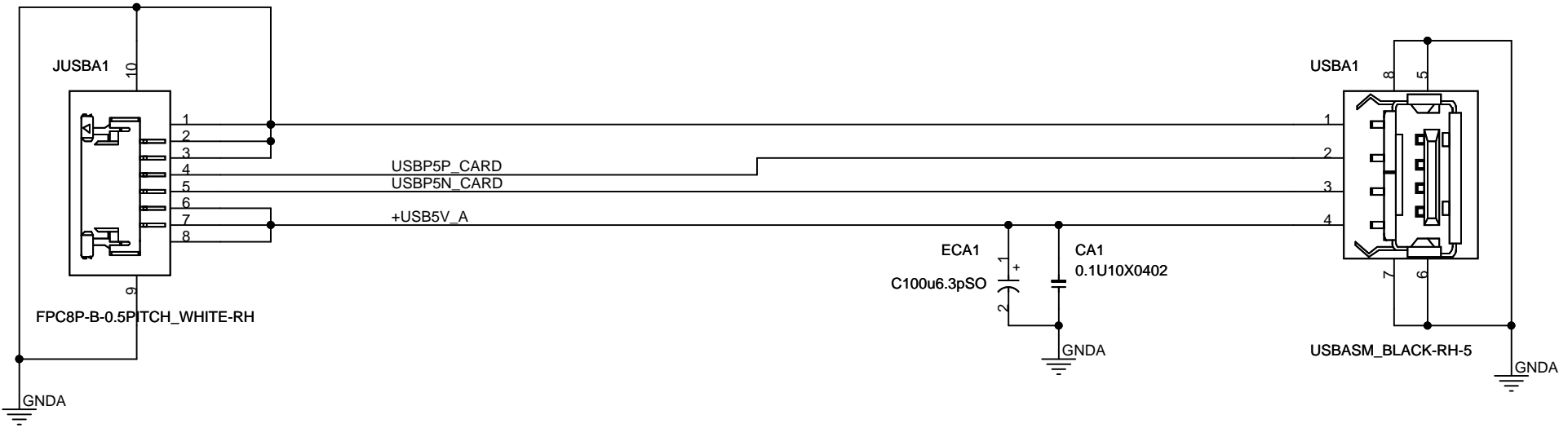


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Power on Sequence required:

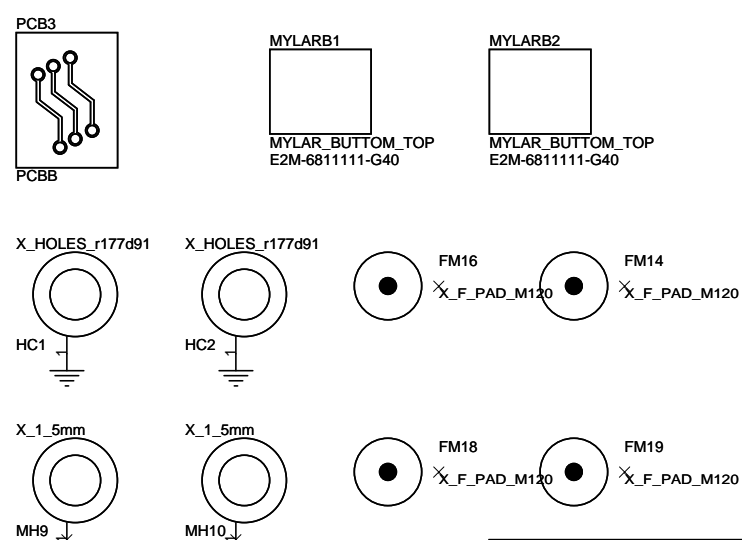
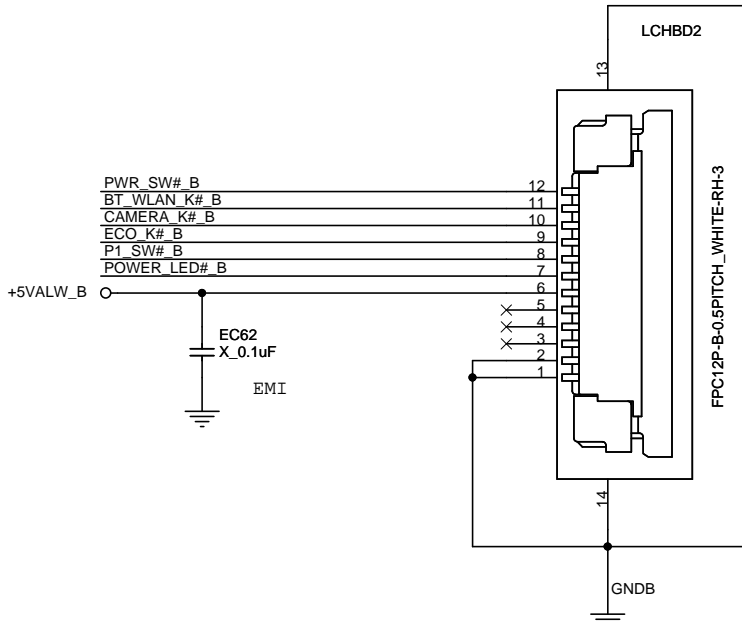
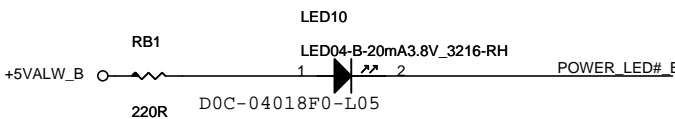
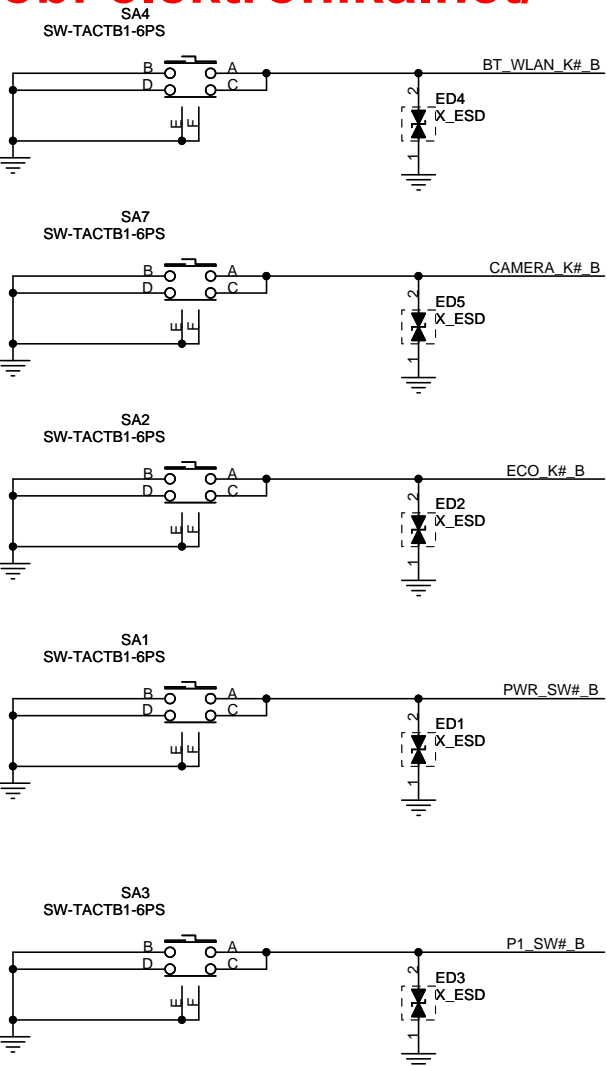
- SB800:**
- 1, +3.3VDUAL ramp before +1.1VDUAL
 - 2, +3.3V ramp before +1.8v
 - 3, +1.8V ramp before +1.1v
 - 4, +3.3v ramp before +1.1v
 - 5, +3.3VALW_R ramping down time > 300us
 - 6, 50uS <= All power rails except +3.3VALW_R <= 40mS
 - 7, 100uS <= +3.3VALW_R <= 40mS
- RS880:**
- 1, 0 < (+3.3V) - (+1.8v) < 2.1
 - 2, +1.8V ramp before +1.1v
 - 3, +1.1V ramp before VCC_NB



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