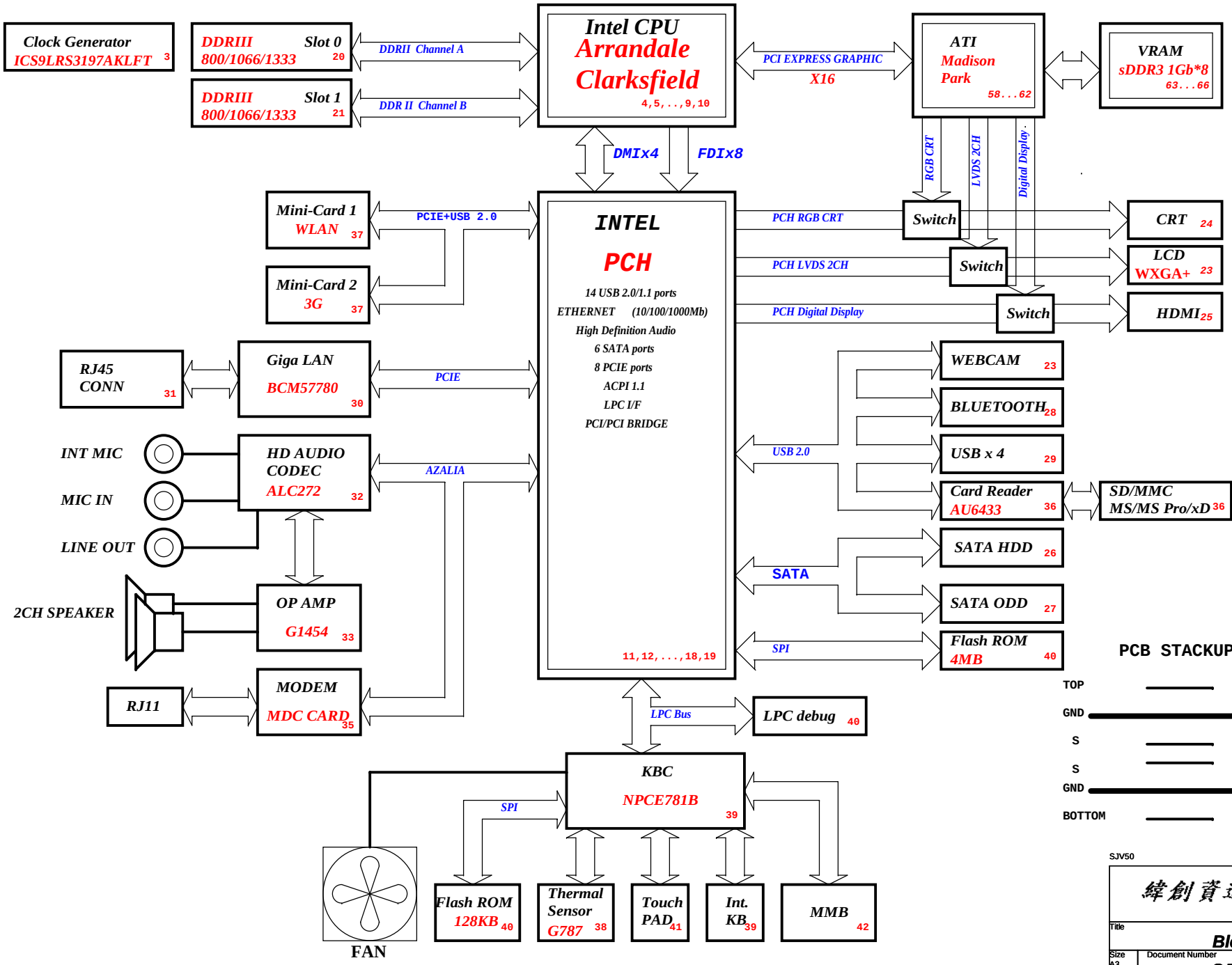
SJV50-CP Block Diagram

Project code: 91.4GH01.001
PCB P/N : 48.4GH01.0SB
REVISION : 09284-SB



PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

CPU DC/DC
ISL62882

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 45,46

SYSTEM DC/DC
TPS51123

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 47

SYSTEM DC/DC
TPS51117

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 48

SYSTEM DC/DC
TPS51117

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 48

SYSTEM DC/DC
TPS51117

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 49

RT9025

INPUTS	OUTPUTS
3D3V_S0	1D8V_S0 50

G2997

INPUTS	OUTPUTS
1D5V_S3	0D75_S0 50

SYSTEM DC/DC
ISL62881

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 52

SYSTEM DC/DC
TPS51117

INPUTS	OUTPUTS
DCBATOUT	+VGA_CORE 53

CHARGER
ISL88731A

INPUTS	OUTPUTS
DCBATOUT	BT+ 51

SJV50

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	LAN
LANE2	MiniCard WLAN

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel (X)
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print (X)
11	Blue Tooth
12	MINIC2
13	Cardreader

SJV50

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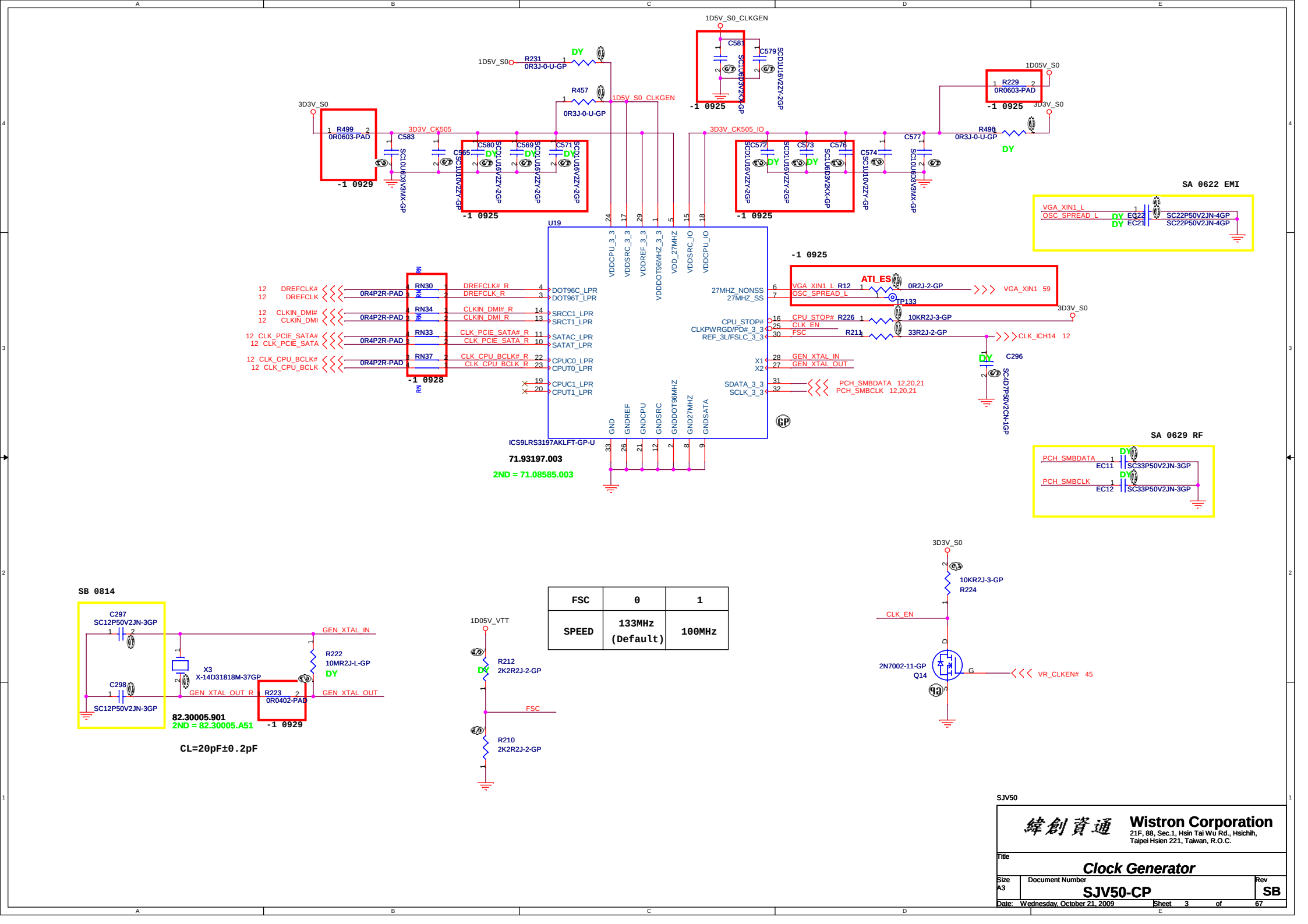
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1D5V_S0
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0R3J-0-U-GP
DY
R457
0R3J-0-U-GP
3D3V_S0
R499
0R0603-PAD
-1 0929
3D3V_CK505
C583
C565
C580
C569
C571
-1 0925
3D3V_CK505_IO
C572
C573
C576
C577
C574
C581
C579
R229
0R0603-PAD
R496
0R3J-0-U-GP
SA 0622 EMI
VGA_XIN1_L
OSC_SPREAD_L
EC22
EC21
SC22P50V2JN-4GP
U19
ICS9LRS3197AKLFT-GP-U
71.93197.003
2ND = 71.08585.003
ATI_ES
0R2J-2-GP
VGA_XIN1 59
TP133
CPU_STOP# R226
10KR2J-3-GP
CLK_EN
FSC R211
33R2J-2-GP
CLK_ICH14 12
C296
SC4D7P50V2CN-1GP
GEN_XTAL_IN
GEN_XTAL_OUT
PCH_SMBDATA 12,20,21
PCH_SMBCLK 12,20,21
SA 0629 RF
EC11
EC12
SC33P50V2JN-3GP
RN30
RN34
RN33
RN37
0R4P2R-PAD
-1 0928
DREFCLK#
DREFCLK
CLKIN_DMI#
CLKIN_DMI
CLK_PCIE_SATA#
CLK_PCIE_SATA
CLK_CPU_BCLK#
CLK_CPU_BCLK
SB 0814
C297
C298
SC12P50V2JN-3GP
X3
X-14D31818M-37GP
R222
10MR2J-L-GP
R223
0R0402-PAD
82.30005.901
2ND = 82.30005.A51
CL=20pF±0.2pF
1D05V_VTT
R212
2K2R2J-2-GP
R210
2K2R2J-2-GP
FSC
FSC 0 1
SPEED 133MHz (Default) 100MHz
10KR2J-3-GP
R224
2N7002-11-GP
Q14
VR_CLKEN# 45
SJV50
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Clock Generator
Size A3
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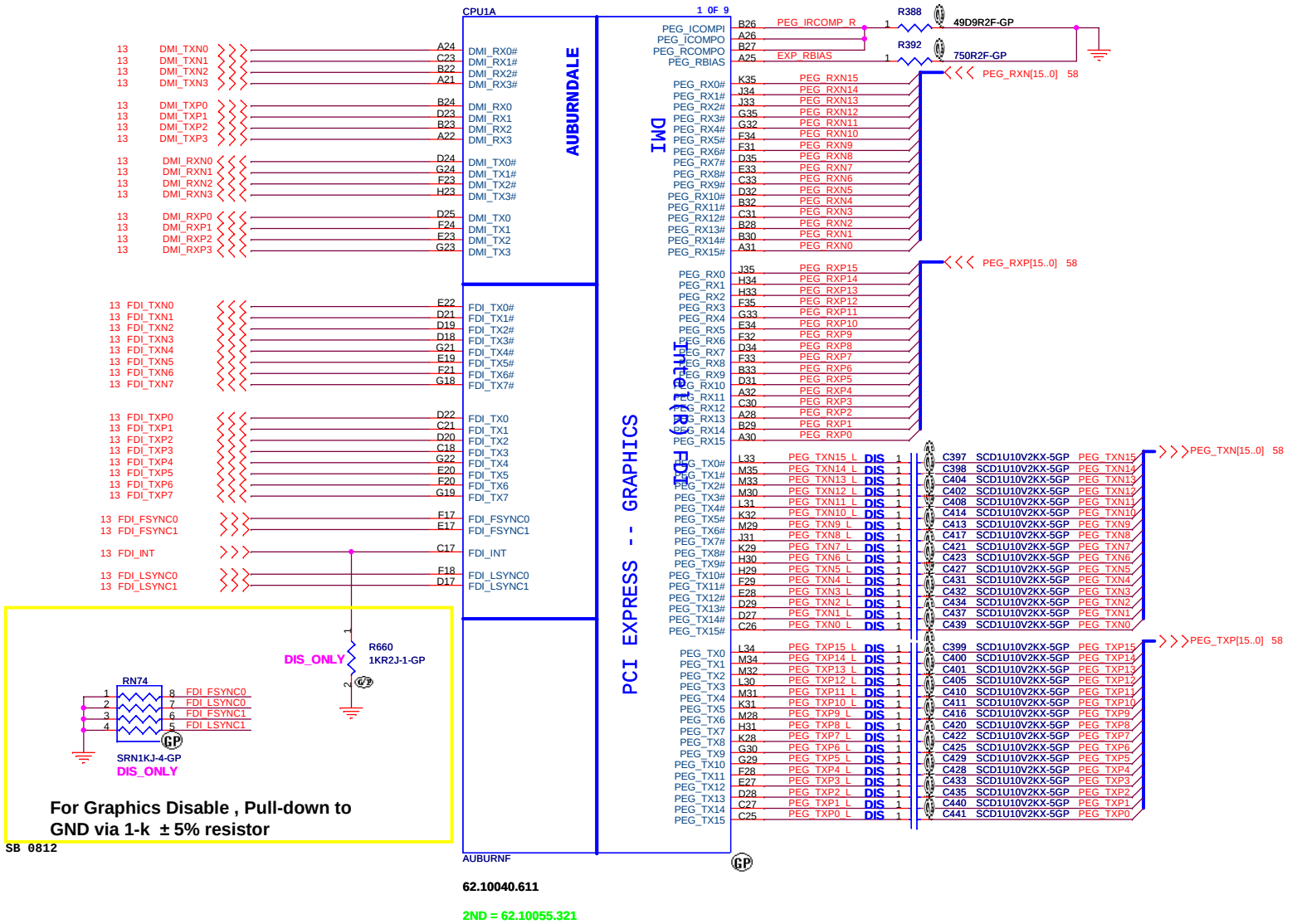

SJV50

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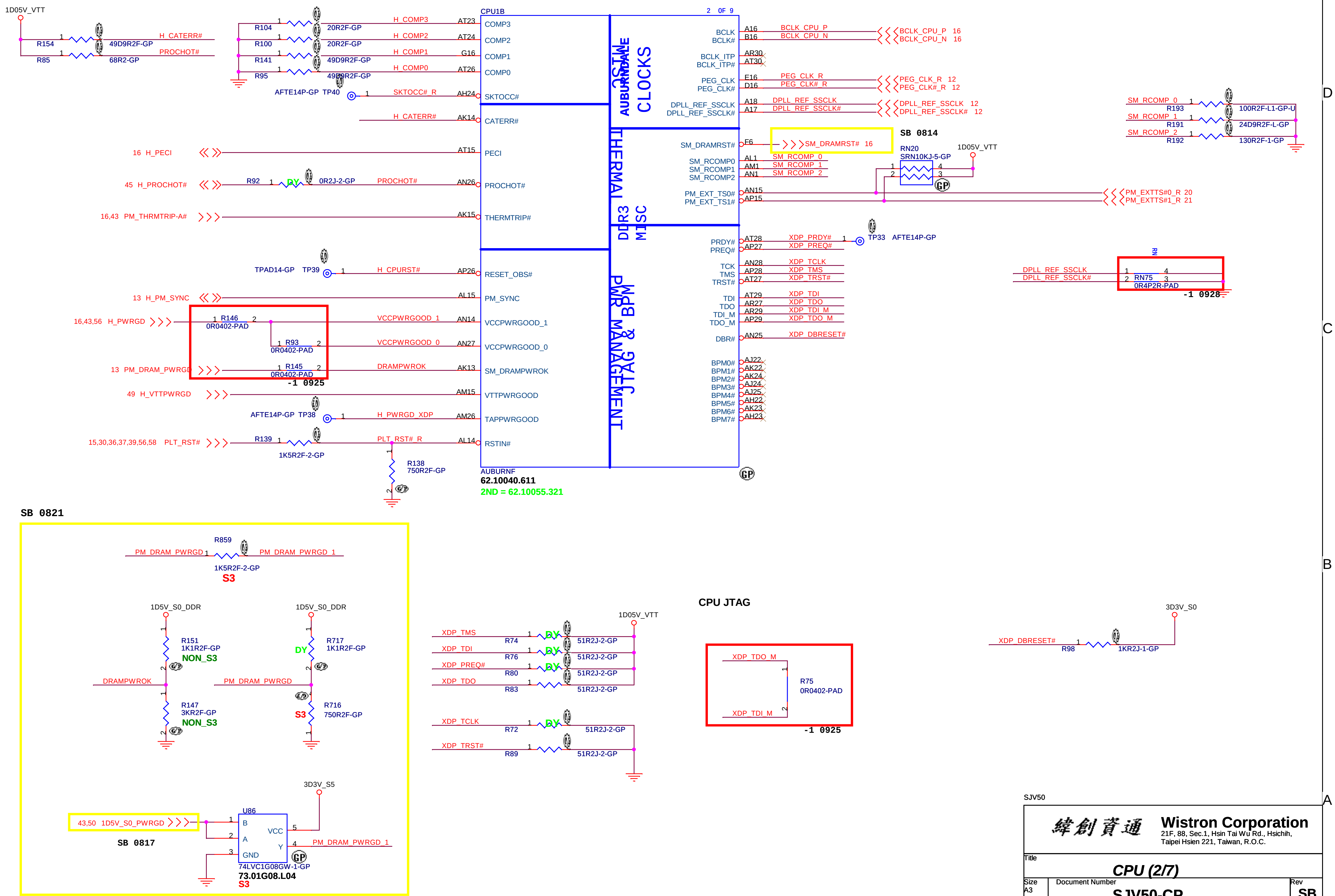

CPU1B
2 OF 9
COMP3
COMP2
COMP1
COMP0
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
RESET_OBS#
PM_SYNC
VCCPWRGOOD_1
VCCPWRGOOD_0
SM_DRAMPWROK
VTTPWRGOOD
TAPPWRGOOD
RSTIN#
MISC
THERMAL
PWR MANAGEMENT
CLOCKS
DDR3 MISC
JTAG & BPM
BCLK
BCLK#
BCLK_ITP
BCLK_ITP#
PEG_CLK
PEG_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PM_EXT_TS0#
PM_EXT_TS1#
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
TDI_M
TDO_M
DBR#
BPM0#
BPM1#
BPM2#
BPM3#
BPM4#
BPM5#
BPM6#
BPM7#
AUBURNF
62.10040.611
2ND = 62.10055.321
1D05V_VTT
R154 49D9R2F-GP H_CATERR#
R85 68R2-GP PROCHOT#
R104 20R2F-GP H_COMP3 AT23
R100 20R2F-GP H_COMP2 AT24
R141 49D9R2F-GP H_COMP1 G16
R95 49D9R2F-GP H_COMP0 AT26
AFTE14P-GP TP40 SKTOCC#_R AH24
H_CATERR# AK14
16 H_PECI AT15
45 H_PROCHOT# R92 DY 0R2J-2-GP PROCHOT# AN26
16,43 PM_THRMTRIP-A# AK15
TPAD14-GP TP39 H_CPURST# AP26
13 H_PM_SYNC AL15
16,43,56 H_PWRGD R146 0R0402-PAD VCCPWRGOOD_1 AN14
R93 0R0402-PAD VCCPWRGOOD_0 AN27
13 PM_DRAM_PWRGD R145 0R0402-PAD DRAMPWROK AK13
-1 0925
49 H_VTTPWRGD AM15
AFTE14P-GP TP38 H_PWRGD_XDP AM26
15,30,36,37,39,56,58 PLT_RST# R139 1K5R2F-2-GP PLT_RST#_R AL14
R138 750R2F-GP
A16 BCLK_CPU_P BCLK_CPU_P 16
B16 BCLK_CPU_N BCLK_CPU_N 16
AR30
AT30
E16 PEG_CLK_R PEG_CLK_R 12
D16 PEG_CLK#_R PEG_CLK#_R 12
A18 DPLL_REF_SSCLK DPLL_REF_SSCLK 12
A17 DPLL_REF_SSCLK# DPLL_REF_SSCLK# 12
F6 SM_DRAMRST# 16
SB 0814
AL1 SM_RCOMP_0
AM1 SM_RCOMP_1
AN1 SM_RCOMP_2
RN20 SRN10KJ-5-GP
1D05V_VTT
AN15 PM_EXTTS#0_R 20
AP15 PM_EXTTS#1_R 21
AT28 XDP_PRDY# TP33 AFTE14P-GP
AP27 XDP_PREQ#
AN28 XDP_TCLK
AP28 XDP_TMS
AT27 XDP_TRST#
AT29 XDP_TDI
AR27 XDP_TDO
AR29 XDP_TDI_M
AP29 XDP_TDO_M
AN25 XDP_DBRESET#
AJ22 AK22 AK24 AJ24 AJ25 AH22 AK23 AH23
SM_RCOMP_0 R193 100R2F-L1-GP-U
SM_RCOMP_1 R191 24D9R2F-L-GP
SM_RCOMP_2 R192 130R2F-1-GP
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
RN75 0R4P2R-PAD
-1 0928
SB 0821
R859 PM_DRAM_PWRGD PM_DRAM_PWRGD_1 1K5R2F-2-GP S3
1D5V_S0_DDR
R151 1K1R2F-GP NON_S3
DRAMPWROK
R147 3KR2F-GP NON_S3
1D5V_S0_DDR
DY R717 1K1R2F-GP
PM_DRAM_PWRGD
S3 R716 750R2F-GP
3D3V_S5
U86
43,50 1D5V_S0_PWRGD
SB 0817
B A GND VCC Y
PM_DRAM_PWRGD_1
74LVC1G08GW-1-GP
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S3
CPU JTAG
1D05V_VTT
XDP_TMS R74 DY 51R2J-2-GP
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XDP_TDO_M
R75 0R0402-PAD
XDP_TDI_M
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3D3V_S0
XDP_DBRESET# R98 1KR2J-1-GP

SJV50

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Title: **CPU (2/7)**

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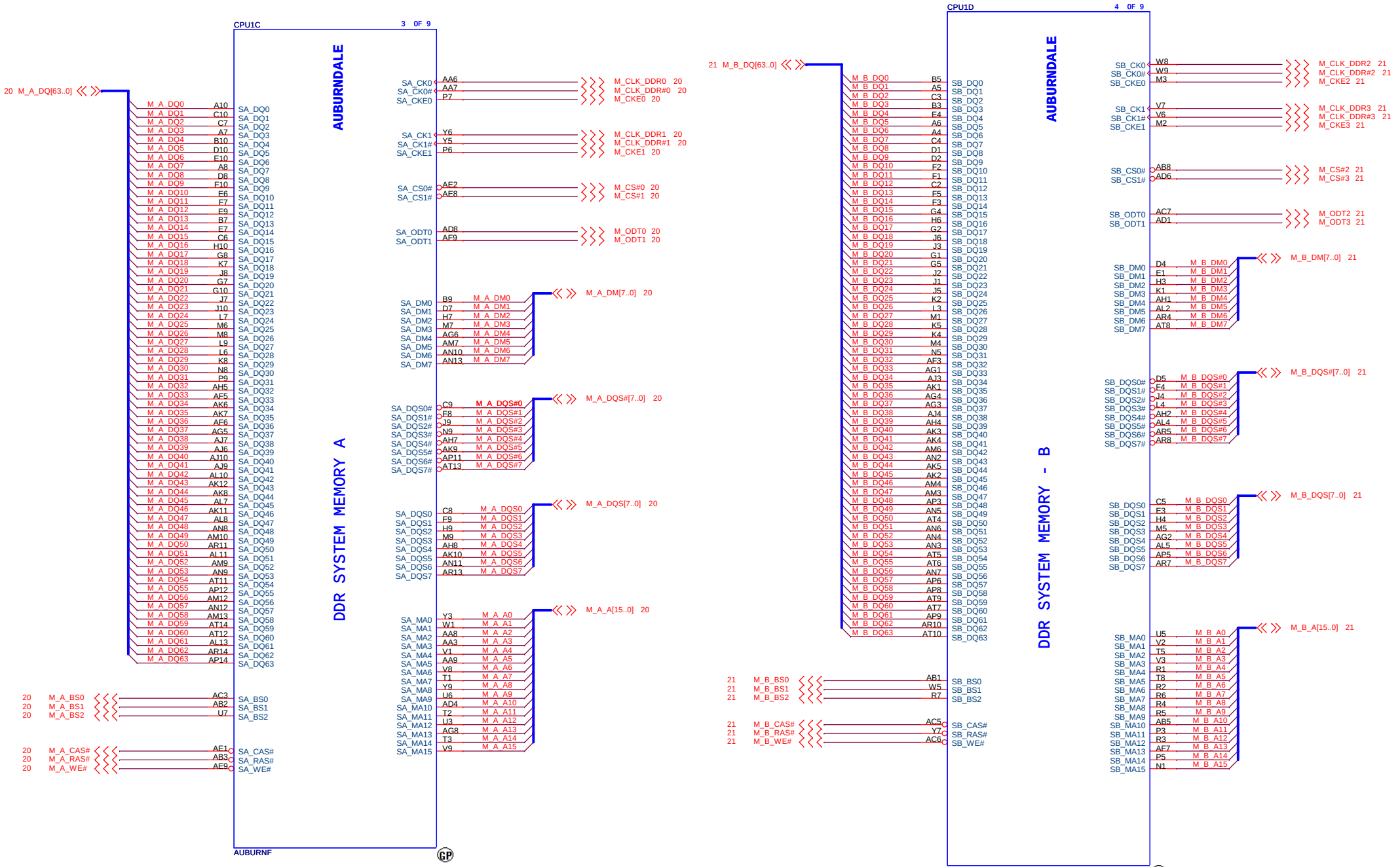
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DDR SYSTEM MEMORY A
AUBURNF
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M_A_DQ2 C7
M_A_DQ3 A7
M_A_DQ4 B10
M_A_DQ5 D10
M_A_DQ6 E10
M_A_DQ7 A8
M_A_DQ8 D8
M_A_DQ9 F10
M_A_DQ10 E6
M_A_DQ11 F7
M_A_DQ12 E9
M_A_DQ13 B7
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20 M_A_BS2
AC3 AB2 U7
SA_BS0 SA_BS1 SA_BS2
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20 M_A_RAS#
20 M_A_WE#
AE1 AB3 AE9
SA_CAS# SA_RAS# SA_WE#
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SA_CK0# AA7
SA_CKE0 P7
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M_CLK_DDR#0 20
M_CKE0 20
SA_CK1 Y6
SA_CK1# Y5
SA_CKE1 P6
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SA_CS1# AE8
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SA_ODT1 AF9
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SA_DQS3# N9 M_A_DQS#3
SA_DQS4# AH7 M_A_DQS#4
SA_DQS5# AK9 M_A_DQS#5
SA_DQS6# AP11 M_A_DQS#6
SA_DQS7# AT13 M_A_DQS#7
M_A_DQS#[7..0] 20
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SA_DQS4 AH8 M_A_DQS4
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SA_MA4 V1 M_A_A4
SA_MA5 AA9 M_A_A5
SA_MA6 V8 M_A_A6
SA_MA7 T1 M_A_A7
SA_MA8 Y9 M_A_A8
SA_MA9 U6 M_A_A9
SA_MA10 AD4 M_A_A10
SA_MA11 T2 M_A_A11
SA_MA12 U3 M_A_A12
SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15
M_A_A[15..0] 20
2ND = 62.10055.321
62.10040.611
CPU1D
4 0F 9
AUBURNDALE
DDR SYSTEM MEMORY - B
AUBURNF
SJV50
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M_B_DQ0 B5
M_B_DQ1 A5
M_B_DQ2 C3
M_B_DQ3 B3
M_B_DQ4 F4
M_B_DQ5 A6
M_B_DQ6 A4
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M_B_DQ23 J1
M_B_DQ24 J5
M_B_DQ25 K2
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M_B_DQ30 M4
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M_B_DQ33 AG1
M_B_DQ34 AJ3
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M_B_DQ41 AK4
M_B_DQ42 AM6
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M_B_DQ44 AK5
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M_B_DQ49 AN5
M_B_DQ50 AT4
M_B_DQ51 AN6
M_B_DQ52 AN4
M_B_DQ53 AN3
M_B_DQ54 AT5
M_B_DQ55 AT6
M_B_DQ56 AN7
M_B_DQ57 AP6
M_B_DQ58 AP8
M_B_DQ59 AT9
M_B_DQ60 AT7
M_B_DQ61 AP9
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21 M_B_BS0
21 M_B_BS1
21 M_B_BS2
AB1 W5 R7
SB_BS0 SB_BS1 SB_BS2
21 M_B_CAS#
21 M_B_RAS#
21 M_B_WE#
AC5 Y7 AC6
SB_CAS# SB_RAS# SB_WE#
SB_CK0 W8
SB_CK0# W9
SB_CKE0 M3
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M_CLK_DDR#2 21
M_CKE2 21
SB_CK1 V7
SB_CK1# V6
SB_CKE1 M2
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M_CKE3 21
SB_CS0# AB8
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SB_DM2 H3 M_B_DM2
SB_DM3 K1 M_B_DM3
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SB_DM6 AR4 M_B_DM6
SB_DM7 AT8 M_B_DM7
M_B_DM[7..0] 21
SB_DQS0# D5 M_B_DQS#0
SB_DQS1# F4 M_B_DQS#1
SB_DQS2# J4 M_B_DQS#2
SB_DQS3# L4 M_B_DQS#3
SB_DQS4# AH2 M_B_DQS#4
SB_DQS5# AL4 M_B_DQS#5
SB_DQS6# AR5 M_B_DQS#6
SB_DQS7# AR8 M_B_DQS#7
M_B_DQS#[7..0] 21
SB_DQS0 C5 M_B_DQS0
SB_DQS1 E3 M_B_DQS1
SB_DQS2 H4 M_B_DQS2
SB_DQS3 M5 M_B_DQS3
SB_DQS4 AG2 M_B_DQS4
SB_DQS5 AL5 M_B_DQS5
SB_DQS6 AP5 M_B_DQS6
SB_DQS7 AR7 M_B_DQS7
M_B_DQS[7..0] 21
SB_MA0 U5 M_B_A0
SB_MA1 V2 M_B_A1
SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AE7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15
M_B_A[15..0] 21
2ND = 62.10055.321
62.10040.611
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (3/7)
Size A3
Document Number SJV50-CP
Rev SB
Date: Wednesday, October 21, 2009
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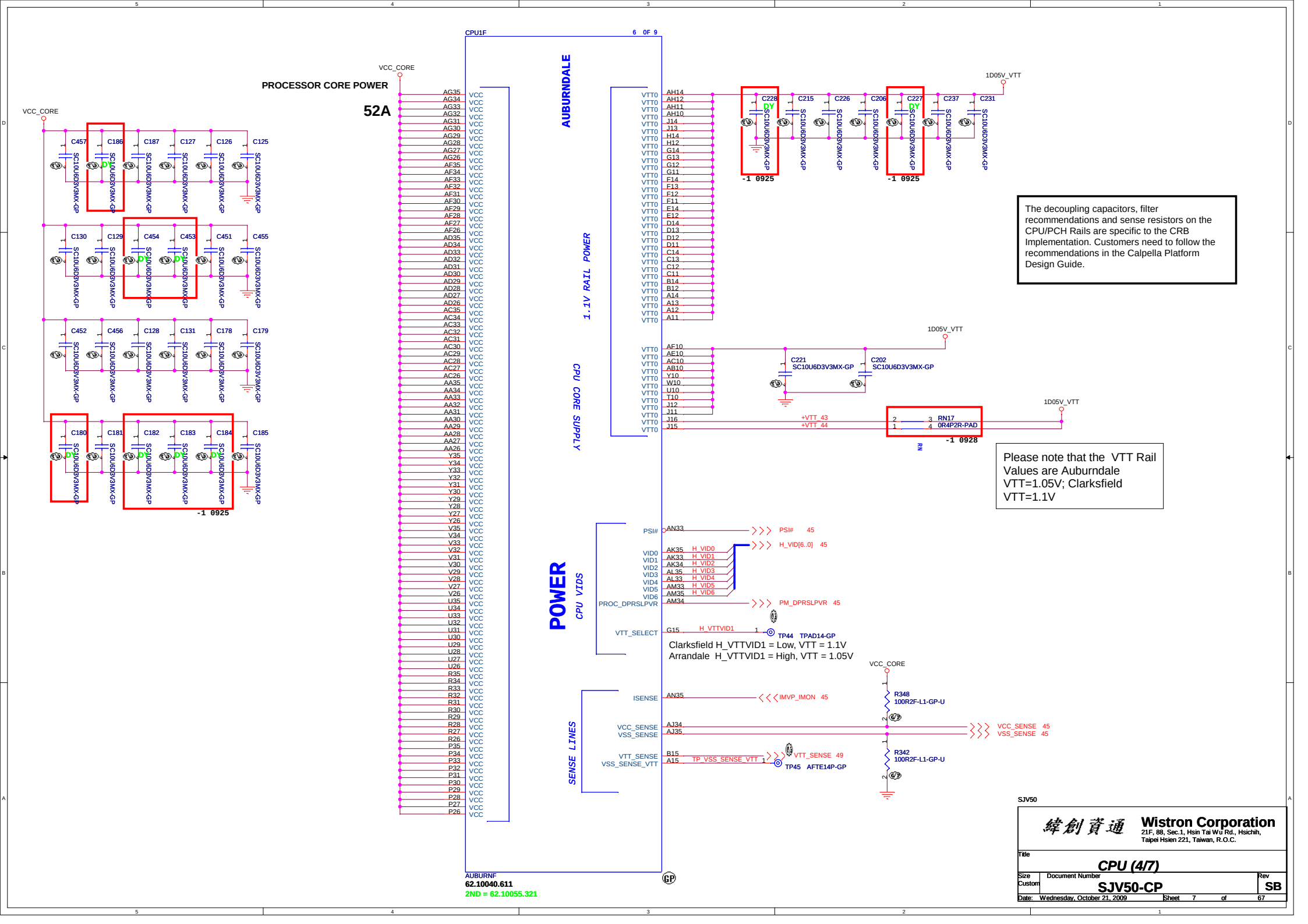
PROCESSOR CORE POWER
52A
VCC_CORE
CPU1F
6 0F 9
AUBURNDALE
1.1V RAIL POWER
CPU CORE SUPPLY
POWER
CPU VIDS
SENSE LINES
1D05V_VTT
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
AUBURNF
62.10040.611
2ND = 62.10055.321
SJV50
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
CPU (4/7)
SJV50-CP
SB
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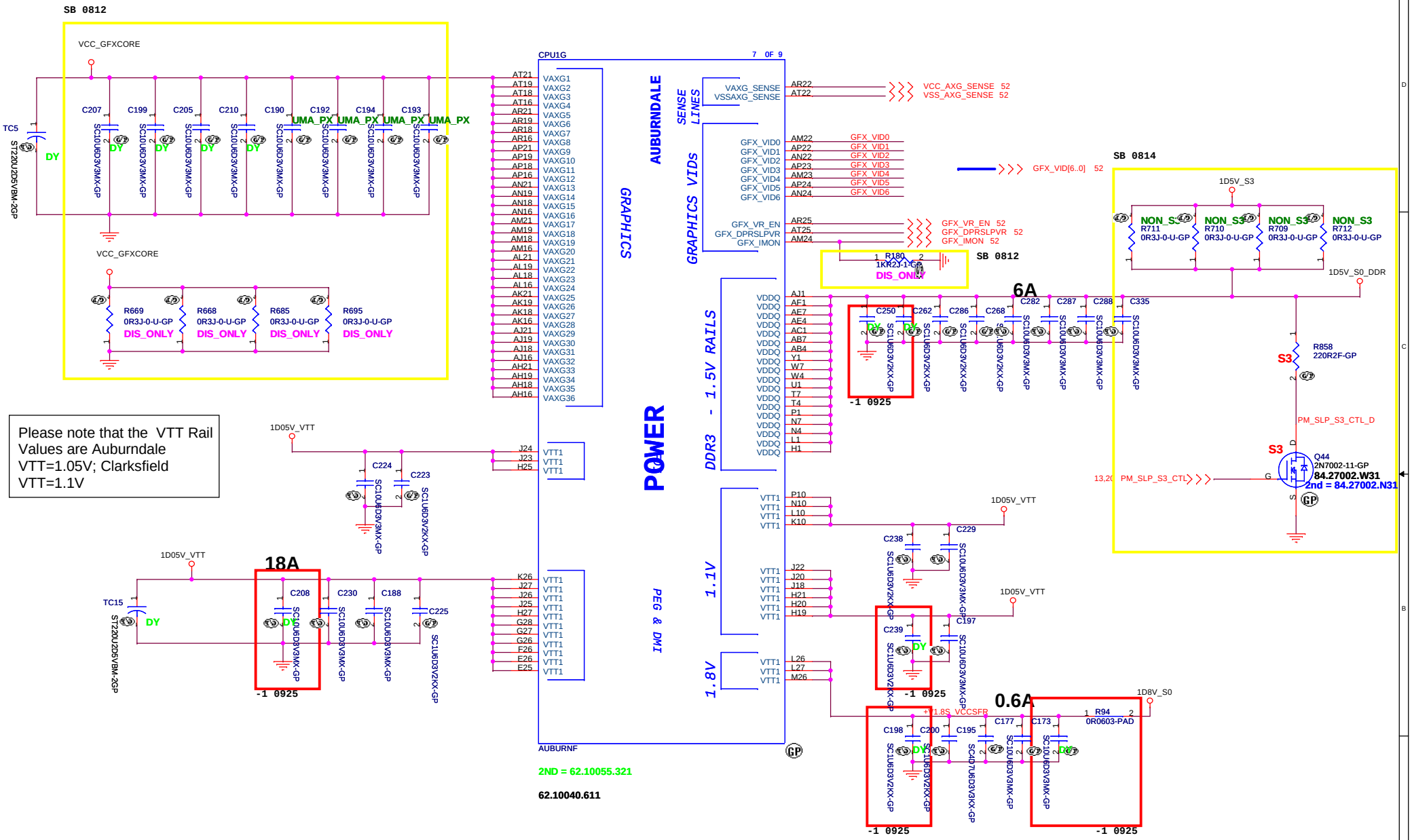

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Title: CPU (5/7)

Size	Document Number	Rev
A3	SJV50-CP	SB

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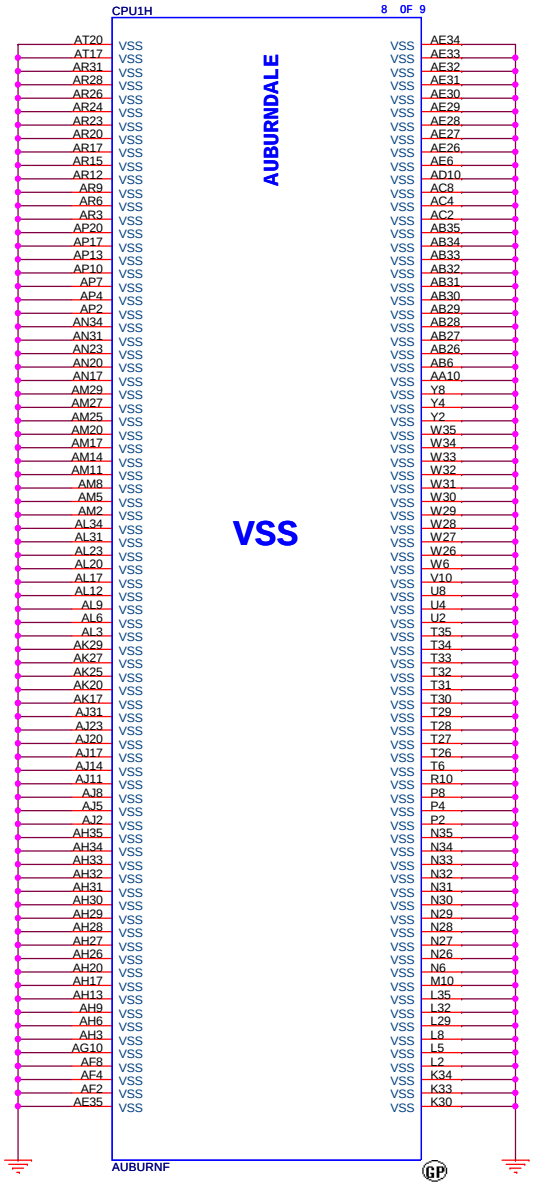
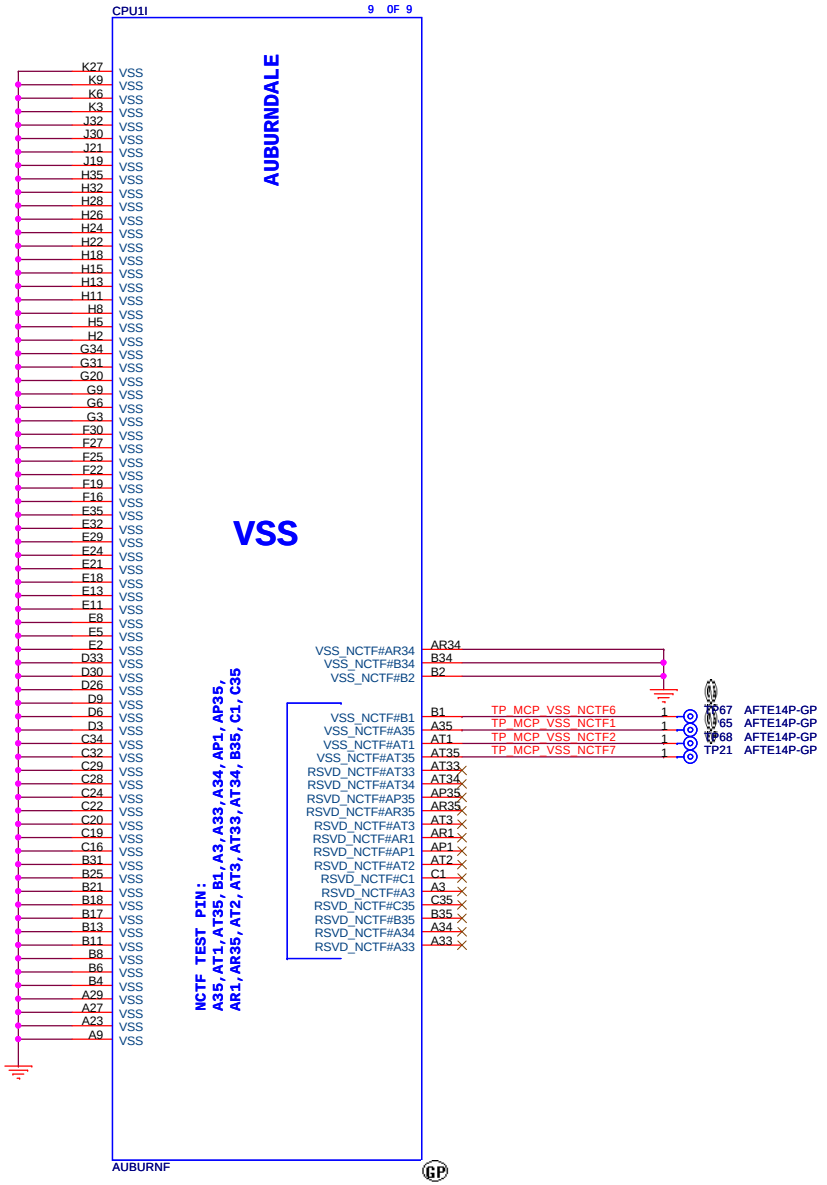


2ND = 62.10055.321

62.10040.611



2ND = 62.10055.321

62.10040.611

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Title: ***CPU (6/7)***

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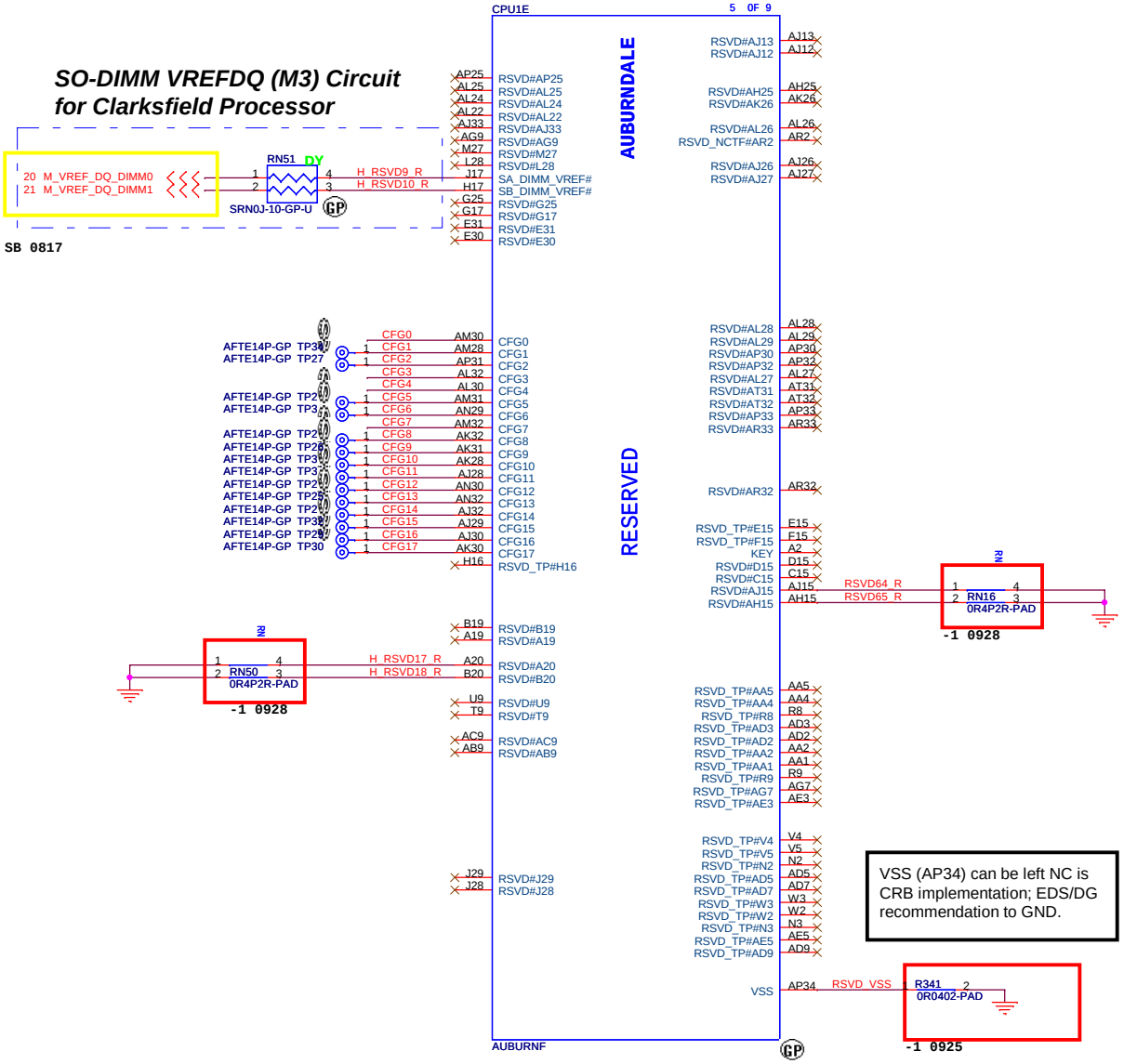
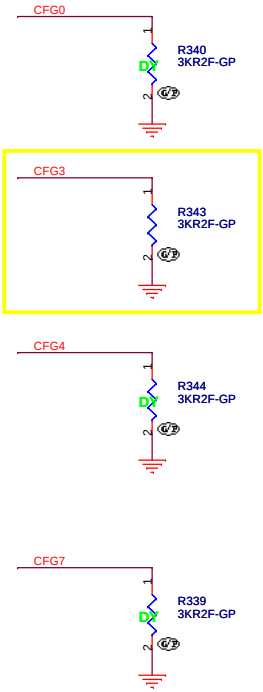
SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor





PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

SJV50

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Title: **CPU (7/7)**

Size	Document Number	Rev
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integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

ICH_RTCX1
ICH_RTCX2
R443 10MR2J-L-GP
X6
X-32D768KHZ-34GPU
82.30001.661
C554 SC7P50V2DN-2GP
C549 SC7P50V2DN-2GP

RTC_AUX_S5
RN22 SRN20KJ-GP-U
C263 SC1U6D3V2KX-GP
C281 SC1U6D3V2KX-GP
G57 GAP-OPEN

SA 0629 RF
ACZ_RST# DY EC14 SC33P50V2JN-3GP
ACZ_SYNC DY EC18 SC33P50V2JN-3GP
ACZ_BIT_CLK DY EC16 SC33P50V2JN-3GP
ACZ_SDATAOUT DY EC17 SC33P50V2JN-3GP

SB 0825
32 ACZ_RST#_AUDIO
32 ACZ_SYNC_AUDIO
32 ACZ_BITCLK_AUDIO
32 ACZ_SDATAOUT_AUDIO
R397 10R2J-2-GP
R423 10R2J-2-GP
R420 10R2J-2-GP
R422 47R2J-2-GP
ACZ_RST#
ACZ_SYNC
ACZ_BIT_CLK
ACZ_SDATAOUT

35 ACZ_RST#_MDC
35 ACZ_SYNC_MDC
35 ACZ_BTCLK_MDC
35 ACZ_SDATAOUT_MDC
R398 33R2J-2-GP
R424 33R2J-2-GP
R419 33R2J-2-GP
R421 33R2J-2-GP

NO REBOOT STRAP
3D3V_S0
R465 DY 1KR2J-1-GP ACZ_SPKR

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

-1 0925
3D3V_S5
PCH_JTAG_TMS R493 DY 200R2J-L1-GP
PCH_JTAG_TDO R485 DY 200R2J-L1-GP
PCH_JTAG_TDI R492 DY 200R2J-L1-GP
PCH_JTAG_RST# R490 DY 10KR2J-3-GP
PCH_JTAG_TMS R477 DY 100R2J-2-GP
PCH_JTAG_TDO R486 DY 100R2J-2-GP
PCH_JTAG_TDI R487 DY 100R2J-2-GP
PCH_JTAG_RST# R491 DY 51R2F-2-GP
PCH_JTAG_TCK R227 51R2F-2-GP
When unused all JTAG pins may be NC

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
3D3V_S0 R480 DY 8K2R2J-3-GP SPI_MOSI_R

SA 0709 EMI
ACZ_BTCLK_MDC
ACZ_BITCLK_AUDIO DY EC13 SC22P50V2JN-4GP
DY EC15 SC22P50V2JN-4GP

RTC_AUX_S5
R189 1MR2J-1-GP SM_INTRUDER#
R188 330KR2F-L-GP ICH_INTVRMEN

PCH1A 1 OF 10

ICH_RTCX1	B13	RTCX1	RTC
ICH_RTCX2	D13	RTCX2	
ICH_RTCRST#	C14	RTCRST#	
SRTCRST#	D17	SRTCRST#	
SM_INTRUDER#	A16	INTRUDER#	
ICH_INTVRMEN	A14	INTVRMEN	
ACZ_BIT_CLK	A30	HDA_BCLK	IHDA
ACZ_SYNC	D29	HDA_SYNC	
32 ACZ_SPKR	P1	SPKR	
ACZ_RST#	C30	HDA_RST#	
32 ACZ_SDATAIN0	G30	HDA_SDIN0	
35 ACZ_SDATAIN1	F30	HDA_SDIN1	
HDA_SDIN2	E32	HDA_SDIN2	
	F32	HDA_SDIN3	
ACZ_SDATAOUT	B29	HDA_SDO	
39 ME_UNLOCK#	H32	HDA_DOCK_EN#/GPIO33	SATA
HDA_DOCK_EN#	J30	HDA_DOCK_RST#/GPIO13	
PCH_JTAG_TCK	M3	JTAG_TCK	JTAG
PCH_JTAG_TMS	K3	JTAG_TMS	
PCH_JTAG_TDI	K1	JTAG_TDI	
PCH_JTAG_TDO	J2	JTAG_TDO	
PCH_JTAG_RST#	J4	TRST#	
40 PCH_SPI_CLK	BA2	SPI_CLK	SPI
40 PCH_SPI_CS#0	AV3	SPI_CS0#	
	AY3	SPI_CS1#	
40 PCH_SPI_MOSI	AY1	SPI_MOSI	
40 SPI_MOSO_R	AV1	SPI_MISO	

-1 0925
R171 0R0402-PAD
R172 DY 8K2R2J-3-GP

FWH0/LAD0	D33	LPC_LAD0 39	LPC
FWH1/LAD1	B33	LPC_LAD1 39	
FWH2/LAD2	C32	LPC_LAD2 39	
FWH3/LAD3	A32	LPC_LAD3 39	
FWH4/LFRAME#	C34	LPC_LFRAME# 39	
LDRQ0#	A34		
LDRQ1#/GPIO23	F34	PCH_GPIO23 → TP47 AFTE14P-GP	
SERIRQ	AB9	INT_SERIRQ 39	
SATA0RXN	AK7	SATA_RXN0 26	HDD
SATA0RXP	AK6	SATA_RXP0 26	
SATA0TXN	AK11	SATA_TXN0 26	
SATA0TXP	AK9	SATA_TXP0 26	
SATA1RXN	AH6		
SATA1RXP	AH5		
SATA1TXN	AH9		
SATA1TXP	AH8		
SATA2RXN	AF11		
SATA2RXP	AF9		
SATA2TXN	AF7		
SATA2TXP	AF6		
SATA3RXN	AH3		
SATA3RXP	AH1		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	AD9	SATA_RXN4 27	ODD
SATA4RXP	AD8	SATA_RXP4 27	
SATA4TXN	AD6	SATA_TXN4 27	
SATA4TXP	AD5	SATA_TXP4 27	
SATA5RXN	AD3		
SATA5RXP	AD1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	AF16		
SATAICOMPI	AF15	SATAICOMP R187 37D4R2F-GP → 1D05V_S0	
SATALED#	T3	SATA_LED# → SATA_LED# 42	
SATA0GP/GPIO21	Y9	SATA_DET#0_R	
SATA1GP/GPIO19	V1	SATA_DET#1_R	

IBEXPEAK-M-GP-NF

RN39 SRN10KJ-7GP
SATA_LED#
SATA_DET#0_R
INT_SERIRQ
SATA_DET#1_R
3D3V_S0

RTC_AUX_S5 -1 0925
R244 0R0603-PAD
RTC_PWR_L
C311 SC1U10V2ZY-GP
D10 BAS40CW-GP
83.00040.E81
2nd = 83.00040.M81
3D3V_AUX_S5
RTC_PWR
R239 1KR2J-1-GP
RTC_BAT
RTC1 BAT-CON2-1-GP-U
62.70001.011

SJV50

Wistron Corporation
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Title: PCH (1/9)
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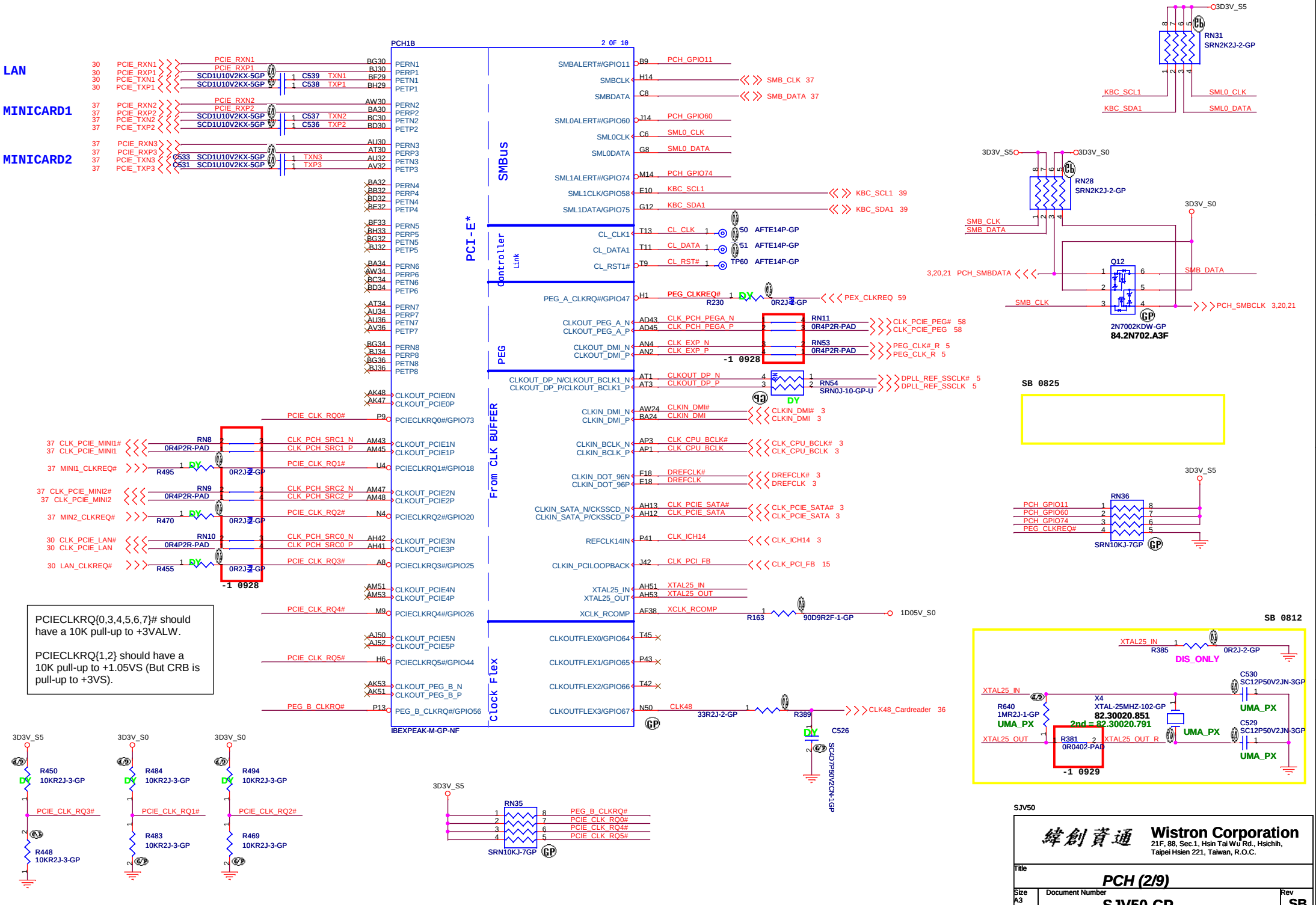
LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
SB 0825
SB 0812
-1 0928
-1 0929
2N7002KDW-GP
84.2N702.A3F
SRN10KJ-7GP
SRN0J-10-GP-U
SJV50
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PCH (2/9)
SJV50-CP
Date: Wednesday, October 21, 2009
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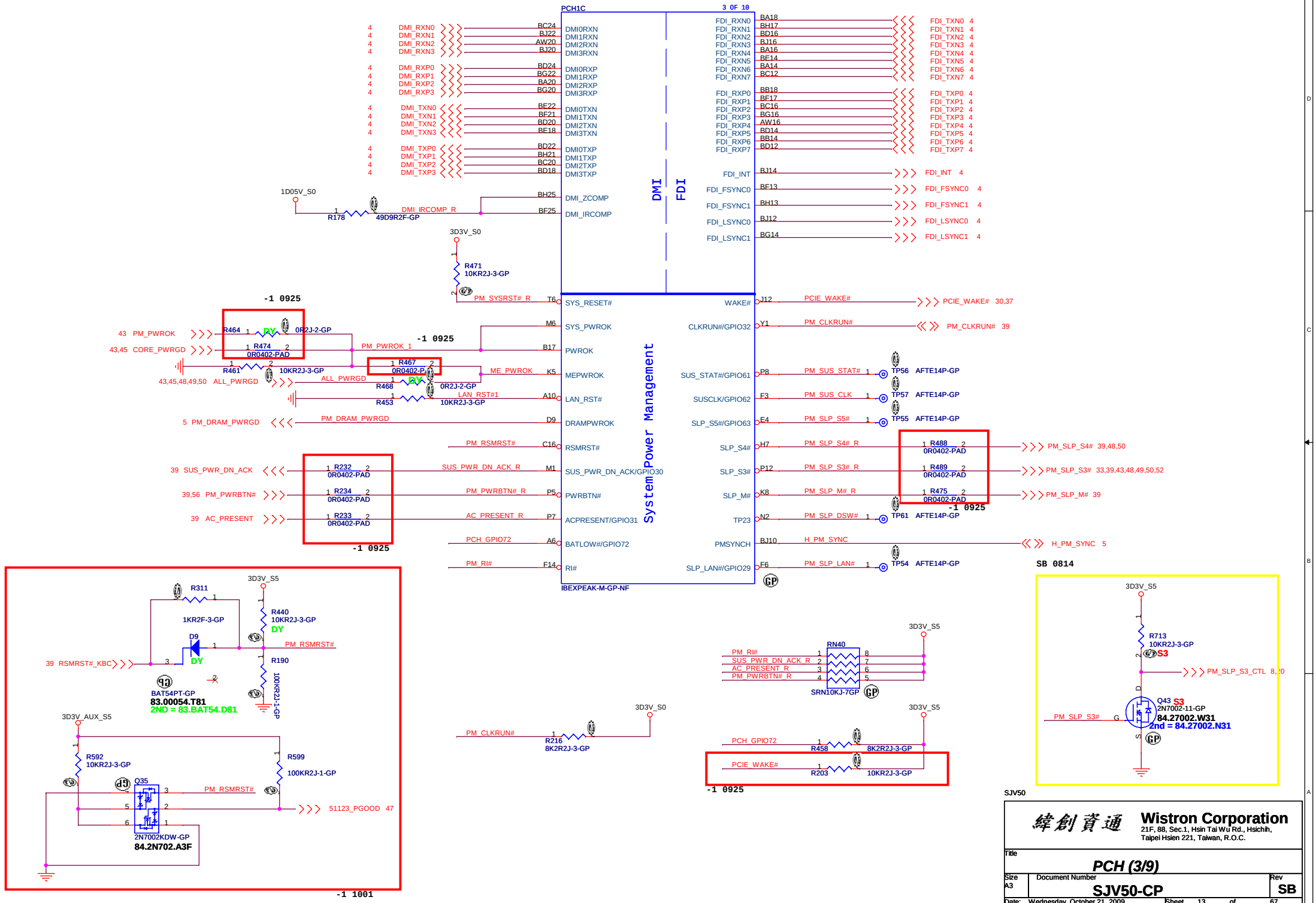

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Title	***PCH (3/9)***	
Size A3	Document Number **SJV50-CP**	Rev **SB**
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SB 0812

3D3V_S0

RN48
SRN10KJ-5-GP
UMA_PX
LCTL_CLK
LCTL_DATA

R153 2K37R2F-GP
UMA_PX
LIBG

R149 0R2J-2-GP
UMA_PX
LVDS_VREF

RN49
SRN150F-1-GP
UMA_PX
PCH_BLUE
PCH_GREEN
PCH_RED

PCH1D

4 OF 10

22 PCH_BL_ON	T48	L_BKLTEN	Digital Display Interface	SDVO_TVCLKINN	BJ46
23 PCH_LCDVDD_ON	T47	L_VDD_EN		SDVO_TVCLKINP	BG46
23 L_BKLTCTL	Y48	L_BKLTCTL		SDVO_STALLN	BJ48
				SDVO_STALLP	BG48
22 CLK_DDC_EDID	AB48	L_DDC_CLK		SDVO_INTN	BF45
22 DAT_DDC_EDID	Y45	L_DDC_DATA		SDVO_INTP	BH45
LCTL_CLK	AB46	L_CTRL_CLK			
LCTL_DATA	V48	L_CTRL_DATA			
LIBG	AP39	LVD_IBG		SDVO_CTRLCLK	T51
L_LVBG	AP41	LVD_VBG		SDVO_CTRLDATA	T53
LVDS_VREF	AT43	LVD_VREFH			
	AT42	LVD_VREFL			
				DDPB_AUXN	BG44
				DDPB_AUXP	BJ44
				DDPB_HPD	AU38
22 PCH_TXACLK-	AV53	LVDSA_CLK#	LVDS	DDPB_0N	BD42
22 PCH_TXACLK+	AV51	LVDSA_CLK		DDPB_0P	BC42
22 PCH_TXAOUT0-	BB47	LVDSA_DATA#0		DDPB_1N	BJ42
22 PCH_TXAOUT1-	BA52	LVDSA_DATA#1		DDPB_1P	BG42
22 PCH_TXAOUT2-	AY48	LVDSA_DATA#2		DDPB_2N	BB40
	AV47	LVDSA_DATA#3		DDPB_2P	BA40
22 PCH_TXAOUT0+	BB48	LVDSA_DATA0		DDPB_3N	AW38
22 PCH_TXAOUT1+	BA50	LVDSA_DATA1		DDPB_3P	BA38
22 PCH_TXAOUT2+	AY49	LVDSA_DATA2			
	AV48	LVDSA_DATA3		DDPC_CTRLCLK	Y49
				DDPC_CTRLDATA	AB49
22 PCH_TXBCLK-	AP48	LVDSB_CLK#			
22 PCH_TXBCLK+	AP47	LVDSB_CLK		DDPC_AUXN	BE44
				DDPC_AUXP	BD44
22 PCH_TXBOUT0-	AY53	LVDSB_DATA#0		DDPC_HPD	AV40
22 PCH_TXBOUT1-	AT49	LVDSB_DATA#1			
22 PCH_TXBOUT2-	AU52	LVDSB_DATA#2		DDPC_0N	BE40
	AT53	LVDSB_DATA#3		DDPC_0P	BD40
22 PCH_TXBOUT0+	AY51	LVDSB_DATA0		DDPC_1N	BF41
22 PCH_TXBOUT1+	AT48	LVDSB_DATA1		DDPC_1P	BH41
22 PCH_TXBOUT2+	AU50	LVDSB_DATA2		DDPC_2N	BD38
	AT51	LVDSB_DATA3		DDPC_2P	BC38
				DDPC_3N	BB36
				DDPC_3P	BA36
22 PCH_BLUE	AA52	CRT_BLUE	CRT	DDPD_CTRLCLK	U50
22 PCH_GREEN	AB53	CRT_GREEN		DDPD_CTRLDATA	U52
22 PCH_RED	AD53	CRT_RED			
				DDPD_AUXN	BC46
24 PCH_DDCCLK	V51	CRT_DDC_CLK		DDPD_AUXP	BD46
24 PCH_DDCDATA	V53	CRT_DDC_DATA		DDPD_HPD	AT38
				DDPD_0N	BJ40
24 PCH_HSYNC	Y53	CRT_HSYNC		DDPD_0P	BG40
24 PCH_VSYNC	Y51	CRT_VSYNC		DDPD_1N	BJ38
				DDPD_1P	BG38
CRT_IREF	AD48	DAC_IREF		DDPD_2N	BF37
	AB51	CRT_IRTN		DDPD_2P	BH37
				DDPD_3N	BE36
				DDPD_3P	BD36

IBEXPEAK-M-GP-NF

TPAD14-GP TP46

R126 1KR2D-1-GP

1K 0.5% ohm

PCH_HDMI_CLK 25
PCH_HDMI_DATA 25
PCH_HDMI_DETECT 25

SB 0812

PCH_HDMI_DATA2- L	C76	SCD1U10V2KX-5GP UMA_PX	PCH_HDMI_DATA2- 25
PCH_HDMI_DATA2+ L	C77	SCD1U10V2KX-5GP UMA_PX	PCH_HDMI_DATA2+ 25
PCH_HDMI_DATA1- L	C62	SCD1U10V2KX-5GP UMA_PX	PCH_HDMI_DATA1- 25
PCH_HDMI_DATA1+ L	C63	SCD1U10V2KX-5GP UMA_PX	PCH_HDMI_DATA1+ 25
PCH_HDMI_DATA0- L	C68	SCD1U10V2KX-5GP UMA_PX	PCH_HDMI_DATA0- 25
PCH_HDMI_DATA0+ L	C69	SCD1U10V2KX-5GP UMA_PX	PCH_HDMI_DATA0+ 25
PCH_HDMI_CLK- L	C66	SCD1U10V2KX-5GP UMA_PX	PCH_HDMI_CLK- 25
PCH_HDMI_CLK+ L	C67	SCD1U10V2KX-5GP UMA_PX	PCH_HDMI_CLK+ 25

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Title: PCH (4/9)

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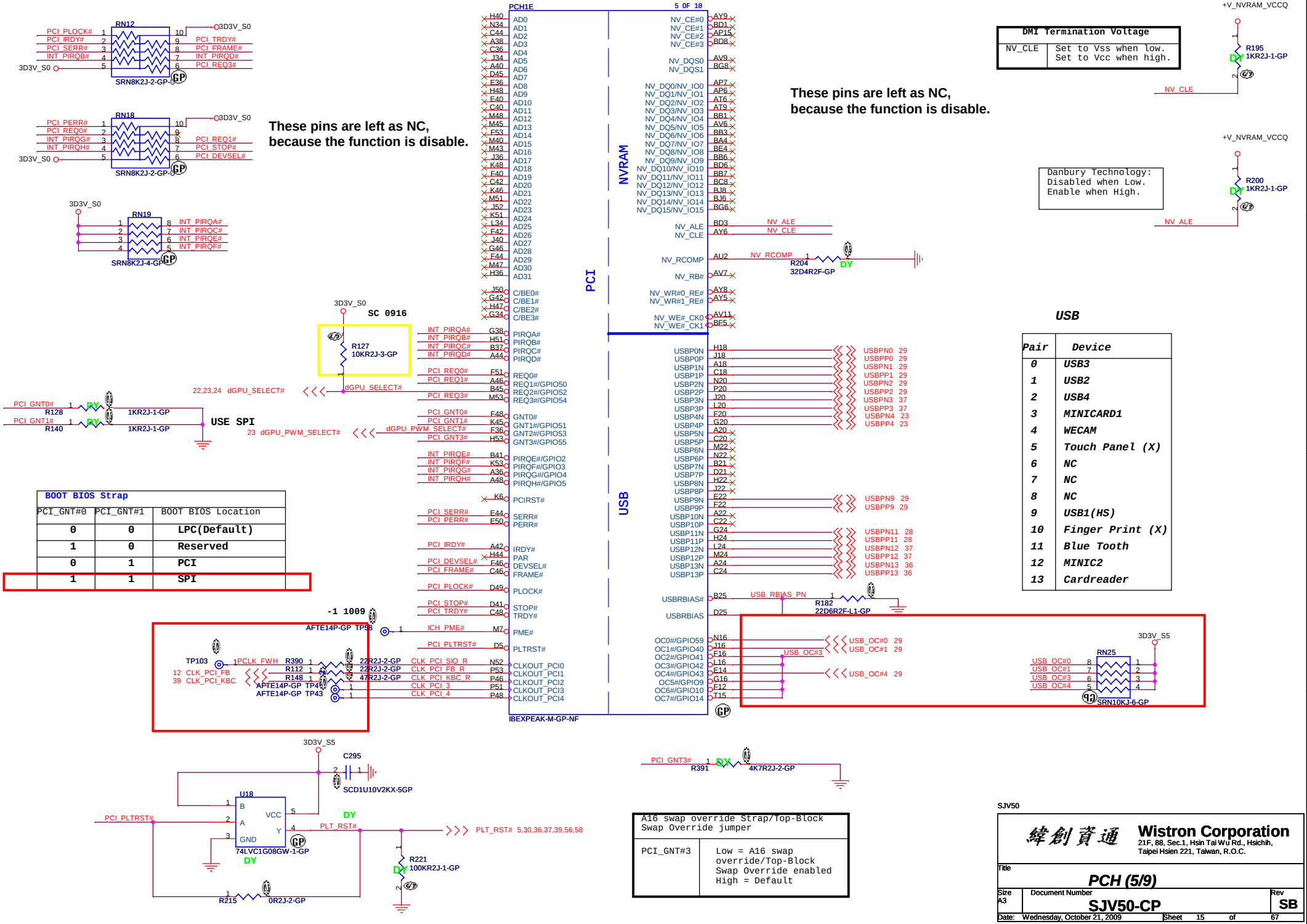

DMI Termination Voltage

NV_CLE	Set to Vss when low. Set to Vcc when high.

BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

USB

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel (X)
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print (X)
11	Blue Tooth
12	MINIC2
13	Cardreader

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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Title: PCH (5/9)

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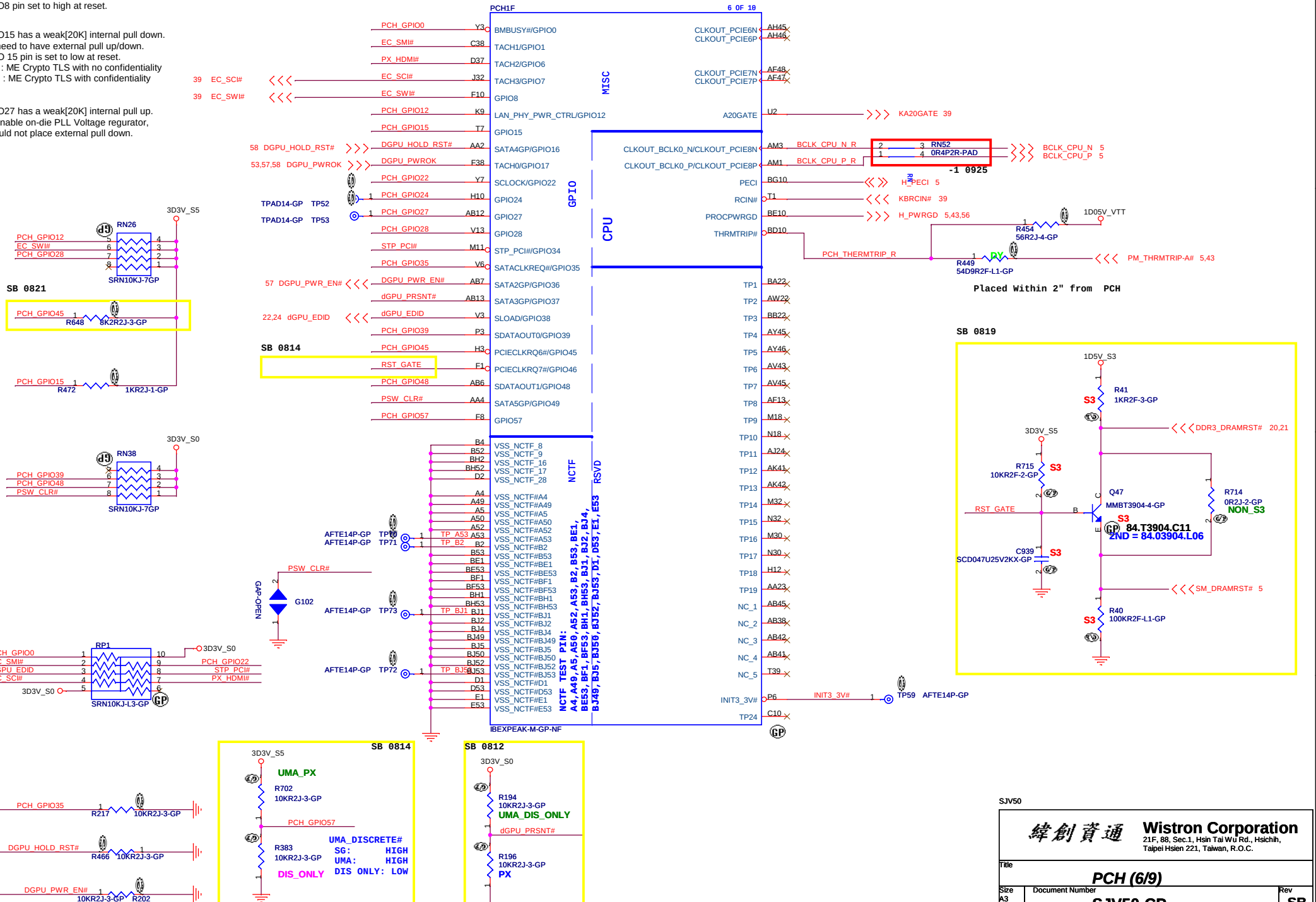
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (6/9)

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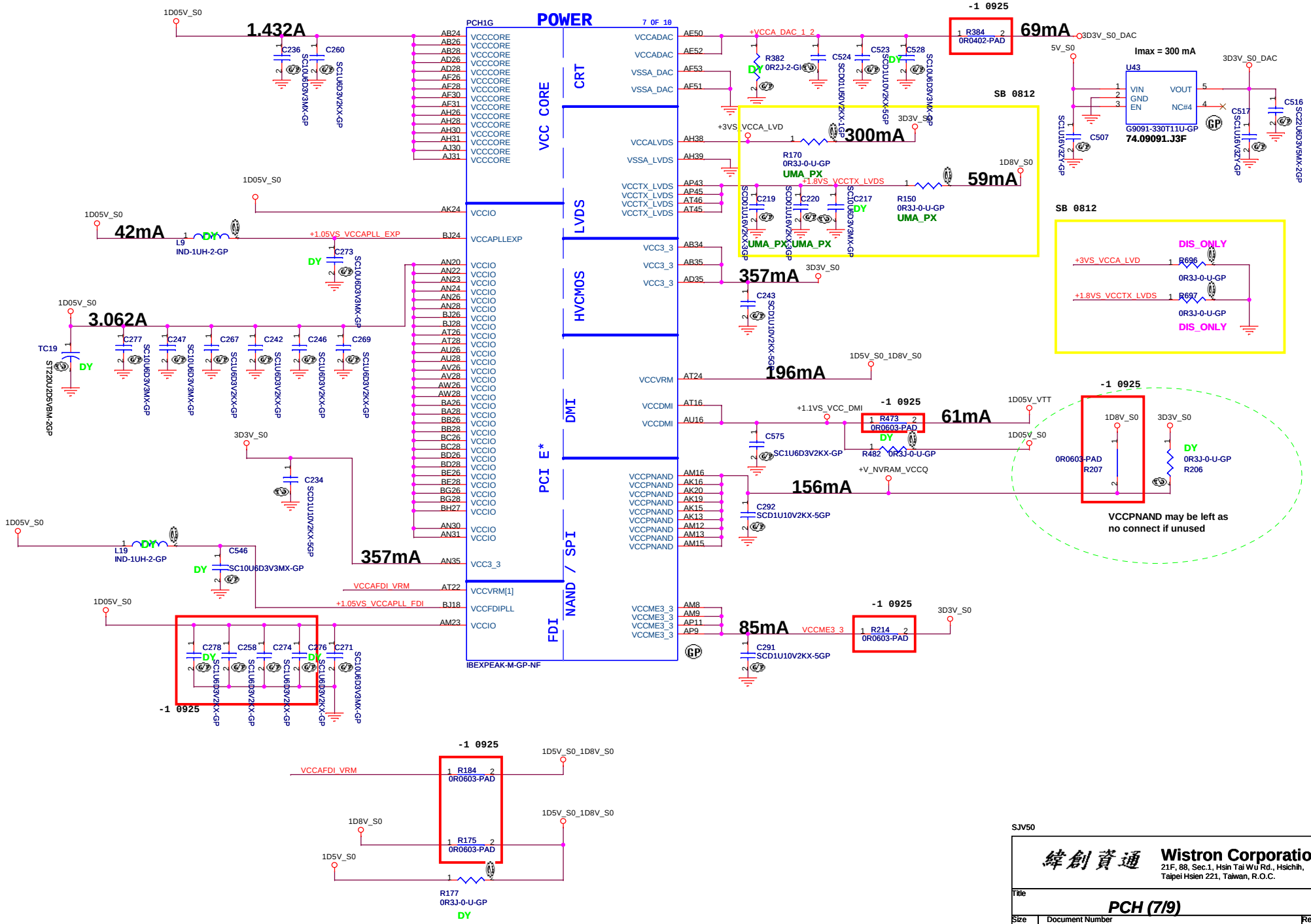
POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
42mA
357mA
357mA
196mA
61mA
156mA
85mA
69mA
300mA
59mA
-1 0925
SB 0812
Imax = 300 mA
G9091-330T11U-GP
74.09091.J3F
DIS_ONLY
VCCPNAND may be left as no connect if unused
IBEXPEAK-M-GP-NF
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (7/9)
SJV50-CP
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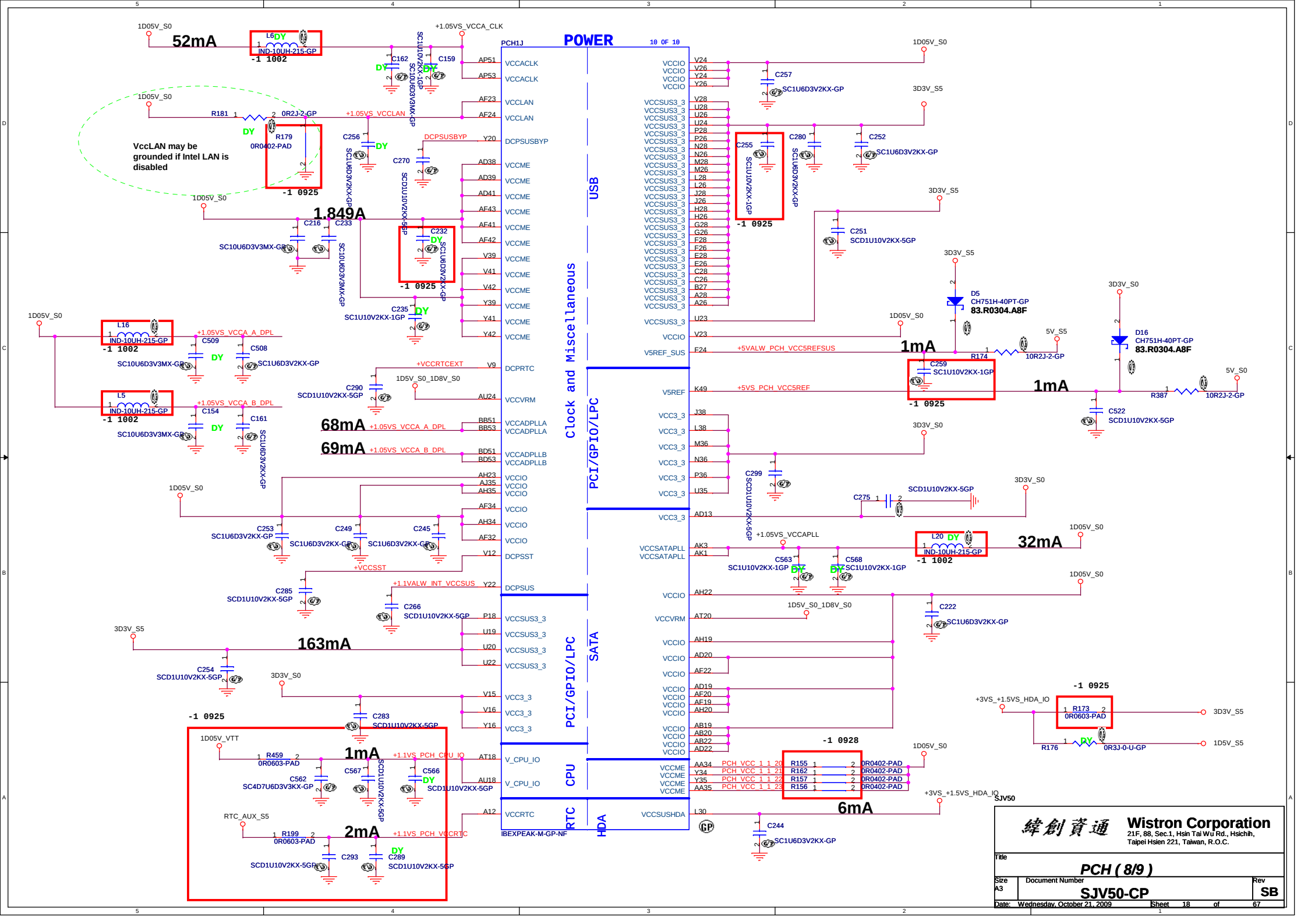
POWER
10 OF 10
PCH1J
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
52mA
1.849A
68mA
69mA
163mA
1mA
2mA
1mA
1mA
6mA
32mA
VccLAN may be grounded if Intel LAN is disabled
-1 1002
-1 0925
-1 0928
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
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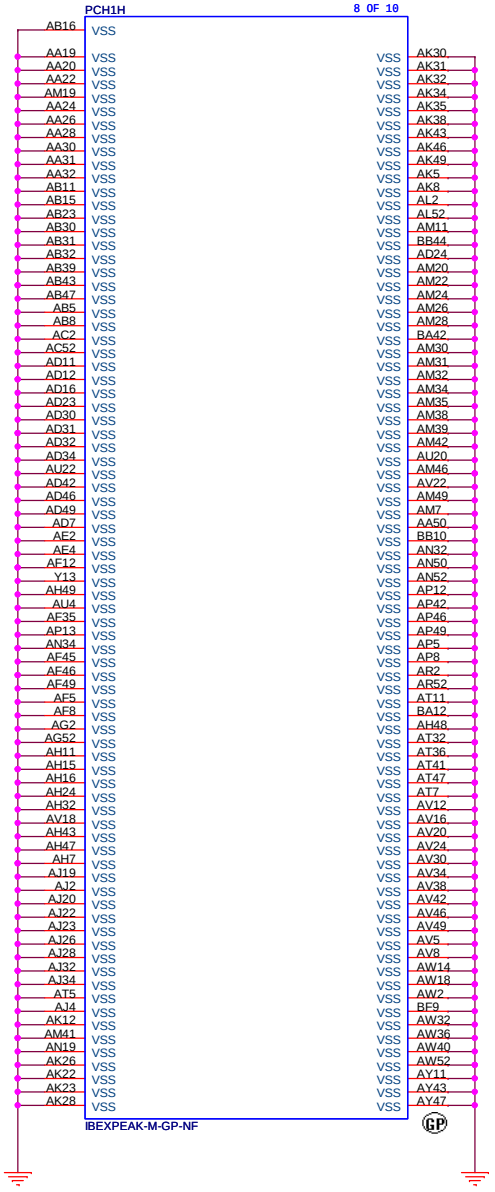

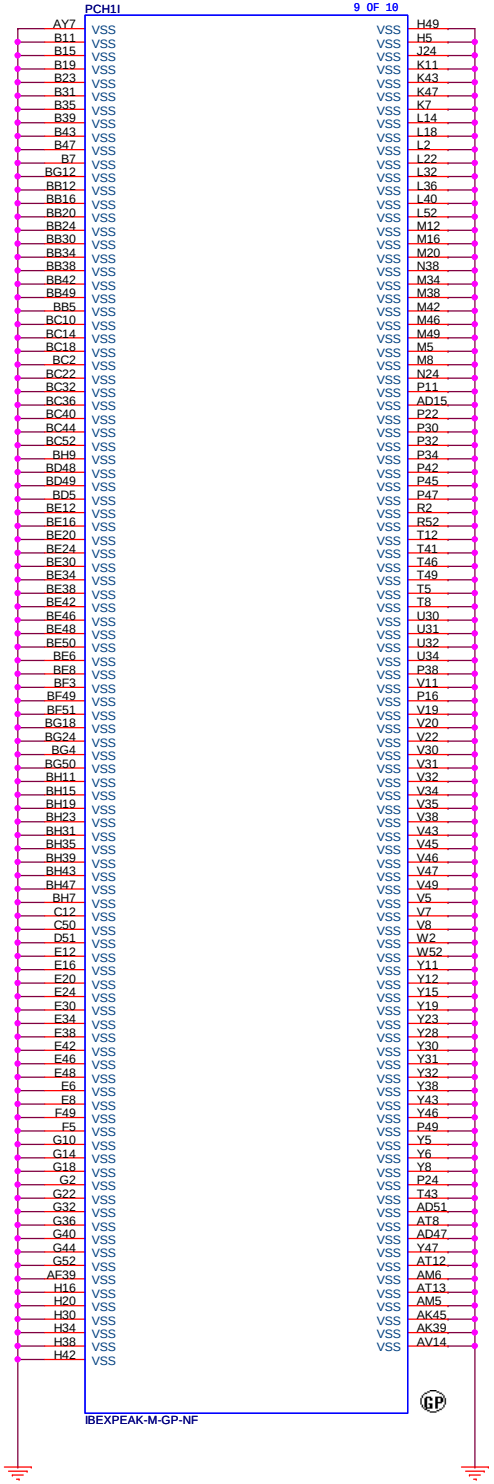

SJV50

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (9/9)***

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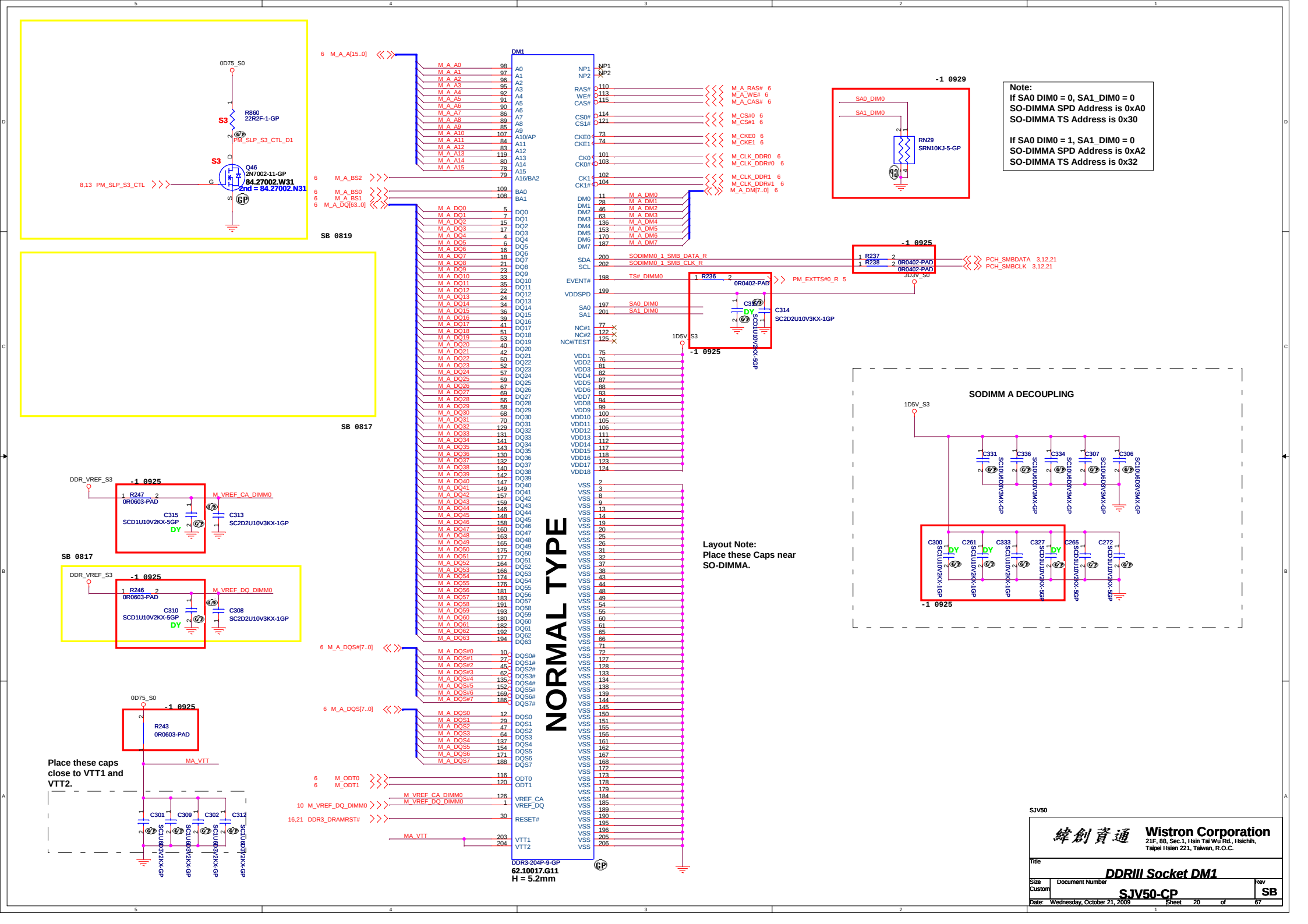
0D75_S0
R860
22R2F-1-GP
S3
PM_SLP_S3_CTL_D1
Q46
2N7002-11-GP
84.27002.W31
2nd = 84.27002.N31
8,13 PM_SLP_S3_CTL
SB 0819
SB 0817
DM1
NORMAL TYPE
DDR3-204P-9-GP
62.10017.G11
H = 5.2mm
-1 0929
SA0_DIM0
SA1_DIM0
RN29
SRN10KJ-5-GP
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
-1 0925
R237
R238
0R0402-PAD
PCH_SMBDATA 3,12,21
PCH_SMBCLK 3,12,21
3D3V_S0
R236
PM_EXTTS#0_R 5
C314
SC2D2U10V3KX-1GP
SCD1U10V2KX-5GP
1D5V_S3
SODIMM A DECOUPLING
C331
C336
C334
C307
C306
SCU10U6D3V3MX-GP
C300
C261
C333
C327
C265
C272
SCD1U10V2KX-1GP
SCD1U10V2KX-5GP
DY
Layout Note:
Place these Caps near
SO-DIMMA.
DDR_VREF_S3
R247
0R0603-PAD
M_VREF_CA_DIMM0
C315
C313
SC2D2U10V3KX-1GP
R246
M_VREF_DQ_DIMM0
C310
C308
R243
MA_VTT
Place these caps
close to VTT1 and
VTT2.
C301
C309
C302
C312
SCU10U6D3V2KX-GP
M_A_A[15..0]
M_A_BS2
M_A_BS0
M_A_BS1
M_A_DQ[63..0]
M_A_DQS#[7..0]
M_A_DQS[7..0]
M_ODT0
M_ODT1
M_VREF_CA_DIMM0
M_VREF_DQ_DIMM0
DDR3_DRAMRST#
M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6
M_CS#0 6
M_CS#1 6
M_CKE0 6
M_CKE1 6
M_CLK_DDR0 6
M_CLK_DDR#0 6
M_CLK_DDR1 6
M_CLK_DDR#1 6
M_A_DM[7..0] 6
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM1
Size Custom
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SJV50-CP
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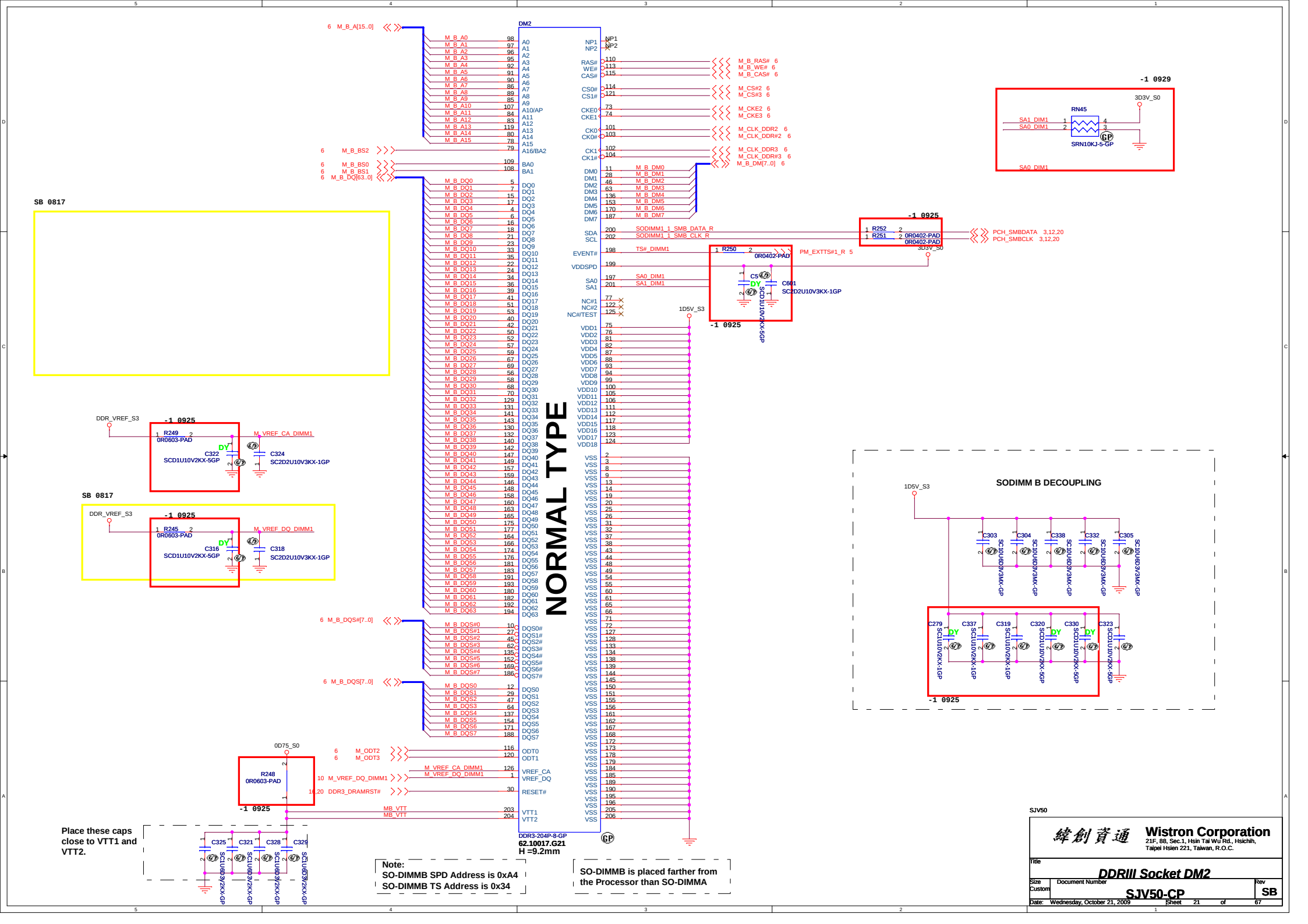
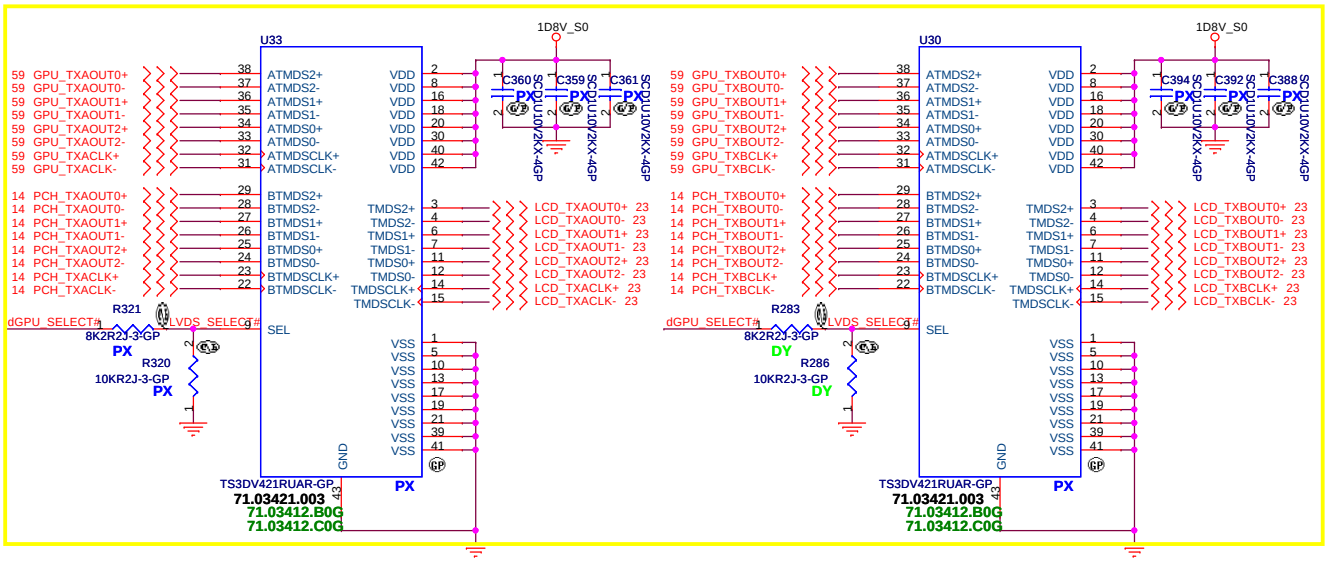
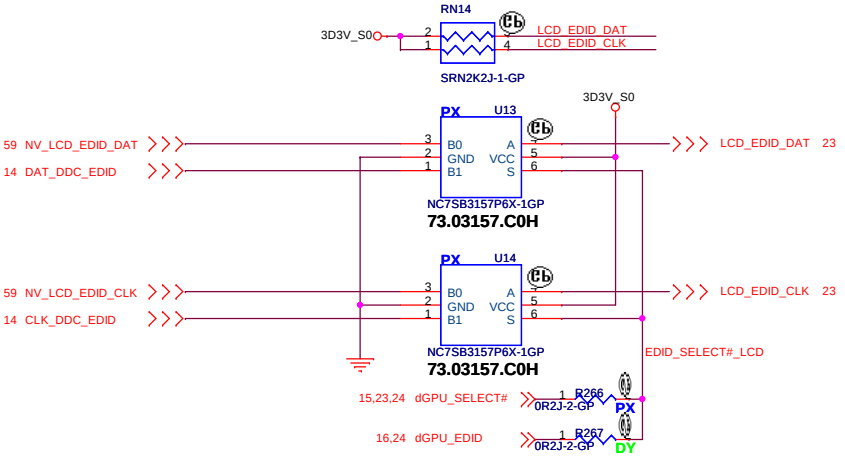
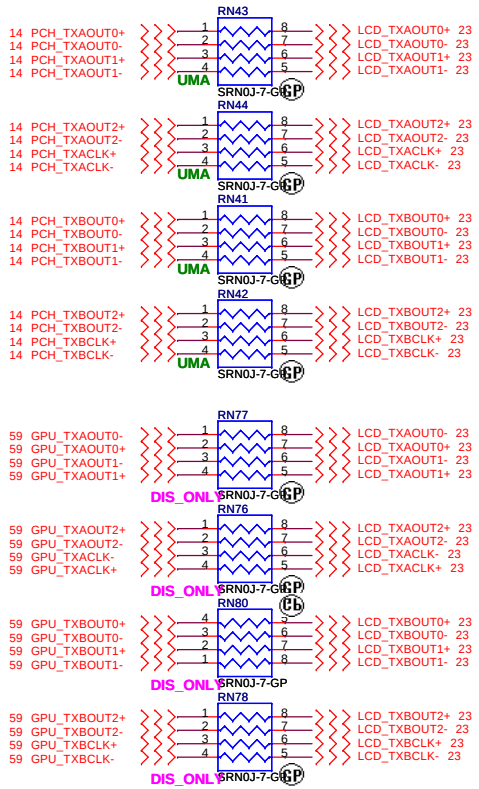

DM2
NORMAL TYPE
DDR3-204P-8-GP
62.10017.G21
H =9.2mm
SB 0817
SB 0817
-1 0925
-1 0929
SODIMM B DECOUPLING
Place these caps close to VTT1 and VTT2.
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRIII Socket DM2
SJV50-CP
SB
Wednesday, October 21, 2009
21
67



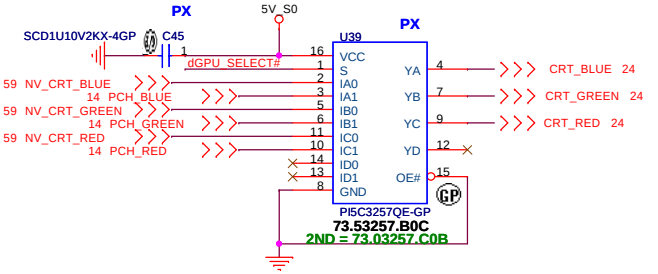


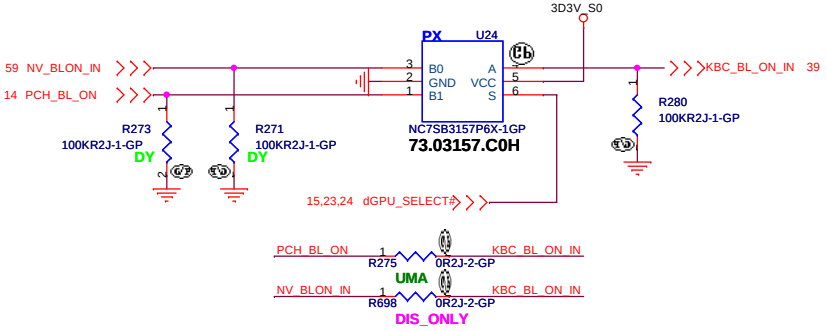


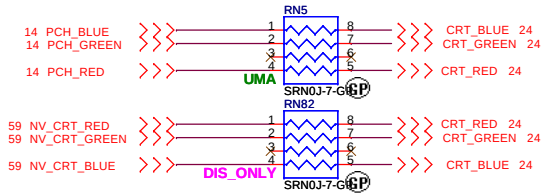
FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1







SJV50

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Title: **PX_SWITCH**

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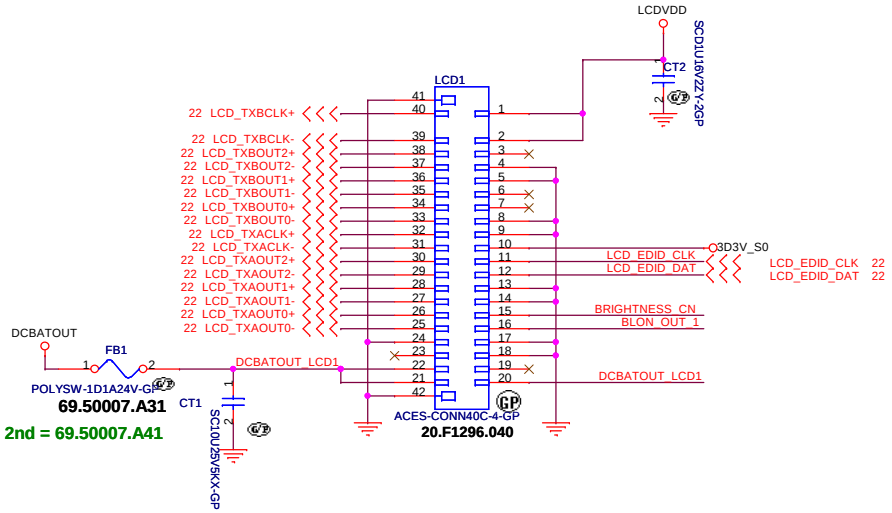
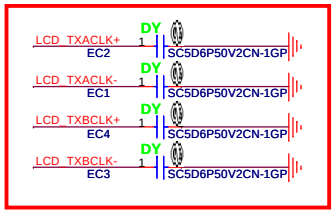
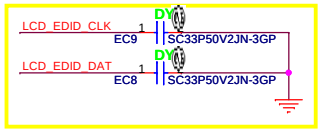
LCD/INVERTER/CCD CONN



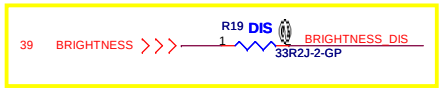


modify by RF

SA 0629 RF

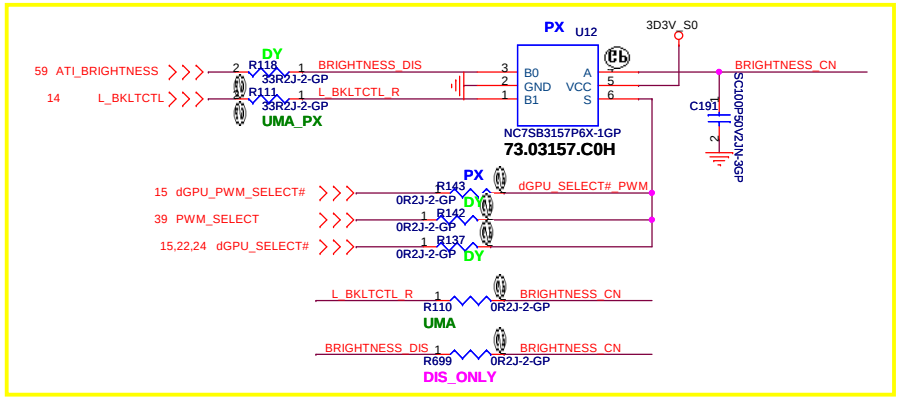


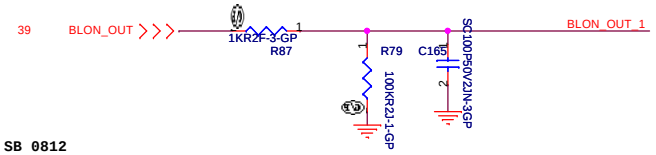
SC 0911



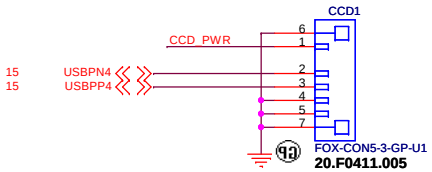
Reserve direct connector to KBC

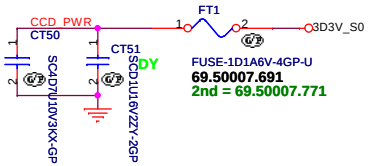
SC 0911



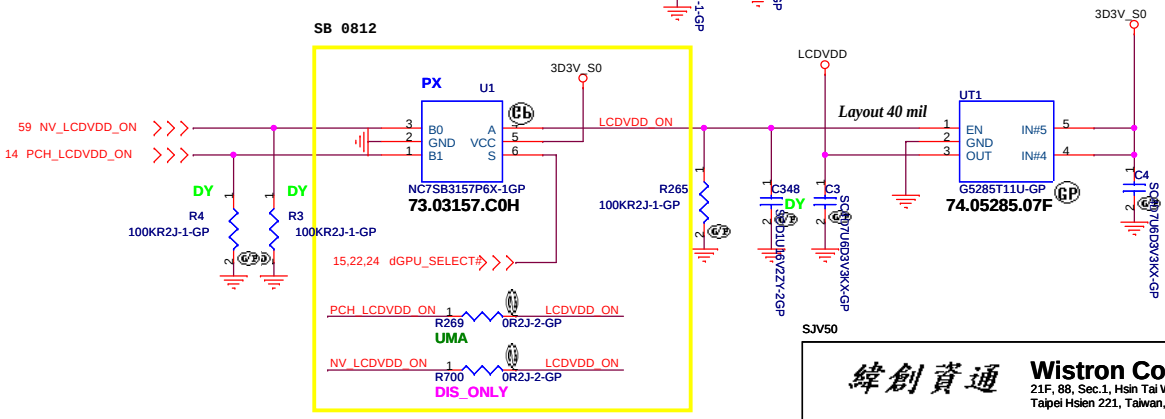


CCD

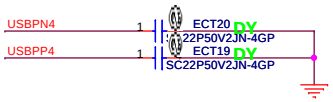


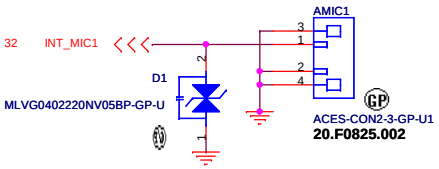


SB 0812



Internal Mic





SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

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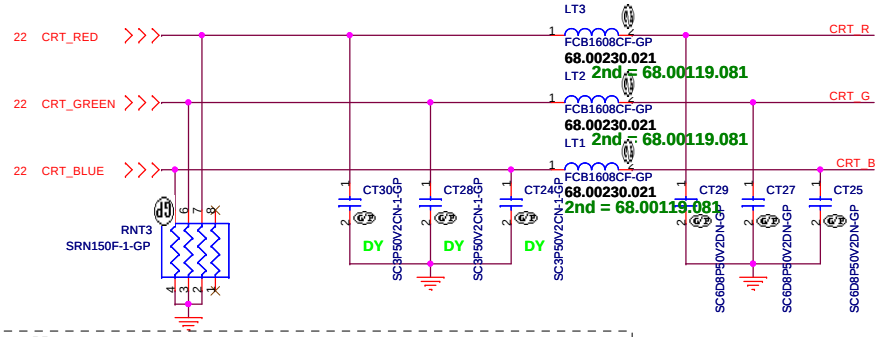
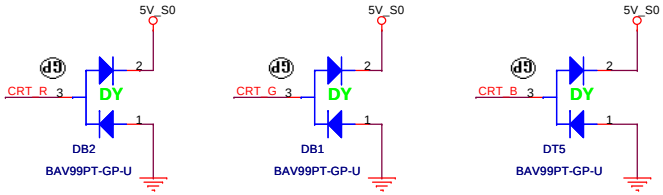
Layout Note:
Place these resistors close to the CRT-out connector



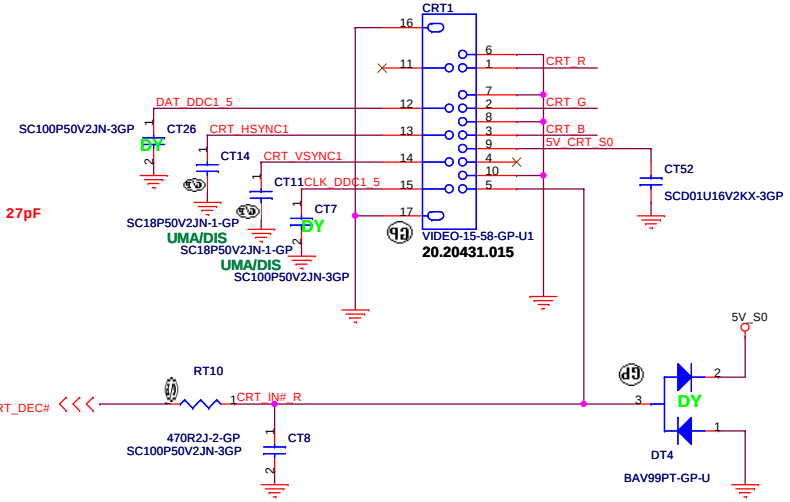
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

500mA



CRT I/F & CONNECTOR

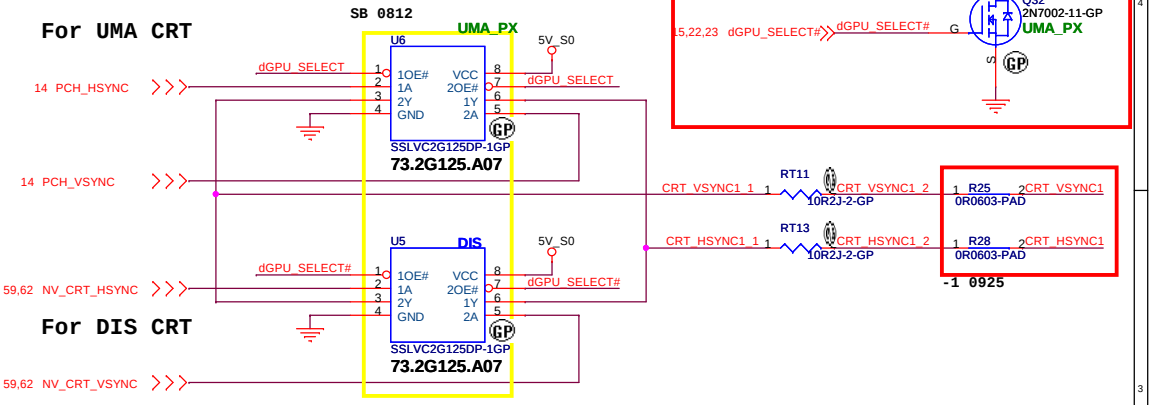
CT87 and CT43
FOR UMA,change to 27pF
(78.27034.1FL)



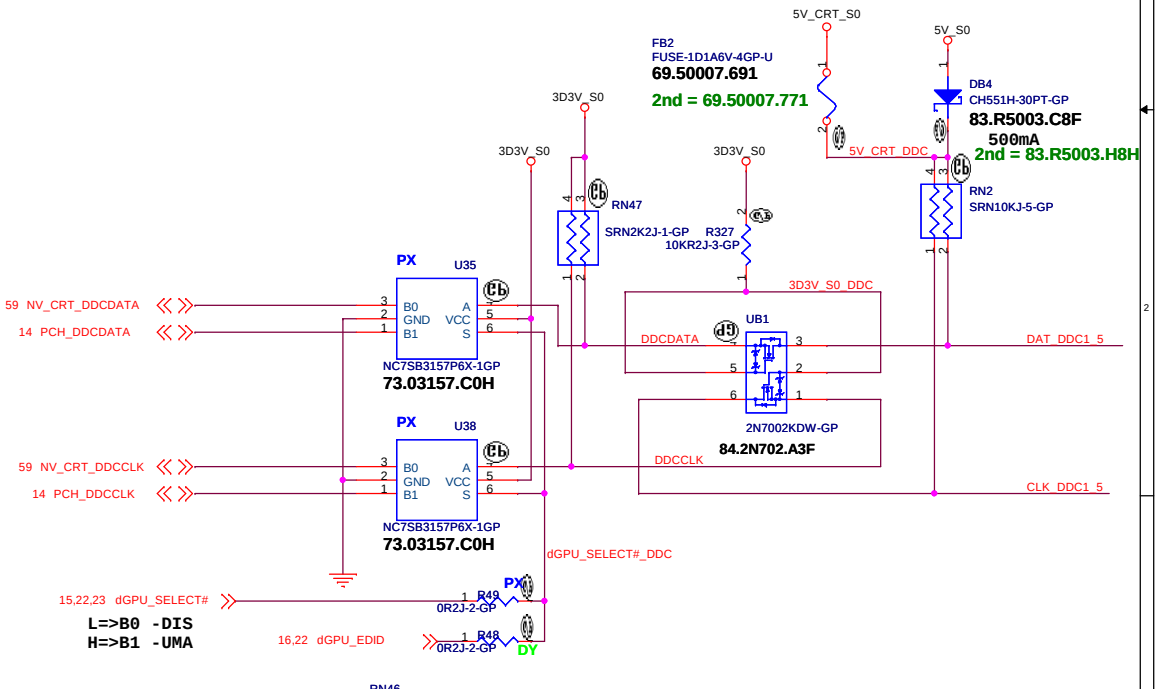
6 1 7 2 8 3 9 4 10 5

Hsync & Vsync level shift

L=>B0 -UMA
H=>B1 -DIS



DDC_CLK & DATA level shift



SJV50

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT CONN**

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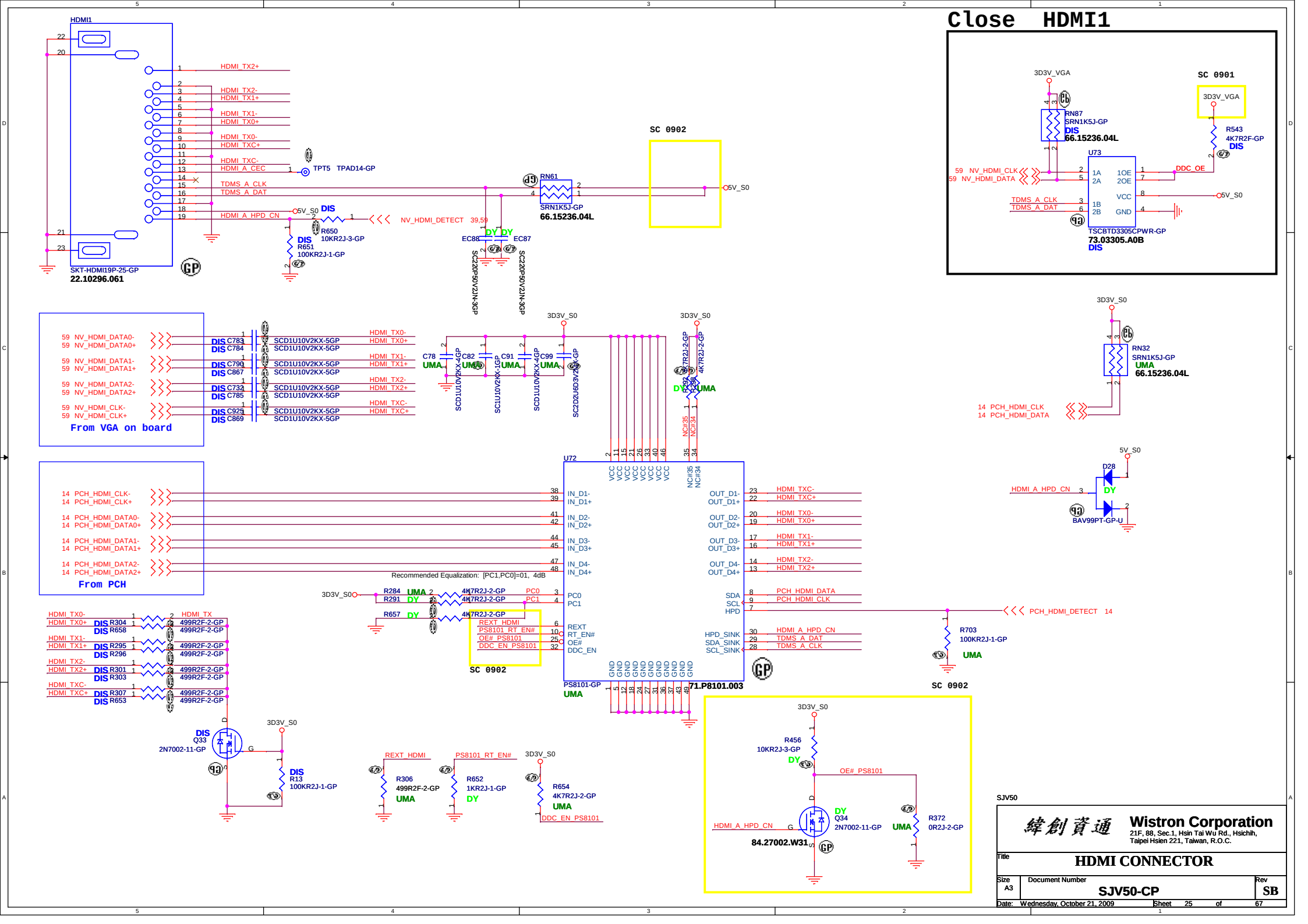
Close HDMI1
HDMI1
SKT-HDMI19P-25-GP
22.10296.061
HDMI_TX2+
HDMI_TX2-
HDMI_TX1+
HDMI_TX1-
HDMI_TX0+
HDMI_TX0-
HDMI_TXC+
HDMI_TXC-
HDMI_A_CEC
TPT5 TPAD14-GP
TDMS_A_CLK
TDMS_A_DAT
HDMI_A_HPD_CN
5V_S0
DIS
R650 10KR2J-3-GP
R651 100KR2J-1-GP
NV_HDMI_DETECT 39,59
SC 0902
RN61
SRN1K5J-GP
66.15236.04L
EC88
EC87
SC220P50V2JN-3GP
SC 0901
3D3V_VGA
RN87 SRN1K5J-GP
R543 4K7R2F-GP
U73
TSCBTD3305CPWR-GP
73.03305.A0B
59 NV_HDMI_CLK
59 NV_HDMI_DATA
DDC_OE
From VGA on board
59 NV_HDMI_DATA0-
59 NV_HDMI_DATA0+
59 NV_HDMI_DATA1-
59 NV_HDMI_DATA1+
59 NV_HDMI_DATA2-
59 NV_HDMI_DATA2+
59 NV_HDMI_CLK-
59 NV_HDMI_CLK+
SCD1U10V2KX-5GP
C783
C784
C790
C867
C732
C785
C925
C869
C78
C82
C91
C99
SC1U10V2KX-1GP
SC2D2U6D3V2KX-GP
4K7R2J-2-GP
UMA
DY
3D3V_S0
RN32 SRN1K5J-GP 66.15236.04L
14 PCH_HDMI_CLK
14 PCH_HDMI_DATA
From PCH
14 PCH_HDMI_CLK-
14 PCH_HDMI_CLK+
14 PCH_HDMI_DATA0-
14 PCH_HDMI_DATA0+
14 PCH_HDMI_DATA1-
14 PCH_HDMI_DATA1+
14 PCH_HDMI_DATA2-
14 PCH_HDMI_DATA2+
U72
PS8101-GP
71.P8101.003
IN_D1-
IN_D1+
IN_D2-
IN_D2+
IN_D3-
IN_D3+
IN_D4-
IN_D4+
OUT_D1-
OUT_D1+
OUT_D2-
OUT_D2+
OUT_D3-
OUT_D3+
OUT_D4-
OUT_D4+
HDMI_TXC-
HDMI_TXC+
HDMI_TX0-
HDMI_TX0+
HDMI_TX1-
HDMI_TX1+
HDMI_TX2-
HDMI_TX2+
SDA
SCL
HPD
PCH_HDMI_DATA
PCH_HDMI_CLK
HPD_SINK
SDA_SINK
SCL_SINK
HDMI_A_HPD_CN
TDMS_A_DAT
TDMS_A_CLK
Recommended Equalization: [PC1,PC0]=01, 4dB
PC0
PC1
REXT
RT_EN#
OE#
DDC_EN
REXT_HDMI
PS8101_RT_EN#
OE#_PS8101
DDC_EN_PS8101
R284
R291
R657
4K7R2J-2-GP
SC 0902
PCH_HDMI_DETECT 14
R703 100KR2J-1-GP
D28
BAV99PT-GP-U
HDMI_TX0-
HDMI_TX0+
HDMI_TX1-
HDMI_TX1+
HDMI_TX2-
HDMI_TX2+
HDMI_TXC-
HDMI_TXC+
R304
R658
R295
R296
R301
R303
R307
R653
499R2F-2-GP
Q33
2N7002-11-GP
R13 100KR2J-1-GP
R306 499R2F-2-GP
R652 1KR2J-1-GP
R654 4K7R2J-2-GP
R456 10KR2J-3-GP
Q34 2N7002-11-GP
R372 0R2J-2-GP
84.27002.W31
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI CONNECTOR
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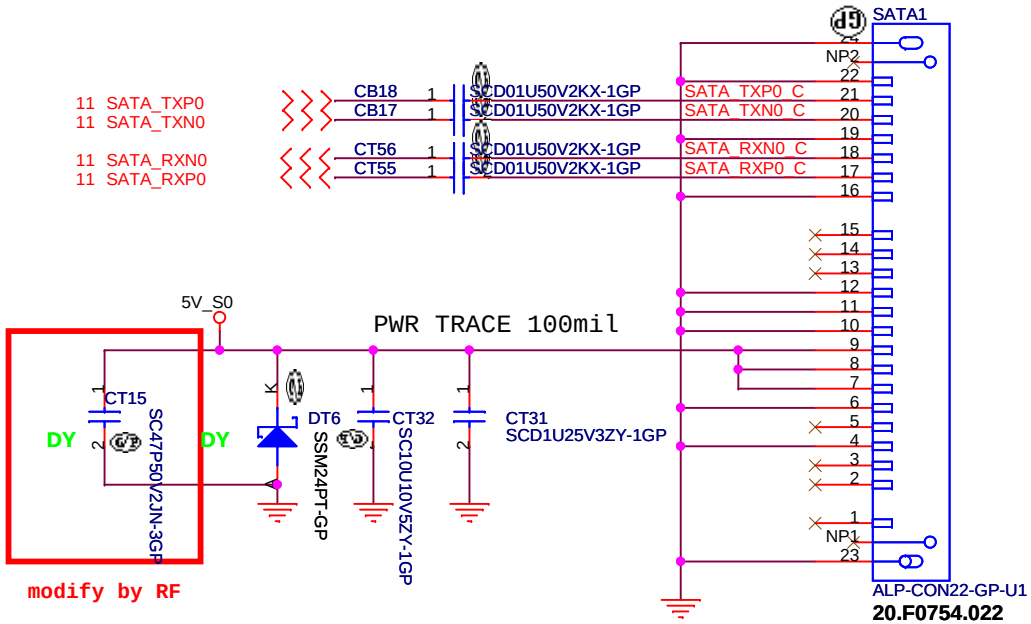
SATA Connector



SJV50

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD CONN	
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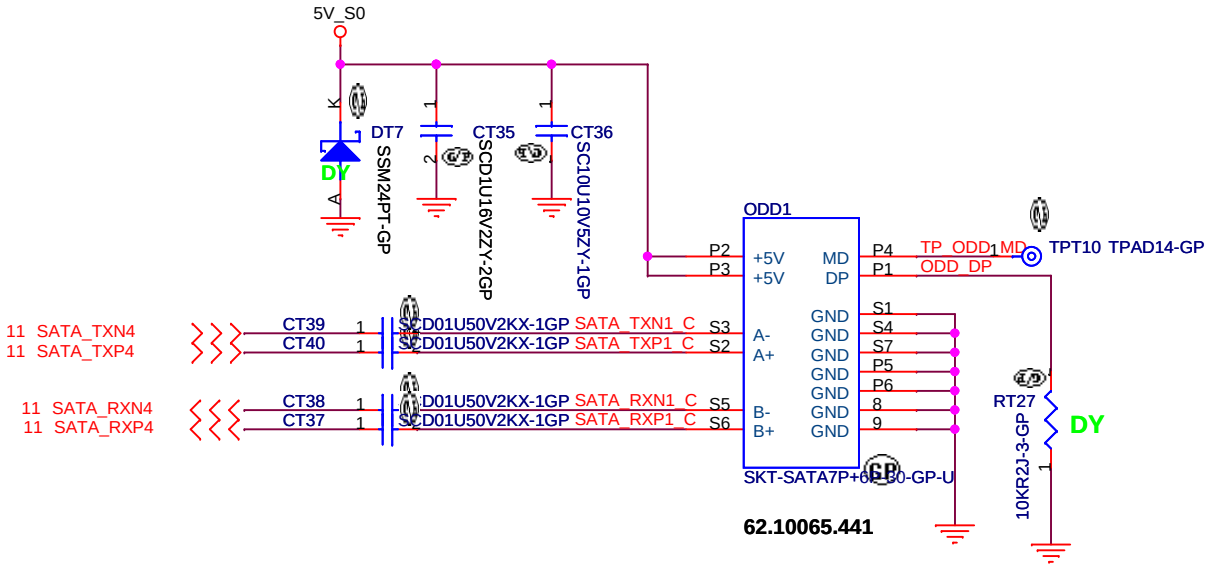
ODD Connector



SJV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ODD		
Size	Document Number: SJV50-CP	Rev: SB
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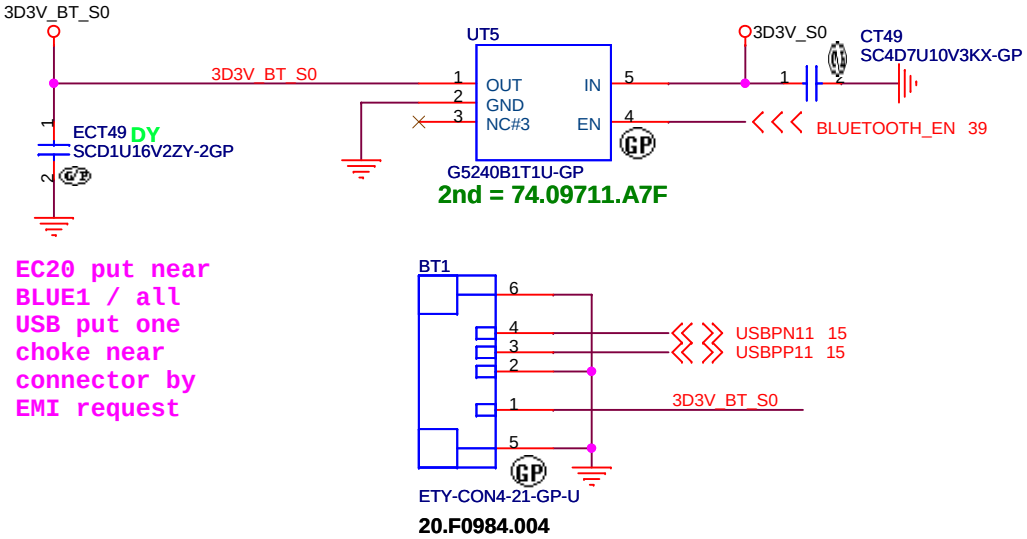
BLUETOOTH MODULE



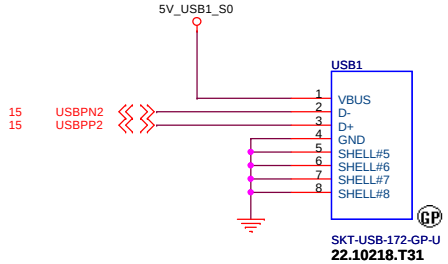
SJV50

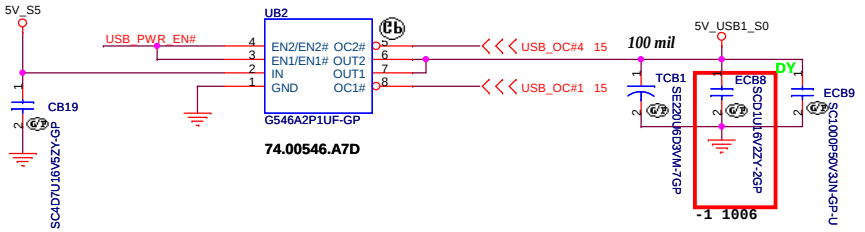
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

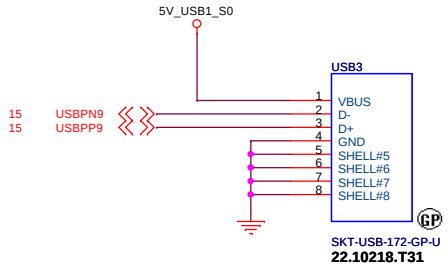
Title: BLUETOOTH

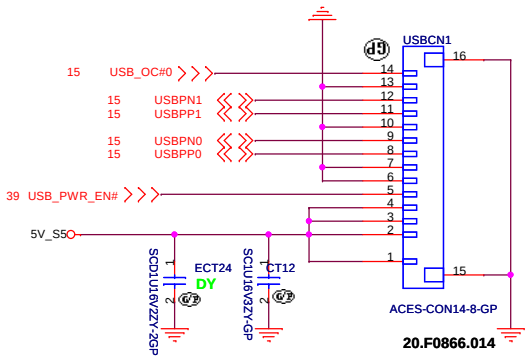
Size	Document Number	Rev
	SJV50-CP	SB

Date: Wednesday, October 21, 2009 Sheet 28 of 67



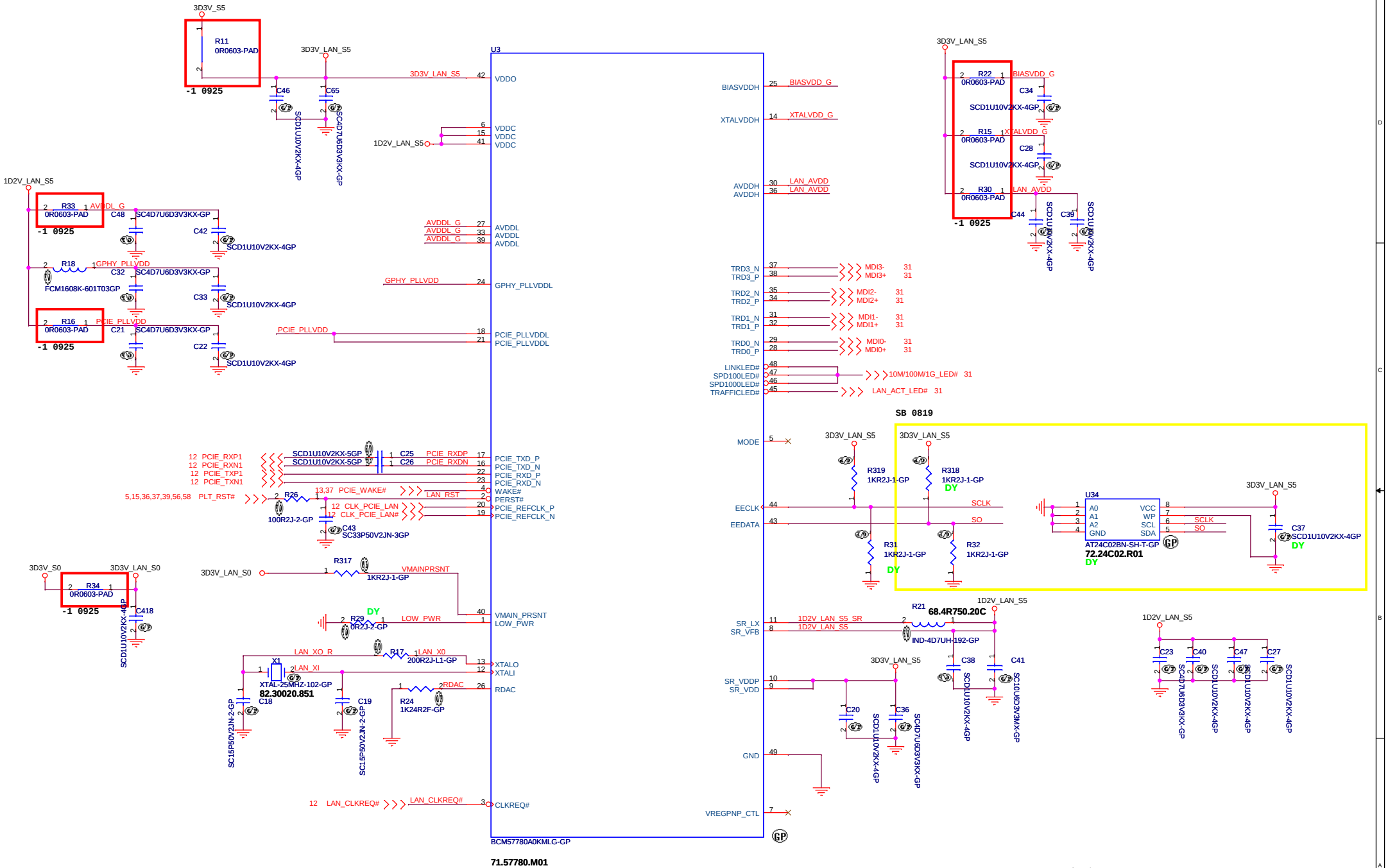






SJV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*USB CONN*	
Size	Document Number SJV50-CP	Rev SB
Date: Wednesday, October 21, 2009	Sheet 29 of 67	


U3
BCM57780A0KMLG-GP
71.57780.M01
SB 0819
3D3V_S5
3D3V_LAN_S5
1D2V_LAN_S5
3D3V_S0
3D3V_LAN_S0
R11 0R0603-PAD -1 0925
R33 0R0603-PAD -1 0925
R18 FCM1608K-601T03GP
R16 0R0603-PAD -1 0925
R34 0R0603-PAD -1 0925
R22 0R0603-PAD
R15 0R0603-PAD
R30 0R0603-PAD -1 0925
R26 100R2J-2-GP
R317 1KR2J-1-GP
R29 0R2J-2-GP
R17 200R2J-L1-GP
R24 1K24R2F-GP
R319 1KR2J-1-GP
R318 1KR2J-1-GP DY
R31 1KR2J-1-GP DY
R32 1KR2J-1-GP
R21 68.4R750.20C
IND-4D7UH-192-GP
X1 XTAL-25MHZ-102-GP 82.30020.851
U34 AT24C02BN-SH-T-GP 72.24C02.R01 DY
C46 C65 C48 C42 C32 C33 C21 C22 C34 C28 C44 C39 C418 C18 C19 C43 C25 C26 C20 C36 C38 C41 C23 C40 C47 C27 C37
SCD1U10V2KX-4GP
SC4D7U6D3V3KX-GP
SC33P50V2JN-3GP
SC15P50V2JN-2-GP
SC1U6D3V3MX-GP
VDDO
VDDC
VDDC
VDDC
AVDDL
AVDDL
AVDDL
GPHY_PLLVDDL
PCIE_PLLVDDL
PCIE_PLLVDDL
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
WAKE#
PERST#
PCIE_REFCLK_P
PCIE_REFCLK_N
VMAIN_PRSNT
LOW_PWR
XTALO
XTALI
RDAC
CLKREQ#
BIASVDDH
XTALVDDH
AVDDH
AVDDH
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
MODE
EECLK
EEDATA
SR_LX
SR_VFB
SR_VDDP
SR_VDD
GND
VREGPNP_CTL
BIASVDD_G
XTALVDD_G
LAN_AVDD
LAN_AVDD
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
10M/100M/1G_LED#
LAN_ACT_LED#
SCLK
SO
SCL
SDA
VCC
WP
A0
A1
A2
GND
PCIE_RXP1
PCIE_RXN1
PCIE_TXP1
PCIE_TXN1
PLT_RST#
CLK_PCIE_LAN
CLK_PCIE_LAN#
LAN_RST
LAN_XO_R
LAN_XI
LAN_X0
LAN_CLKREQ#
1D2V_LAN_S5_SR
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM57780
Size Custom
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Date: Wednesday, October 21, 2009
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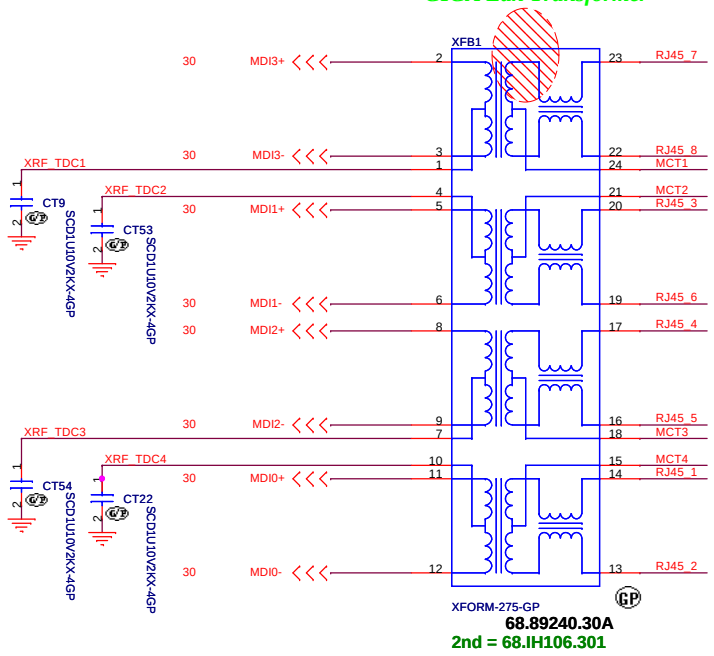
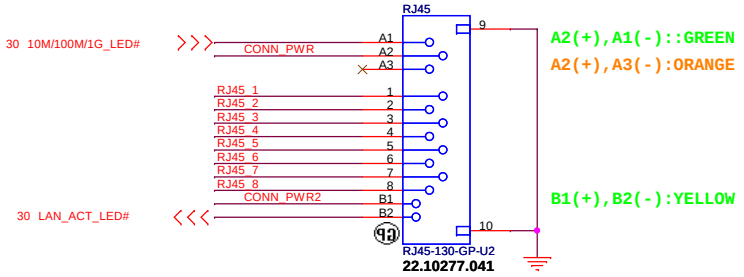
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

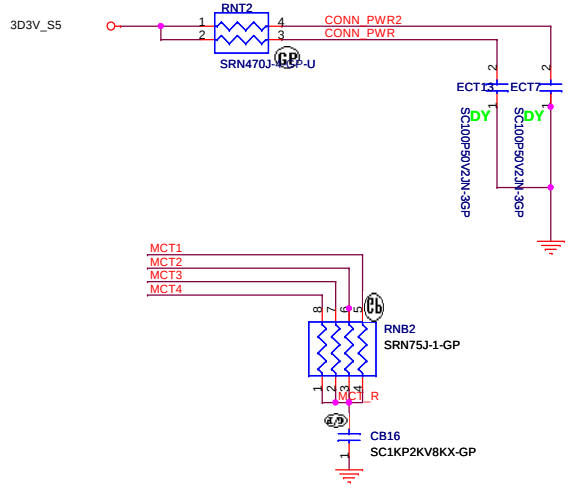
LAN Connector

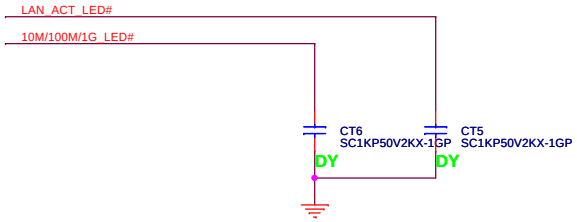
LAN Connector

GIGA Lan Transformer





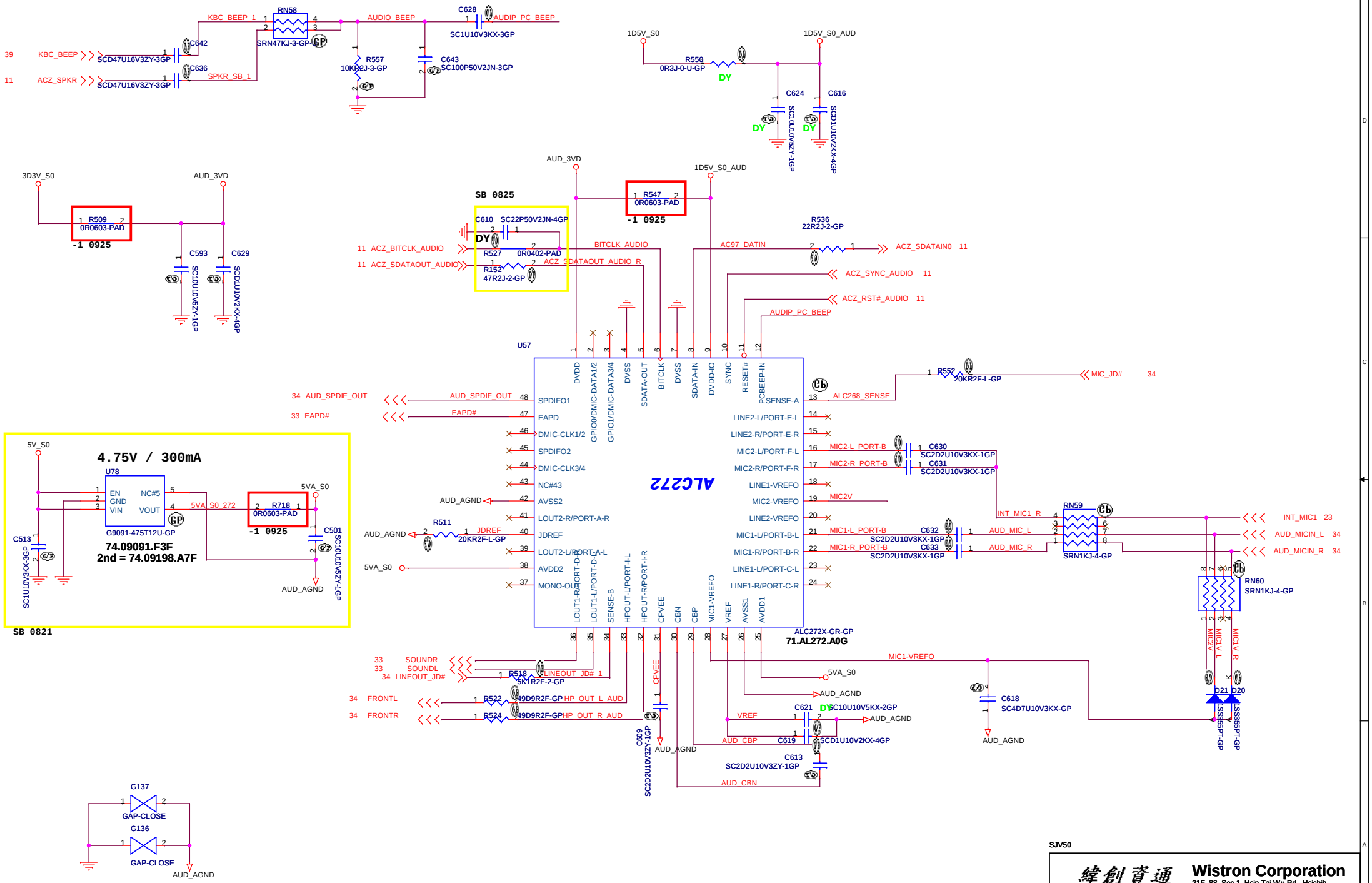




SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**		
Size: A3	Document Number: SJV50-CP	Rev: SB
Date: Wednesday, October 21, 2009	Sheet 31 of 67	

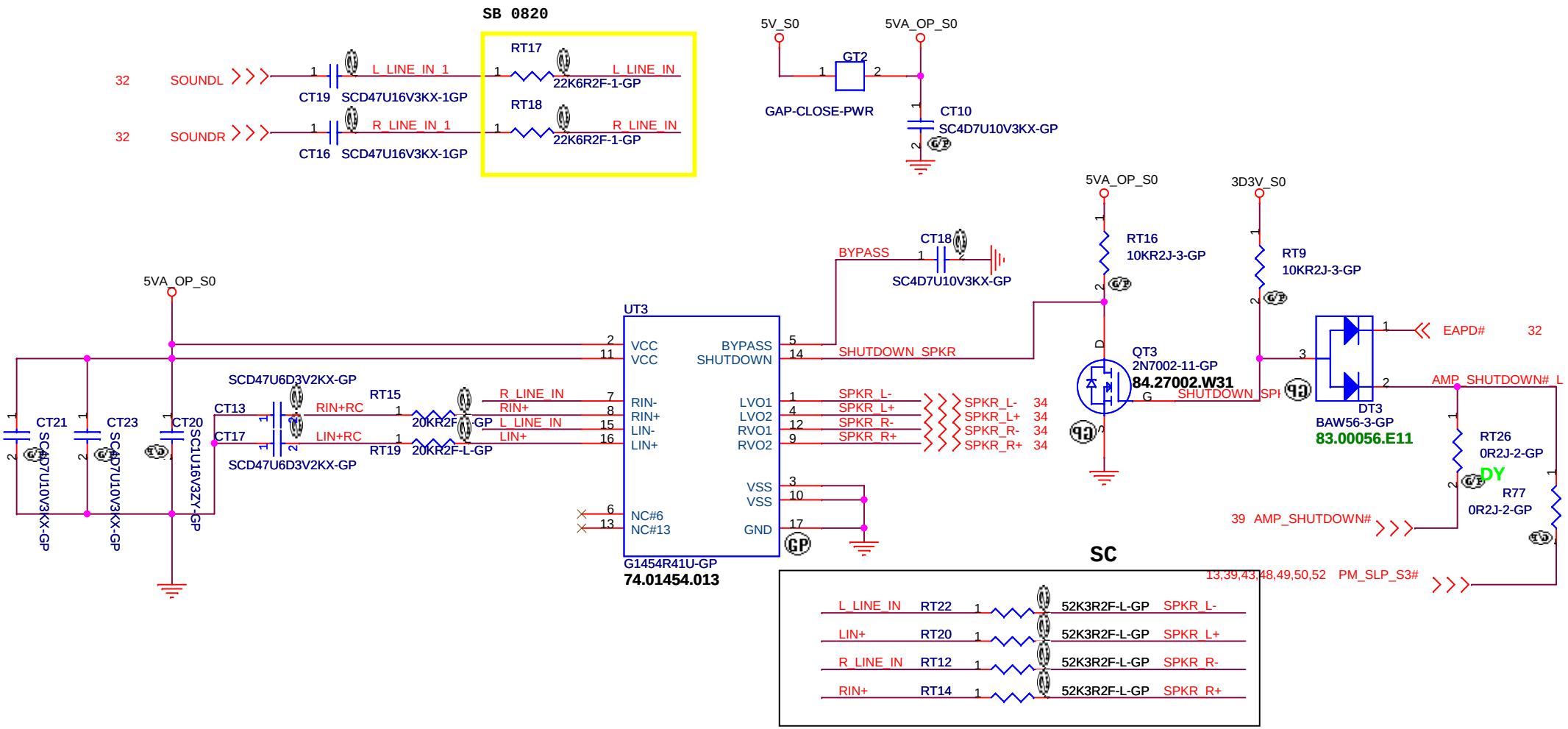


SJV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Azalia codec ALC272*		
Size: A3	Document Number: SJV50-CP	Rev: SB
Date: Wednesday, October 21, 2009	Sheet 32 of 67	

AUDIO OP AMPLIFIER



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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO AMP AND JACK*

Size	Document Number	Rev
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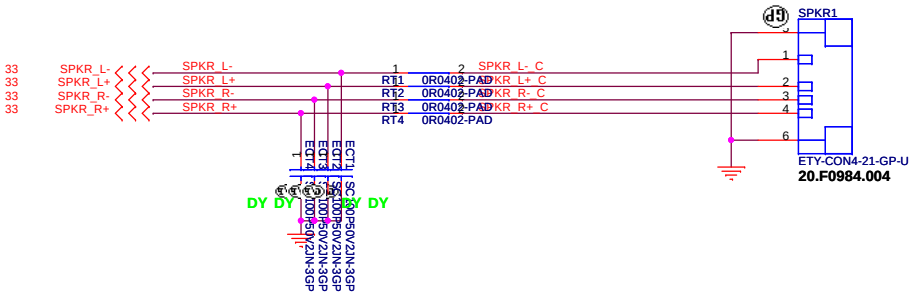
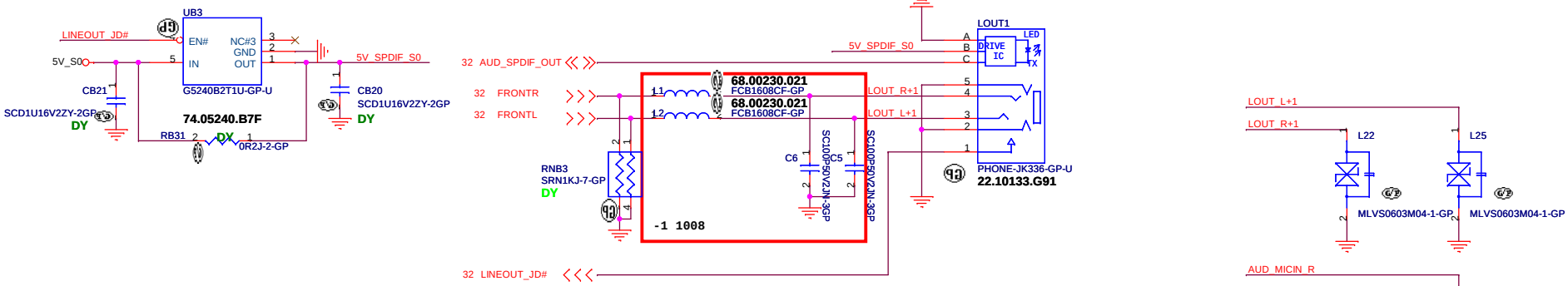
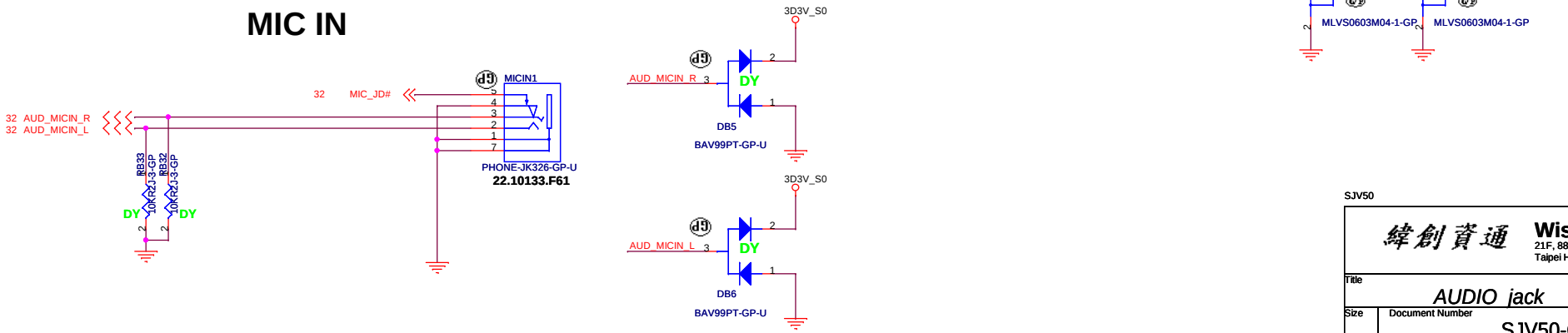
Internal Speaker



LINE OUT

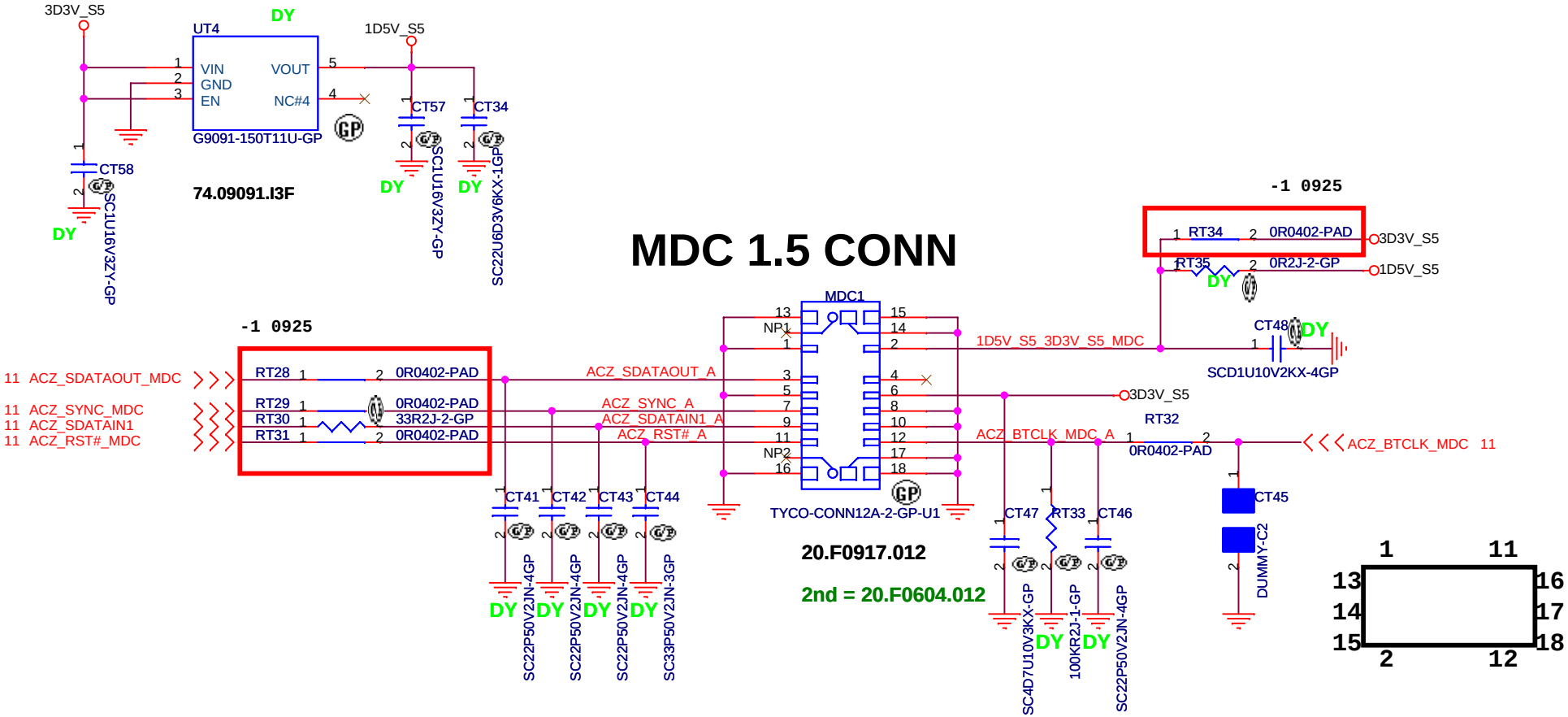


MIC IN



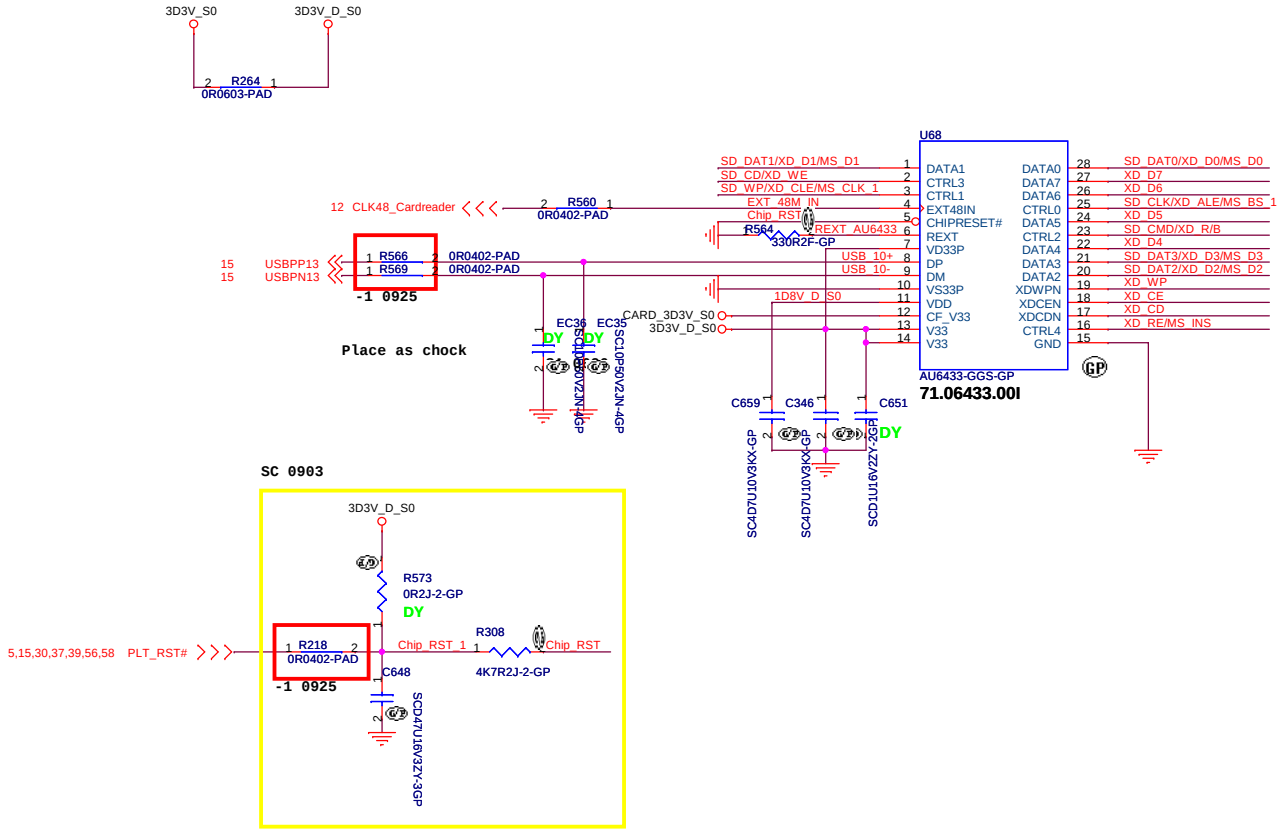
SJV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO jack*	
Size	Document Number: SJV50-CP	Rev: SB
Date: Wednesday, October 21, 2009	Sheet 34 of 67	

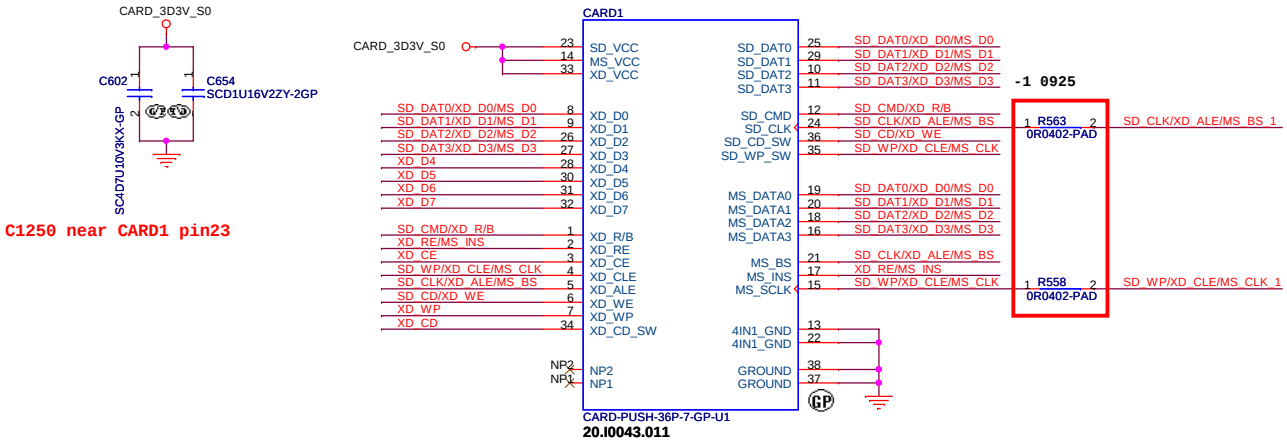


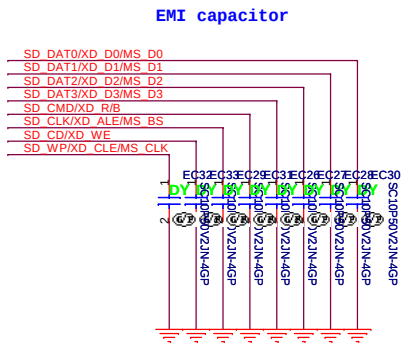
SJV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MDC***	
Size	Document Number **SJV50-CP**	Rev SB
Date: Wednesday, October 21, 2009	Sheet 35 of	67



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)





SJV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *Cardreader*		
Size	Document Number: SJV50-CP	Rev: SB
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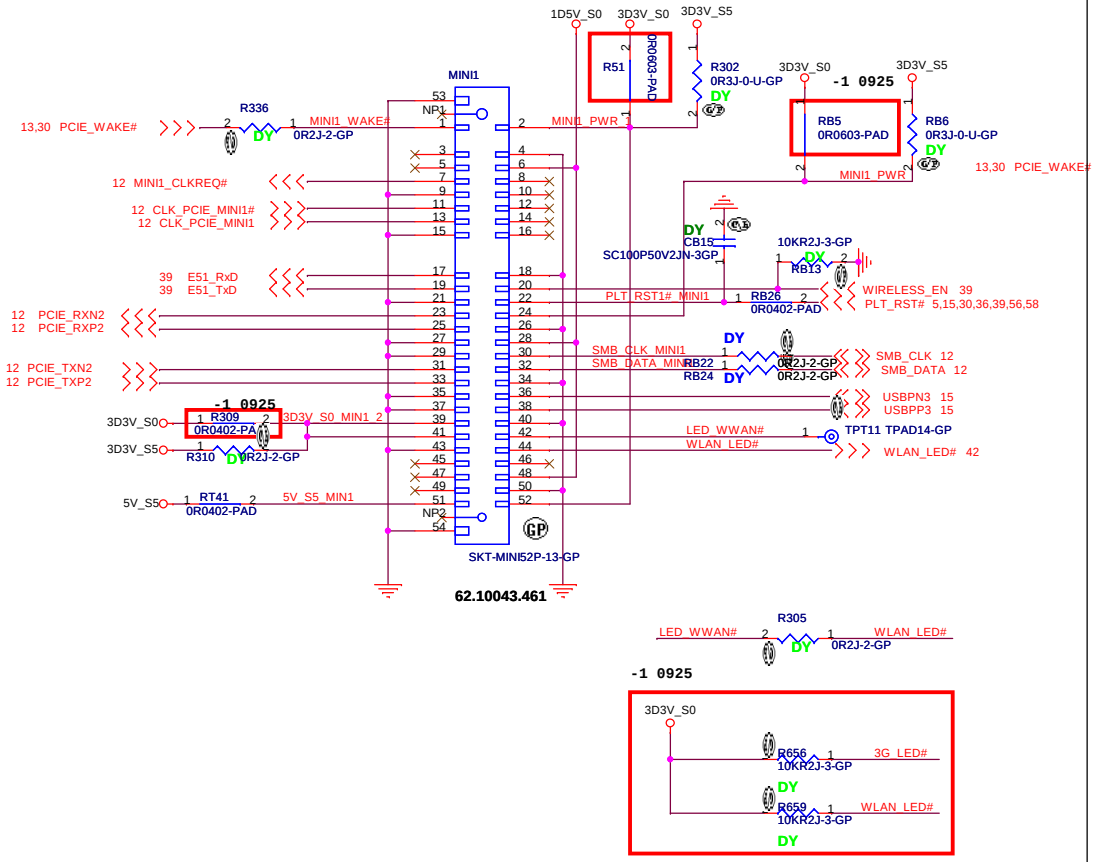
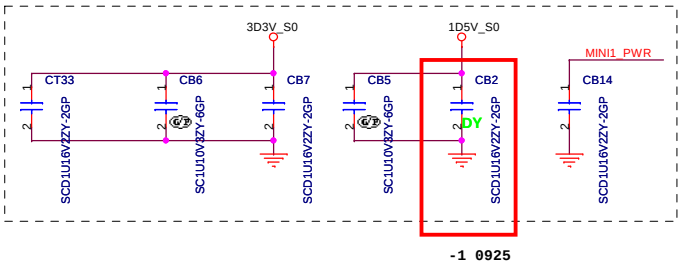
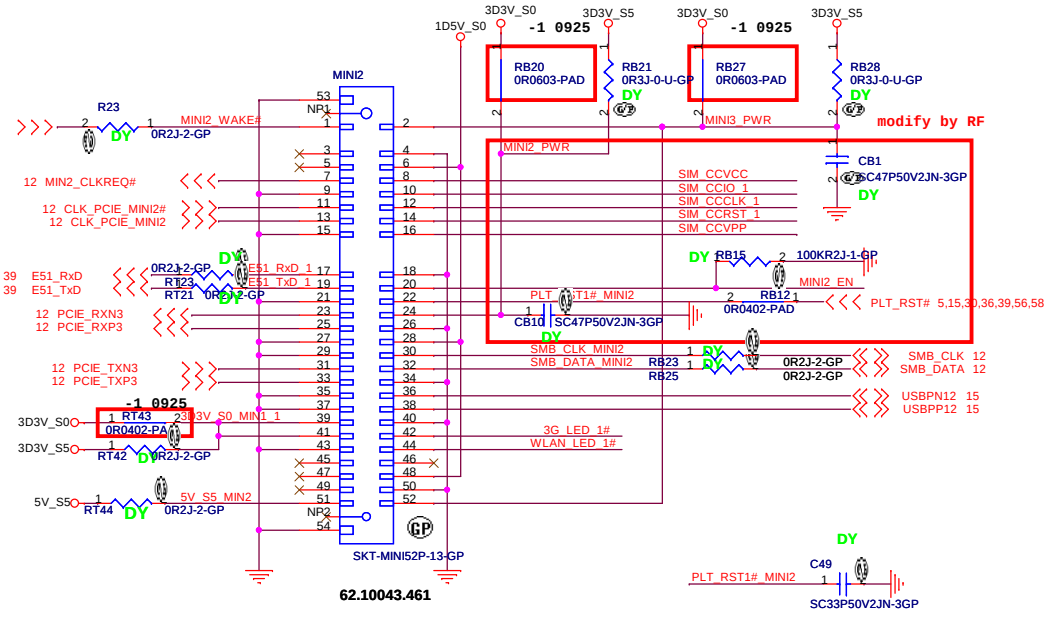
Mini Card Connector(WLAN) Half Card
Support debug-card



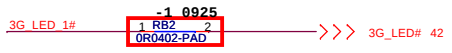
Place near MINI1



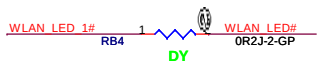
Mini Card Connector(Robson2 and 3G)



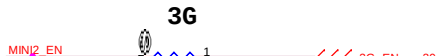
3G



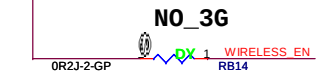
NO_3G



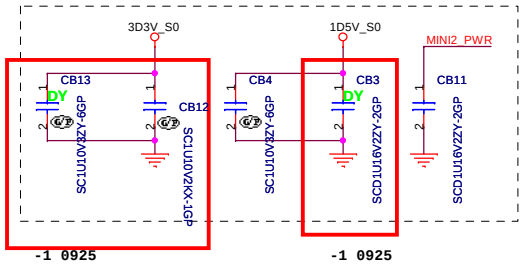
3G

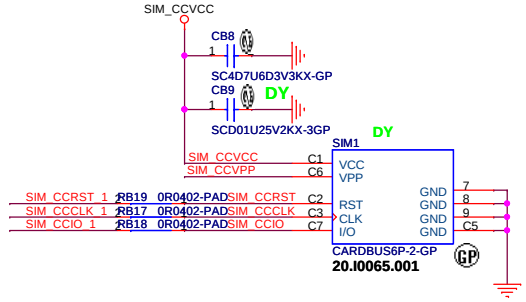


NO_3G



Place near MINIC2





SJV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size: A3	Document Number: SJV50-CP	Rev: SB
Date: Wednesday, October 21, 2009	Sheet 37 of 67	

for T8 thermal diode

84.T3904.C11

2nd = 84.03904.P11

Q3 MMBT3904-4-GP

C118 SC2200P50V2KX-2GP

G787_DP2

G787_DN2

C1252 & C1254 CLOSE TO G787

for system thermal diode

84.T3904.C11

2nd = 84.03904.P11

Q15 MMBT3904-4-GP

C326 SC2200P50V2KX-2GP

G787_DP1

G787_DN1

3D3V_S0

3D3V_AUX_S5

RN23 SRN10KJ-7GP

-1 0929

RSMRST#_CTRL

Q11

RSMRST#

PURE_HW_SHUTDOWN#

2N7002-11-GP

2ND = 84.27002.N31

D7 BAT54PT-GP

2ND = 83.BAT54.D81

83.00054.T81

DY

C544 SCD1U16V2ZY-2GP

RSMRST# 39,43

(dummy, KBC already delay)

5V_S0

R426 100R2J-2-GP

C532 SCD1U16V2KX-3GP

5V_S0_THERMAL

C147 SC10U6D3V3MX-GP

U15

VCC DVCC DP2DN3 DN2DP3 DXP1 SGND1 NC#1 NC#3 NC#12

SDA SCL THERM_SET THERM# ALERT# TEST GND

G787S11U-GP

74.00787.0B9

SMBD_THERM 39,42,59

SMBC_THERM 39,42,59

THERM_SET

PURE_HW_SHUTDOWN#

ALERT#

R183 10KR2J-3-GP

TP28

TP49 TPAD14-GP

R429 21KR2F-GP

R430 49K9R2F-L-GP

T8=90C

THERM_SET = [(Tset-72) x 0.02+0.34] x VCC

39 FAN_TACH1

R350 0R2J-2-GP DY

R351 10KR2J-3-GP DY

D15 RB551V30-GP

83.R5003.H8H

2ND = 83.5R003.08F

-1 0925

39 FAN1_PWM

R106 0R0402-PAD

SCD1U16V2ZY-2GR

EC7 DY

SC 0902

FAN1_PWM_R

FAN_TACH1_D

FAN1

ACES-CON4-GP-U1

20.F0714.004

2ND = 20.D0196.104

For CPU FAN

C450 SC10U10V2ZY-1GP

D14 RB551V30-GP

2ND = 83.5R003.08F

83.R5003.H8H

SJV50

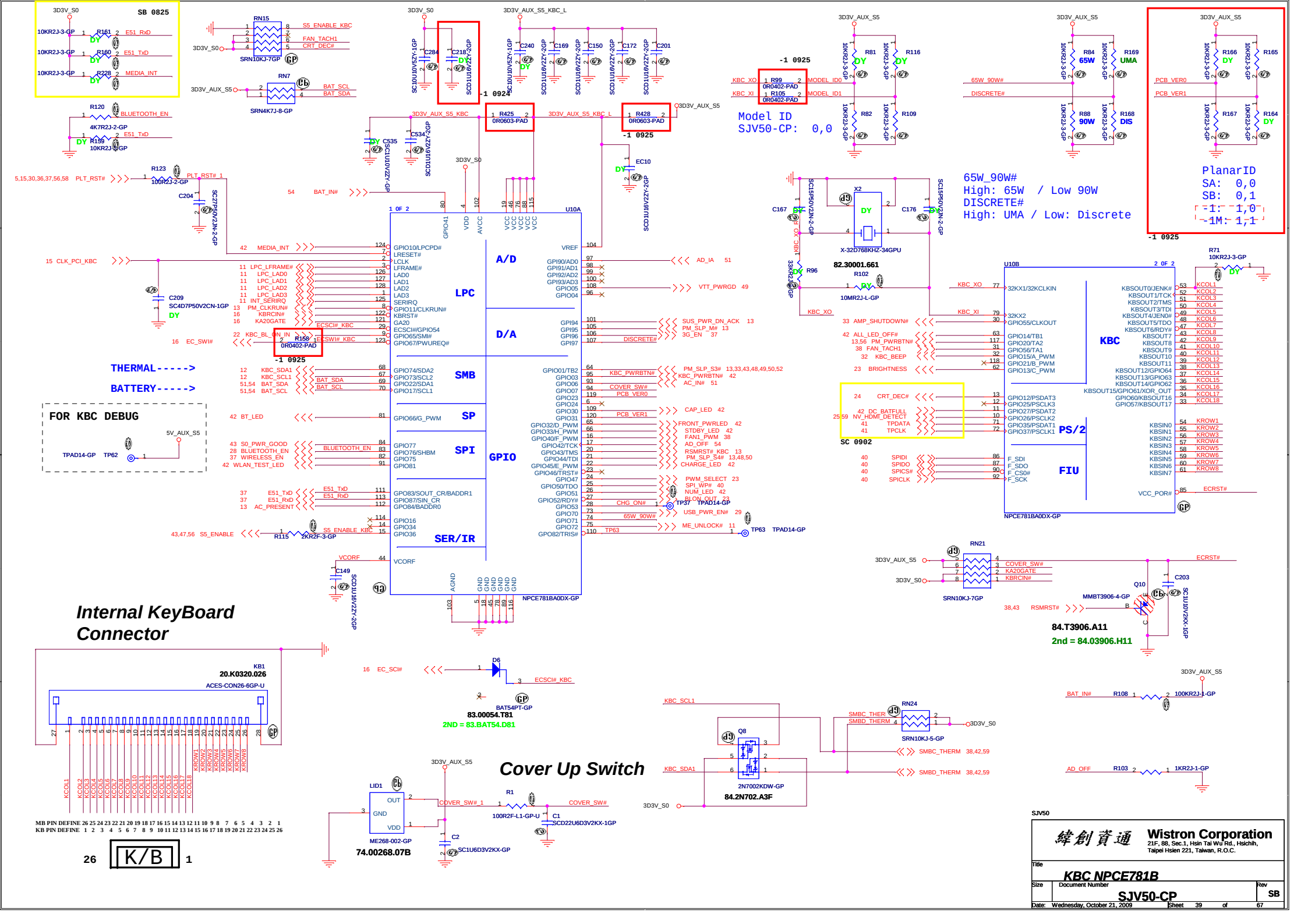
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Connector

Size: | Document Number: SJV50-CP | Rev: SB

Date: Wednesday, October 21, 2009 | Sheet 38 of 67


SB 0825
Internal KeyBoard Connector
KB1
20.K0320.026
ACES-CON26-6GP-U
Cover Up Switch
LID1
ME268-002-GP
74.00268.07B
Model ID
SJV50-CP: 0,0
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
-1 0925
U10A
NPCE781BA0DX-GP
U10B
NPCE781BA0DX-GP
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
THERMAL----->
BATTERY----->
FOR KBC DEBUG
82.30001.661
X-32D768KHZ-34GPU
84.T3906.A11
2nd = 84.03906.H11
83.00054.T81
2ND = 83.BAT54.D81
84.2N702.A3F
SC 0902
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
26 K/B 1
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC NPCE781B
Size
Document Number
SJV50-CP
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SB
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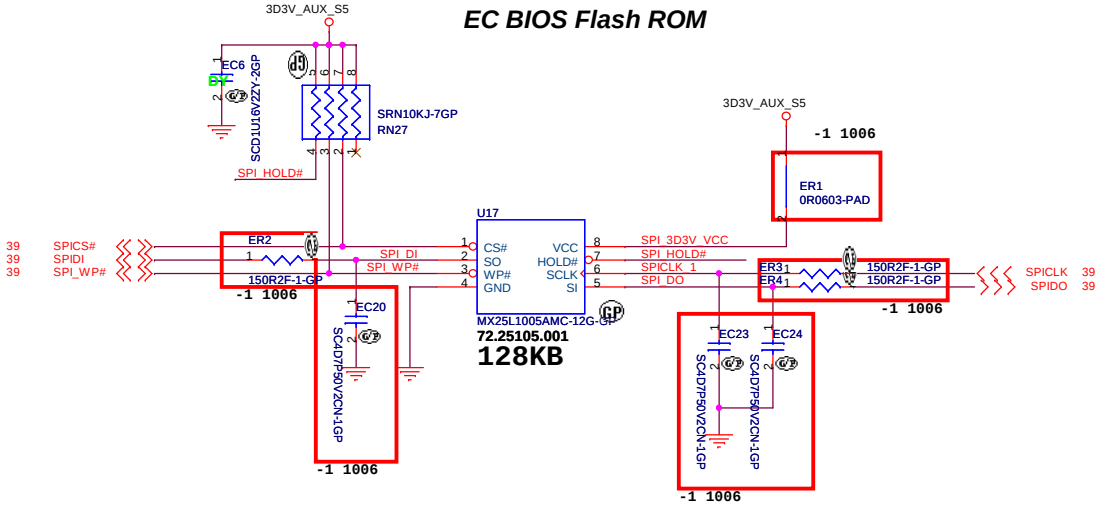
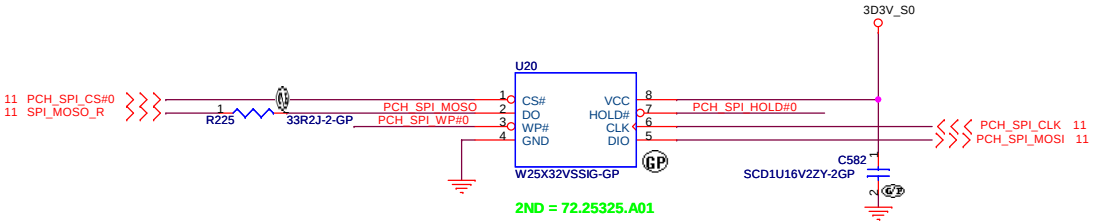
Sheet 39 of 67

EC BIOS Flash ROM



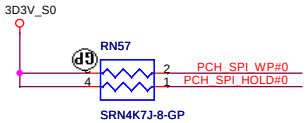
System BIOS Flash ROM



32M Bits

GOLDEN FINGER FOR DEBUG BOARD

-1 1009



SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

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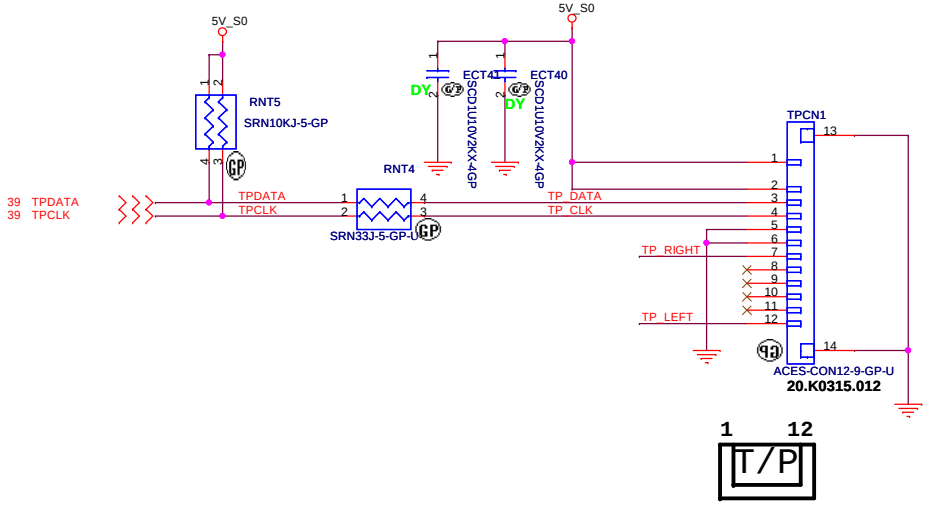
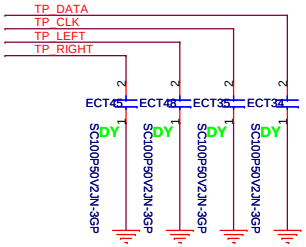
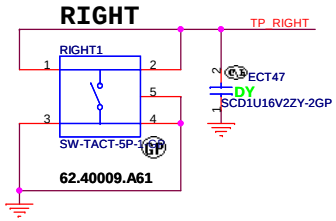
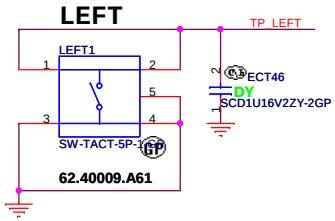
TOUCH PAD









SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch PAD and FP

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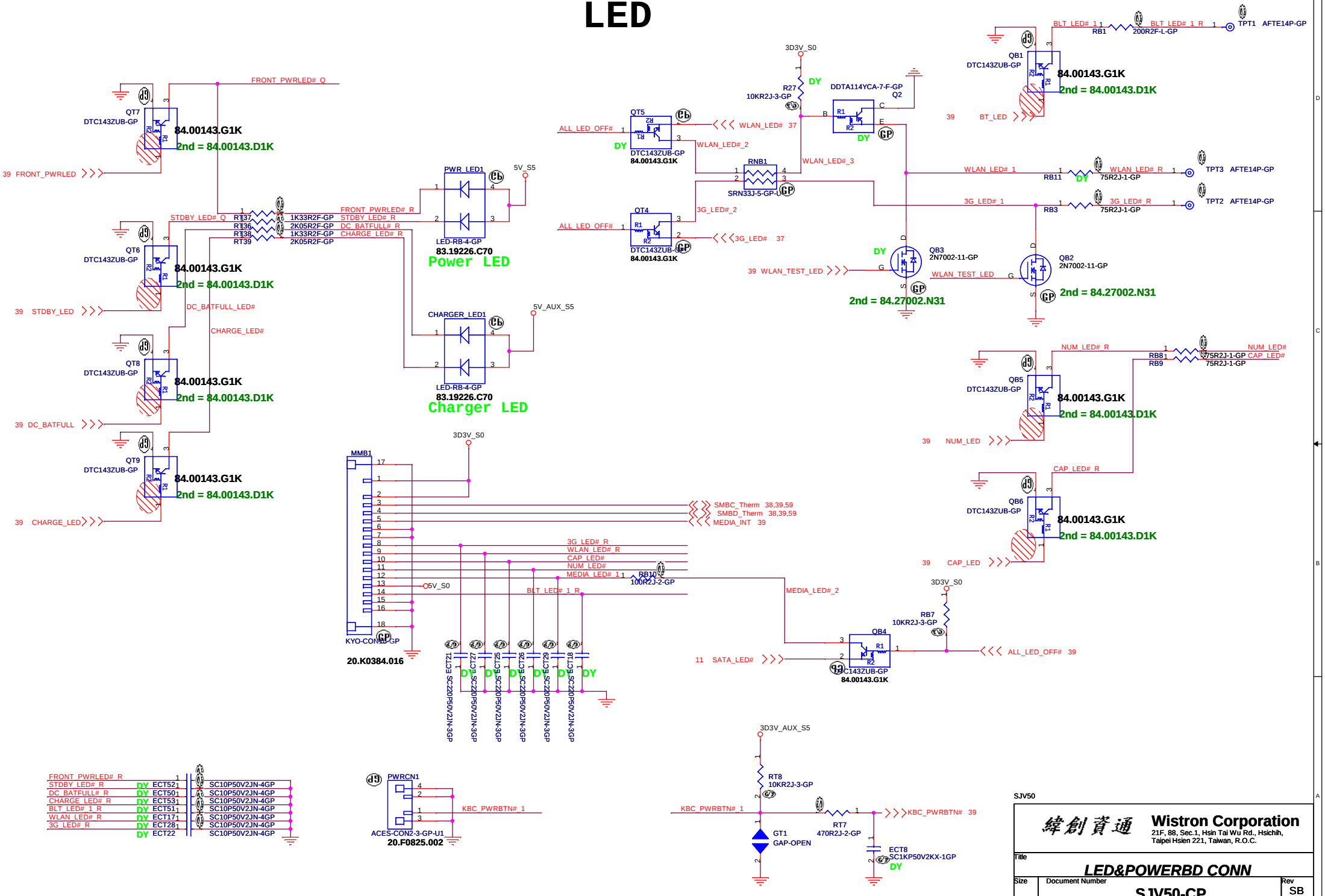
LED

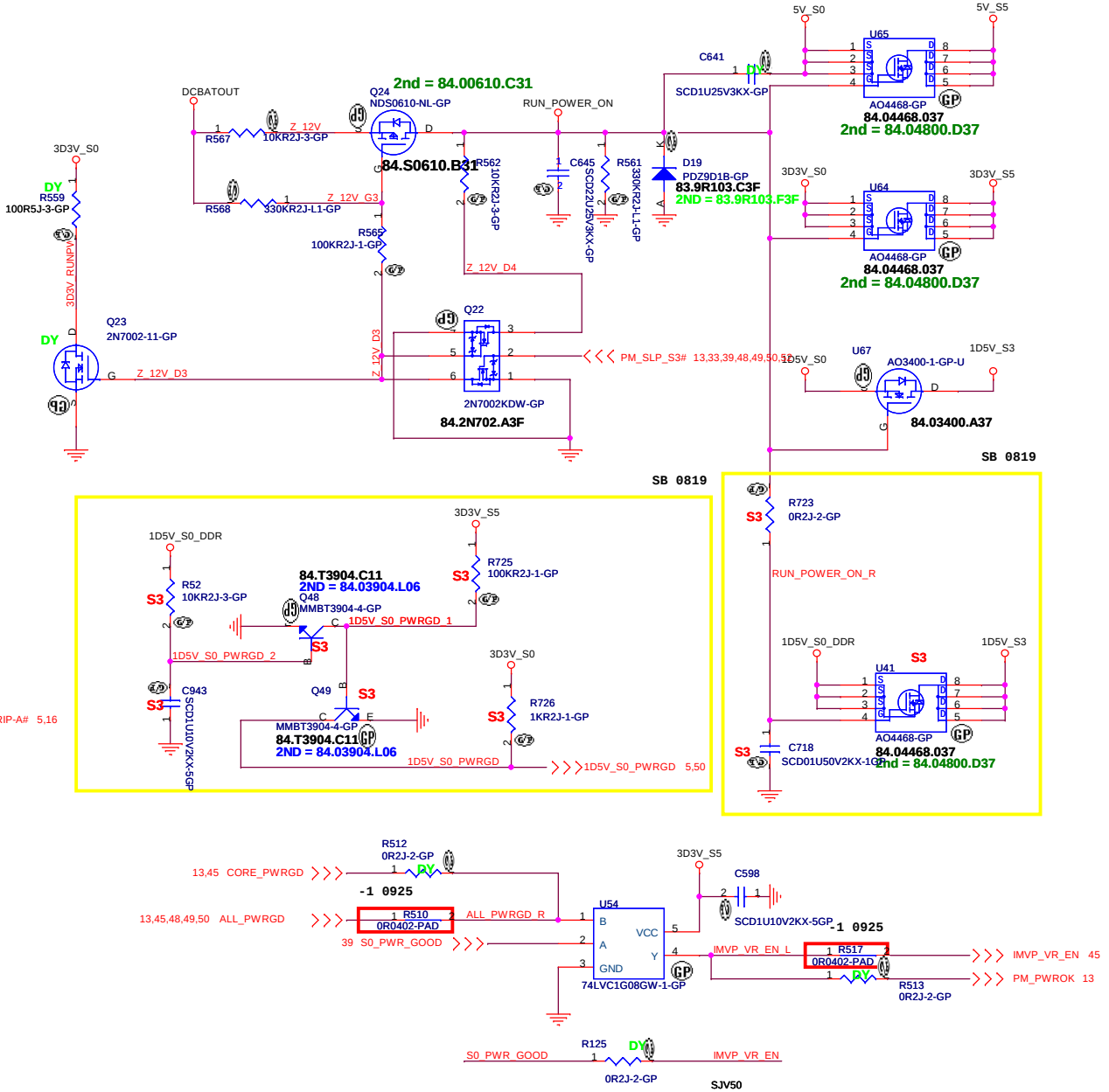


SJV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LED&POWERBD CONN***
Size	Document Number: **SJV50-CP** Rev: SB
Date: Wednesday, October 21, 2009	Sheet 42 of 67

Run Power

-1 1001



SJV50

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Title: RUN POWER and 3D3V_AUX_S5

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ISL62883 VCC_CORE

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6

IMVP_VR_EN

VCC_SENSE
VSS_SENSE

DCBATOUT_62883
5V_S5
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD → CORE_PWRGD

Output Power
VCC_CORE_PWR → VCC_CORE(Imax=65A)

TPS51123 5V/3D3V

DCBATOUT_51123_1
DCBATOUT_51123_2

S5_ENABLE

ALL_PWRGD

Input Power
VIN_1
VIN_2

Input Signal
EN1
EN2

Output Signal
PGOOD

Output Power
5V(O) → 5V_S5 (8A)
3D3V(O) → 3D3V_S5 (6A)
5V_AUX(O) → 5V_AUX_S5 (100mA)
3D3V_AUX(O) → 3D3V_AUX_S5 (100mA)

RT9026 0D75V_S0

5V_S5
1D5V_S3
PM_SLP_S3#
PM_SLP_S4#

VIN
VLDOIN
S3
S5

VTT → 0D75V_S0 (1.2A)
VTTREF → DDR_VREF_S3

RT9025 1D8V

5V_S5
3D3V_S0
PM_SLP_S3#
ALL_PWRGD

VIN
VLDOIN
EN
PGOOD

1D8V (O) → 1D85V_S0

RT9025 1D5V

5V_S5
DCBATOUT_7141_1D5V
PM_SLP_S4#
ALL_PWRGD

Input Power
VDD
VCC

Input Signal
EN

Output Signal
PGOOD

Output Power
1D5V (O) → 1D5V_S3 (10A)

Charger BQ24745

BATT_SENSE
AD+

Input Signal
FBS

Input Power
ACN

Output Signal
ACGOOD# → AC_IN#
SRSET → AD_IA

Output Power
VOUT (O) → BT+
VOUT (O) → DCBATOUT

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O) → AD_IN#

Output Power
VCC(O) → AD+

RT8209B 1D05V

5V_S5
DCBATOUT_RT8209B_1D05V
PM_SLP_S3#
ALL_PWRGD

Input Power
VDD
VCC

Input Signal
EN

Output Signal
PGOOD

Output Power
1D05V (O) → 1D05V_S0 (10A)

SJV50

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Title: **Power Block Diagram**

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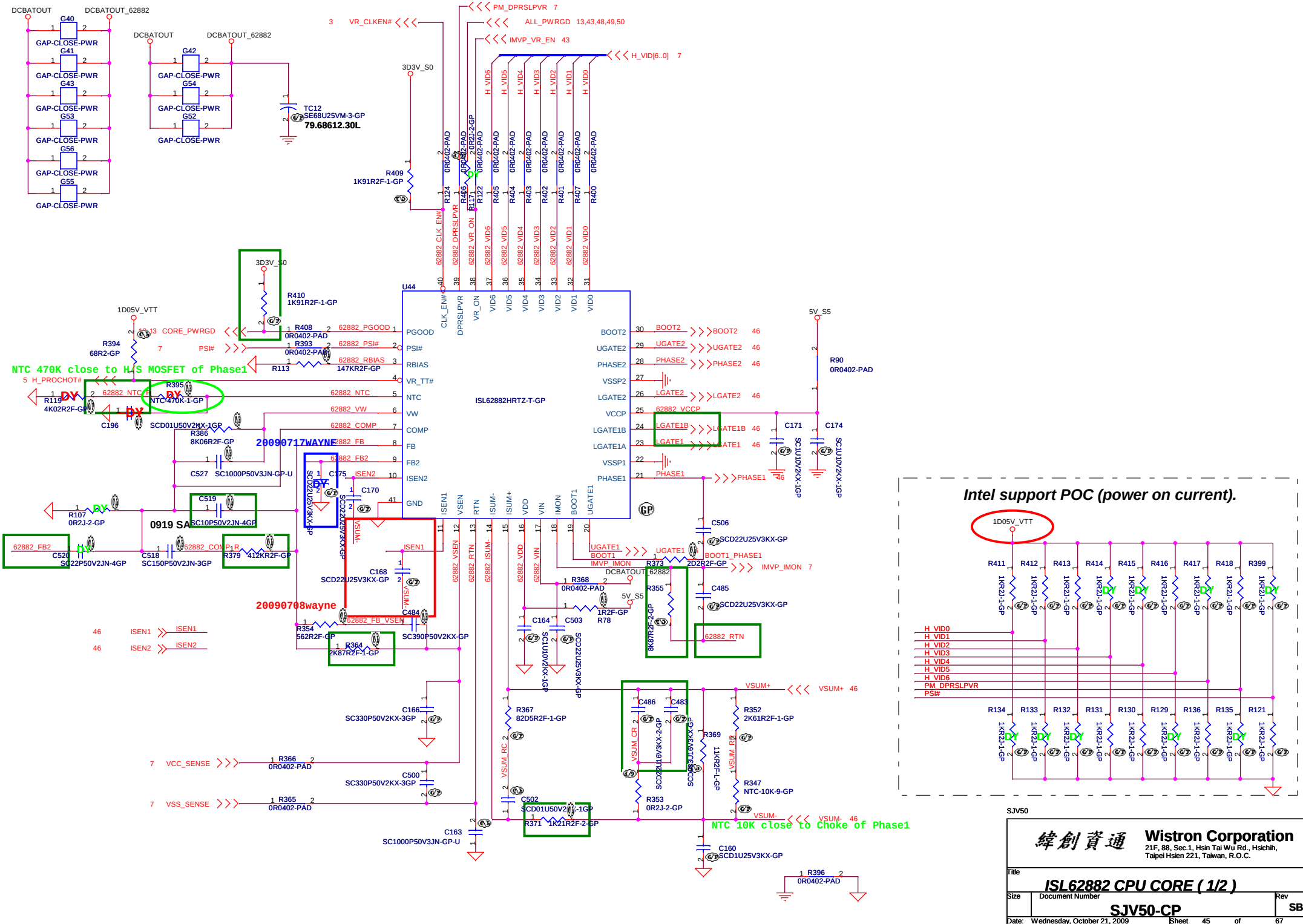
DCBATOUT
DCBATOUT_62882
G40
G41
G43
G53
G56
G55
G42
G54
G52
GAP-CLOSE-PWR
TC12
SE68U25VM-3-GP
79.68612.30L
3D3V_S0
R409
1K91R2F-1-GP
VR_CLKEN#
PM_DPRSLPVR 7
ALL_PWRGD 13,43,48,49,50
IMVP_VR_EN 43
H_VID[6..0] 7
R410
1K91R2F-1-GP
1D05V_VTT
CORE_PWRGD
PSI#
R394
68R2-GP
NTC 470K close to H/S MOSFET of Phase1
H_PROCHOT#
R119
4K02R2F-GP
R395
NTC-470K-1-GP
C196
SCD01U50V2KX-1GP
R386
8K06R2F-GP
C527
SC1000P50V3JN-GP-U
20090717WAYNE
C519
SC10P50V2JN-4GP
0919 SA
R107
0R2J-2-GP
C520
SC22P50V2JN-4GP
C518
SC150P50V2JN-3GP
R379
412KR2F-GP
C175
C170
C168
SCD22U25V3KX-GP
20090708wayne
R354
562R2F-GP
R364
2K87R2F-1-GP
C484
SC390P50V2KX-GP
C166
SC330P50V2KX-3GP
C500
SC330P50V2KX-3GP
R366
0R0402-PAD
R365
0R0402-PAD
VCC_SENSE
VSS_SENSE
C163
SC1000P50V3JN-GP-U
U44
ISL62882HRTZ-T-GP
PGOOD
PSI#
RBIAS
VR_TT#
NTC
VW
COMP
FB
FB2
ISEN2
GND
ISEN1
VSEN
RTN
ISUM-
ISUM+
VDD
VIN
IMON
BOOT1
UGATE1
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
LGATE1B
LGATE1A
VSSP1
PHASE1
CLK_EN#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
VID1
VID0
R408
0R0402-PAD
R393
0R0402-PAD
R113
147KR2F-GP
R124
R406
R117
R122
R405
R404
R403
R402
R401
R407
R400
5V_S5
R90
0R0402-PAD
C171
C174
SC1U10V2KX-1GP
C506
SCD22U25V3KX-GP
R373
2D2R2F-GP
IMVP_IMON 7
R368
0R0402-PAD
R355
C485
SCD22U25V3KX-GP
R78
1R2F-GP
C164
C503
SCD1U10V2KX-1GP
SCD22U25V3KX-GP
8K87R2F-2-GP
62882_RTN
R367
82D5R2F-1-GP
C486
C483
SCD22U16V3KX-2-GP
SCD22U16V3KX-GP
R369
11KR2F-GP
R352
2K61R2F-1-GP
R347
NTC-10K-9-GP
R353
0R2J-2-GP
VSUM+ 46
VSUM- 46
NTC 10K close to Choke of Phase1
C502
SCD01U50V2KX-1GP
R371
1K21R2F-2-GP
C160
SCD1U25V3KX-GP
R396
0R0402-PAD
Intel support POC (power on current).
1D05V_VTT
R411
R412
R413
R414
R415
R416
R417
R418
R399
R134
R133
R132
R131
R130
R129
R136
R135
R121
1KR2J-1-GP
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PM_DPRSLPVR
PSI#
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62882 CPU CORE (1/2)
Size
Document Number
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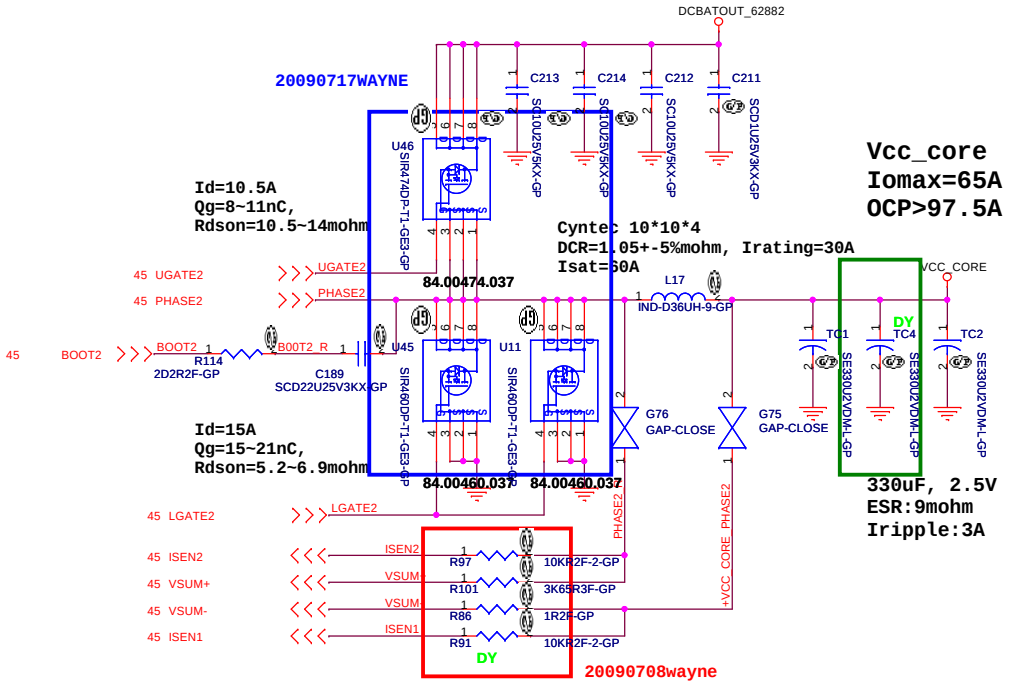

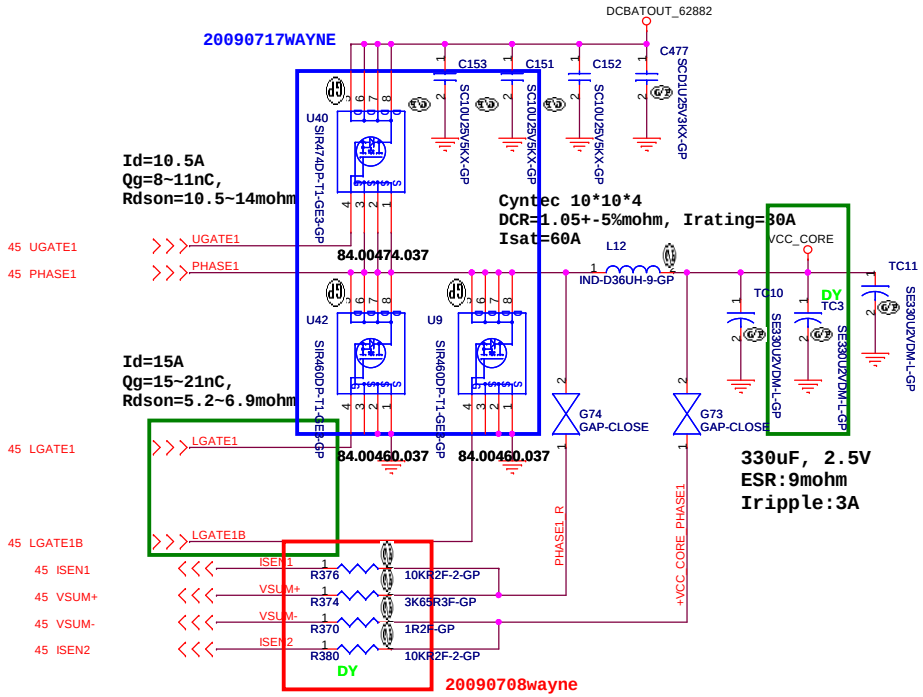

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62882 CPU CORE (1/2)

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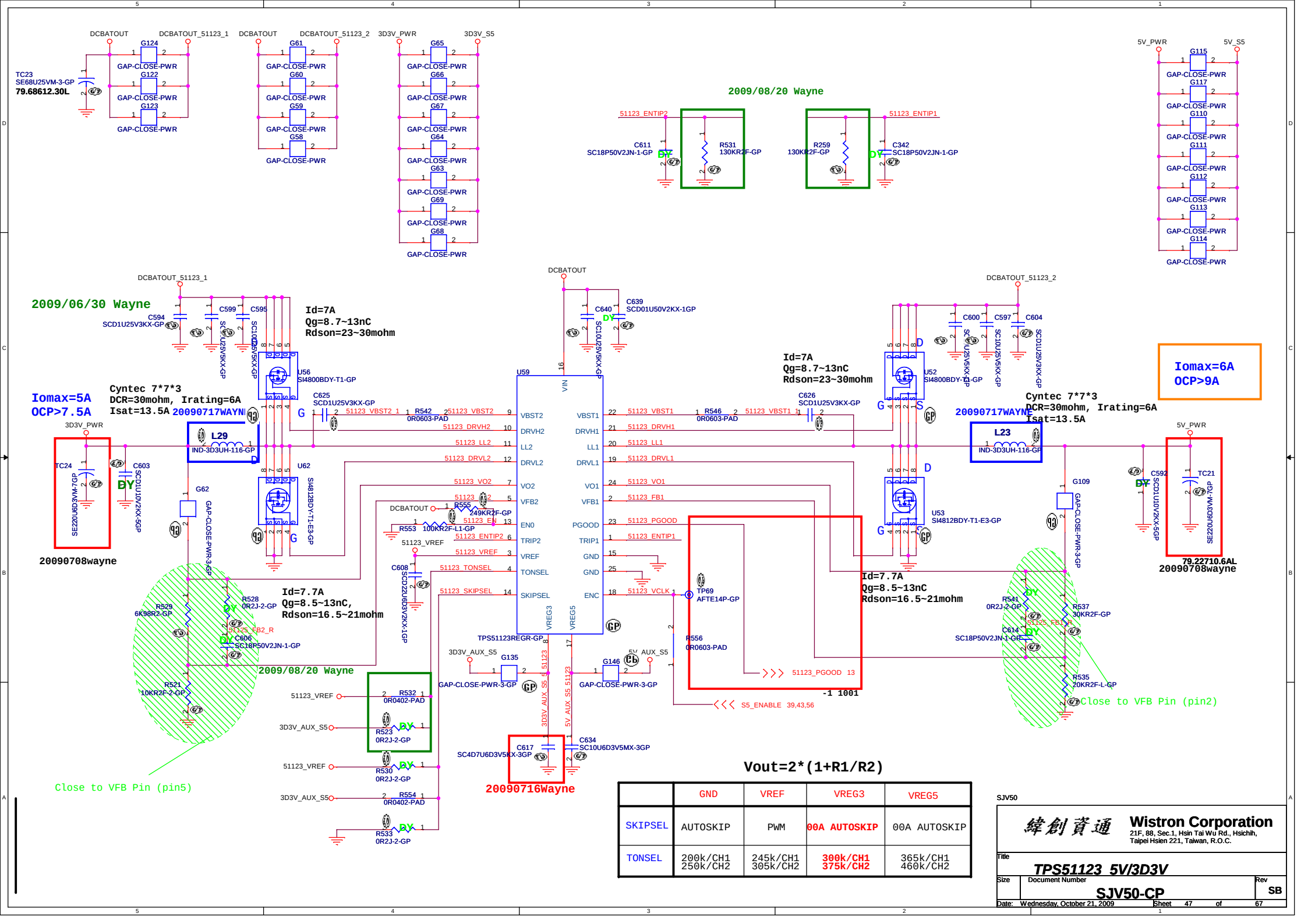

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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Title: TPS51123 5V/3D3V

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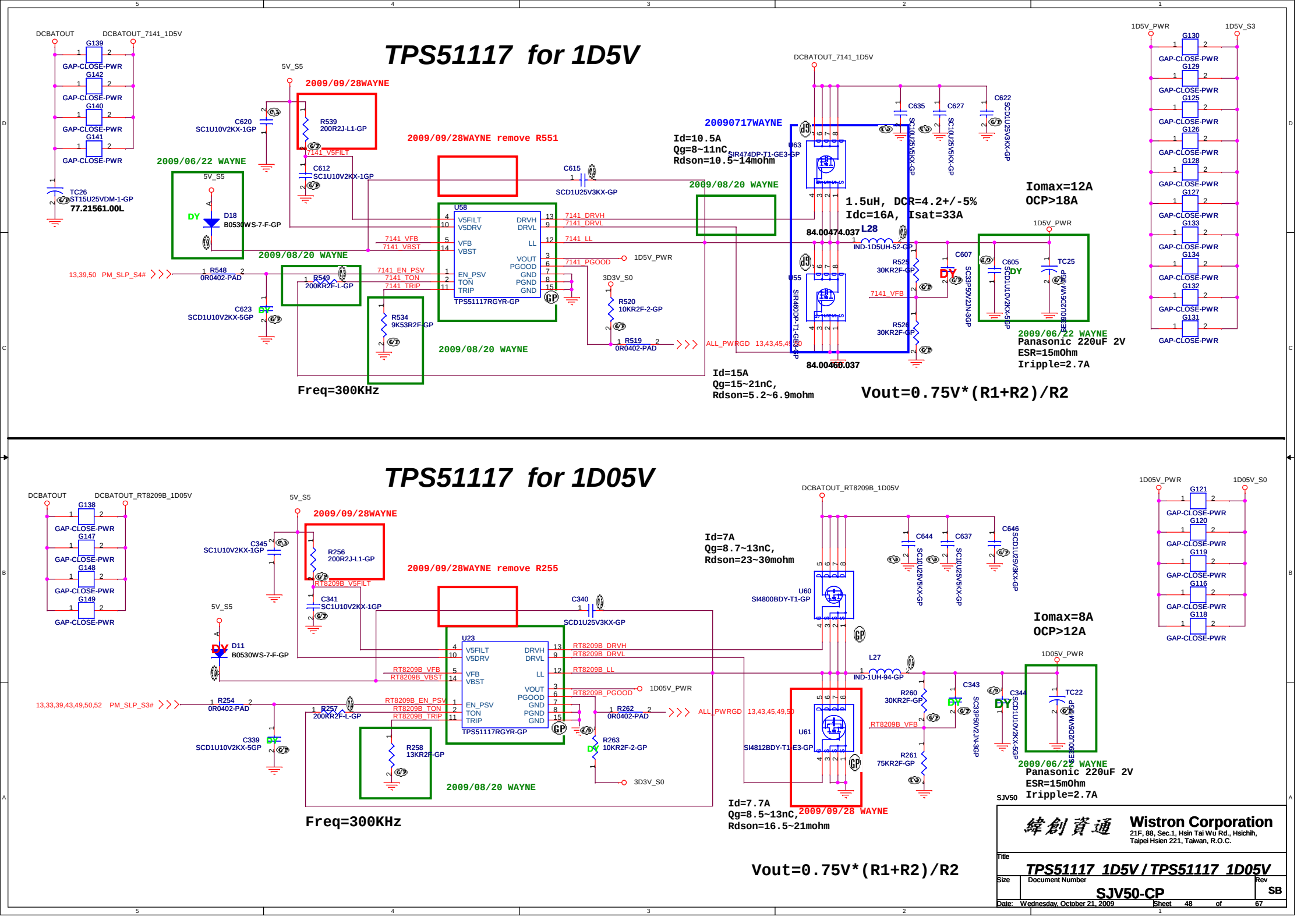
TPS51117 for 1D5V
DCBATOUT
DCBATOUT_7141_1D5V
GAP-CLOSE-PWR
TC26
ST15U25VDM-1-GP
77.21561.00L
5V_S5
2009/09/28WAYNE
C620
SC1U10V2KX-1GP
R539
200R2J-L1-GP
7141_V5FILT
C612
SC1U10V2KX-1GP
2009/09/28WAYNE remove R551
2009/06/22 WAYNE
D18
B0530WS-7-F-GP
2009/08/20 WAYNE
13,39,50 PM_SLP_S4#
R548
0R0402-PAD
R549
200KR2F-L-GP
C623
SCD1U10V2KX-5GP
R534
9K53R2F-GP
U58
V5FILT
V5DRV
VFB
VBST
EN_PSV
TON
TRIP
DRVH
DRVL
LL
VOUT
PGOOD
GND
PGND
TPS51117RGYR-GP
7141_VFB
7141_VBST
7141_EN_PSV
7141_TON
7141_TRIP
7141_DRVH
7141_DRVL
7141_LL
7141_PGOOD
1D5V_PWR
3D3V_S0
R520
10KR2F-2-GP
R519
0R0402-PAD
ALL_PWRGD 13,43,45,49,50
C615
SCD1U25V3KX-GP
2009/08/20 WAYNE
Freq=300KHz
20090717WAYNE
Id=10.5A
Qg=8~11nC
Rdson=10.5~14mohm
U63
SIR474DP-T1-GE3-GP
84.00460.037
U55
SIR468DP-T1-GE3-GP
84.00474.037
1.5uH, DCR=4.2+/-5%
Idc=16A, Isat=33A
L28
IND-1D5UH-52-GP
C635
C627
C622
SCD1U25V3KX-GP
SC10U25V5KX-GP
R525
30KR2F-GP
R526
30KR2F-GP
C607
SC33P50V2JN-3GP
C605
SCD1U10V2KX-5GP
TC25
SEE-330U2D0M-GP
Iomax=12A
OCP>18A
2009/06/22 WAYNE
Panasonic 220uF 2V
ESR=15mOhm
Iripple=2.7A
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
Vout=0.75V*(R1+R2)/R2
G130
G129
G125
G126
G128
G127
G133
G134
G132
G131
1D5V_S3
TPS51117 for 1D05V
DCBATOUT_RT8209B_1D05V
G138
G147
G148
G149
C345
SC1U10V2KX-1GP
R256
200R2J-L1-GP
RT8209B_V5FILT
C341
SC1U10V2KX-1GP
2009/09/28WAYNE remove R255
D11
B0530WS-7-F-GP
13,33,39,43,49,50,52 PM_SLP_S3#
R254
0R0402-PAD
R257
200KR2F-L-GP
C339
SCD1U10V2KX-5GP
R258
13KR2F-GP
U23
RT8209B_VFB
RT8209B_VBST
RT8209B_EN_PSV
RT8209B_TON
RT8209B_TRIP
RT8209B_DRVH
RT8209B_DRVL
RT8209B_LL
RT8209B_PGOOD
TPS51117RGYR-GP
C340
SCD1U25V3KX-GP
R262
0R0402-PAD
R263
10KR2F-2-GP
3D3V_S0
2009/08/20 WAYNE
Freq=300KHz
Id=7A
Qg=8.7~13nC,
Rdson=23~30mohm
U60
SI4800BDY-T1-GP
U61
SI4812BDY-T1-E3-GP
C644
C637
C646
SC10U25V5KX-GP
SCD1U25V3KX-GP
L27
IND-1UH-94-GP
R260
30KR2F-GP
R261
75KR2F-GP
C343
SC33P50V2JN-3GP
C344
SCD1U10V2KX-5GP
TC22
SEE-330U2D0M-GP
Iomax=8A
OCP>12A
2009/06/22 WAYNE
Panasonic 220uF 2V
ESR=15mOhm
Iripple=2.7A
Id=7.7A
Qg=8.5~13nC,
Rdson=16.5~21mohm
2009/09/28 WAYNE
Vout=0.75V*(R1+R2)/R2
G121
G120
G119
G116
G118
1D05V_PWR
1D05V_S0
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51117 1D5V / TPS51117 1D05V
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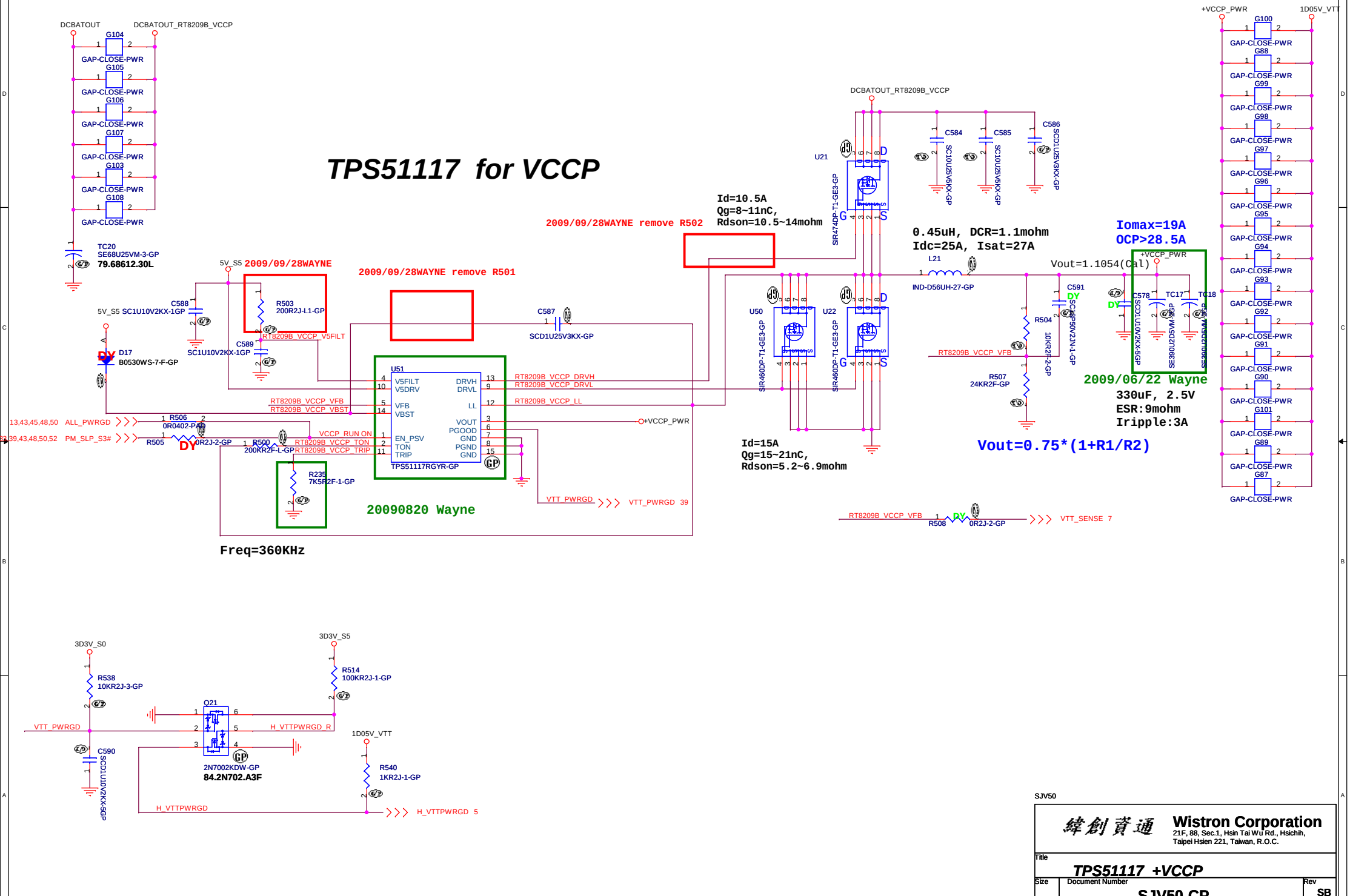

SJV50

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Title	***TPS51117 +VCCP***	
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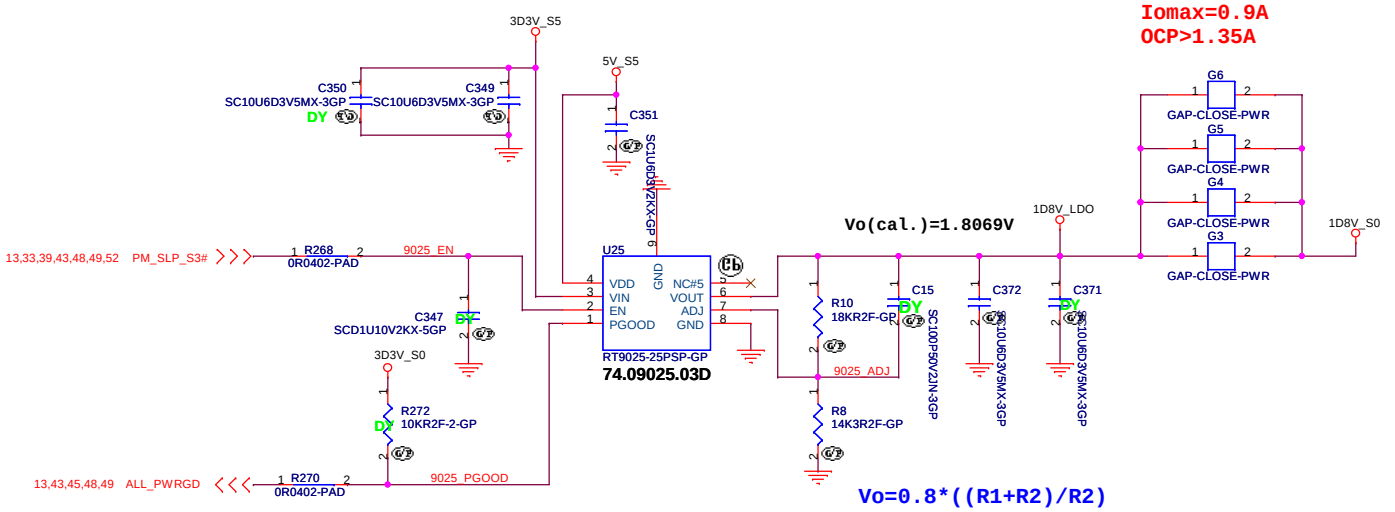
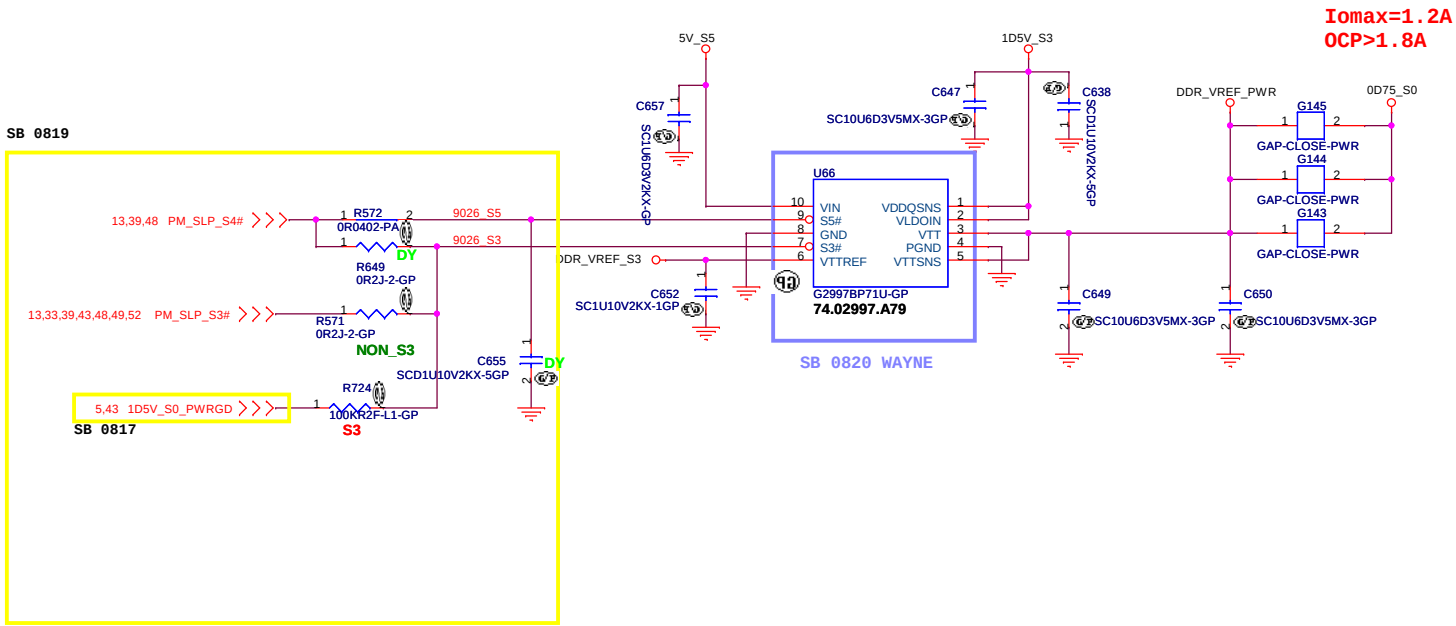
RT9025 for 1D8V_S0



G2997 for 0D75V_S3



SJV50

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*RT9025_1D8V/G2997_0D75*	
Size	Document Number: SJV50-CP	Rev: SB
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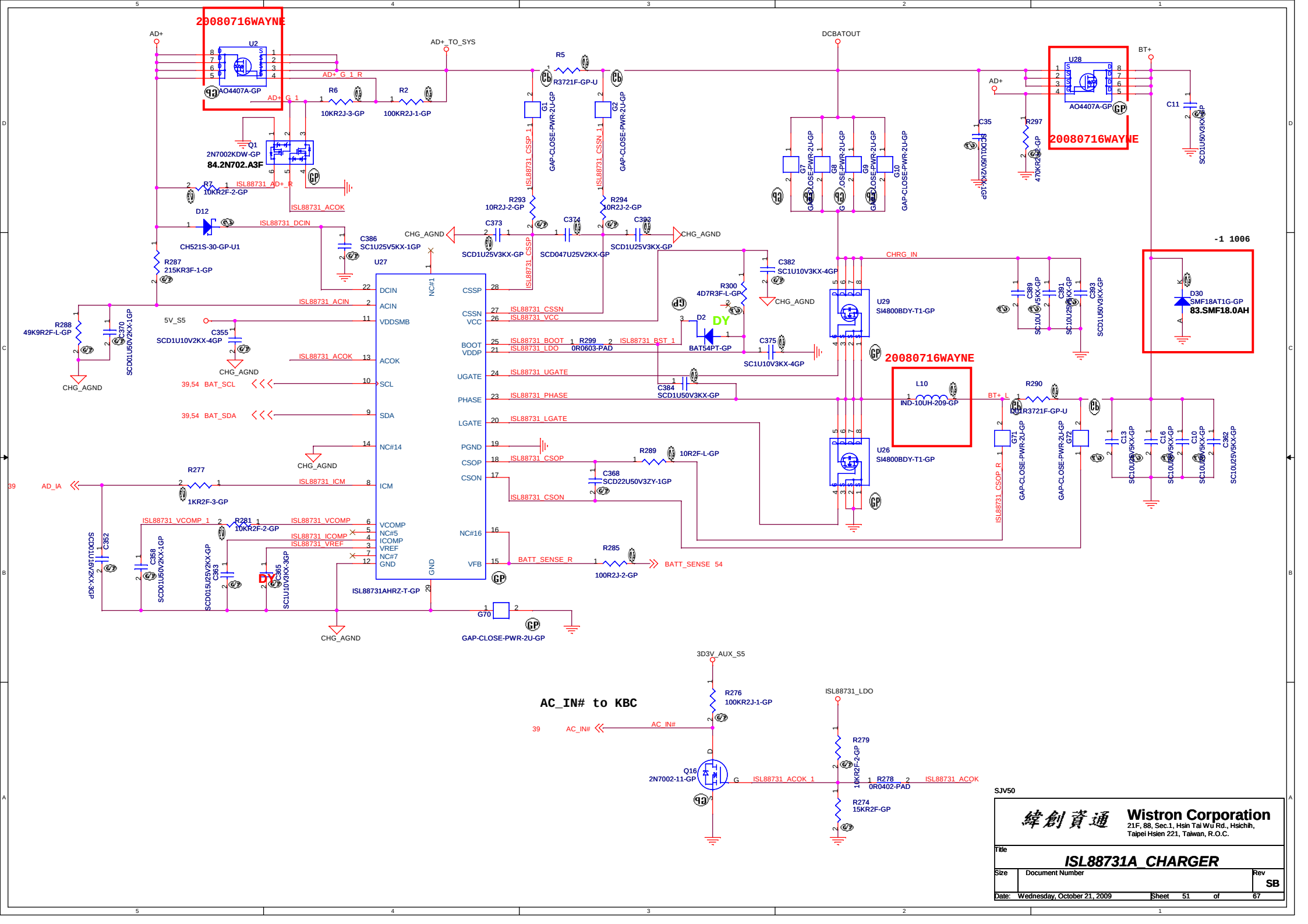
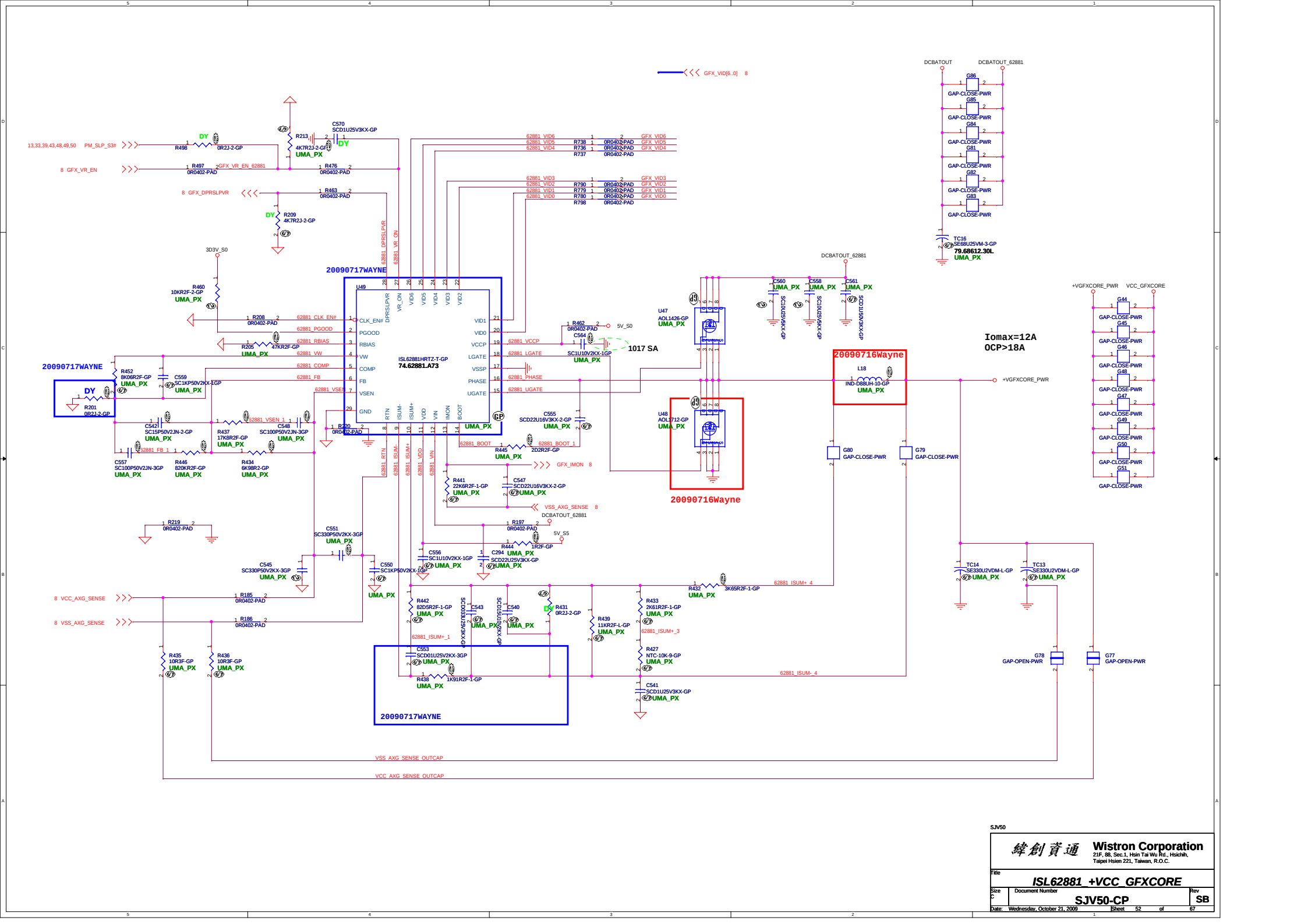

20080716WAYNE
U2
AO4407A-GP
AD+
AD+_TO_SYS
AD+_G_1_R
AD+_G_1
R6
10KR2J-3-GP
R2
100KR2J-1-GP
R5
R3721F-GP-U
Q1
2N7002KDW-GP
84.2N702.A3F
R7
10KR2F-2-GP
ISL88731_AD+_R
ISL88731_ACOK
D12
CH521S-30-GP-U1
ISL88731_DCIN
C386
SC1U25V5KX-1GP
R287
215KR3F-1-GP
CHG_AGND
C373
SCD1U25V3KX-GP
C374
SCD047U25V2KX-GP
C393
SCD1U25V3KX-GP
R293
10R2J-2-GP
R294
10R2J-2-GP
ISL88731_CSSP_1
ISL88731_CSSN_1
GAP-CLOSE-PWR-2U-GP
DCBATOUT
U28
AO4407A-GP
C35
SCD1U50V2KX-GP
R297
470KR2J-GP
C11
SCD1U50V3KX-GP
BT+
-1 1006
D30
SMF18AT1G-GP
83.SMF18.0AH
U27
ISL88731AHRZ-T-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
R288
49K9R2F-L-GP
C370
SCD01U50V2KX-1GP
5V_S5
C355
SCD1U10V2KX-4GP
39,54 BAT_SCL
39,54 BAT_SDA
R277
1KR2F-3-GP
AD_IA
R281
10KR2F-2-GP
C352
C358
SCD01U50V2KX-1GP
C363
SCD015U25V2KX-GP
C365
SC1U10V3KX-3GP
ISL88731_ACIN
ISL88731_VCOMP_1
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
ISL88731_ICM
ISL88731_CSSP
ISL88731_CSSN
ISL88731_VCC
ISL88731_BOOT
ISL88731_LDO
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
ISL88731_CSOP
ISL88731_CSON
R299
0R0603-PAD
ISL88731_BST_1
R300
4D7R3F-L-GP
D2
BAT54PT-GP
DY
C375
SC1U10V3KX-4GP
C382
SC1U10V3KX-4GP
C384
SCD1U50V3KX-GP
R289
10R2F-L-GP
C368
SCD22U50V3ZY-1GP
R285
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 54
G70
GAP-CLOSE-PWR-2U-GP
CHRG_IN
U29
SI4800BDY-T1-GP
U26
SI4800BDY-T1-GP
L10
IND-10UH-209-GP
BT+_L
R290
DCR3721F-GP-U
C389
SC10U25V5KX-GP
C391
SC10U25V5KX-GP
C393
SCD1U50V3KX-GP
G71
G72
GAP-CLOSE-PWR-2U-GP
C13
C16
C10
C362
SC10U25V5KX-GP
ISL88731_CSOP_R
AC_IN# to KBC
3D3V_AUX_S5
R276
100KR2J-1-GP
AC_IN#
Q16
2N7002-11-GP
ISL88731_ACOK_1
R279
10KR2F-2-GP
R278
0R0402-PAD
R274
15KR2F-GP
ISL88731_LDO
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A_CHARGER
Size
Document Number
Rev
SB
Date: Wednesday, October 21, 2009
Sheet 51 of 67



SJV50

Wistron Corporation
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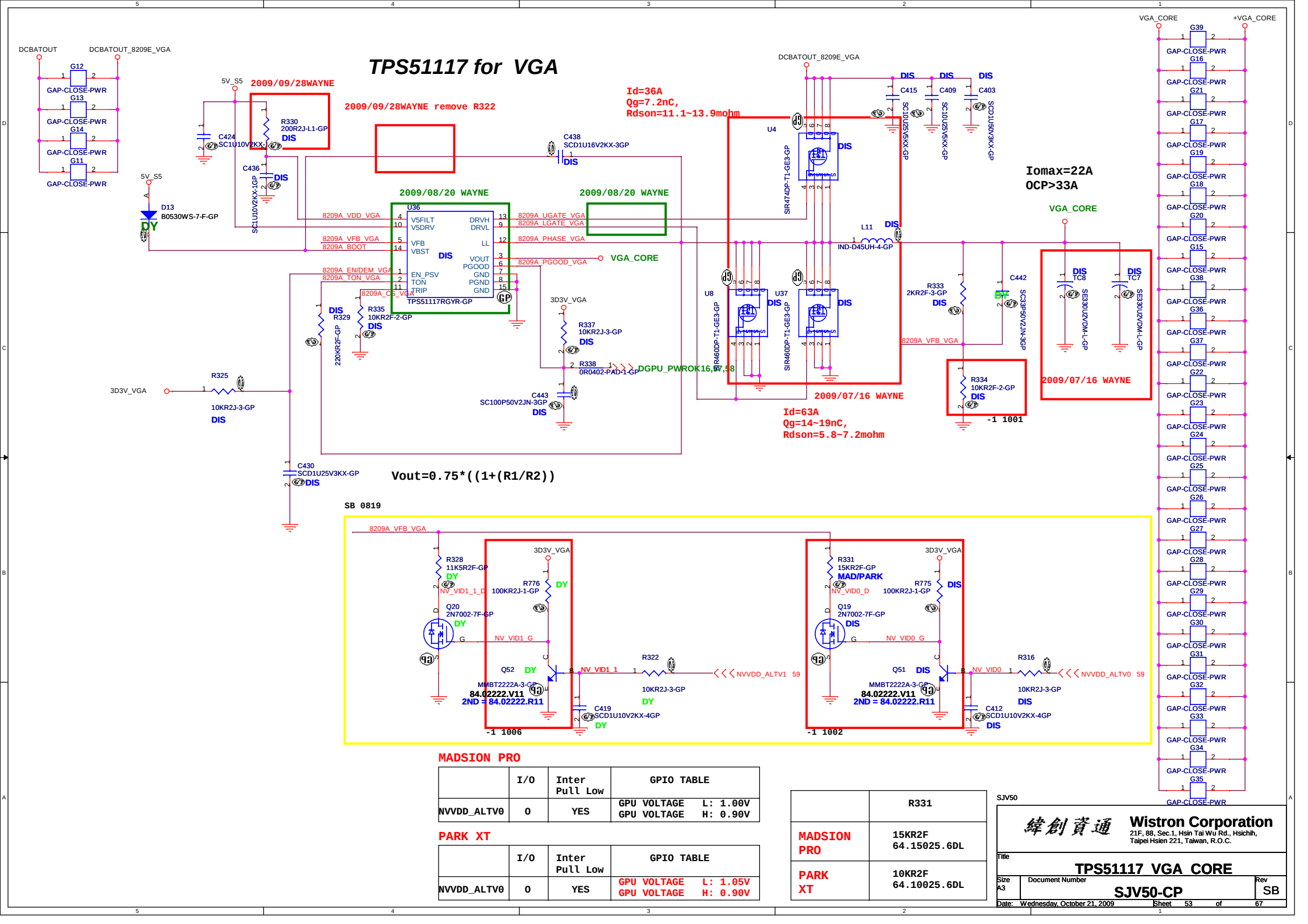
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62881_+VCC_GFXCORE

Size	Document Number	Rev
C	SJV50-CP	SB

Date: Wednesday, October 21, 2009 Sheet 52 of 67



MADSION PRO

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

PARK XT

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.05V GPU VOLTAGE H: 0.90V

	R331
MADSION PRO	15KR2F 64.15025.6DL
PARK XT	10KR2F 64.10025.6DL

SJV50

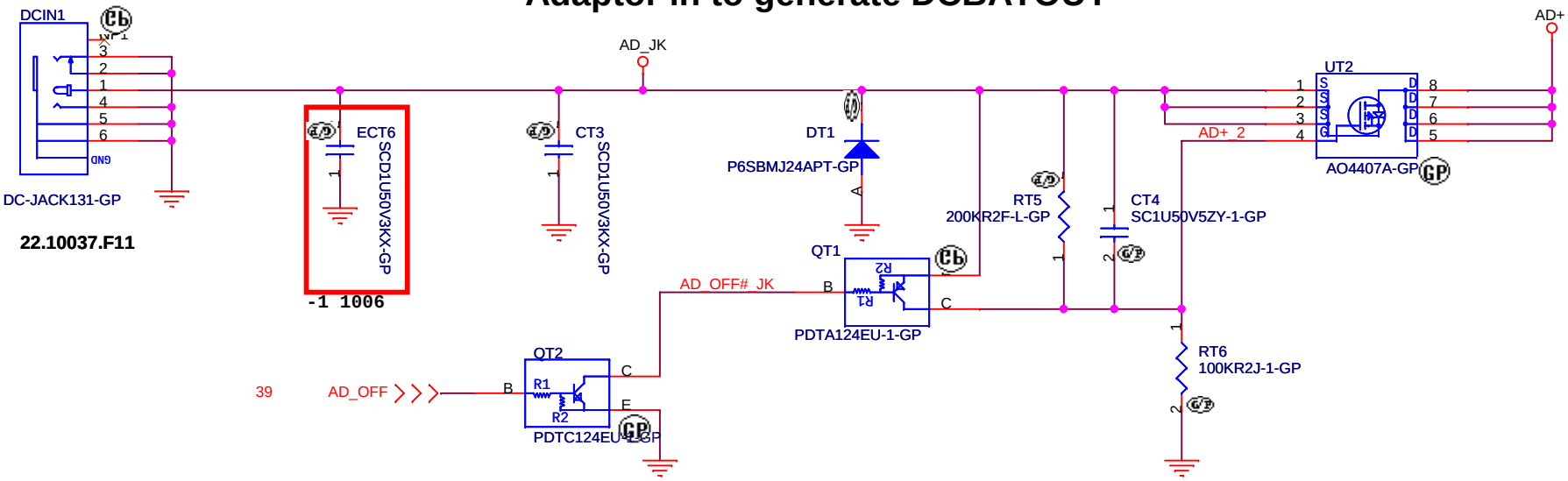
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51117 VGA CORE

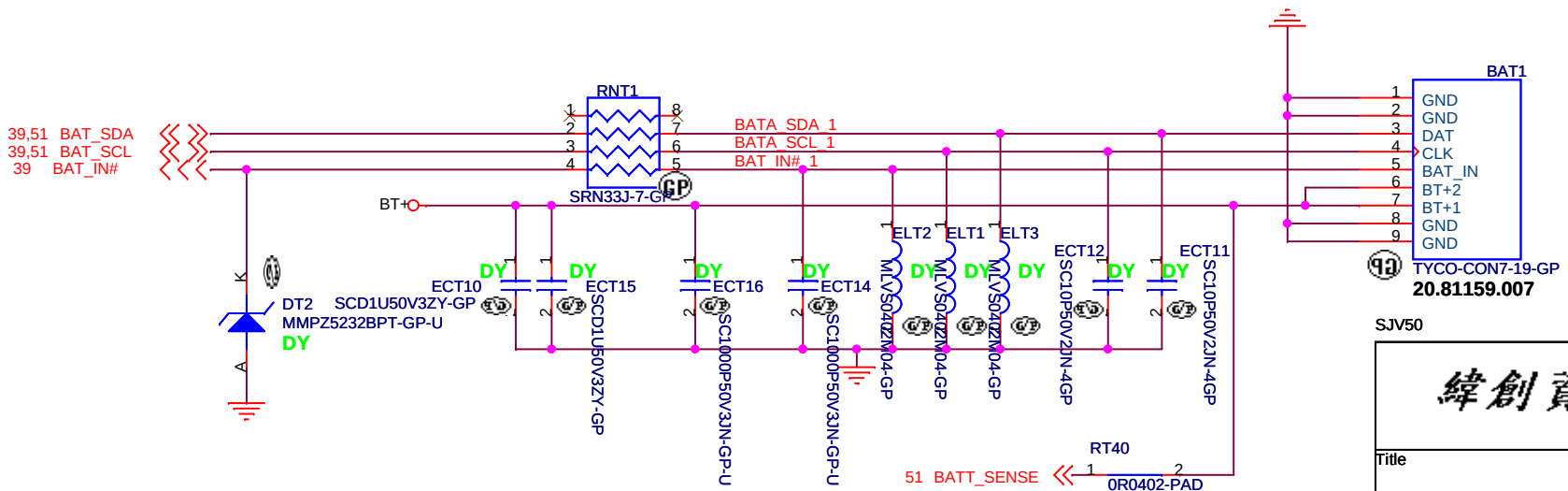
Size	Document Number	Rev
A3	SJV50-CP	SB

Date: Wednesday, October 21, 2009 Sheet 53 of 67

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



SJV50

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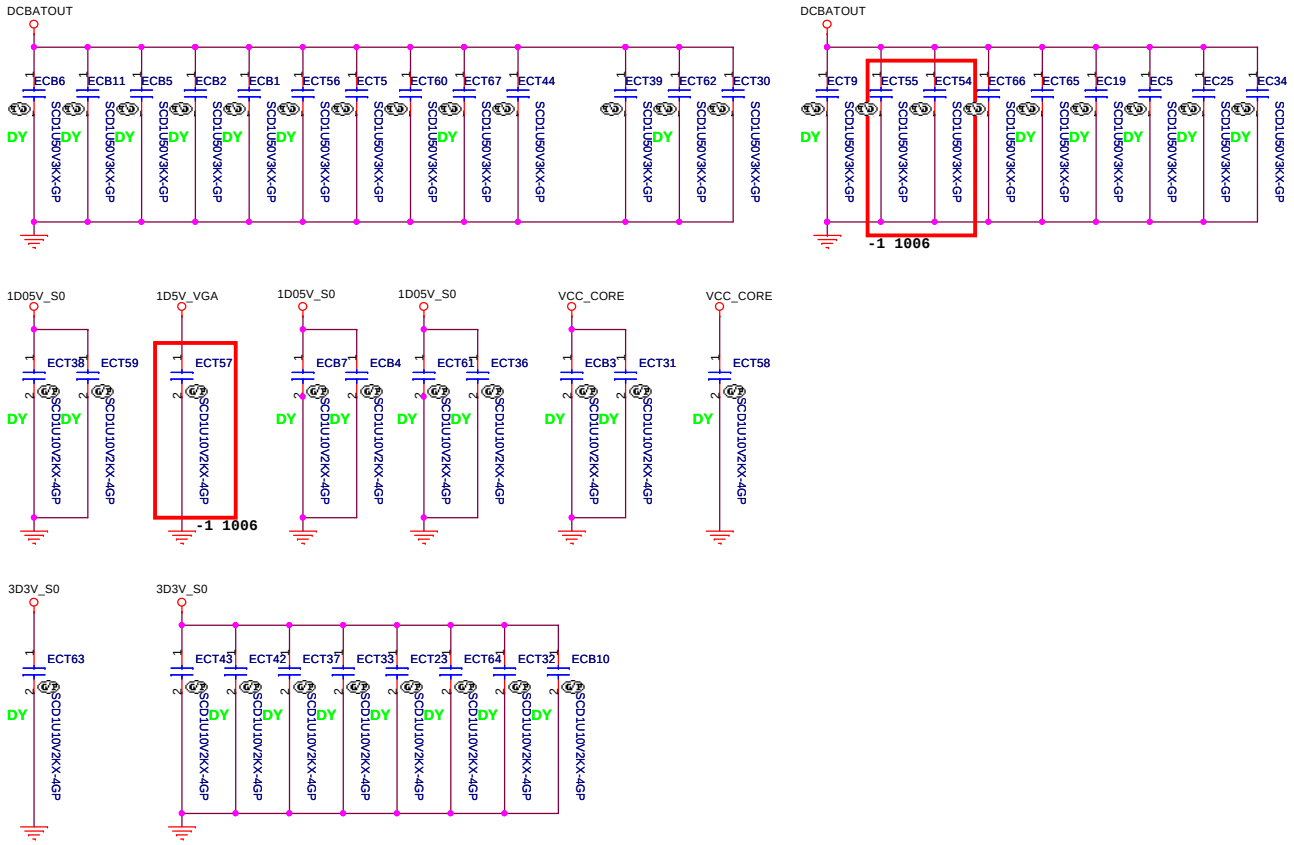
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
	SJV50-CP	SB

Date: Wednesday, October 21, 2009 Sheet 54 of 67



CPU

H1 H2 H3

ZZ.00PAD.801 HOLE2542-GP

34.42Y01.021 34.42Y01.021 34.42Y01.021

NB

H4

ZZ.00PAD.801 HOLE2542-GP

34.42Y01.021

VGA

H5 H6

ZZ.00PAD.801 HOLE2542-GP

34.42Y01.021 34.42Y01.021

MDC

H7 HOLE H8 HOLE

ZZ.0HOLE.XXX

34.42Y01.021 34.42Y01.021

MINICARD

HB1 HOLE H20 HOLE

34.4B804.001 DY

H14

ZZ.00PAD.801 HOLE2542-GP

34.42Y01.021

GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9

HOLE355X355R111-S1-GP HOLE315X315R91-S1-GP

GNDT1 HOLE

ZZ.0HOLE.XXX

SPRING_GND3 SPRING-58-GP

34.4B312.002

SJV50

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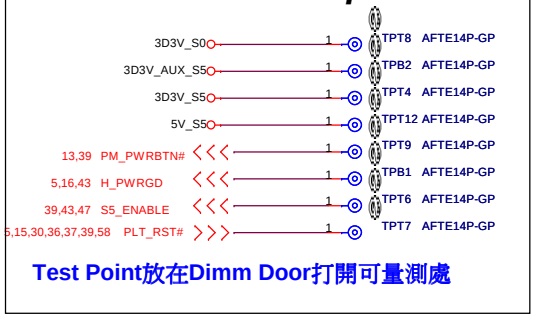
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size | Document Number: SJV50-CP | Rev: SB

Date: Wednesday, October 21, 2009 | Sheet 55 of 67

Check test point



Test Point放在Dimm Door打開可量測處

SJV50

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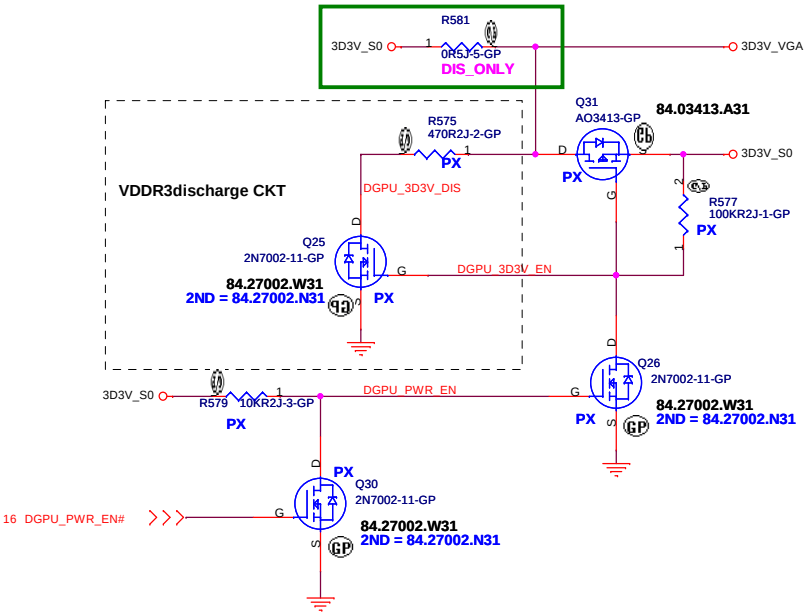
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AFTE_TP***

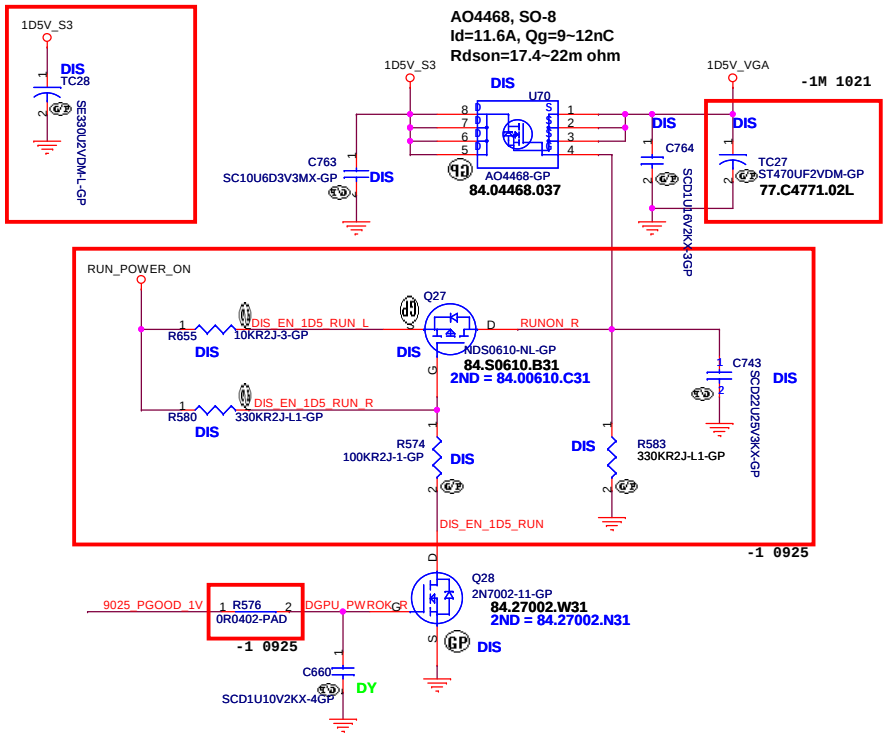
Size	Document Number	Rev
A3	SJV50-CP	SB

Date: Wednesday, October 21, 2009 Sheet 56 of 67

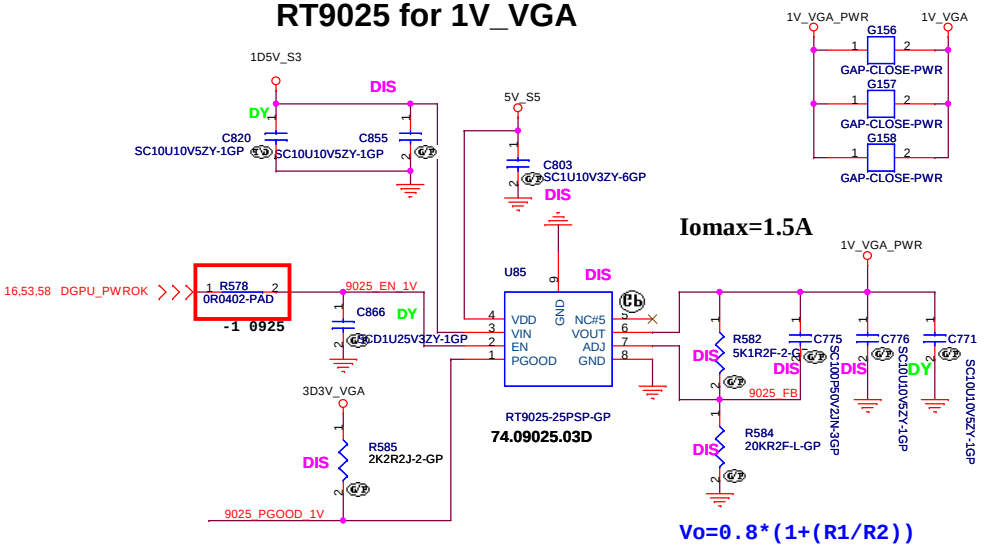
+3VS to 3.3V_DELAY Transfer



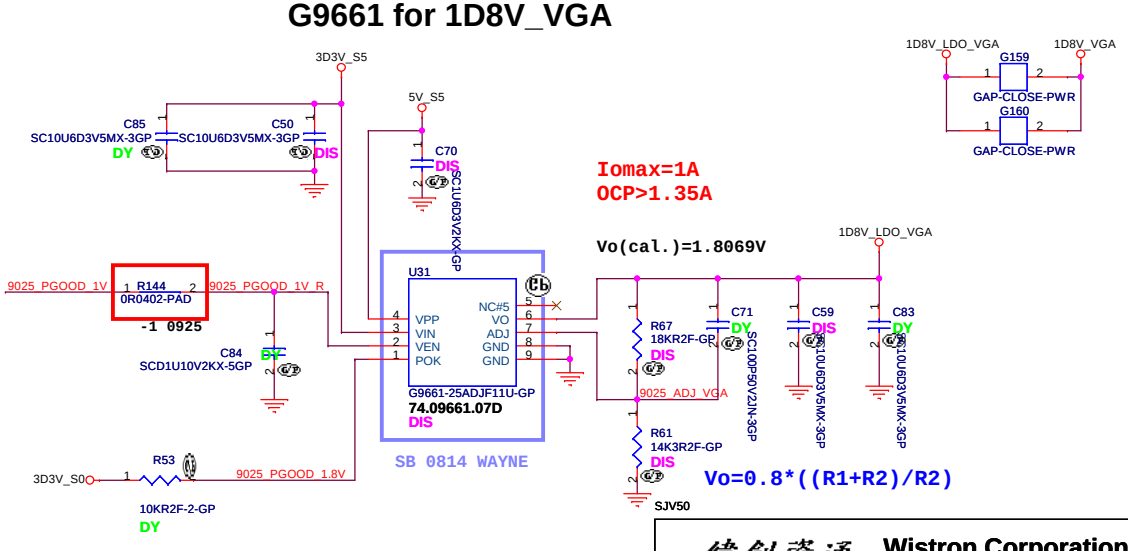
-1M 1021



RT9025 for 1V_VGA



G9661 for 1D8V_VGA

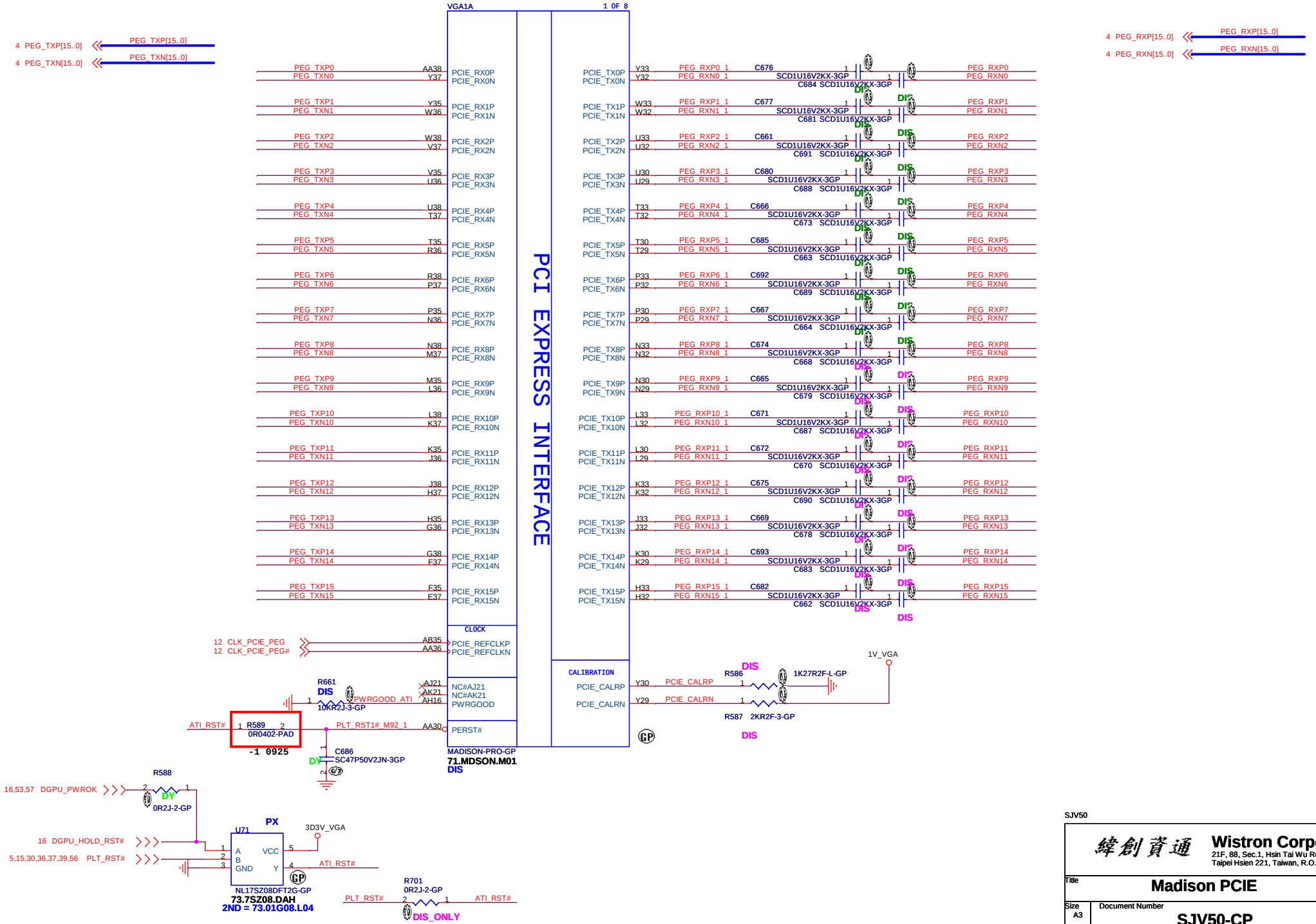


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI POWER

Size: A3 | Document Number: SJV50-CP | Rev: SB

Date: Wednesday, October 21, 2009 | Sheet 57 of 67



SJV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Madison PCIE	
Size A3	Document Number SJV50-CP	Rev SB
Date: Wednesday, October 21, 2009	Sheet 58 of 67	

Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)

It's strap for GDDR3-136ball
Need to Clarify

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

For Thermal sensor

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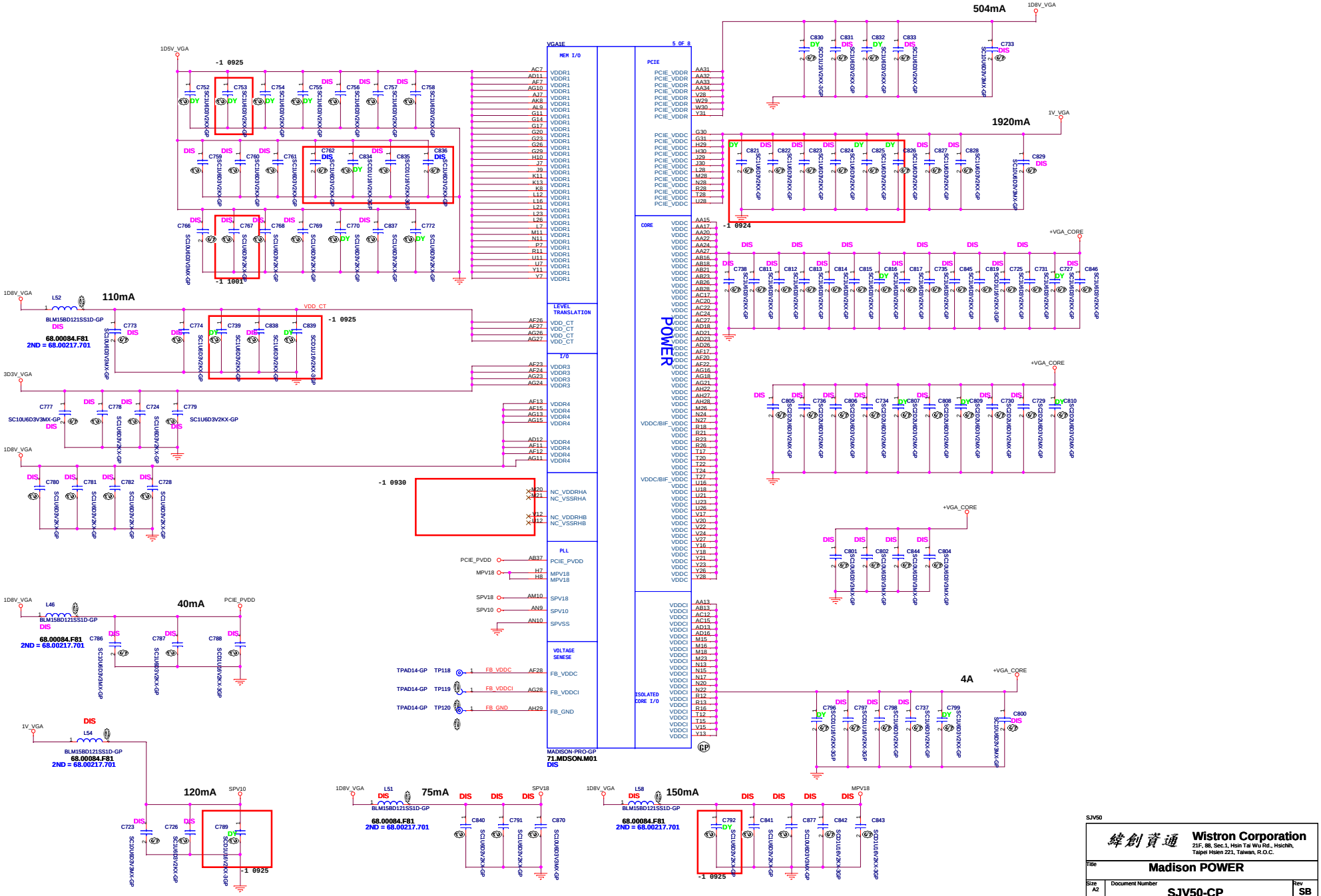
Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison IO

Size: A2 | Document Number: SJV50-CP | Rev: SB

Date: Wednesday, October 21, 2009 | Sheet 59 of 67



SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison POWER

Size: A2 | Document Number: SJV50-CP | Rev: SB

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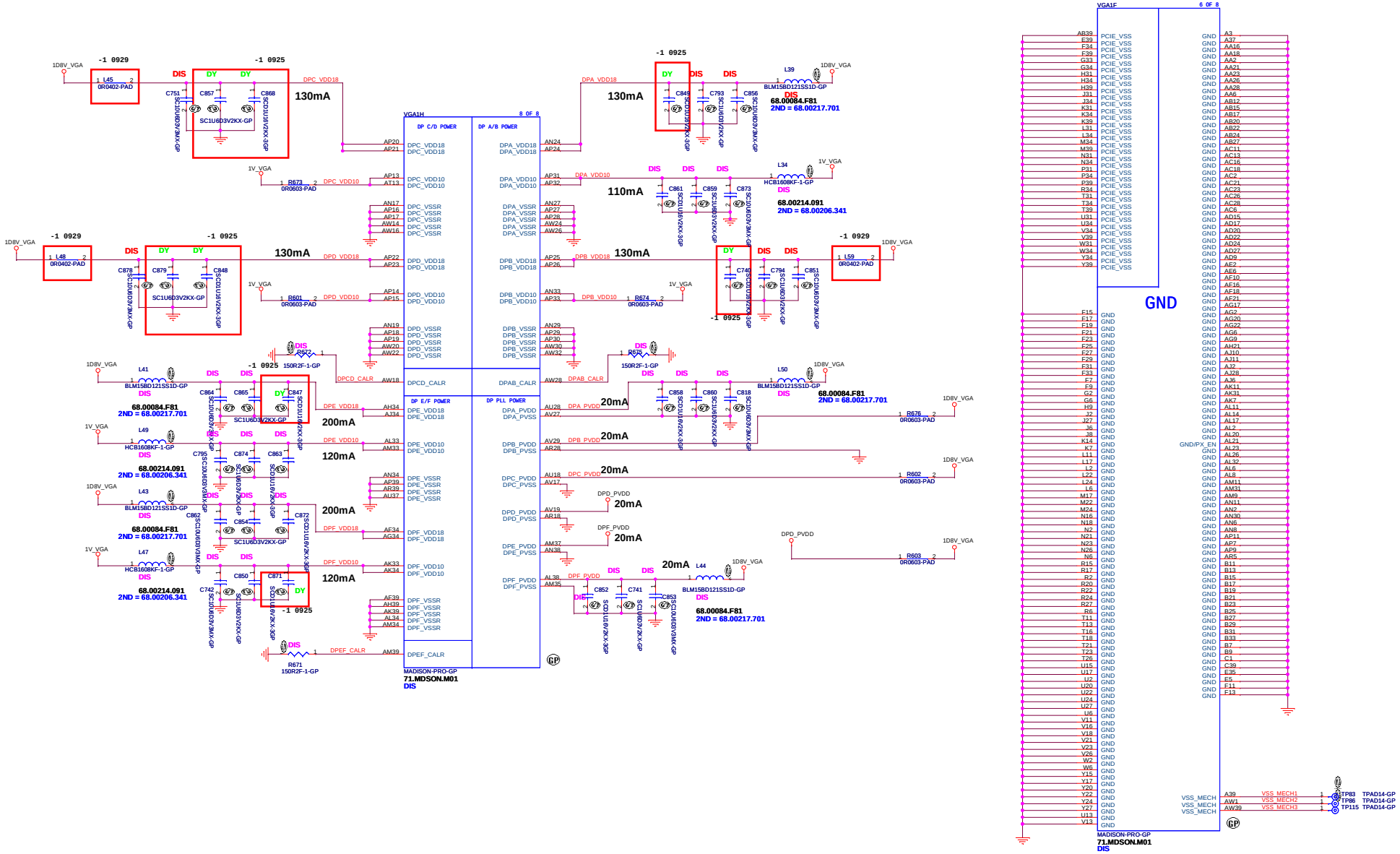

SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DP POWER_GND**

Size	Document Number	Rev
A2	SJV50-CP	SB

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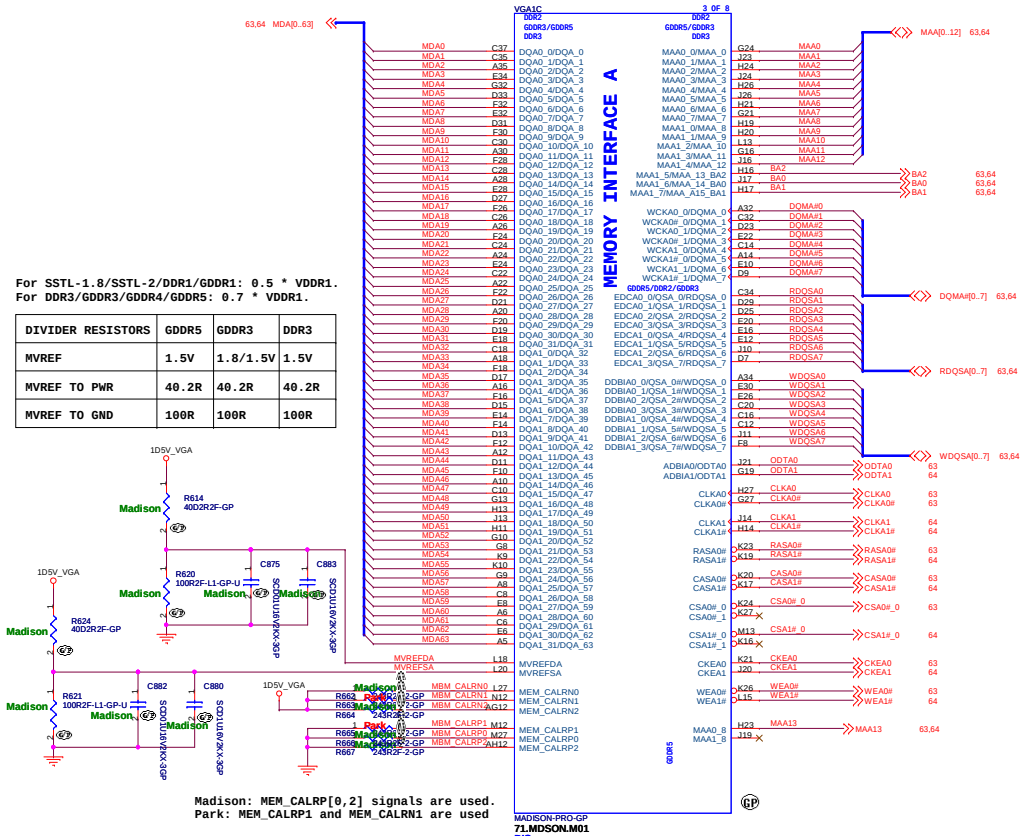
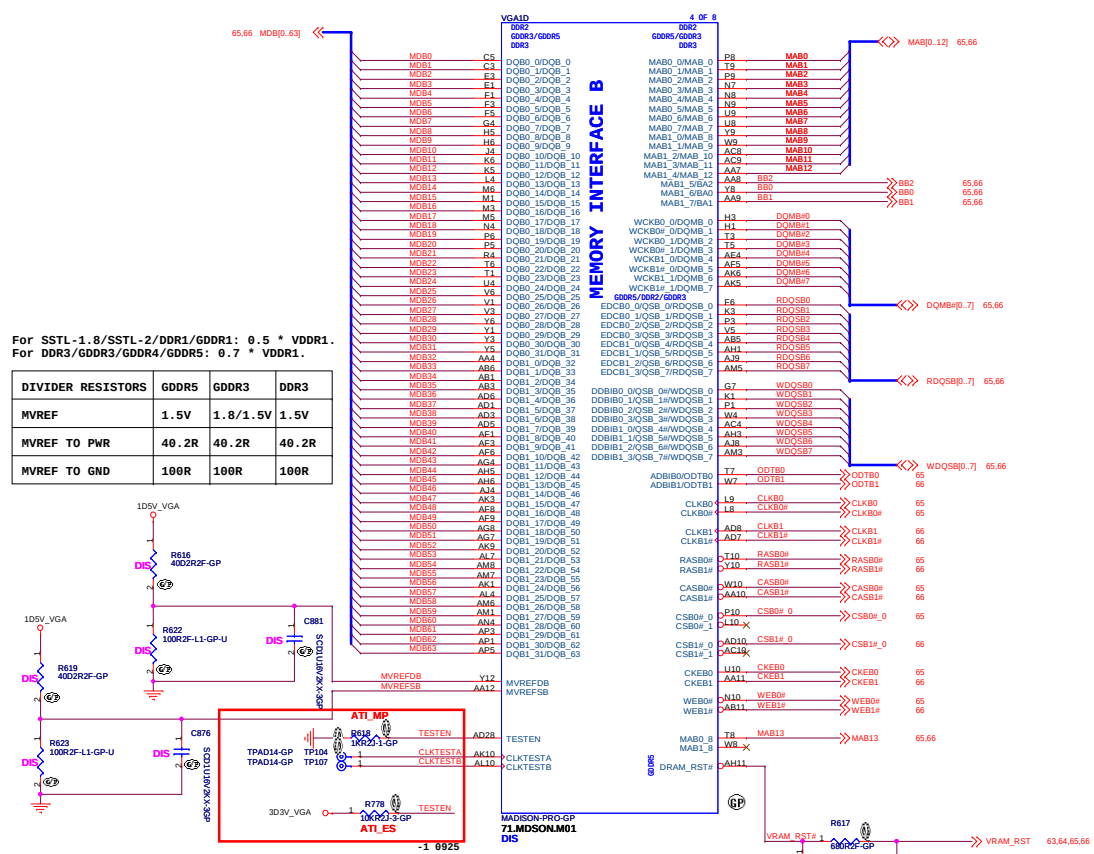


For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used



For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

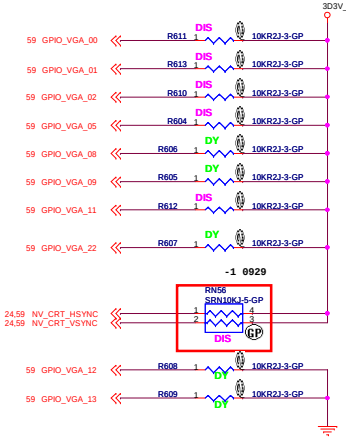
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			



Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

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Title: Madison Memory / Straps

Size: A2 | Document Number: SJV50-CP | Rev: SB

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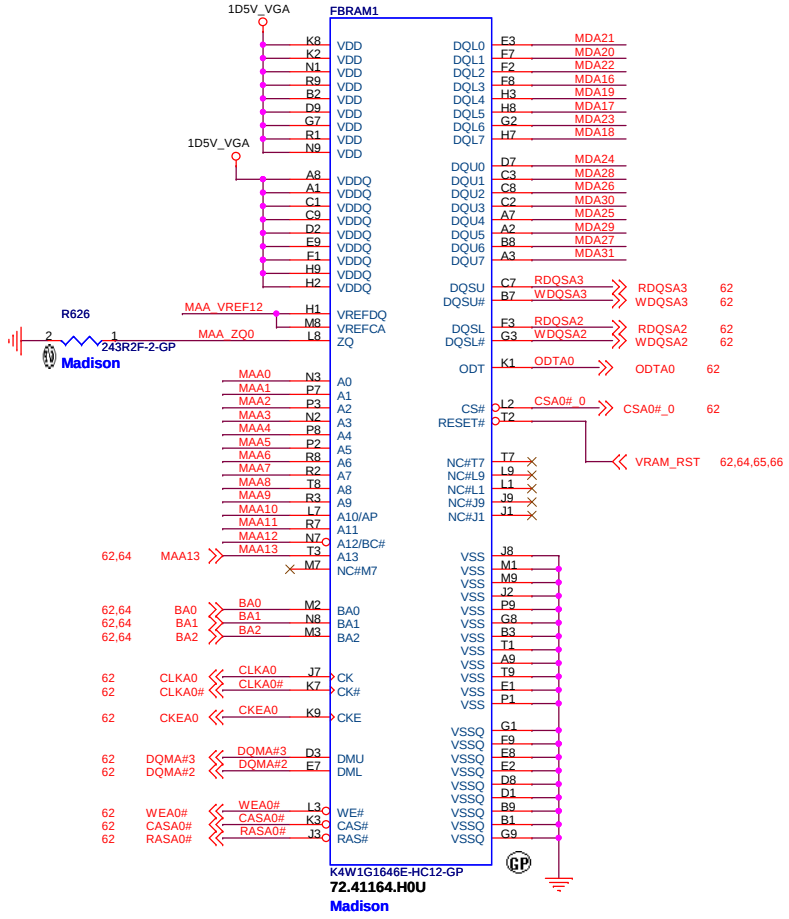
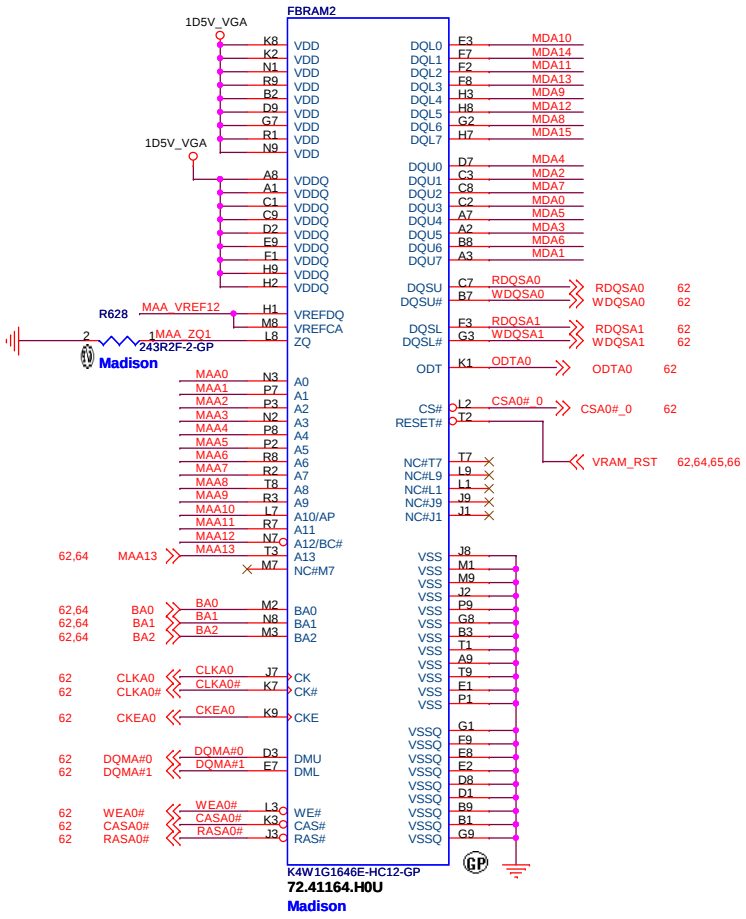
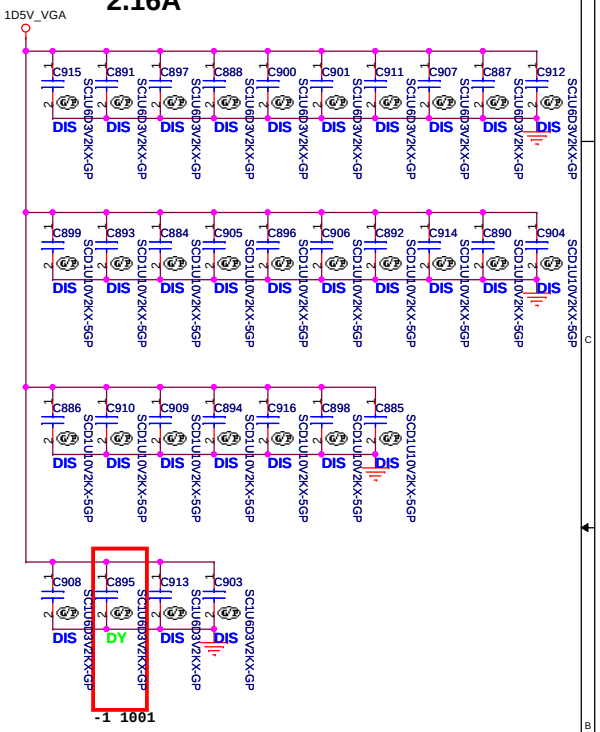
DDR3

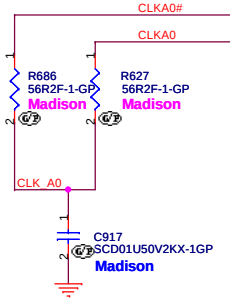


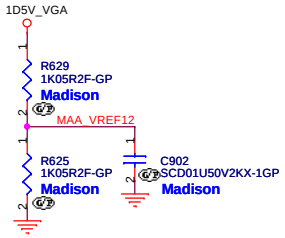


2.16A



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U





62,64 DQMA#[0..7]
62,64 RDQSA[0..7]
62,64 WDQSA[0..7]
62,64 MAA[0..12] MAA[0..12]
62,64 MDA[0..63] MDA[0..63]

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*VRAM(1/4)*
Size A3 / Document Number	SJV50-CP
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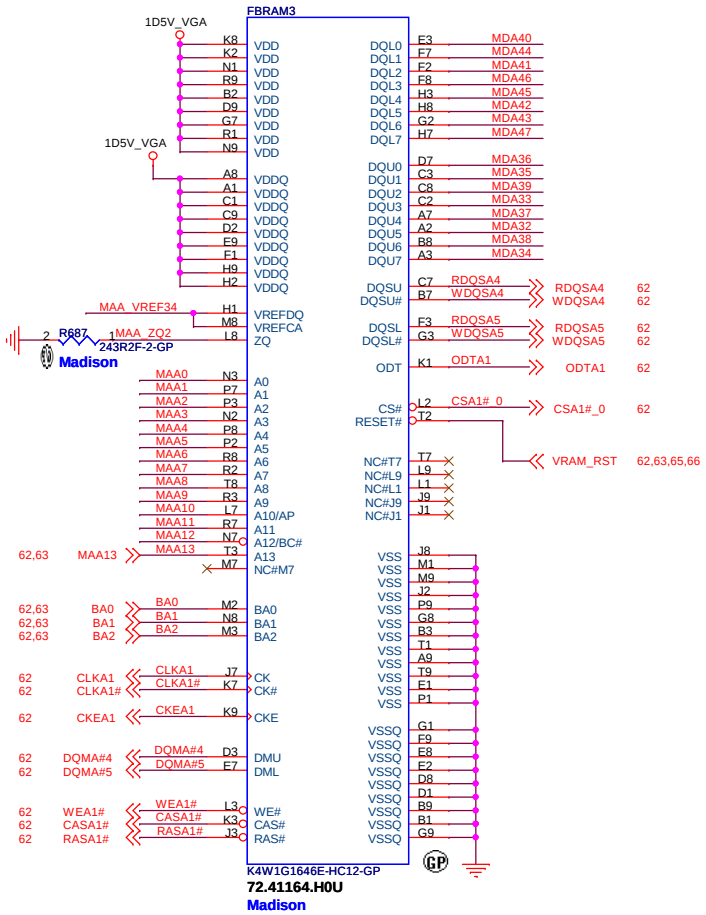
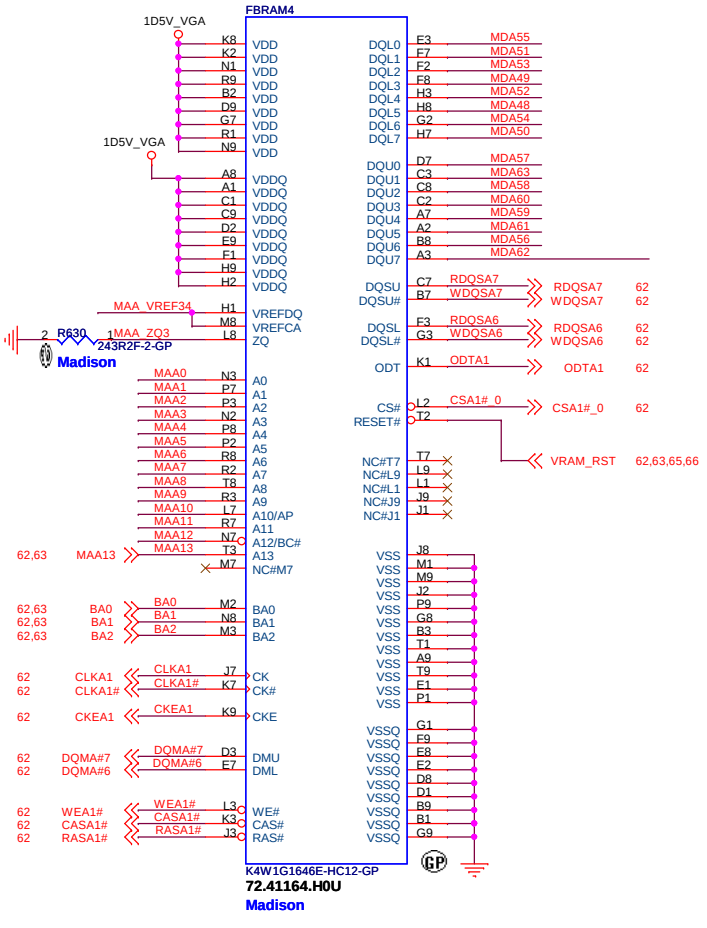
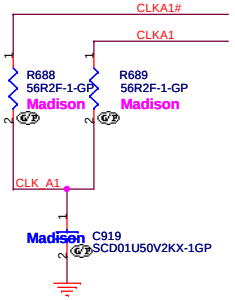
Date: Wednesday, October 21, 2009	Sheet 63 of 67

DDR3







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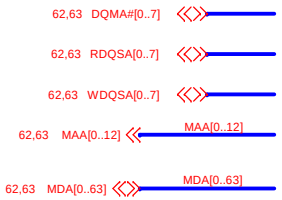
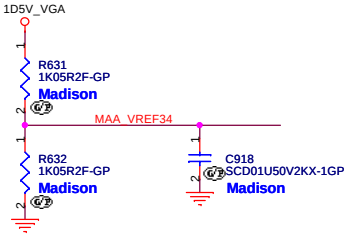
HYNIX: 72.51G63.C0U

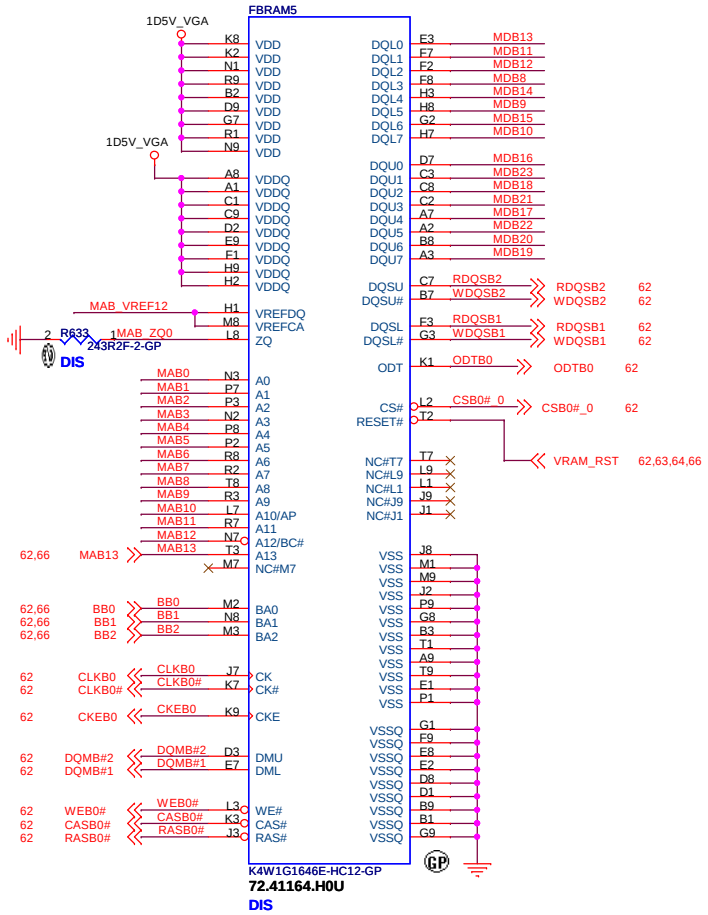


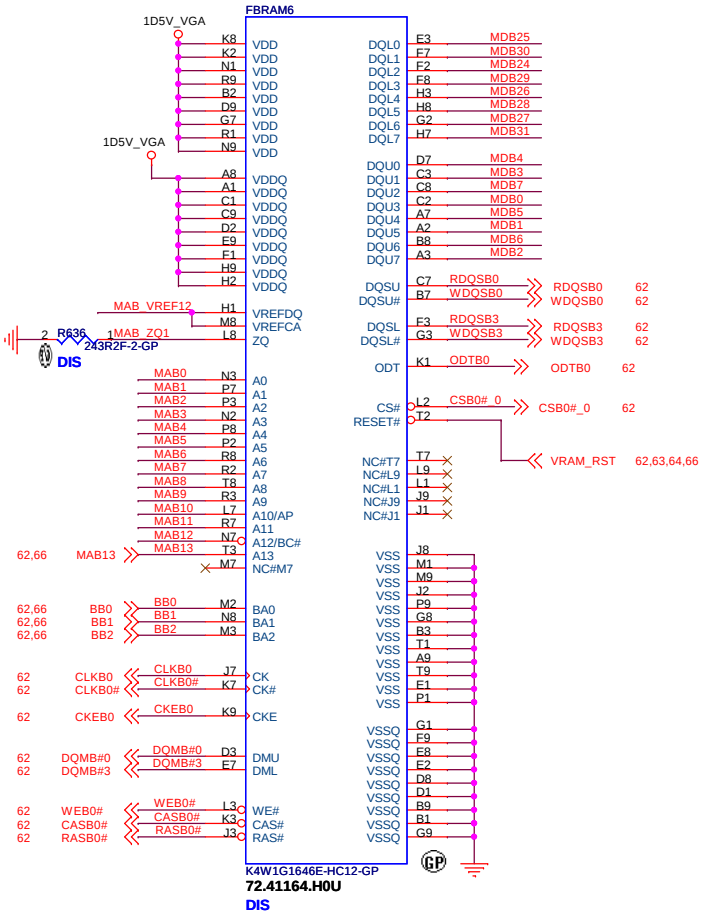


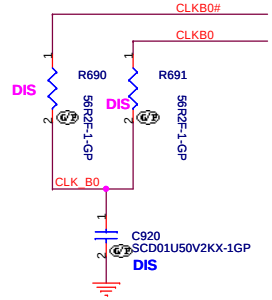
SJV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *VRAM(2/4)*		
Size: A3	Document Number: SJV50-CP	Rev: SB
Date: Wednesday, October 21, 2009	Sheet 64 of 67	

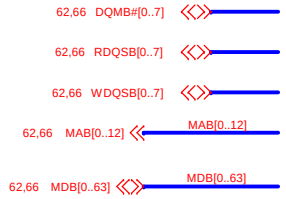
DDR3

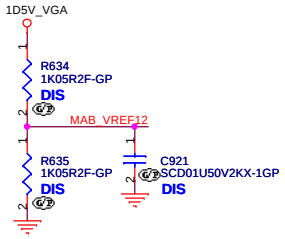






SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



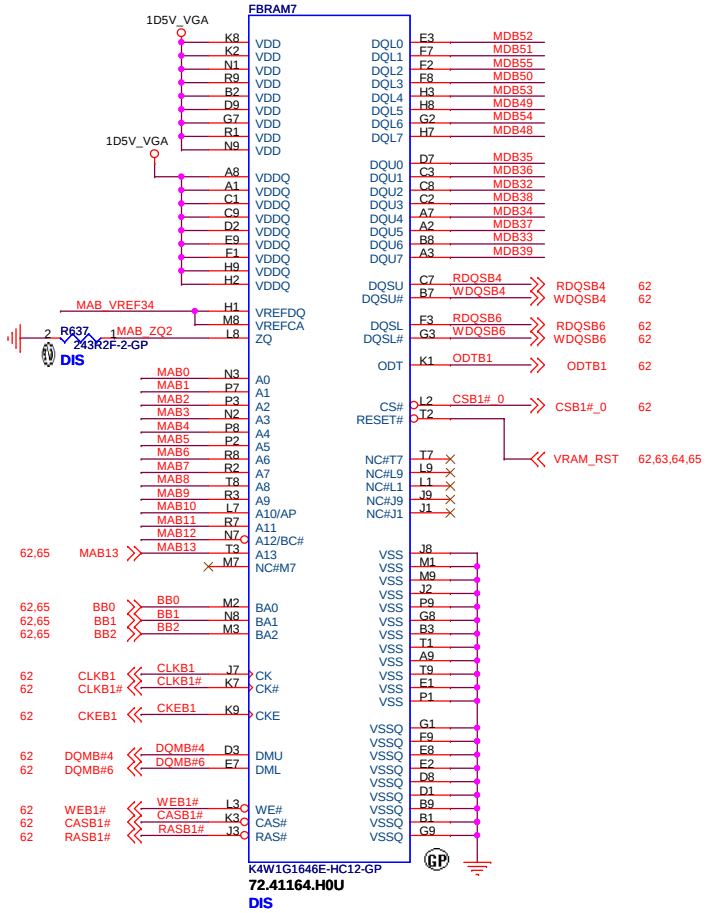


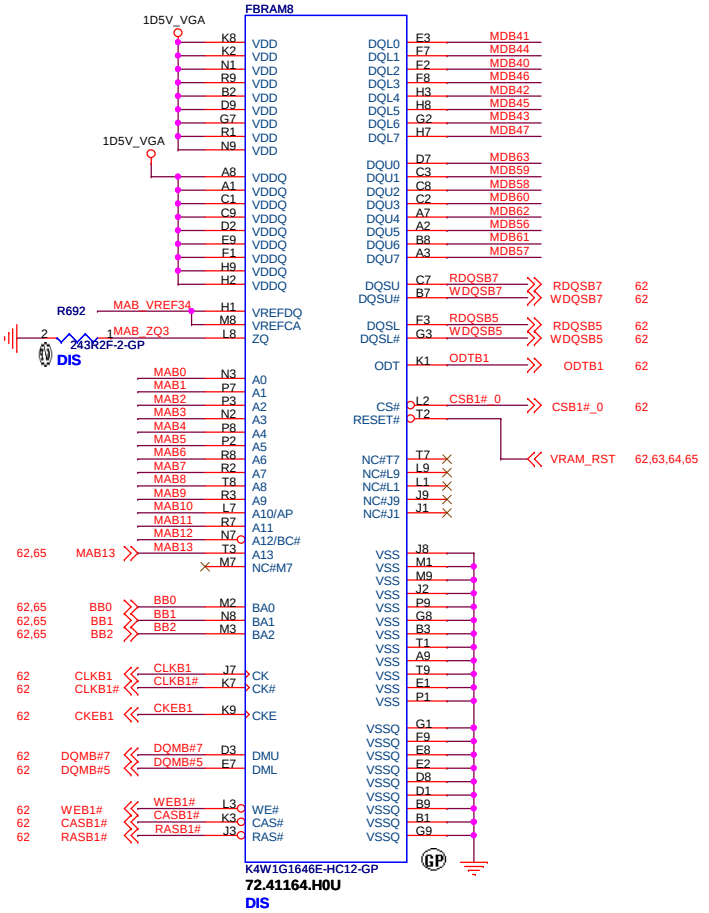
SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*VRAM(3/4)*	
Size A3	Document Number **SJV50-CP**	Rev **SB**
Date: Wednesday, October 21, 2009	Sheet 65 of 67	

DDR3





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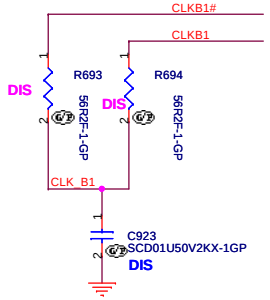

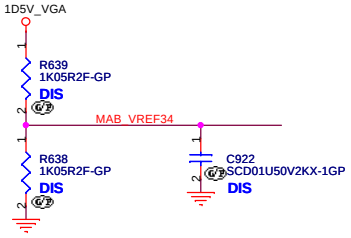

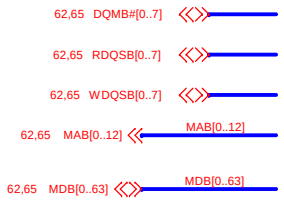

SJV50

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Title: *VRAM(4/4)*		
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SB
0812
Page57-66: change GPU
Page24: swap U5 & U6
Page15: change R112 to 22ohm
Page43: D8 change to 83.00016.B11 83.00016.K11 83.00016.F11
Page25: change PS8325 to PS8271
Page4: add R660 RN74 for DIS_ONLY
Page8: add R180 R668 R669 R685 R695 for DIS_ONLY
Page8: change C190 C192 C193 C194 to UMA_PX
Page5: add RN75 for DIS_ONLY
Page52: change GFX to UMA_PX
Page12: change R385 to DIS_ONLY and X4 C529 C530 to UMA_PX and add R381 R640
Page14: change RN48 RN49 R149 R153 C62 C63 C66 C67 C68 C69 C76 C77 to UMA_PX
Page16: cahgne R194 to UMA_DIS_ONLY and change R196 to PX
Page17: change R150 R170 C219 C220 to UMA_PX and add R696 R697 for DIS_ONLY
Page22: change U30 U33 R320 R321 C359 C360 C361 C388 C392 C394 to PX
Page22: add RN76 RN77 RN78 RN80 for DIS_ONLY
Page22: change U13 U14 R266 to PX and add RN81 for DIS_ONLY
Page22: change U24 to PX and add R698 for DIS_ONLY
Page22: change U39 C45 to PX and add RN82 for DIS_ONLY
Page23: change U12 R143 to PX and change R111 to UMA_PX and add R699 for DIS_ONLY
Page23: change U1 to PX and add R700 for DIS_ONLY
Page24: change U6 to UMA_PX
Page24: change U35 U38 R49 to PX and add RN83 for DIS_ONLY
Page40: change R84 to 65W and change R88 to 90W
0814
Page50: DY R571 and add R649
Page59: add R774 DY
Page53: change R334 to 7.5K(64.75015.6DL) and add Q51 R775
Page53: change R331 to 15K(64.15025.6DL) DY and change R322 R328 C419 DY
Page3: change C297 C298 from 27p to 12p
Page32: codec co-layout
Page11: change 1D05V_S0 to 3D3V_S5
Page5,8,10,13,16,20,21,43,50: System Level Implemention to Reduce S3 State Power On
0817
Page59: swap SWAP NV_HDMI_DATA0+/- and NV_HDMI_DATA2+/-
Page43: add Q48, R725, R726, R52 and C943 for 1D5V_S0_PWRGD level shift
Page5: change U86 pin1,2 connection to 1D5V_S0_PWRGD
Page50: change R724 pin1 connection to 1D5V_S0_PWRGD
Page32: R778 option ALC271
Page10: RN51 DY, change netname M_VREF_DQ_DIMM0, M_VREF_DQ_DIMM1
Page20: del R67 U80 R791 R65 R66; R289 C403 C402 no-option , off-page M_VREF_DQ_DIMM0
Page21: del R67 U80 R791 R65 R66; R289 C403 C402 no-option , off-page M_VREF_DQ_DIMM0
0819
Page43: U41 change to 84.04468.037
Page59: change VGA_XIN1 connect to VGA1B.AW34
Page53: R331 DIS, Q51 DY to keep +VGA_CORE 1.05V
Page59: change RN79 to R378
Page23: change R19 pin2 connecot to BRIGHTNESS_DIS
Page5: RN75 mount
Page20: del R718 RN84
Page24: U6 change to 73.2G125.A07 UMA_PX(the same as U5), and modify enable to High active
Page43: Q48 change to Q48 and Q49
Page16: Q47 change to BJT 84.T3904.C11
Page50: del Q45
Page16: C939 change to 47nF
Page30: U34 R318 C37 DY, R32 mount
0820
Page33: change RT17 RT18 to 22K for gain
Page63-66: swap the signals of VRAM
Page47: change R542 R546 to 63.00000.00L
0821
Page43: change part reference C593 to C718
Page32: change codec co-layout to ALC272
Page5: change R151.1 to 1D5V_S0_DDR
Page16: change RN32 to R648 single resister
Page47: R532 mount,R523 DY
Page47: change R531,R259 to 64.13035.6DL
Page48: change R539 to 64.10R05.55L
Page48: change R549 to 64.20035.6DL
Page48: change R534 to 64.95315.6DL
Page48: change U23,U58 to 74.51117.073
Page48: Delete R543
Page48: change R258 to 64.13025.6DL
Page49: change U51 to 74.51117.073
Page49: change R235 to 64.75015.6DL
Page53: change U36 to 74.51117.073
Page53: Delete R326
Page50: change U66 to 74.02997.A79
Page33: delete R708
0824
Page52: change U49 to 74.62881.A73
0825
Page12: delete R228
Page32: add R152
Page11: change R422 to 63.47034.1DL
Page39: add R228 DY
0827
Page25: delete D3
0916
Page15: change R127 to 63.10334.1DL mount

SJV50

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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